Vivado Design Suite User Guide

Release Notes, Installation, and Licensing

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Revision History

The following table shows the revision history for this document.

Section	Revision Summary
07/23/2018 Version 2018.2	
Architecture Support	Added new Architecture Support.
06/06/2018 Version 2018.2	
What's New	Added What's New details for the 2018.2 release.
Download Verification	Added the Download Verification new section.
04/12/2018 Version 2018.1	
Intellectual Property (IP)	Added new Intellectual Property updates.
04/04/2018 Version 2018.1	
What's New	Added What's New details for the 2018.1 release.
Compatible Third-Party Tools	Added latest version numbers for the Third-Party Tools updates.
Checking Required Libraries	Added the Checking Required Libraries new section.

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Release Notes 2018.2

What's New

Vivado® 2018.2 introduces the new production device support. Vivado 2018.2 also has additional ease of use improvements to ensure you can increase your overall efficiency and get your products to market faster.

The following devices and features are also updated in this release.

Device Support

This release of Vivado introduces the following device related changes.

The following devices are in production:

- Zynq UltraScale+ RFSoC:
  - XCZU21DR (-1, -2, -2LE)
  - XCZU25DR (-1, -2, -2LE)
  - XCZU27DR (-1, -2, -2LE)
  - XCZU28DR (-1, -2, -2LE)
  - XCZU29DR (-1, -2, -2LE)
- XA Zynq UltraScale+ MPSoC:
  - XAZU4EV (-1, -1L, -1Q)
  - XAZU5EV (-1, -1L, -1Q)
- Defense-Grade Zynq UltraScale+ MPSoCs:
  - XQZU5EG (-1M)
  - XQZU5EV (-1M)
- Spartan-7
  - XC7S6 (-1, -2, -1L)
  - XC7S15 (-1, -2, -1L)

- Artix-7
  - XC7A25T (-3)
  - XC7A12T (-3)

The following devices are enabled in Vivado WebPack:

- Spartan-7:
  - XC7S6
  - XC7S15
- XA Zynq UltraScale+ MPSoC:
  - XAZU4EV
  - XAZU5EV

Vivado Tools

System Generator for DSP

- Supported MATLAB Versions: R2017a, R2017b and R2018a.
- Support for Zynq UltraScale+ RFSoC production devices.

Vivado HLS

- New **Schedule Viewer** accessible from the Analysis Perspective to graphically display dependencies of operations and control steps.
- Overall faster processing of source code embedded directives (pragmas).
- Redesigned `dataflow` directive checks to help guide toward optimal solution.
- Performance enhancements with both higher clock rates (+4% on average) and reduced design latency with 10% less clock cycles for design completion.
- Five additional math.h optimized functions for fixed-point data types (pow, abs, sincos, acos, and asin).
- Co-simulation waveforms are enhanced to clearly display DATAFLOW transactions.
- New DRCs added to the Vivado HLS GUI DRC tab to expedite timing closure and strengthen pragma checks.

Model Composer

- **Supported MATLAB Versions**: R2017a, R2017b and R2018a.

- New Color Detection Example: Color Detection algorithm to segment yellow traffic signs in input video stream, demonstrates how to use blocks from Model Composer library and how to import additional Xilinx-optimized reVISION xfOpenCV function to build a synthesizable design.
- **Overflow Detection for Fixed-Point Data Types**: Data Type Conversion block supports detection of Saturation and Wrap on Overflows for Fixed-point data type conversions in the design.
- **Enhancements to C/C++ Function Import**: Ease-of-use enhancements and Block GUI improvements make it easier to create and use Custom Blocks in your design through the C/C++ Function Import feature.
- **Linear Algebra Block**: New optimized QR Inverse block added into the Model Composer Linear Algebra library that contains the Hermitian, Matrix Multiply, Submatrix and Transpose blocks.

Simulation Flows and Verification IP

- `xsim.ini` file now contains all the pre-compiled IP library mappings.

Implementation

- Placement now includes replication by default to improve delays on high fanout nets. The `-fanout_opt` option is no longer needed and the `-no_fanout_opt` option is used to disable placer replication.

Hierarchical Design Flows

- Tandem Configuration
  - Xilinx PCIe IP for UltraScale+ devices supports Reconfigurable Stage Twos. When using the Tandem PCIe with Field Updates feature, users can select any compatible (i.e. implemented in context with the current stage 1 image) stage 2 bitstream to complete the initial configuration of the device. These stage 2 bitstreams are formatted as partial bitstreams and can therefore be used to dynamically reconfigure the user application while the PCIe link remains active. See PG213 for more information.
- Partial Reconfiguration
  - Zynq-7000 devices with a single-core processor (Z-7007S, Z-7012S, Z-7014S) are now supported.

Xilinx Embedded Software and Tools

- Linux
  - Non-secure partial bitstream support without Device Tree Overlay (DTO) through FPGA Manager.
  - SDFEC Device Driver (public release).
- Secure Library Enhancements
  - Enhanced Key Revocation with User eFuses.
  - RSA 3072bit key support.
  - Xilinx Secure Library (XilSecure) now supports decryption, commanded from Uboot, for Bootgen images encrypted with the device key.
- PetaLinux
  - Ultra96 BSP (public release).

Important Information

Licensing

The Vivado 2017.3 and beyond releases introduces the following changes in licensing that are listed below:

- Starting with Vivado 2017.3, activation licensing is no longer supported. Existing activation licenses have been replaced with certificate based license that can be accessed from www.xilinx.com/getlicense.
- Flexera version for license management tool has been upgraded to 11.14.1. Vivado 2017.3 is the last release that will support Solaris operating system for Flex license management tools. Xilinx will continue to support Window and Linux operating systems for Flex license management tools.
- Anyone using floating license will require to upgrade licensing utilities to Flex 11.14.1. These new licensing utilities are available on download page of www.xilinx.com.
- Please note that Flex version upgrade does not affect valid license files, in other words, existing valid license files will work just fine with Vivado 2017.3 release after you upgrade licensing utilities.

Vivado Naming Conventions

The following are the required naming conventions when working with the Vivado Design Suite. Failing to follow these naming conventions might introduce potential risk to the design or the tool, and cause unpredictable behavior in the design flow.

- Source files names must start with a letter (A-Z, a-z) and must contain only alphanumeric characters (A-Z, a-z, 0-9) and underscores (_).
- Output files names must start with a letter (A-Z, a-z) and must contain only alphanumeric characters (A-Z, a-z, 0-9) and underscores (_).
- Project names must start with a letter (A-Z, a-z) and must contain only alphanumeric characters (A-Z, a-z, 0-9) and underscores (_).
- Project directory names must start with a letter (A-Z, a-z) and should contain only alphanumeric characters (A-Z, a-z, 0-9), tilde (~) and underscores (_).

CAUTION! *The Windows operating system has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use the shortest possible names and directory locations when creating projects, defining IP or managed IP projects, or creating block designs.*

The following characters are not supported for project, file, or directory names:

- ! # $ % ^ & * ( ) ` ; < > ? , [ ] { } ' " |
- tab (\t)
- return (\r)
- new line (\n)
- / or \ (As part of the directory or file name rather than as a path delimiter)

The following character is not supported for directory names:

- . (dot as terminal character)

The following character is not supported for file or project names:

- @

Note: In the Vivado IDE, the @ character is not supported for new file or project names. The Vivado IDE does allow an existing file on disk that uses the @ character to be added to a project. The Vivado IDE can open a project that includes the @ character in the project name. Using the Tcl Console, you can create a project with a name that contains the @ character.

IMPORTANT: *Spaces in directory and file names are supported by the Windows operating system. However, you should avoid using spaces in order to preserve portability of the project or files between the Windows and Linux operating systems.*

The Vivado Design Suite supports the use of forward slashes (/) as path delimiters for both Windows and Linux platforms. Backslashes (\) are allowed as path delimiters on the Windows platform only.

Any characters not explicitly mentioned above are not supported for project, file, or directory names.

Vivado Design Suite Documentation Update

In the 2018.2 Vivado Design Suite Documentation release, not all documentation will be available at first customer ship. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2018.2 documentation suite.

Known Issues

Vivado Design Suite Tools Known Issues can be found at Answer Record 70860.

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Chapter 2

Architecture Support and Requirements

Operating Systems

Xilinx® supports the following operating systems on x86 and x86-64 processor architectures.

Microsoft Windows Support

- Windows 7 SP1 Professional (64-bit), English/Japanese.
- Windows 10.0 Fall Creators update (version 1709), 10.0 Version 1803 (64-bit), English/Japanese.

Linux Support

- Red Hat Enterprise Workstation/Server 7.2, 7.3, and 7.4 (64-bit)
- Red Hat Enterprise Workstation 6.6, 6.7, 6.8, and 6.9 (64-bit)
- SUSE Linux Enterprise 11.4 and 12.3 (64-bit)
- CentOS 7.2, 7.3, and 7.4 (64-bit)
- CentOS 6.7, 6.8, and 6.9 (64-bit)
- Ubuntu Linux 16.04.3 LTS (64-bit)

Note: Please refer to *PetaLinux Tools Documentation: Reference Guide* (UG1144) [Ref 22] for more information on Installation Requirements for supported Operating Systems with PetaLinux.

Architectures

The following table lists architecture support for commercial products in the Vivado Design Suite WebPACK™ tool versus all other Vivado Design Suite editions. For non-commercial support all Xilinx Automotive devices are supported in the Vivado Design Suite WebPACK tool when available as production devices in the tools.

Table 2-1: **Architecture Support**

	Vivado WebPACK Tool	Vivado Design Suite (All Other Editions)
Zynq® Device	Zynq-7000 SoC Device • XC7Z010, XC7Z015, XC7Z020, XC7Z030, XC7Z007S, XC7Z012S, and XC7Z014S	Zynq-7000 SoC Device • All
Zynq® UltraScale™+ MPSoC	UltraScale+ MPSoC • XCZU2EG, XCZU2CG, XCZU3EG, XCZU3CG XCZU4EG, XCZU4CG, XCZU4EV, XCZU5EG, XCZU5CG, XCZU5EV, XCZU7EV, XCZU7EG, and XCZU7CG	UltraScale+ MPSoC • All
Zynq® UltraScale+™ RFSoC	Zynq® UltraScale+™ RFSoC • None	Zynq® UltraScale+™ RFSoC • All
Virtex® FPGA	Virtex-7 FPGA • None Virtex UltraScale™ FPGA • None	Virtex-7 FPGA • All Virtex UltraScale FPGA • All Virtex UltraScale+ FPGA • All
Kintex® FPGA	Kintex-7 FPGA • XC7K70T, XC7K160T Kintex UltraScale™ FPGA • XCKU025, XCKU035 Kintex UltraScale+ FPGA • XCKU3P. XCKU5P	Kintex-7 FPGA • All Kintex UltraScale FPGA • All Kintex UltraScale+ FPGA • All
Artix® FPGA	Artix-7 FPGA • XC7A12T, XC7A15T, XC7A25T, XC7A35T, XC7A50T, XC7A75T, XC7A100T, XC7A200T	Artix-7 FPGA • All
Spartan®-7	Spartan-7 • XC7S6, XC7S15 • XC7S25, XC7S50 • XC7S75, XC7S100	Spartan-7 • All

Compatible Third-Party Tools

Table 2-2: **Compatible Third-Party Tools**

Third-Party Tool	Red Hat Linux	Red Hat Linux-64	SUSE Linux	Windows-7/10 32-bit	Windows-7/10 64-bit	Ubuntu
Simulation						
Mentor Graphic ModelSim SE/DE/PE (10.6c)	Yes	Yes	Yes	Yes	Yes	N/A
Mentor Graphics Questa Advanced Simulator(10.6c)	Yes	Yes	Yes	Yes	Yes	N/A
Cadence Incisive Enterprise Simulator (IES) (15.20.042)	Yes	Yes	Yes	N/A	N/A	N/A
Cadence Xcelium Parallel Simulator (17.10.005)	Yes	Yes	Yes	N/A	N/A	N/A
Synopsys VCS and VCS MX (N-2017.12)	Yes	Yes	Yes	N/A	N/A	N/A
The MathWorks MATLAB® and Simulink® (R2017a, R2017b, and R2018a)	Yes	Yes	No	N/A	Yes	No
Aldec Active-HDL (10.4a)(1)	N/A	N/A	N/A	Yes	Yes	N/A
Aldec Riviera-PRO (2017.10)	Yes	Yes	Yes	Yes	Yes	N/A
Synthesis(2)						
Synopsys Synplify/Synplify Pro (M-2017.03-SP1)(3)	Yes	Yes	Yes	Yes	Yes	N/A
Mentor Graphics Precision RTL/Plus (2016.1)	Yes	Yes	Yes	Yes	Yes	N/A
Equivalence Checking						
Cadence Encounter Conformal (9.1)(4)	Yes	Yes	Yes	N/A	N/A	N/A
OneSpin 360 (2016_12)	Yes	Yes	Yes	N/A	N/A	N/A

Notes:

1. Support for Aldec simulators is offered by Aldec.
2. Most Vivado IP can only be synthesized by Vivado synthesis, because the RTL source can include encrypted files. To use this IP in a third-party synthesis flow, the synthesized netlist can be exported from the Vivado tool in a suitable format for use in the third-party synthesis project.
3. Contact Synopsys for availability of Synplify Overlay or Service Pack.
4. Cadence Encounter Conformal Support is for RTL2Gate using Synopsys Synplify only.

IMPORTANT: *The versions listed in Table 2-2 are the minimum required versions to use with the Vivado tools. Previous versions are not tested.*

System Requirements

This section provides information on system memory requirements, cable installation, and other requirements and recommendations.

The lab exercises require the installation of MATLAB 2014a (or later) and Vivado Design Suite 2014.2 (or later).

System Memory Recommendations

For memory recommendations for the Vivado Design Suite tools, see: System Memory Requirements.

Operating Systems and Available Memory

The Microsoft Windows and Linux operating system (OS) architectures have limitations on the maximum memory available to a Xilinx program. Users targeting the largest devices and most complex designs might encounter this limitation. The Vivado Design Suite has optimized memory and enabled support for applications to increase RAM memory available to Xilinx tools.

Cable Installation Requirements

Platform Cable USB II is a high-performance cable that enables Xilinx design tools to program and configure target hardware.

Note: The Xilinx Parallel Cable IV is no longer supported for debugging or programming.

RECOMMENDED: *To install Platform Cable USB II, a system must have at least a USB 1.1 port. For maximum performance, Xilinx recommends using Platform Cable USB II with a USB 2.0 port.*

The cable is officially supported on the 64-bit versions of the following operating systems: Windows-7, Windows-10, Red Hat Linux Enterprise, and SUSE Linux Enterprise 12. Additional platform specific notes are as follows:

- Root privileges are required.
- SUSE Linux Enterprise 11: The fxload software package is required to ensure correct Platform Cable USB II operation. The fxload package is not automatically installed on SUSE Linux Enterprise 11 distributions, and must be installed by the user or System Administrator.

For additional information regarding Xilinx cables, see the following documents:

- *Platform Cable USB II Data Sheet* (DS593) [Ref 13]

Equipment and Permissions

The following table lists related equipment, permissions, and network connections.

Table 2-3: **Equipment and Permissions Requirements**

Item	Requirement
Directory permissions	Write permissions must exist for all directories containing design files to be edited.
Monitor	16-bit color VGA with a minimum recommended resolution of 1024 by 768 pixels.
Ports	To program devices, you must have an available parallel or USB port appropriate for your Xilinx programming cable. Specifications for ports are listed in the documentation for your cable. ***Note:*** Installation of the cable driver software requires Windows-10. If you are not using one of these operating systems, the cables might not work properly.

Note: X Servers/ Remote Desktop Servers, such as Exceed, ReflectionX, and XWin32, are not supported.

Network Time Synchronization

When design files are located on a network machine, other than the machine with the installed software, the clock settings of both machines must be set the same. These times must be synchronized on a regular basis for continued proper functioning of the software.

Download and Installation

This guide explains how to download and install the Vivado® Design Suite tools, which includes the Vivado Integrated Design Environment (IDE), High Level Synthesis tool, and System Generator for DSP and Model Composer.

Downloading the Vivado Design Suite Tools

Xilinx® Design Tools users have multiple choices for download and installation.

Xilinx introduced **Vivado Lab Edition**, which features a dedicated and streamlined environment for programming and debugging devices in lab settings.

TIP: *No license is required to use Vivado Lab Edition tools.*

For users wishing to install one of the full Vivado Editions, there are three choices.

Vivado Design Suite - HLx Editions:

- **WebPack and Editions**: Web installer for windows
- **WebPack and Editions**: Web installer for Linux
- **All OS Single File Download**

All Editions and download options are available on the Xilinx website: Downloads

For the optimum download experience:

- Allow pop-ups from https://www.o-ms.com/.
- Set security settings to allow for secure and non-secure items to be displayed on the same page.

To download a full Edition of the Vivado Design Suite:

1. Select the **Vivado Design Tools** tab in the web page.
2. Under the Version heading, click the version of the tools you want to download.
3. Click the link for the installer you want to download.

To download the Vivado Lab Edition tools, go to the Vivado Design Tools tab, select a version of 2017.1 or newer, and download the file associated with the Vivado Lab Edition.

Note: The Full Edition installers work only on 64-bit machines.

Download Verification

Digest, **Signature** and **Public Key** are provided on download page for the purpose of download verification.

Download verification allows users to prove the authenticity and integrity of downloaded file with fair degree of certainty. **Authentication** validates that downloaded file was created by the signee, in this case signee is Xilinx Inc. In other words, it shows that downloaded file is not forged by a third party. **Integrity** validates that contents of downloaded file are not tampered by third party. In summary, download verification allows users to validate if downloaded file indeed is prepared by Xilinx and if the contents of the downloaded file have been altered or not.

RECOMMENDED: *Download verification step is completely optional but highly recommended – users can skip following steps to install the tools, right after downloading it from downloads page on Xilinx website.*

Note: The download verification does not apply to Windows based downloads. Windows executables are signed with **Extended Validation Code Signing Certificates**. Microsoft's SmartScreen® Application Reputation filter will produced warnings for downloaded files that have been tampered in any way.

There are two ways users can verify the authenticity and integrity of downloaded file. Please pick one or both of the following methods to ensure the authenticity and integrity of downloaded file.

1. Verifying the Signature
2. Verifying the Digest.

For both of the above methods, users are required to download, import and trust the public key.

Download, Import and Trust Xilinx Public Key

Download Xilinx Public Key

Xilinx public key can be downloaded from download page on Xilinx website. The key name for Xilinx public key is - **xilinx-master-signing-key.asc** .

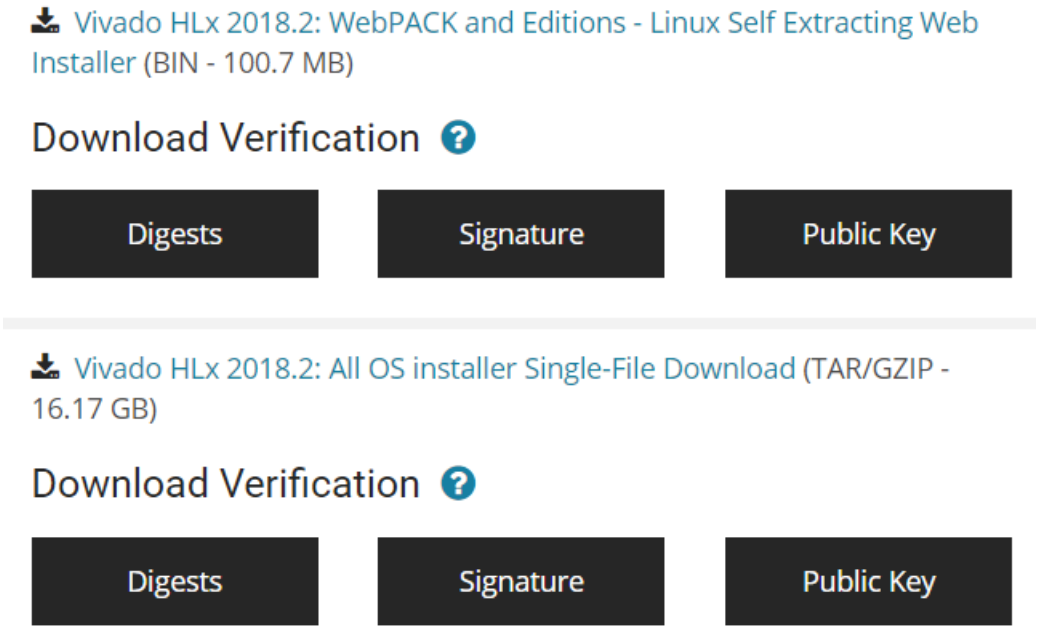

Figure 3-1: **Digest, Signature, and Public Key on Download Page**

Import Public Key with GPG

After the Xilinx public key is downloaded, the next step is to import the public key with GPG. You can use following command to import Xilinx's public key.

```
gpg --import ./xilinx-master-signing-key.asc
```

The output of successfully import key should look like below.

```
myuser@mymachine:$ gpg --import ./xilinx-master-signing-key.asc
gpg: keybox '/home/myuser/.gnupg/pubring.kbx' created
gpg: /home/myuser/.gnupg/trustdb.gpg: trustdb created
gpg: key 0x85D4B4BB1D692FDB: public key "Xilinx, Inc. (Xilinx Software signing
gpg: Total number processed: 1
gpg:               imported: 1
myuser@mymachine:$
```

Figure 3-2: **Import Public Key**

Trust Xilinx Public Key

Once you have confirmed that you have downloaded and imported the legitimate Xilinx public key, you can now set the trust level to "ultimate". This will allow verification of the key signed by Xilinx.

1. Use following command to first list the public keys:

```
gpg --list-keys
```

```
myuser@mymachine:$ gpg --list-keys
/home/myuser/.gnupg/pubring.kbx
------------------------------
pub   rsa4096/0x85D4B4BB1D692FDB 2018-04-10 [SC]
      Key fingerprint = 745F 4D5B 2402 441F 410F  BD0D 85D4 B4BB 1D69 2FDB
uid                   [ unknown] Xilinx, Inc. (Xilinx Software signing key) <so
sub   rsa4096/0xE80A66CA2B176EF9 2018-04-10 [S]
sub   rsa4096/0xF991913DFE46B839 2018-04-10 [E]
sub   rsa4096/0xC93822D0B9087126 2018-04-10 [A]
myuser@mymachine:$
```

Figure 3-3: **List Keys**

2. Use the following command to specify the key that needs to be edited.

```
gpg --edit-key 0x85D4B4BB1D692FDB
```

```
myuser@mymachine:$ gpg --edit-key 0x85D4B4BB1D692FDB
gpg (GnuPG) 2.1.15; Copyright (C) 2016 Free Software Foundation, Inc.
This is free software: you are free to change and redistribute it.
There is NO WARRANTY, to the extent permitted by law.


pub  rsa4096/0x85D4B4BB1D692FDB
     created: 2018-04-10  expires: never       usage: SC
     trust: unknown       validity: unknown
sub  rsa4096/0xE80A66CA2B176EF9
     created: 2018-04-10  expires: never       usage: S
sub  rsa4096/0xF991913DFE46B839
     created: 2018-04-10  expires: never       usage: E
sub  rsa4096/0xC93822D0B9087126
     created: 2018-04-10  expires: never       usage: A
[ unknown] (1). Xilinx, Inc. (Xilinx Software signing key) <software@xilinx.co
```

Figure 3-4: **Edit Keys**

3. Use the following command to set the trust level for the legitimate key.

```
trust
```

```
gpg> trust
pub  rsa4096/0x85D4B4BB1D692FDB
     created: 2018-04-10  expires: never       usage: SC
     trust: unknown       validity: unknown
sub  rsa4096/0xE80A66CA2B176EF9
     created: 2018-04-10  expires: never       usage: S
sub  rsa4096/0xF991913DFE46B839
     created: 2018-04-10  expires: never       usage: E
sub  rsa4096/0xC93822D0B9087126
     created: 2018-04-10  expires: never       usage: A
[ unknown] (1). Xilinx, Inc. (Xilinx Software signing key) <software@xilinx.co

Please decide how far you trust this user to correctly verify other users' key
(by looking at passports, checking fingerprints from different sources, etc.)

  1 = I don't know or won't say
  2 = I do NOT trust
  3 = I trust marginally
  4 = I trust fully
  5 = I trust ultimately
  m = back to the main menu
```

Figure 3-5: **Trust Keys**

4. Enter 5 at the prompt.

```
Your decision? 5
Do you really want to set this key to ultimate trust? (y/N) y

pub  rsa4096/0x85D4B4BB1D692FDB
     created: 2018-04-10  expires: never       usage: SC
     trust: ultimate      validity: unknown
sub  rsa4096/0xE80A66CA2B176EF9
     created: 2018-04-10  expires: never       usage: S
sub  rsa4096/0xF991913DFE46B839
     created: 2018-04-10  expires: never       usage: E
sub  rsa4096/0xC93822D0B9087126
     created: 2018-04-10  expires: never       usage: A
[ unknown] (1). Xilinx, Inc. (Xilinx Software signing key) <software@xilinx.com
Please note that the shown key validity is not necessarily correct
unless you restart the program.

gpg> q
myuser@mymachine:$
```

Figure 3-6: **Set Ultimate Trust for the Key**

Now that you have downloaded, imported and trusted the Xilinx public key – you can ensure the authenticity and integrity of the downloaded file by verifying the signature or verifying the digest. Please note that you can pick one or both of methods to ensure the authenticity and integrity of downloaded file.

Verifying the Signature

In order to verify the downloaded file that matches its signature, you need to download the signature file from download page on Xilinx website.

Once the signature file has been downloaded and stored, you can run following command to verify the signature.

```
gpg -v --verify Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64.bin.sig
Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64.bin
```

```
myuser@mymachine:$ gpg -v --verify Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64
gpg: Signature made Wed Apr 11 16:21:12 2018 UTC
gpg:                using RSA key 0xE80A66CA2B176EF9
gpg: using subkey 0xE80A66CA2B176EF9 instead of primary key 0x85D4B4BB1D692FDB
gpg: using pgp trust model
gpg: checking the trustdb
gpg: 1 key processed (0 validity counts cleared)
gpg: marginals needed: 3  completes needed: 1  trust model: pgp
gpg: depth: 0  valid:   1  signed:   0  trust: 0-, 0q, 0n, 0m, 0f, 1u
gpg: Good signature from "Xilinx, Inc. (Xilinx Software signing key) <software@
Primary key fingerprint: 745F 4D5B 2402 441F 410F  BD0D 85D4 B4BB 1D69 2FDB
     Subkey fingerprint: B887 532B 4A76 72C3 168C  58C8 E80A 66CA 2B17 6EF9
gpg: binary signature, digest algorithm SHA512, key algorithm rsa4096
myuser@mymachine:$
```

Figure 3-7: **Signature Verification**

Verifying Digest

This is an alternative verification method to ensure the authenticity and integrity of downloaded file. This method uses the "digest" or "hash values" which is the output of various cryptographic hash functions. In order to verify the downloaded file using digest, you need to download the digest file from download page on Xilinx website. The current digest file support MD5, SHA1, SHA256, SHA512 hashing algorithms.

Once the digest file has been downloaded and stored, you need to first authenticate the digest file to make sure that it is indeed coming from Xilinx Inc.

Authenticate Digest File

Run the following command to verify the signature that ensures that digest file is indeed coming from Xilinx Inc.

```
gpg -v --verify Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64.bin.digests
```

```
myuser@mymachine:$ gpg -v --verify Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64.
gpg: armor header: Hash: SHA512
gpg: original file name=''
gpg: Signature made Wed Apr 11 21:49:42 2018 UTC
gpg:                using RSA key 0xE80A66CA2B176EF9
gpg: using subkey 0xE80A66CA2B176EF9 instead of primary key 0x85D4B4BB1D692FDB
gpg: using pgp trust model
gpg: checking the trustdb
gpg: 1 key processed (0 validity counts cleared)
gpg: marginals needed: 3  completes needed: 1  trust model: pgp
gpg: depth: 0  valid:   1  signed:   0  trust: 0-, 0q, 0n, 0m, 0f, 1u
gpg: Good signature from "Xilinx, Inc. (Xilinx Software signing key) <software@x
Primary key fingerprint: 745F 4D5B 2402 441F 410F  BD0D 85D4 B4BB 1D69 2FDB
     Subkey fingerprint: B887 532B 4A76 72C3 168C  58C8 E80A 66CA 2B17 6EF9
gpg: textmode signature, digest algorithm SHA512, key algorithm rsa4096
myuser@mymachine:$
```

Figure 3-8: **Authenticate Digest File**

Now after the authentication is done, you can verify the digest either by using hashing executable or by using OpenSSL.

Using Hashing Executable

You can run following command to verify the digest using hashing executable – sha256. Please note you can use other hashing executable as well such as md5sum, sha1sum, sha512sum.

```
sha256sum -c Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64.bin.digests
```

```
myuser@mymachine:$ sha256sum -c Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64.bin
Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64.bin: OK
sha256sum: WARNING: 19 lines are improperly formatted
myuser@mymachine:$



Note: The OK response tells us that the hash value for that particular hash func
The program also warns us that there are 19 improperly formatted lines, but this
This is because each file contains lines for several different hash values (as m
but each *sum program verifies only the line for its own hash function.
In addition, there are lines for the PGP signature which the *sum programs do no
```

Figure 3-9: **Verify Using Hashing Executable**

Using OpenSSL

You can also verify the digest using OpenSSL – run following command to verify the digest using OpenSSL. Output of the command is a computed hash value that you need to compare to the contents of digest file.

```
openssl dgst -sha256 Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64.bin
```

```
penssl dgst -sha256 Xilinx_Vivado_SDK_Web_2018.2_0410_1926_Lin64.bin
_SDK_Web_2018.2_0410_1926_Lin64.bin)= 058bbc714a8c10c3badb02f11f6d0ca65c9153aa733
```

Figure 3-10: **Verify Using OpenSSL**

Installing the Vivado Design Suite Tools

This section explains the installation process for all platforms for the Vivado Design Suite.

Installation Preparation

IMPORTANT: *Before starting installation the follow steps must be completed:*

- Check the links in Important Information section in Chapter 1 for any installation issues pertaining to your system or configuration.
- Make sure your system meets the requirements described in Chapter 2, Architecture Support and Requirements.
- Disable anti-virus software to reduce installation time.
- Close all open programs before you begin installation.
- The Vivado Design Suite installer does not set global environment variables, such as XILINX, on Windows.

Lab Edition, Full Product Download, or DVD

If you downloaded the Lab Edition or full product installation, decompress the file and run `xsetup` (for Linux) or `xsetup.exe` (for Windows) to launch the installation. If you received a DVD, which only contains the full Edition products, launch `xsetup(.exe)` directly.

RECOMMENDED: *Xilinx recommends the use of 7-zip or WinZip (v.15.0 or newer) to decompress the downloaded tar.gz file.*

Lightweight Installer Download

If you downloaded the lightweight installer, launch the downloaded file. You are prompted to log in and use your regular Xilinx login credentials to continue with the installation process.

After entering your login credentials, you can select between a traditional web-based installation or a full install image download.

- The **Download and Install Now** choice allows you to select specific tools and device families on following screens, downloads only the files required to install those selections, and then installs them for you.
- The **Download Full Image** requires you to select a download destination and to choose whether you want a Windows only, Linux only, or an install that supports both operating systems. There are no further options to choose with the **Download Full Image** selection, and installation needs to be done separately by running the xsetup application from the download directory.

Note: Lab Edition is not supported through a lightweight installer. You may download the single-file download image for Lab Edition.

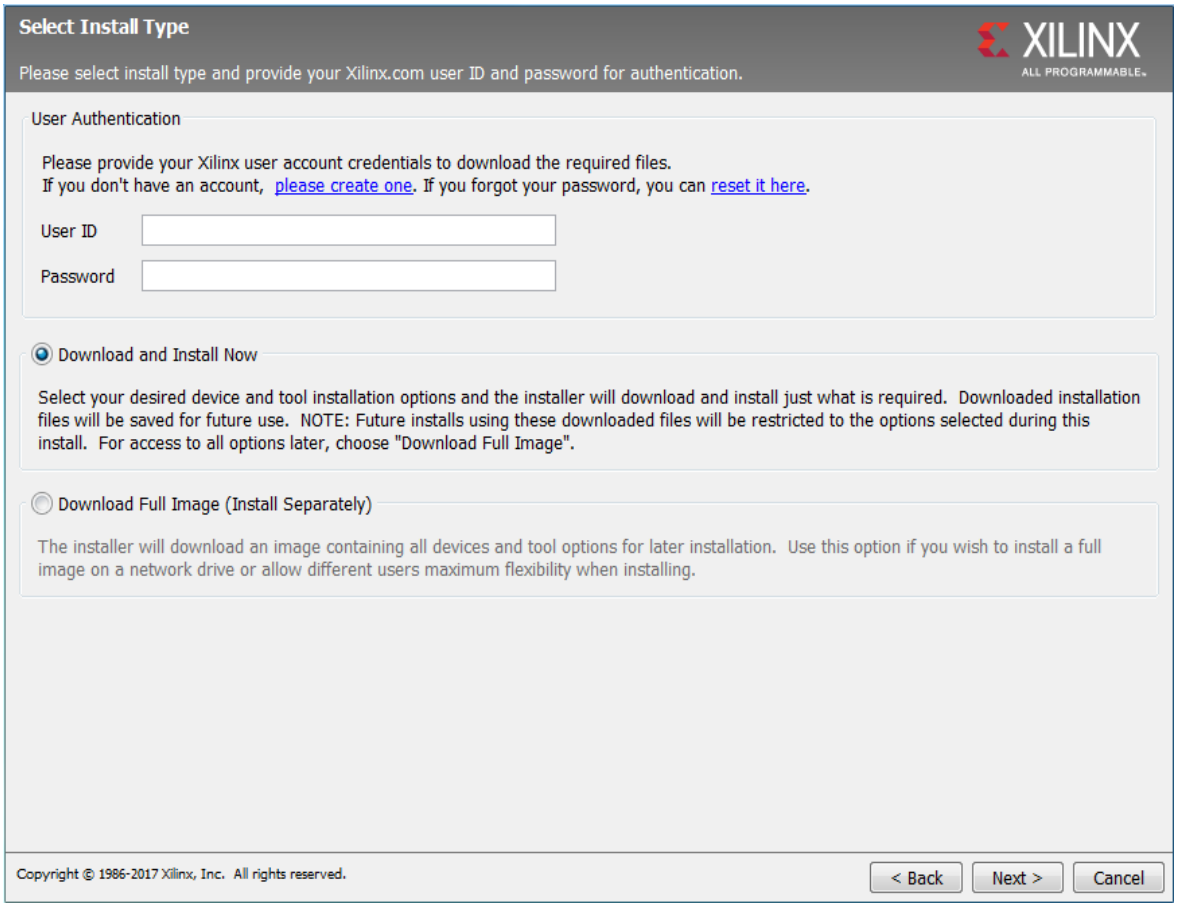

Figure 3-11: **Vivado Design Suite Installation - Select Installation Source**

Connectivity

The installer connects to the internet through the system proxy settings in Windows. These settings can be found under **Control Panel > Network and Internet > Internet Options**. For Linux users, the installer uses Firefox browser proxy settings (when explicitly set) to determine connectivity.

Figure 3-12: **Vivado Design Suite Installation - Connectivity**

If there are connectivity issues, verify the following:

1. If you are using alternate proxy settings to the ones referred to, select the **Manual Proxy Configuration** option to specify the settings.

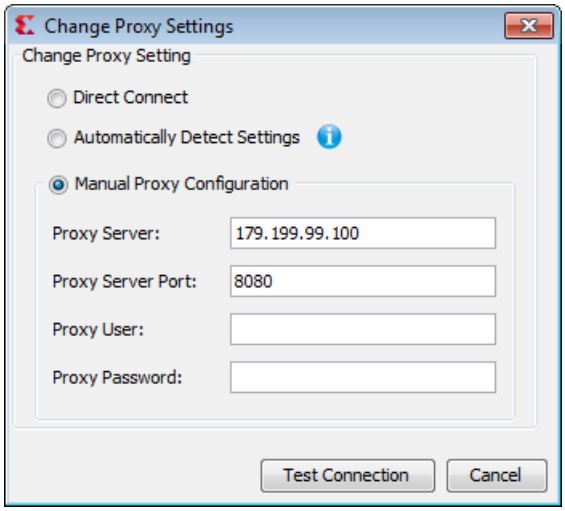

Figure 3-13: **Vivado Design Suite Installation - Change Proxy Settings**

2. Check if your company firewall requires a proxy authentication with a username and password. If so, select the **Manual Proxy Configuration** option in the dialog box above.
3. For Linux users, if either the **Use System settings** or the **Auto detect settings** option is selected in the Firefox browser, you must manually set the proxy in installer.

License Agreements

Carefully read the license agreements before continuing with the installation. If you do not agree to the terms and conditions, cancel the installation and contact Xilinx.

Edition Selection

Select the edition or standalone tool that is required. You can also install the Xilinx Software Development Kit (XSDK) as part of the Vivado WebPACK, System and Design editions.

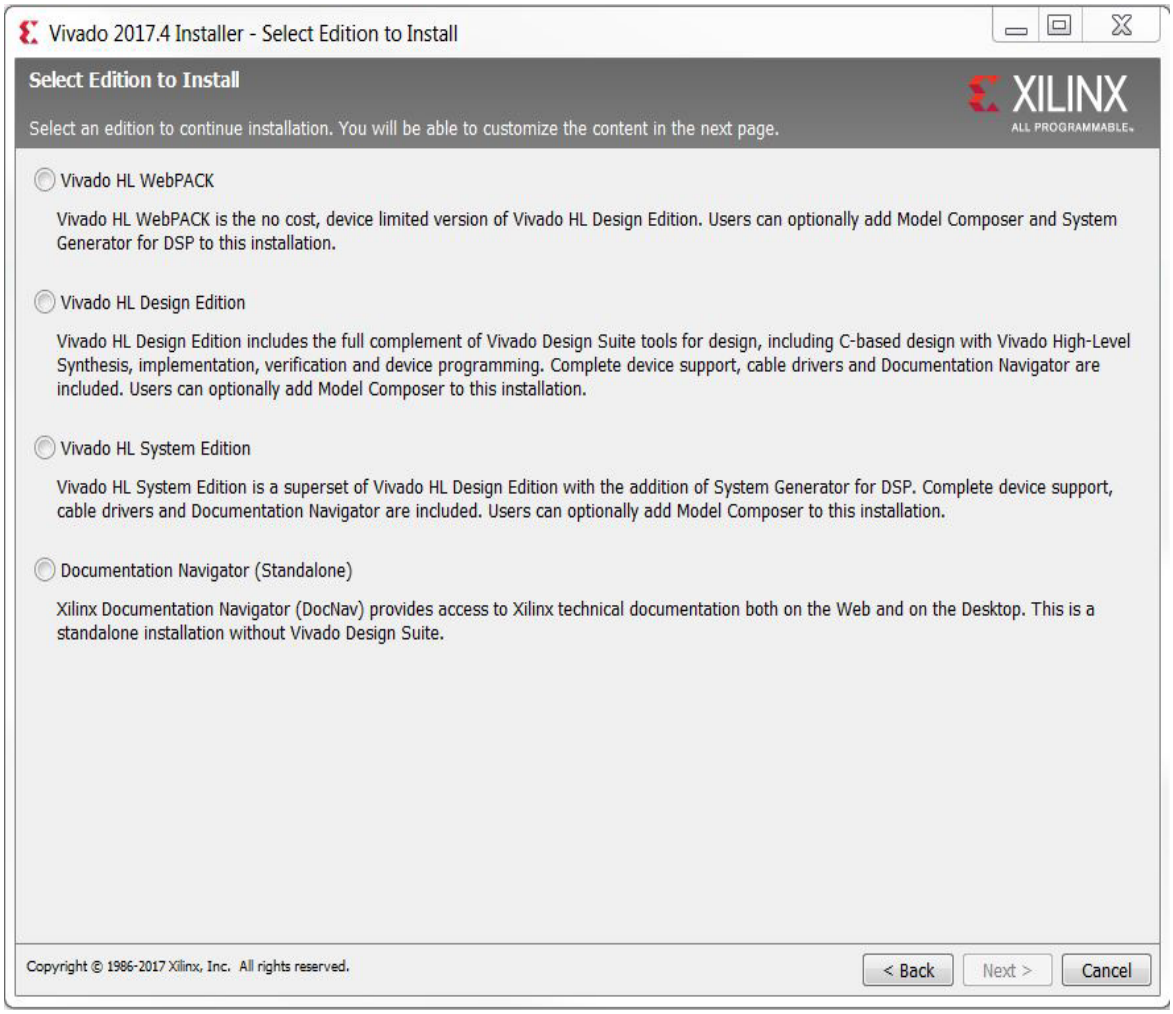

Figure 3-14: **Vivado Design Suite Installation - Select Products**

Vivado WebPACK and Design edition users will also be able to upgrade to a higher edition post installation. See Adding Additional Tools and Devices, page 31 for more details.

Tools, Devices, and Options

Customize the installation by choosing the design tools, device families and installation options. Selecting only what you need helps to minimize the time taken to download and install the product. You will be able to add to this installation later by clicking **Add Design Tools or Devices** from either the operating system Start Menu or the **Vivado > Help** menu.

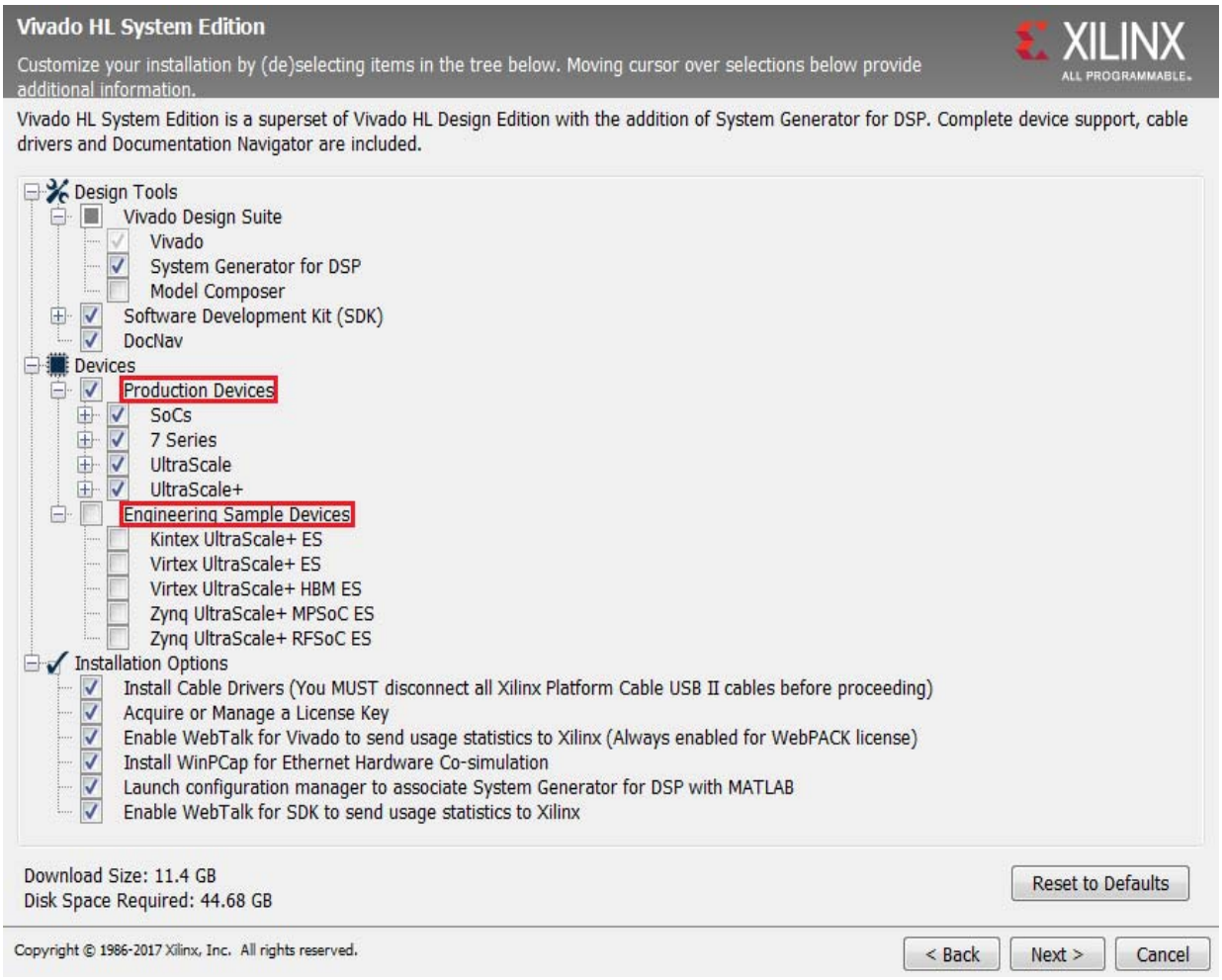

Figure 3-15: **Vivado Design Suite Installation - Vivado System Edition**

Shortcuts and File Associations

You can customize the creation of the program group entries (Start Menu) and the creation of desktop shortcuts. Optionally, you can also create file associations to launch Vivado project files directly with this version of Vivado. The shortcut creation and file association options can be applied to the current user or all users.

Installing Cable Drivers

On Windows, **Install Cable Drivers** is an optional selection in the installer.

For Linux, because root or sudo access is required to install drivers, this option has been removed from the Linux installer beginning in Vivado 2015.4. The general Vivado installer can now be run on Linux without root or sudo privileges. To install cable drivers on Linux, there is now a script that must be run as root or sudo post installation.

Script Location: `<Vivado Install Dir>/data/xicom/cable_drivers/lin64/install_script/install_drivers/`

Script Name: `install_drivers`

Installing Windows Driver

Run the following commands in an Administrator command prompt. Note, set or replace %VIVADO_INSTALL_DIR% with the location of your install directory. Replace %log_dir% with the location of the log directory. Note if %log_dir% is not specified a file named install_drivers_wrapper.log will be placed under %VIVADO_INSTALL_DIR%.

```
cd %VIVADO_INSTALL_DIR%\data\xicom\cable_drivers\nt64
install_drivers_wrapper.bat %log_dir% %log_dir%
```

Uninstalling Cable Drivers

On Windows, to uninstall cable drivers run the following commands in an Administrator command prompt. Note, set or replace `%VIVADO_INSTALL_DIR%` with the location of your install directory.

```
cd %VIVADO_INSTALL_DIR%\data\xicom\cable_drivers\nt64
wdreg -inf %cd%\xusbdrvr.inf uninstall
net stop XilinxPC4Driver
del %WINDIR%\system32\drivers\windrvr6.sys
del %WINDIR%\system32\drivers\xusb*.sys
del %WINDIR%\system32\drivers\xpc4drvr.sys
```

Installing Linux Driver

For Linux, because root or sudo access is required to install drivers, this option has been removed from the Linux installer beginning in Vivado 2015.4. The general Vivado installer

can now be run on Linux without root or sudo privileges. To install cable drivers on Linux, there is now a script that must be run as root or sudo post installation.

Run these commands as root. Note replace `${vivado_install_dir}` with the location of your vivado install location.

```
${vivado_install_dir}/data/xicom/cable_drivers/lin64/install_script/install_drivers
/install_drivers
```

Uninstalling Linux Driver

Run these commands as root:

```
rm -f /etc/udev/rules.d/52-xilinx-digilent-usb.rules
rm -f /etc/udev/rules.d/52-xilinx-ftdi-usb.rules
rm -f /etc/udev/rules.d/52-xilinx-pcusb.rules
```

Adding Additional Tools and Devices

You can incrementally add additional tools, devices or even upgrade Vivado editions post-install. This is useful for users that have chosen to install a subset of devices and/or tools.

To add new tools or devices:

- **Start Menu > Xilinx Design Tools > Vivado <version> > Add Design Tools or Devices**.
- Launch **Vivado > Help > Add Design Tools or Devices**.

If you have installed the Vivado WebPACK or Design Edition, you are presented with the option to upgrade the edition.

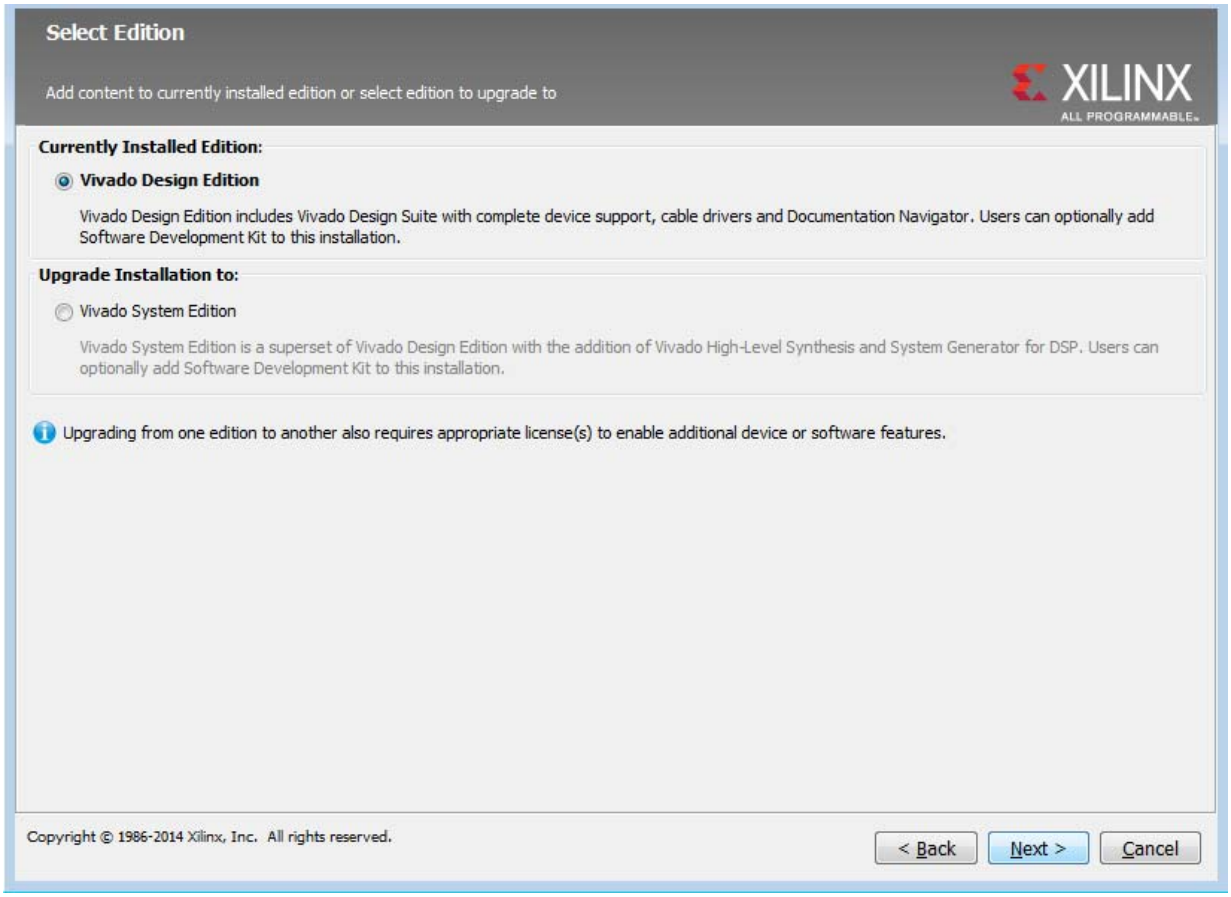

Figure 3-16: **Vivado Design Suite Installation - Select Edition**

Based on the above selection, you are presented with all available tools and devices that can be added to the current installation.

You can also add tools or devices from the Xilinx Information Center (XIC). See the Obtaining Quarterly Releases section for using this flow.

Network Installations

Installing to a network location provides a way for client machines to access the design tools by pointing to it on the network drive. To run the design tools on the network, the client machines must be set up correctly to ensure the environment variables, registry, and program groups all point to the network. The following sections describe the procedure for network setups.

Linux Clients

You must source `settings32.(c)sh` or `settings64.(c)sh` (whichever is appropriate for your operating system) from the area in which the design tools are installed. This sets up the environment to point to this installed location.

To run the design tools from a remotely installed location, run an X Windows display manager, and include a `DISPLAY` environment variable. Define `DISPLAY` as the name of your display. `DISPLAY` is typically `unix:0.0`. For example, the following syntax allows you to run the tools on the host named bigben and to display the graphics on the local monitor of the machine called mynode.

```
setenv DISPLAY mynode:0.0
xhost = bigbenPC Clients
```

Microsoft Windows Clients

1. Install design tools to a PC network server. Make sure your users know the location of the design tools and have access to the installation directory, and they have Administrator privileges for the following steps.
2. From the local client machine, browse to the following directory: `network_install_location\.xinstall\Vivado_<version>` and run the program `networkShortcutSetup.exe`.

   Running this program sets up the Windows settings batch files and **Program Group** or **Desktop** shortcuts to run the Xilinx tools from the remote location.
3. From the client machine, launch the Vivado Design Suite tools by clicking the **Program Group** or **Desktop** shortcuts, or by running the applications on the network drive.

Installing to a Mounted Network Drive

Xilinx design tools are designed to be installed in a directory under ROOT (typically `C:\Xilinx`). The installer normally presents this option when installing to a local driver.

To work around this issue, either specify a UNC path (for example, `\\network_loc\Xilinx\`) or define your target installation directory as `\Xilinx` under the network mount point (For example: `N:\Xilinx`).

Windows 7 default security levels do not allow you to select remote mapped drives. To install Xilinx Design Tools on remote mapped drives, you must change your account control settings using the following steps:

1. Open the Windows Control Panel, from the Windows Start menu, and select 'User Accounts'. If your Control Panel Uses 'Category View', click 'User Accounts' on two successive screens
2. Click 'Change User Account Control settings' and allow the program to make changes.

3. Click and slide the slide-bar down to the second to lowest setting (as seen in the following figure).
4. Click **OK**.

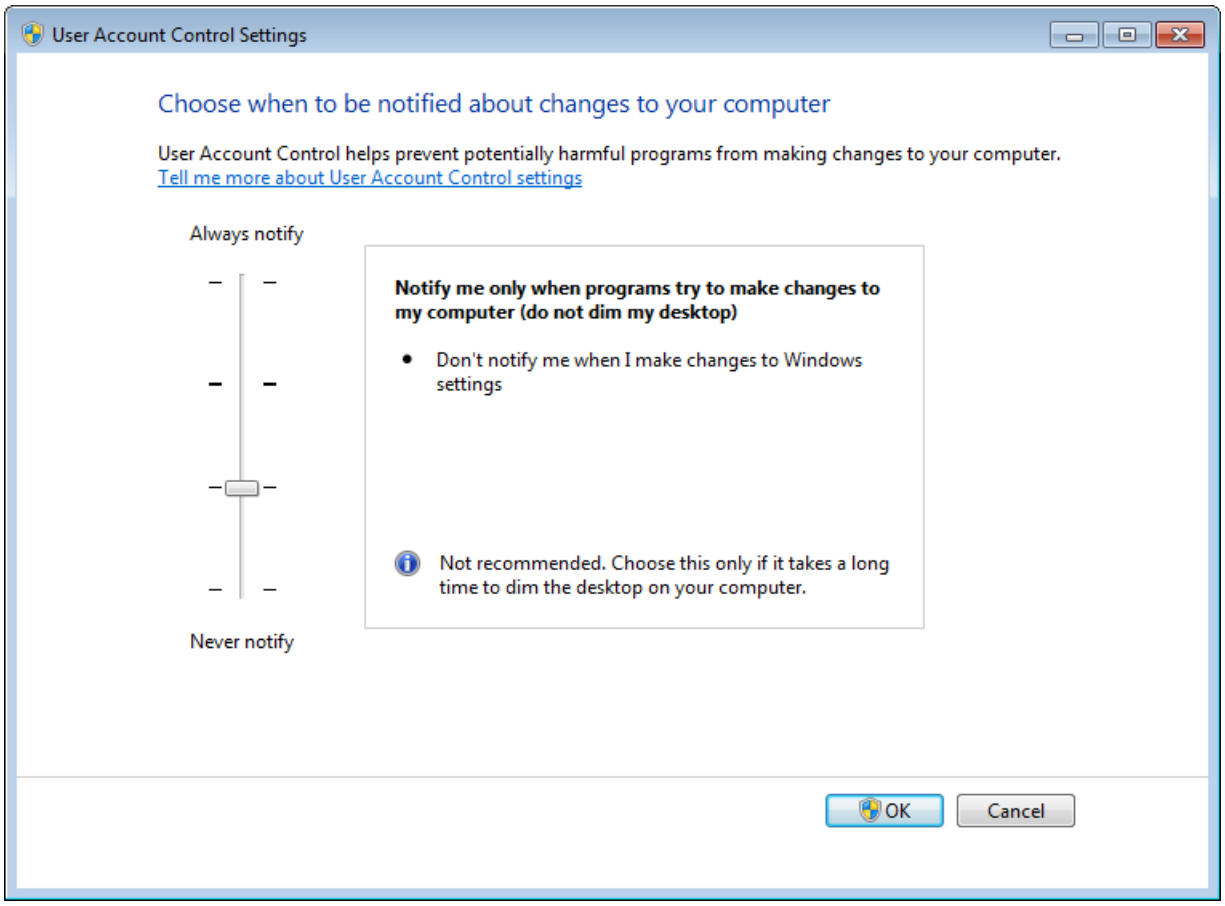

Figure 3-17: **Vivado Design Suite Installation - User Account Control Settings**

RECOMMENDED: *Xilinx recommends that you revisit this procedure to restore your settings to their previous state after installation.*

Note: You are not able to browse to the remote mapped drives using the Xilinx installer. You need to manually type in your installation path which contains a mapped network drive.

Batch Mode Installation Flow

Beginning in Vivado 2015.1, the installer can be run as an unattended batch process. To run unattended, a standard Edition and install location must be specified or a configuration file must be present which tells the installer the install location and which of the tools, devices and options you wish to install.

The installer has a mode in which it can generate a reference option file for you based on common configurations, which you can further edit to customize your installation.

RECOMMENDED: *It is recommended that you generate this reference for each new quarterly release, so that new devices, tools, options or other changes will be accounted for in your options file.*

To begin using batch mode, open a command shell and change to the directory where you have stored your extracted installer.

Note: For Windows, open the command window with administrator privileges and run the xsetup.bat file, found in the \bin directory, and not xsetup.exe with the options below.

Generate Configuration File

Run: `xsetup -b ConfigGen`

This will put you in an interactive mode where you will see the following menu. Choose an edition from the list given below.

1. Vivado HL WebPACK
2. Vivado HL Design Edition
3. Vivado HL System Edition
4. Documentation Navigator (Standalone)

After you select an edition, you will be prompted for a location/filename for your configuration file and the interactive mode will exit.

Below is a sample of a WebPACK configuration file:

```
#### Vivado WebPACK Install Configuration ####
Edition=Vivado WebPACK
Destination=C:\Xilinx
Modules=Vivado:1,Vivado High Level Synthesis:0,Software Development
Kit:0,DocNav:0,Artix-7,Kintex-7,Zynq-7000:1
#### Shortcut creation ####
CreateProgramGroupShortcuts=1
CreateShortcutsForAllUsers=0
ProgramGroupFolder=Xilinx Design Tools
CreateDesktopShortcuts=1
CreateFileAssociation=1
#### Post install tasks ####
## Post install tasks can be configured as shown below.
InstallOptions=Configure WebTalk:1,Install and Initialize Trusted Storage
Licensing:1,Generating installed device list:1,Install VC++ runtime libraries for
64-bit OS:1,Install Cable Drivers:0,Acquire or Manage a License Key:0,run:xic:1
```

Basically, each option in the configuration file matches a corresponding option in the GUI. A value of `1` means that option is selected, a value of `0` means the option is unselected.

Run the Installer

Now that you have edited your configuration file to reflect your installation preferences, you are ready to run the installer. As part of the installer command-line, you will need to indicate your acceptance of the Xilinx and Third Party license agreements, and confirm you understand the WebTalk Terms and Conditions.

Xilinx End-User License Agreement (EULA)

- Xilinx End-User License Agreement

Third Party End-User License Agreement (EULA)

- Third Party End-User License Agreement

WebTalk Terms and Conditions

> By indicating **I AGREE**, I also confirm that I have read Section 13 of the terms and conditions above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at Xilinx Design Tools Webtalk. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

There is a command-line switch, `-a` or `--agree` for you to indicate your agreement to each of the above. If one of the above is left out of the list, or the agree switch is not specified, the installer will exit with an error and will not install.

Example Command Lines

This is an example of the command line for a typical new installation using a configuration file.

```
xsetup --agree XilinxEULA,3rdPartyEULA,WebTalkTerms --batch Install  --config
install_config.txt
```

If you wish to use one of Xilinx's default Edition configurations, you do not have to specify the `--config` option, but since the destination directory is included in the configuration file, you will be required to specify this on the command-line.

```
xsetup --agree 3rdPartyEULA,WebTalkTerms,XilinxEULA --batch Install --edition
"Vivado System Edition" --location "C:\Xilinx"
```

The above command will utilize the default configuration options for the edition specified. To see the default configuration options, use the –b ConfigGen mode as described

above.The batch mode of the Vivado installer can also perform uninstallation and upgrades (adding additional tools and devices). For the full list of the options in the installer batch mode run `xsetup -h` or `xsetup --help`.

Obtaining Quarterly Releases

Xilinx releases quarterly versions of the Vivado Design Suite tools throughout the year. Each quarterly version contains device support updates, new features and bug fixes. The following sections describe how to obtain updates through the Xilinx Information Center.

Xilinx Information Center

Xilinx Information Center (XIC) is the next generation replacement of XilinxNotify. This functionality resides in the task bar (Windows) and periodically checks for new releases and updates from Xilinx. Users can view and dismiss notifications as well as update installations.

In addition, XIC now includes a cockpit from which you can manage all of your Xilinx tool installations. Update, check licenses or uninstall all from the new Manage Installs tab as shown in Figure 3-18.

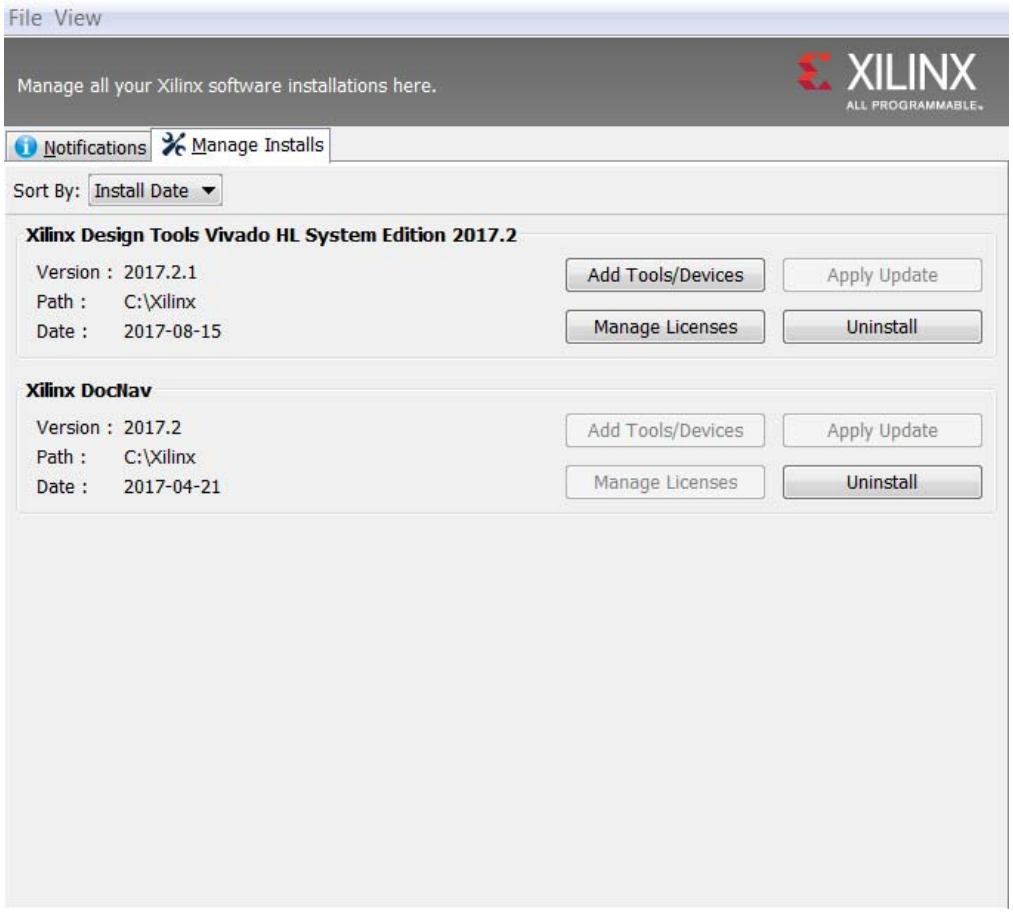

Figure 3-18: **Xilinx Information Center (XIC)**

Uninstalling the Vivado Design Suite Tool

Before uninstalling, make sure to have moved any project files you want to keep outside your Xilinx installation directory structure, or they are deleted.

Note: Xilinx Documentation Navigator is not removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. You need to uninstall it separately if it is no longer required.

Uninstallation

Before uninstalling, make sure to have moved any project files you want to keep outside your Xilinx installation directory structure, or they will be deleted. See below for information on uninstalling Documentation Navigator and Xilinx Information Center.

Uninstalling Documentation Navigator

Xilinx Documentation Navigator will not be removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. If it is no longer required, you will need to uninstall separately either from the Start Menu program group entry 'Uninstall DocNav' or through the corresponding entry in the 'Uninstall or change a program' control panel option (for Windows).

Uninstalling Xilinx Information Center

Xilinx Information Center will not be removed during uninstallation. It is intended to be a standalone application common to multiple versions of Xilinx tools. If it is no longer required, you will need to uninstall separately through the corresponding entry in the 'Uninstall or change a program' control panel option (for Windows).

Uninstalling on Microsoft Windows

To uninstall any Xilinx product, select the Uninstall item from that product's Start Menu folder. For instance, to uninstall Vivado Design Suite: Edition, select **Start > All Programs > Xilinx Design Tools > Vivado 2018.2 > Uninstall**.

If you do not have a program group entry, use the command line option to uninstall:

```
<install_path>\.xinstall\Vivado_2018.2\ xsetup.exe -uninstall
```

Alternatively, use the corresponding entry in the Uninstall or change a program control panel option (for Windows).

Uninstalling on Linux

To uninstall the Vivado Design Suite tool product, launch the uninstaller from the launcher menu: select **Applications > Xilinx Design Tools > Vivado 2018.2 > Uninstall**.

Checking Required Libraries

There may be a requirement to install dependent libraries for certain Linux operating systems. Please refer to Answer Record 66184 on the Xilinx website on how to check which libraries are required to run Vivado tools on Linux.

WebTalk

The WebTalk feature helps Xilinx® understand how you use Xilinx FPGA devices, software, and intellectual property (IP). The information collected and transmitted by WebTalk allows Xilinx to improve the features most important to you as part of our ongoing effort to provide products that meet your current and future needs. When enabled, WebTalk provides information on your use of the Vivado Design Suite tools, SDK, and Petalinux.

WebTalk Participation

Your participation in WebTalk is voluntary except when a paid license is not found.

In these cases, WebTalk data collection and transmission always occurs, regardless of your preference settings. For all other cases, data is not transmitted if you disable WebTalk.

The following table summarizes WebTalk behavior for data transmission to Xilinx from your post-route design, based on your Xilinx license, WebTalk install preference, and user preference settings.

Table 4-1: **WebTalk Behavior for Bitstream Generation or Route Design Flow**

License	WebTalk Install Preference Selected as "Enabled"	WebTalk User Preference Selected as "Enabled"	Send WebTalk Data to Xilinx
WebPACK	X	X	Yes
Edition License	No	X	No
Edition License	Yes	No	No
Edition License	Yes	Yes	Yes

Note: If the device is a WebPACK device, the Tools first look for a WebPACK license.

Setting WebTalk Install Preference

You can enable or disable WebTalk globally during or after installation as described below. During installation you can enable or disable WebTalk installation options by checking or unchecking the **Enable WebTalk to send software, IP and device usage statistics to Xilinx (Always enabled for WebPACK license)** checkbox.

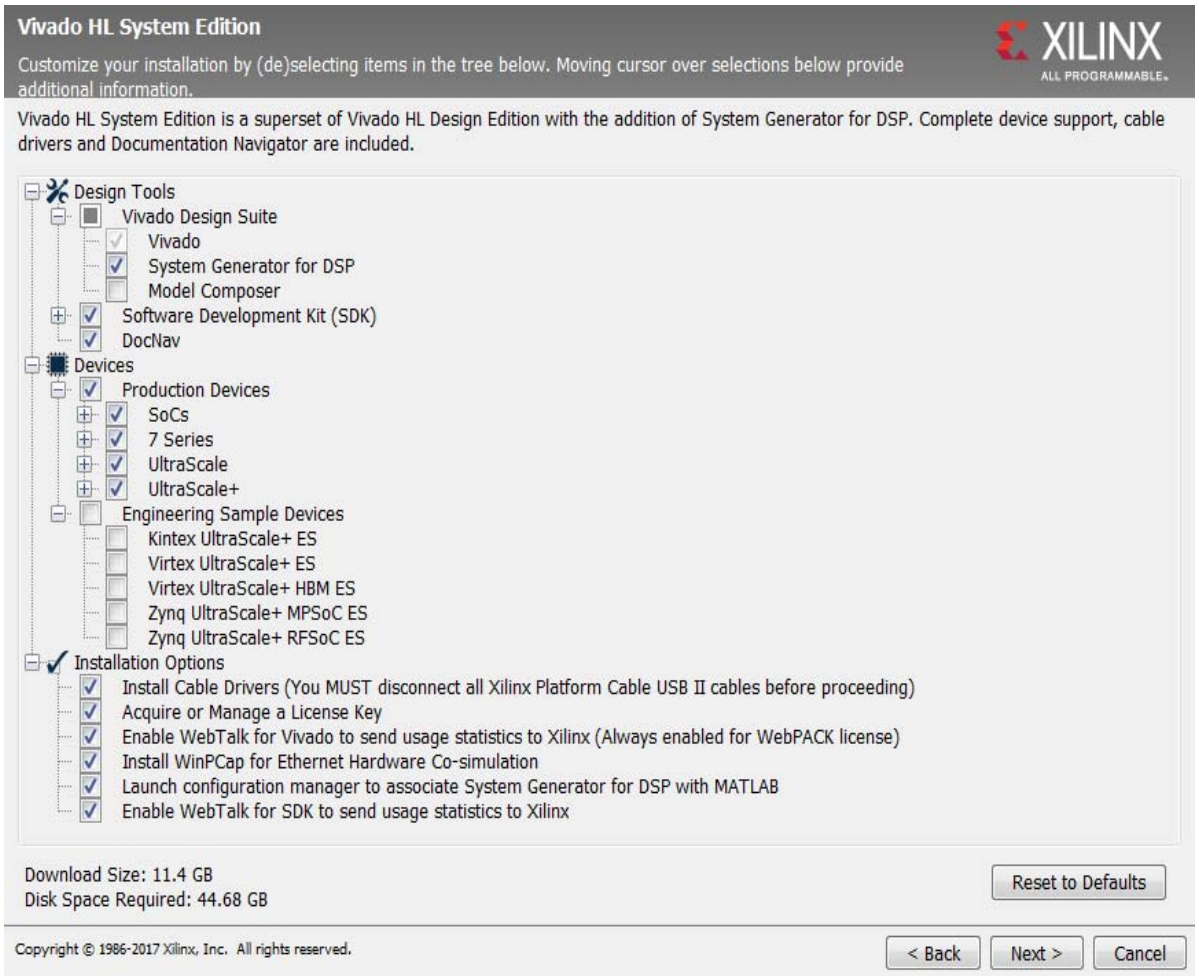

Figure 4-1: **WebTalk Install Options**

You can enable or disable WebTalk installation options using the Tcl command `config_webtalk`:

```
config_webtalk -install on|off
```

- `on` turns WebTalk on for the installation.
- `off` turns WebTalk off for the installation.

Install settings are saved in the following location:

- **Windows 7 and 10**: `<install dir>/vivado/data/webtalk/webtalksettings`
- **Linux**: `<install dir>/vivado/data/webtalk/webtalksettings`

Note: You need administrator privileges to write to the install location.

Setting WebTalk User Preferences

You can enable or disable WebTalk user options by selecting **Tools > Settings**. In the Settings dialog box, click the WebTalk category as shown in the following figure.

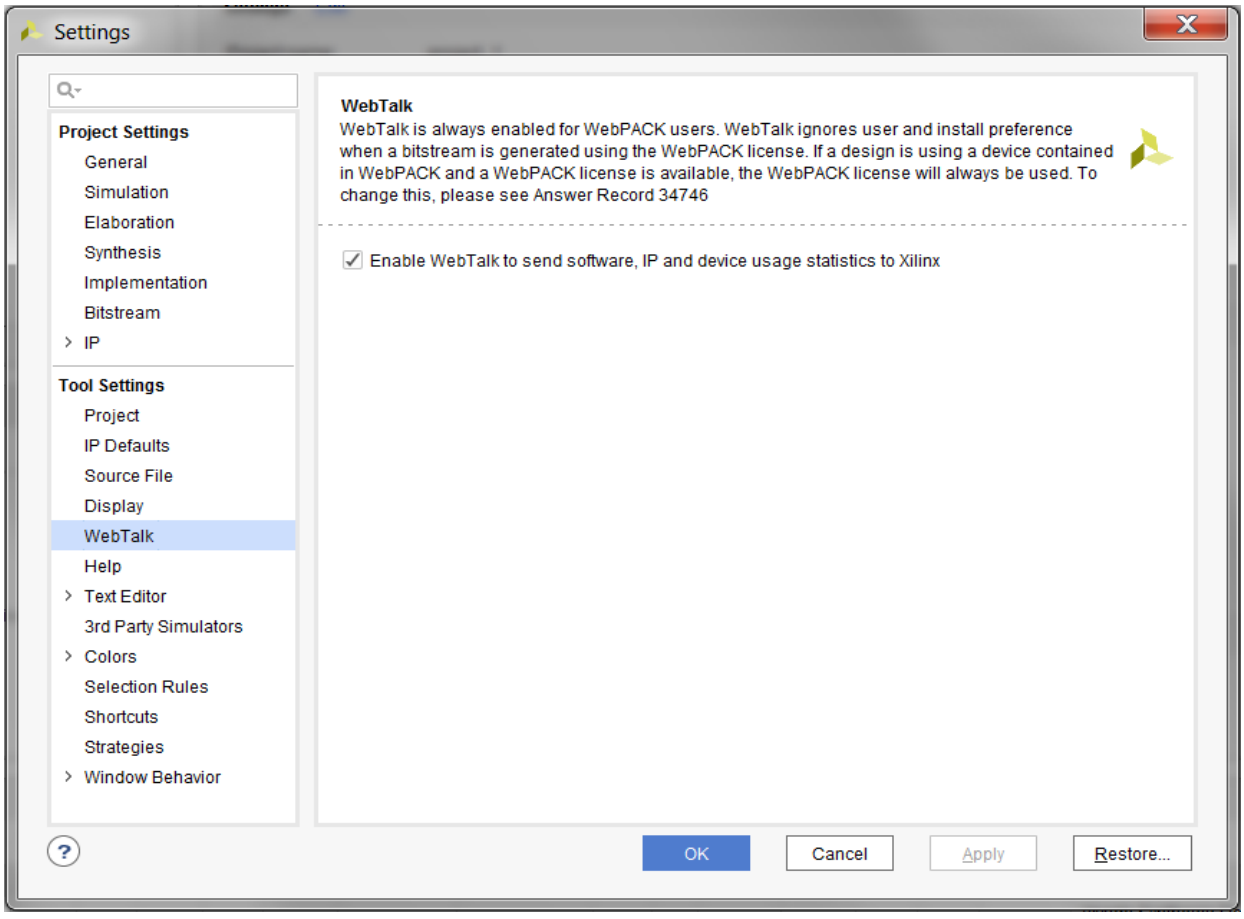

Figure 4-2: **WebTalk User Preferences**

After installation, you can enable or disable WebTalk user options using the `config_webtalk` Tcl command:

```
config_webtalk -user on|off
```

- `on` turns WebTalk on for the current user.
- `off` turns WebTalk off for the current user.

User settings are saved in the following location:

- **Windows 10 or earlier**:

  `%APPDATA%\Xilinx\Common\<version>\webtalk`

  where:

  `%APPDATA%` is:

  `C:\Users\<user>\AppData\Roaming`

- **Linux**:

  `%APPDATA%/.Xilinx/Common/<version>/webtalk`

  where:

  `%APPDATA%` is:

  `/home/<user>`

Checking WebTalk Install and User Preferences

You can also use the `config_webtalk` Tcl command to check the current status of WebTalk settings. The command line option `-info` reports the values for the install setting and the user setting:

```
config_webtalk -info
```

Types of Data Collected

WebTalk does not collect your design netlist or any other proprietary information that can be used to reverse engineer your design. The data Xilinx collects through WebTalk includes:

- Software version
- Platform information (for example, operating system, speed and number of processors, and main memory)
- Unique project ID
- Authorization code

- Date of generation
- Targeted device and family information

For more information on the type of data that is collected, see the *Xilinx Design Tools WebTalk web page* [Ref 16]. To see the specific WebTalk data collected for your design, open the `usage_statistics_webtalk.xml` file in the project directory. You can also open the `usage_statistics_webtalk.html` file for easy viewing of the data transmitted to Xilinx. Additionally, additional data collection files for sub-flows in the Xilinx tools are also generated which include:

- `usage_statistics_ext_xsim.xml`
- `usage_statistices_ext_labtools.xml`
- `usage_statistics_ext_sdk.xml`
- `usage_statistics_ext_petalinux.xml` (along with corresponding html files)

Transmission of Data

WebTalk is invoked after bitstream or route design compilation. WebTalk bundles the collected data in an `usage_statistics_webtalk.xml` file and sends this file to Xilinx by https (hypertext transfer protocol secure) post. Every new compilation for a given design overwrites the previous `usage_statistics_webtalk.xml` file. WebTalk also writes an HTML file equivalent `usage_statistics_webtalk.html` file for easy viewing of the data transmitted to Xilinx. WebTalk also writes to the `vivado.log` (or `runme.log`) file that contains additional information about whether the file was successfully transmitted to Xilinx.

XILINX

Chapter 5

Obtaining and Managing a License

The Xilinx® Product Licensing site is an online service for licensing and administering evaluation and full copies of Xilinx design tools and intellectual property (IP) products. This chapter describes the FLEXnet license generation functionality of the Product Licensing Site.

Licensing Overview

Product Licensing

Xilinx enforces the Xilinx End-User License Agreement at run time in the Xilinx design tools using certificate-based licensing.

- **Certificate-Based Licenses**: This is the license enforcement method Xilinx introduced for the ISE® Design Suite in the ISE 11.1 release. A certificate, commonly referred to as a "license file (`.lic`)" is issued from the Xilinx Product Licensing Site. The certificate is matched to a given machine, server or licensing dongle using your entering host-id which uniquely identifies the machine. This license certificate must remain present on the machine and in the license search path, because the Vivado tools need access to this file to check for a valid license feature during run time.

Note: Flex-ID Dongle licensing for Xilinx Software is supported only on Windows platforms.

IMPORTANT: *Starting with Vivado 2017.3 - Activation Licensing support has been removed. Existing activation licenses have been replaced with certificate based license that can be accessed from* www.xilinx.com/getlicense.

Certificate Licensing Terminology

- **Host ID**: An identifier, placed within certificate licenses, which binds the license to the computer using this identifier. Typical identifiers are: Hard-drive volume ID, Ethernet port MAC address, or USB Dongle ID.
- **Node-Locked License**: A node-locked license allows for the use of a single seat of a product entitlement on a specific machine.

- **Floating License**: A floating license resides on a network server and enables applications to check out a license when they are invoked. At any one time, the number of licenses for simultaneous users is restricted to the number of license seats purchased.
- **License Rehosting**: The act of changing the host ID of a generated license due to machine hardware changes, hard-drive failure or the moving of a license from one machine to another.
- **License Deletion**: The act of removing a license from a machine, and having the entitlement placed back into the Xilinx Product Licensing Account.
- **Affidavit of Destruction**: A click through agreement by which you certify that the license file (.lic) for a rehosted or deleted license will be destroyed and no longer used.

Generating/Installing Certificate-Based Licenses

For certificate-based licenses, as long as you know the Flexera Host ID (Ethernet MAC ID, Drive Serial Number or Dongle ID) you want to lock your license to, you do not need to enter the Xilinx License Management site from one of our utilities. Instead, go directly to www.xilinx.com/getlicense. After logging in and selecting your account, you can select products as described in the Product Selection section.

After one or more licenses are selected on the Create New Licenses page, click the **Generate License** button corresponding to the type of license file you are generating (client/node-locked or server/floating).

The step-by-step instructions below are for generating a floating certificate-based license as this process contains a superset of all other certificate-based license generation flows.

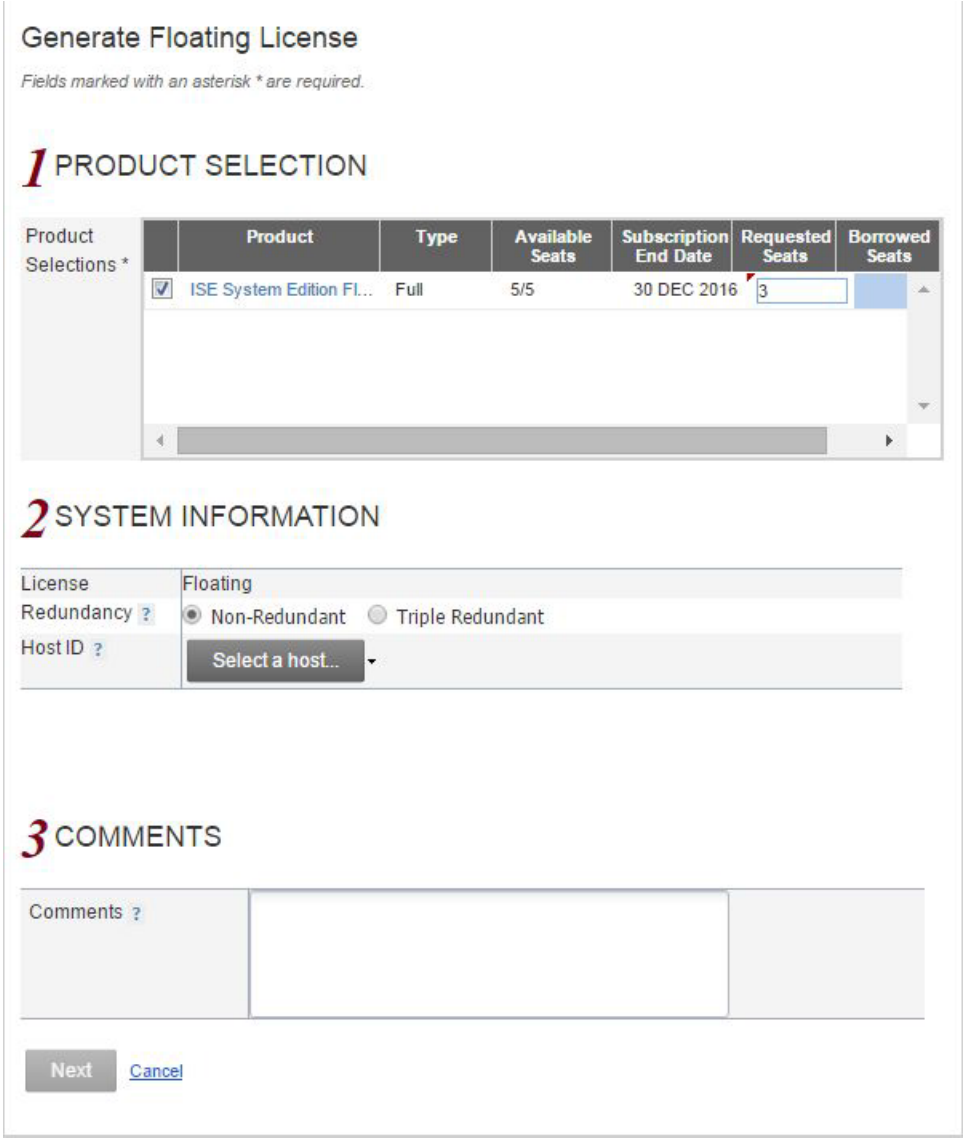

Figure 5-1: **Generate Certificate-Based Floating License**

Certificate-Based Node Locked License

After generating a license file, you will receive an email from 'xilinx.notification@entitlenow.com'.

1. Save the license file (.lic) attached to the e-mail to a temporary director y on your local system.
2. Run the Vivado License Manager:
   - For Windows 10 or earlier: **Select Start > All Programs > Xilinx Design Tools > Vivado 2018.2 > Manage Xilinx Licenses**.

- Windows 8.1: Run the **Manage Xilinx Licenses** app from the full listing of Apps on your Start screen.
- For Linux: Type vlm in a command-line shell.

3. On the left hand pane of Vivado License Manager, expand **Getting a License** and choose **Load License**.
4. If you received a certificate license (`.lic`) file, click the **Copy License** button on the Load License screen.
5. Browse to your license file (`Xilinx.lic`) and click **Open**.
6. This action copies the license file to the `<Homedrive (typically C)>:\.Xilinx (Windows)` or `<Home>/.Xilinx` directory of your computer where it will be automatically found by the Xilinx tools.

Certificate-Based Floating License

1. Select the number of seats required for each product license.

   This is for floating licenses only. All node-locked licenses are for one seat. The number of seats available for a product entitlement is automatically maintained by the system. The Requested Seats field is populated, by default, with zero, although you are allowed to enter any number up to the full number of seats remaining on the product entitlement. A product is removed from the product entitlement table once all seats have been generated.

2. Enter system information.

   For floating certificate-based licenses, the first field is redundancy. A triple-redundant server configuration, also known as a triad, provides a fail over for the license manager software. As long as two of the three servers are running, the license manager can continue to run. This does not apply to node-locked licenses.

   The system information is pre-populated in the Host ID drop-down menu if you arrived at the Product Licensing Site from a link within the Vivado License Manager. If you do not have pre-populated system information, or if you want to add a different host, select the **Add a host** option.

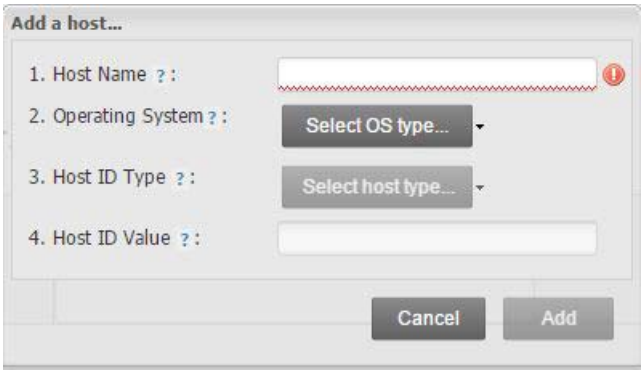

Figure 5-2: **Add a Host**

The Host ID value uniquely identifies the machine to which your design tools or IP is licensed. You can choose a Host ID Type to be a MAC address, a hard drive serial number or a dongle ID.

Note: Not all host ID types are supported for all operating systems. The easiest way to obtain your host ID is to run Vivado License Manager on the machine that serves as the license host.

3. Add a comment.

   Adding a comment to the license key file makes it easier for an administrator to track the allocation of design tools and IP product entitlements among users.

4. Click **Next**.

   The Review License Request form opens, as shown in Figure 5-3.

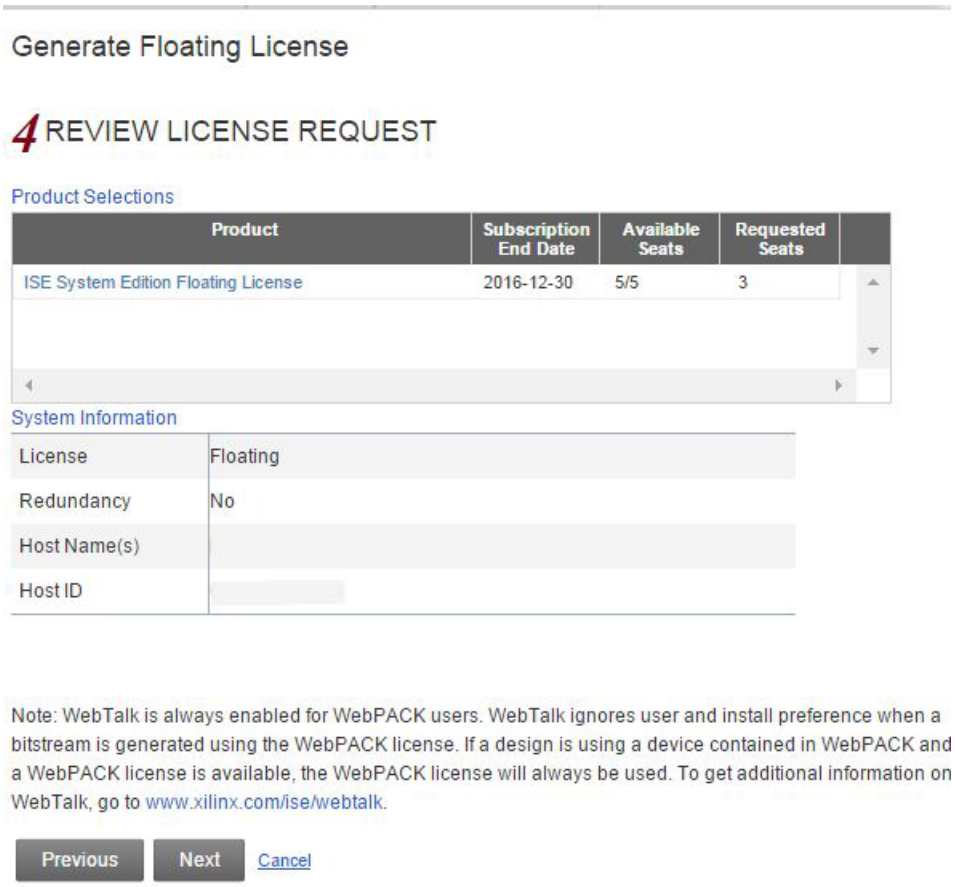

Figure 5-3: **Review License Request**

5. Review your selections.
6. If you are satisfied with your selections, click **Next**.

End-User License Agreements

Xilinx Design Tools and No Charge IP product End User License Agreements (EULAs) are agreed to during the product installation process. A complete copy of this license agreement is located at: `<install directory>/.xinstall/Vivado_2018.2/data/unified_xilinx_eulas.txt`.

If you license IP products, you must accept the terms of the associated IP product EULAs before the license file can be generated.

Third-Party Licenses

A complete copy of the third-party licenses is located at: `<install_directory>/.xinstall/Vivado_2018.2/data/unified_3rd_party_eula.txt`.

License Generation Confirmation

When you finish generating the licenses, you receive a confirmation message summarizing your licensing activity.

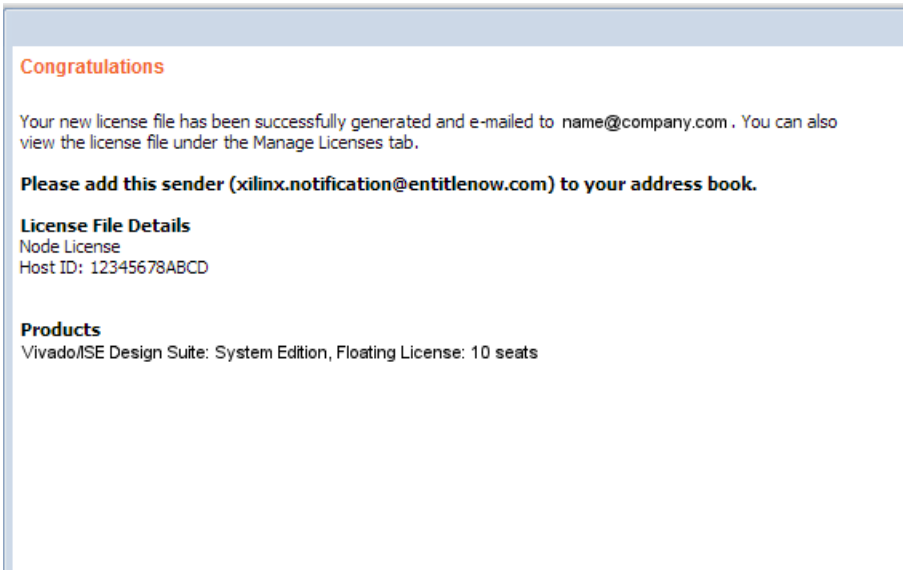

Figure 5-4: **License Generation Confirmation**

You will also receive a license generation confirmation email. This message contains the generated license key file as an attachment. Add xilinx.notification@entitlenow.com as a trusted sender in your email address book.

If you do not receive your license by email, you can download it directly from the Xilinx Licensing Site. See the Managing Licenses on the Xilinx Product Licensing Site section for details.

Serving Certificate-Based Floating Licenses

For existing FLEXnet license servers serving certificate-based licenses, a common practice is to copy the contents of the license file, mailed from `xilinx.notification@entitlenow.com`, into the existing license file on your FLEXnet server.

Note: Restart the floating license server to ensure the new Xilinx licenses are enabled.

For New License Servers

1. Download the appropriate Xilinx FLEXnet license utilities for your server's operating system from the Xilinx Download Center at Downloads.
2. Unzip these utilities into a destination directory. Xilinx recommends you place this directory into your application search path.
3. After the FLEXnet utilities are installed, run the following commands to start the floating license server:
   - Linux

```
<Server Tool directory>/lnx64.o/lmgrd.sh -c <path_to_license>/<license file>.lic -l
<path_to_license>/<log filename>1.log
```

   - Windows

```
<Server Tool directory>\win64.o\lmgrd -c <path_to_license>\<license filename>.lic -
l <path_to_license>\<log filename>.log
```

Client Machines Pointing to a Floating License

1. Run the Vivado License Manager (VLM).
2. Click the Manage Xilinx Licenses tab.
3. On the Manage Xilinx Licenses tab, enter the network path to the license server in the port@server format into the `XILINXD_LICENSE_FILE` field.
4. Click **Set**. The default Xilinx port number is 2100.

For Linux operating systems, licensing environment variables cannot be set using the Vivado License Manager (VLM). The environment variable fields are read only, so they are grayed out and there are no **Set** buttons. The environment variable must be set using the appropriate OS shell and commands.

Managing Licenses On Your Machine

Vivado License Manager

The Vivado® License Manager (VLM) is intended to assist with license generation for Certificate-based licenses only.

Vivado License Manager is installed with Vivado Edition and many standalone tool installations. The following figure shows the VLM.

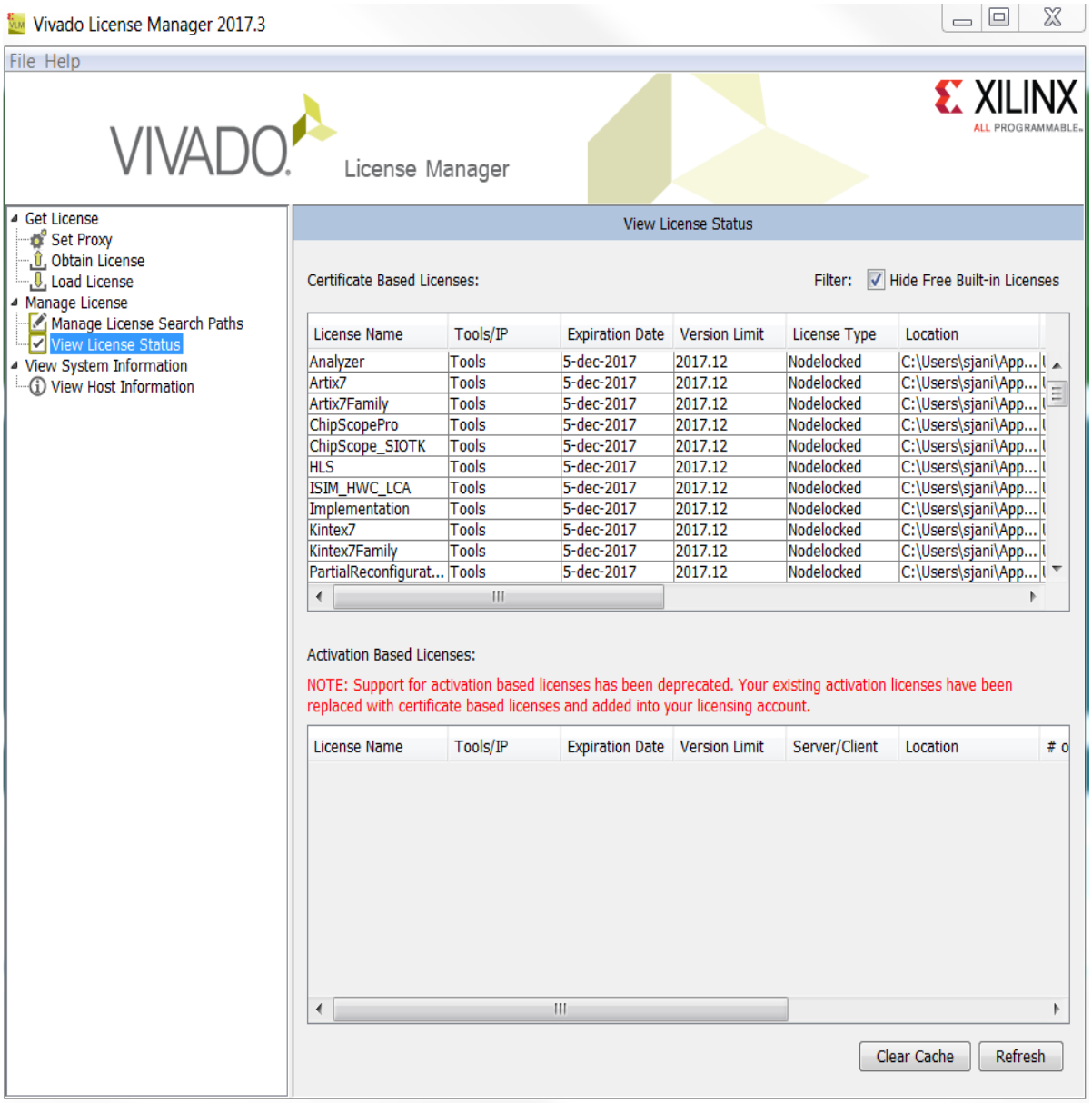

Figure 5-5: **Vivado License Manager**

To Open the Vivado License Manager:

- On Linux, type `VLM` from a command-line shell that has the Xilinx environment loaded.
- On Windows 10 or earlier, you can run this from the Start menu at **Start > Xilinx Design Tools > Vivado 2018.2> Manage Xilinx licenses**.

- On Windows 8.1, run the **Manage Xilinx Licenses** app from the full listing of Apps on your Start screen. You can also run Vivado License Manager from the Help menu of Vivado: **Help > Obtain A License Key** or **Help > Manage License**.

The typical tasks that Vivado License Manager is used for are:

- **Obtaining A License**: Choose from several license options and go to the Xilinx Product Licensing Site to complete the license generation process.
- **Viewing License Status**: See which licenses are visible to the local machine. This is a useful view for debugging licensing issues.
- **Loading Licenses Onto a Local Machine**: After a certificate license (`.lic`) file has been received, it can be placed into the appropriate location on the machine. For step-by-step instructions, see the Installing Your License key section for your license type below.
- **Viewing and Setting (Windows) License Search Locations**: Vivado tools will look in several default locations to try to find authorization to run. If your license is located elsewhere on the machine or on a floating license server, a path to that license must be specified.

RECOMMENDED: *It is recommended that the `XILINXD_LICENSE_FILE` environment variable be used to specify Xilinx license file locations. `LM_LICENSE_FILE` can also be used, but is mainly intended for non-Xilinx or legacy license path use.*

Using the Xilinx Product Licensing Site

The Xilinx Product Licensing site is where certificate based licenses are generated, where certificate-based licenses are modified and where information about license orders reside.

You can access the Xilinx Product Licensing Site in various ways depending upon the type of license being generated.

- If you purchased products which use certificate-based licenses, follow the link included in your order confirmation email. It provides direct access to an account containing your product entitlements.
- To evaluate the Vivado® Design Suite products, go to the Vivado Design Suite Evaluation and WebPACK page.
- To evaluate IP products, go to Intellectual Property page and follow the Evaluate link on the IP product page of interest.
- To access the Product Licensing Site directly, go to https://www.xilinx.com/getlicense. By accessing the site this way, you will be able to create certificate-based licenses as well as perform license account management functions.

When entering the Xilinx Product Licensing Site, you must first register or enter your registration information.

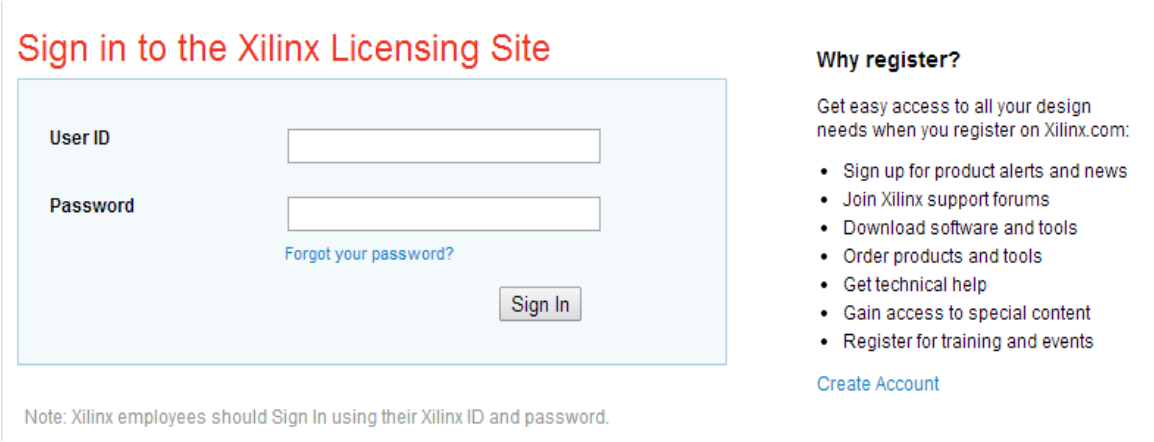

Figure 5-6: **Xilinx Product Licensing Site - Sign In Page**

5. You must first sign in. If you already have a Xilinx user account, enter your user ID and password, and then confirm your contact information is current. If you do not have an account, click the **Create Account** button.

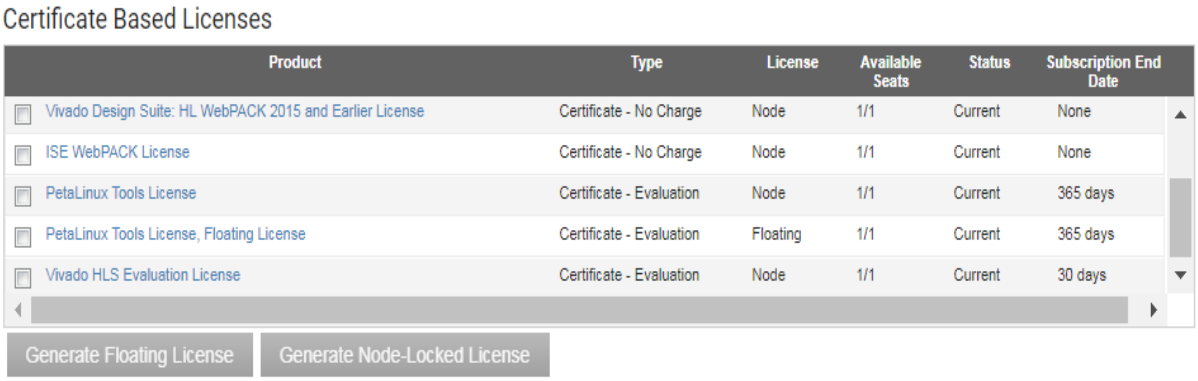

Figure 5-7: **Create New License**

Product Selection

To begin the license generation process for products you have purchased or want to evaluate:

1. Select a product licensing account from the Account drop-down list.

   Note: This selection is not available if you are entitled to evaluation or free products only.

2. Enter product voucher codes for design tools or IP product licenses purchased with kits or for tools purchased from the Xilinx online store (optional).

3. Add evaluation or no-charge IP product entitlements to the product entitlement table (optional).

4. Make your product selections from the product entitlement table.

Entitlement is available for following category: Certificate-based licensing. The type of product entitlements available are Full (purchased), No Charge, or Evaluation. Full and No Charge licenses have a subscription period of one year. Design tool evaluation is for 30 days and IP evaluations are for 120 days.

Floating/server and node-locked/client licenses cannot be combined in the same license file. Selecting an entitlement that contains only one license type causes the **Generate** button for the other license type to become inactive.

For design tools, available seats represents the number of seats available for licensing over the total number of seats purchased. For IP, seats are managed according to the terms of the site-wide license agreement.

Products with a status of **Current** are within their warranty period. Products with a status of Expired have a warranty period end date that has passed. If seats are available, licenses can be generated for either Current or Expired product entitlements.

The Vivado Design Suite: 30-Day System Edition evaluation product entitlement provides access to all the capabilities in the Vivado Design Tools. This product entitlement is automatically included in your product licensing account.

Product vouchers for design tools and IP product licenses can be shipped with a Xilinx or partner development board or design kit. If you have a product voucher card, you can enter the voucher code on the card into the associated text field and click **Redeem Now**. This places the corresponding design tools or IP product entitlement in the product entitlement table which you can use to generate a license key.

To add Evaluation and No Charge IP to the list of product entitlements, click the **Search Now** button in the Add Evaluation and No Charge IP Cores section of the page. This opens an IP product finder tool.

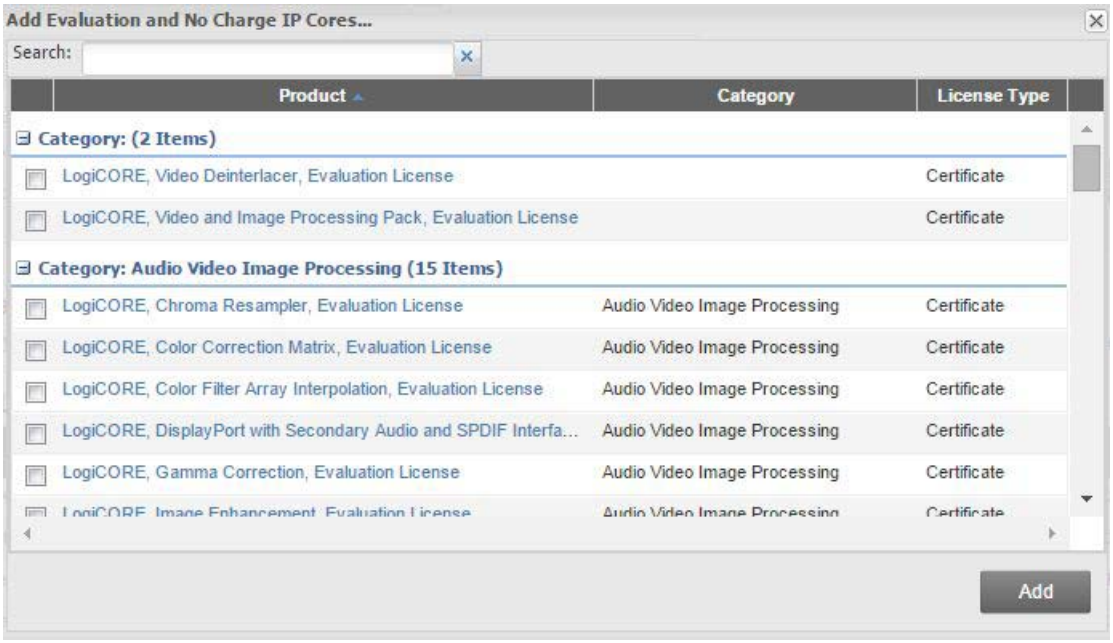

Figure 5-8: **IP Product Selector**

Managing Licenses on the Xilinx Product Licensing Site

The Xilinx Product Licensing Site tracks the licenses that you have generated. Select the Manage Licenses tab to see all licenses generated in your product licensing account.

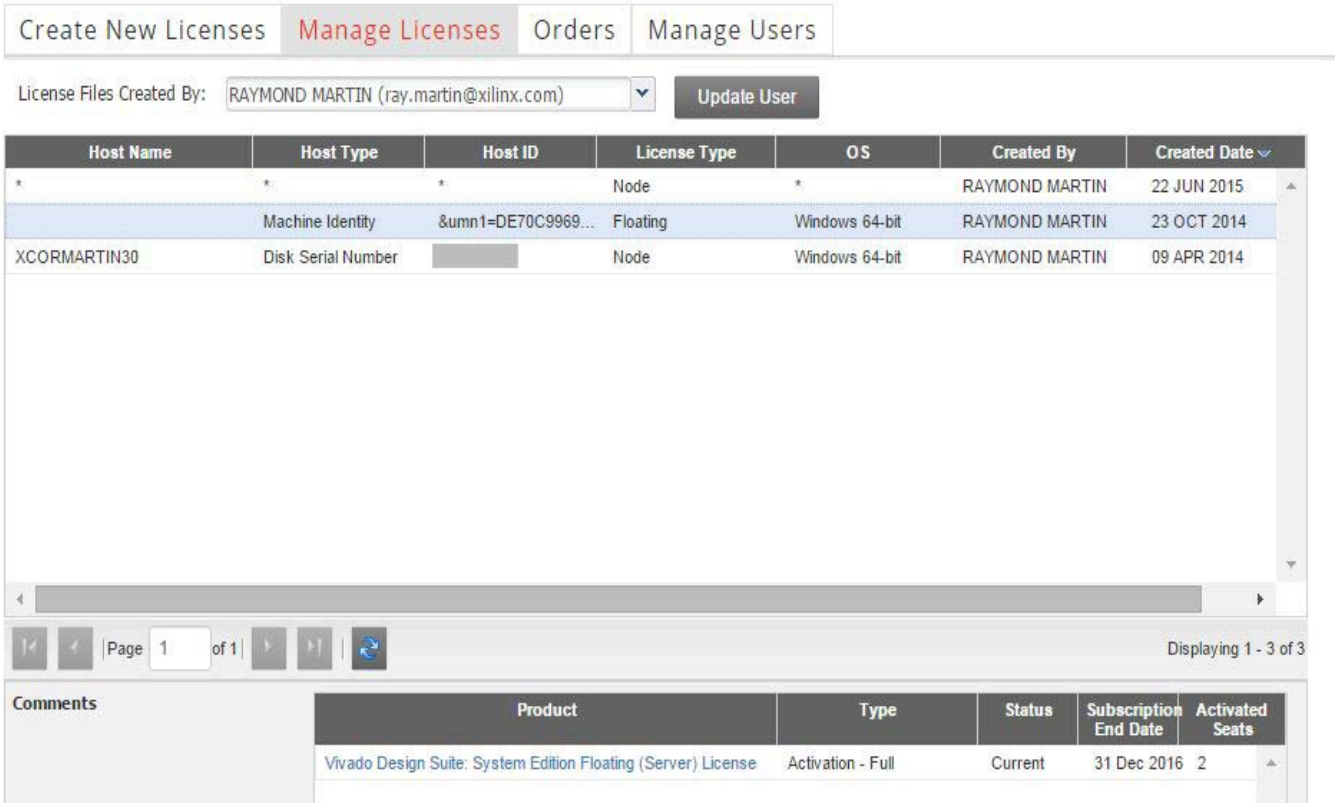

Figure 5-9: **Manage Licenses**

Use the Manage Licenses page to perform the actions described below.

Exploring and Retrieving Your Existing Licenses

Information regarding the licenses in your product licensing account are displayed in a split-section view. Click a row in the master view in the top table, to see detailed information about the licenses in the detail view in the bottom table. The detail view table displays:

- A list of product entitlements enabled by file.
- Comments associated with the file.

The detail view table gives you the ability to:

- Download - If your license file does not arrive through email you can download it here.
- Email - Have the license file emailed to you or another user.
- View - Gives you the ability to view the actual license file.

- Delete - Delete the license file. After a file is deleted the entitlement will then become available on the Create New License page and can be regenerated for another host ID. 
- View the end user license agreement (IP only).

Modifying Licenses

To modify an existing certificated-based license, select the license file in the master view. You can modify a certificated-based license as follows:

Delete Entire License File and Place Entitlement Back into Your Account

1. From the Manage Licenses Tab (see Figure 5-9), select the license file you wish to delete.
2. Click the **Delete** button  located below and to the left of the license file details.
3. Click the **Accept** button to accept the Affidavit of Destruction.

Note: This will delete all license seats in the entire license file and return the entitlements to your account.

Rehost: Change the Node-Locked or License Server Host ID for a License File

1. From the Manage Licenses Tab (see Figure 5-9), select the license file you wish to rehost.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **System Information**.
4. Change or add new Host ID and/or Host Name by using the drop-down list and text entry boxes respectively.
5. Click the **Next** button twice and then click **Accept** to accept the Affidavit of Destruction.

Add Additional Seats to an Existing Licensed Product Entitlement

1. From the Manage Licenses Tab (see Figure 5-9), select the license file to which you wish to add seats.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. For floating licenses, you will be able to change the Requested Seats field and add seats up to the total number of seats available in your entitlement.
5. Click **Next** twice. No Affidavit of Destruction is required for adding seats.

Remove Seats From an Existing Licensed Product Entitlement

1. From the Manage Licenses Tab (see Figure 5-9), select the license file from which you wish to remove seats.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. For floating licenses, you will be able to change the Requested Seats field and reduce the number of seats that will be authorized by this license file.
5. Click the **Next** button twice and then click **Accept** to accept the Affidavit of Destruction.

Add Additional Product Entitlements to a License Key File

1. From the Manage Licenses Tab (see Figure 5-9), select the license file to which you wish to add features/entitlements.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. Check boxes of any new entitlements you wish to add to this license file.
5. Click **Next** twice. No Affidavit of Destruction is required for adding features.

Delete Product Entitlements From a License Key File

1. From the Manage Licenses Tab (see Figure 5-9), select the license file to which you wish to delete features/entitlements.
2. Click the **Modify License** button. The Modify License screen appears.
3. Go to **Product Selection**.
4. Check boxes of any entitlements you wish to remove from this license file.
5. Click the **Next** button twice and then click **Accept** to accept the Affidavit of Destruction.

Modifying a key file uses the same input form as when the license key file was created, except that additional product entitlements of the same license type (floating or node-locked) are made available for adding to the license file.

Reclaiming Deleted License Components

A product entitlement is deleted when one of the following occurs:

- Changing the license server host for a license key file.
- Removing seats from an existing licensed product entitlement.
- Deleting product entitlements from a license key file.

When you delete seats or remove products from your certificate-based license files, the entitlement is essentially "put back" or reallocated into your licensing account. You will find that the number of entitled seats in the Create New Licenses tab of your account is incremented by the same number of seats you deleted previously from existing license files.

Before the reallocation of entitlement occurs, you must first agree to an Affidavit of Destruction. This legal agreement is required to ensure the deactivated product entitlements are no longer being used.

The number of allocation operations is recorded for each user. Administrators are allowed to reallocate product entitlements five times per major release. End users are allowed to reallocate product entitlements three times per major release.

What Happens to Your License Key File

Each time a license is generated for a product entitlement, a FLEXnet increment line and corresponding package line is added to the license key file. When a license key file is modified to add seats for an existing or new product entitlement, additional increment or package lines are added to the license key file.

When a license key file is rehosted or is modified to delete seats or product entitlements, the corresponding increment lines are regenerated or removed from the modified license key file.

Your Licensing Account

Product Licensing Accounts

When you purchase a design tool edition or IP product from Xilinx, you are purchasing a license to use and receive updates for that product for one year. The license to use Xilinx deign tools and IP products is managed through the use of product entitlements. A product entitlement is the determination of:

- Which product was purchased
- The number of seats purchased
- The license type (certificate based, floating, or node-locked)
- The product subscription period (product updates are provided throughout the year)

In addition to managing the product entitlements for your purchased design tools and IP, you can also access product entitlements for No Charge or Evaluation products. Full and No Charge licenses have a subscription period of one year. Design tools evaluations are for 30 days, and IP evaluations are for 120 days.

Generating a license from a product entitlement results in one or more license keys being generated by the website. When installed, the license keys enable the use of the design

tools and IP that were purchased or are being evaluated. Your product entitlements and resulting license key files are managed in a product licensing account on the Xilinx website.

Product licensing accounts are specific to the individual listed on the Xilinx Software Purchase Order, who is either the end-user or administrator of the design tools. All purchases made can be managed in the same product licensing account if a single administrator is named. A company site can have multiple accounts managed by different administrators. The latter is helpful if a site has multiple design teams working on differing projects with different budget pools.

Note: A license can be generated for a product entitlement that has expired; however, it only enables product releases up to the subscription end date. Applying a product update made available after the subscription end date of your license will result in a licensing error the next time the tool is used.

LogiCORE IP License Generation in the Xilinx Design Tools

Any LogiCORE™ IP and design tools entitlements you have purchased appear in your list of entitled products when you log into the Product Licensing Site. Currently, all IP entitlements will generate certificate-based licenses. Licenses for Evaluation and No Charge IP are available on the site in a separate area. Licenses for all your certificate-based design tools and IP can now be generated in one pass. They are emailed to you in a single license file.

User Types and Actions

There are three user types for the Product Licensing Site: customer account administrator, end user, and no-charge user.

Customer Account Administrator

An example of a typical customer account administrator is a CAD tools manager. Every product licensing account must have at least one customer account administrator. A customer account administrator can manage more than one product licensing account.

The responsibilities as the customer account administrator include:

- Generating node-locked or floating licenses for Xilinx design tools and IP products.
- Adding and removing users from the product licensing account.
- Assigning administrative privileges to other users.

The original customer account administrator is the Ship To contact identified during the product ordering process. That person receives an email with instructions on how to download and license each purchased product. The customer account administrator must follow the link in the email, to ensure access to the purchased products.

End User

Adding end users to a product licensing account allows an engineer or design team member the flexibility to manage and generate license keys on their own. The end user can generate license keys for node-locked products entitlements within the account as well as evaluation and "no charge" license keys for design tools and IP products. A customer account administrator can also configure the end user account to allow an end user to generate floating licenses. An end user cannot:

- View or generate floating license keys by default. This privilege can be assigned to them by the customer account administrator.
- View the license keys generated by other users.
- Add or remove other users to or from the product licensing account.

No-Charge User

No-Charge users can:

- Generate a 30-day free evaluation license key that enables Vivado System Edition.
- Generate a 30-day free evaluation license that enables Vivado HLS.
- Generate license keys for evaluation and no charge IP products.
- Generate a WebPACK™ tool license that enables WebPACK features in both ISE and Vivado.

All user types can download products electronically.

Note: A customer who is already licensed for a full version of a Xilinx Design Tools product edition can evaluate other Xilinx Design Tools product editions or IP. These product entitlements are made available in the same product licensing account.

Changing Xilinx User Account Information

IMPORTANT: *It is important to keep your Xilinx User Account up to date. As you change companies, addresses or emails might change.*

Modifying Your Corporate Email Address

1. Go to www.xilinx.com.
2. Click **Sign In**.
3. Expand **Personal Information**.
4. Enter your new corporate email address in the **Enter new Corporate email address** box.
5. Click **Save Profile** button for changes to take effect.

Understanding Your Tool and IP Orders

The Orders tab displays information regarding the purchasing orders that created the entitlements you see in this account.

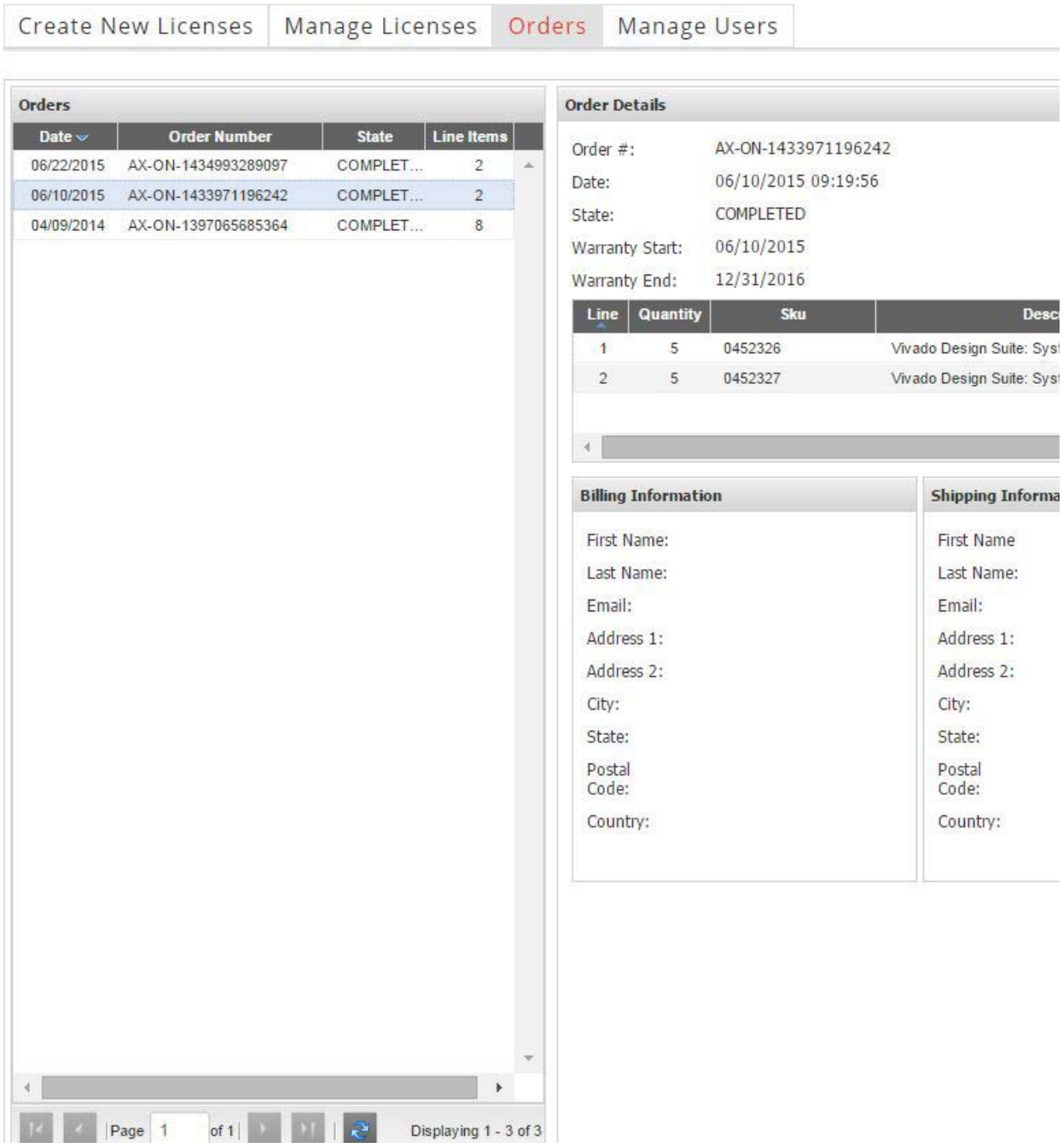

Figure 5-10: **Orders**

- Xilinx order numbers are listed on the left panel of the screen.

- Order details populate on the right panel of the screen when you highlight specific order.
- You might only select one order at a time.
- The order's shipping address information is visible even when product is delivered electronically.

Managing User Access to Product Licensing Account

The responsibility of administering a product licensing account can be transferred or shared with another user. The ability to add or remove users from a product licensing account is managed under the Manage Users tab.

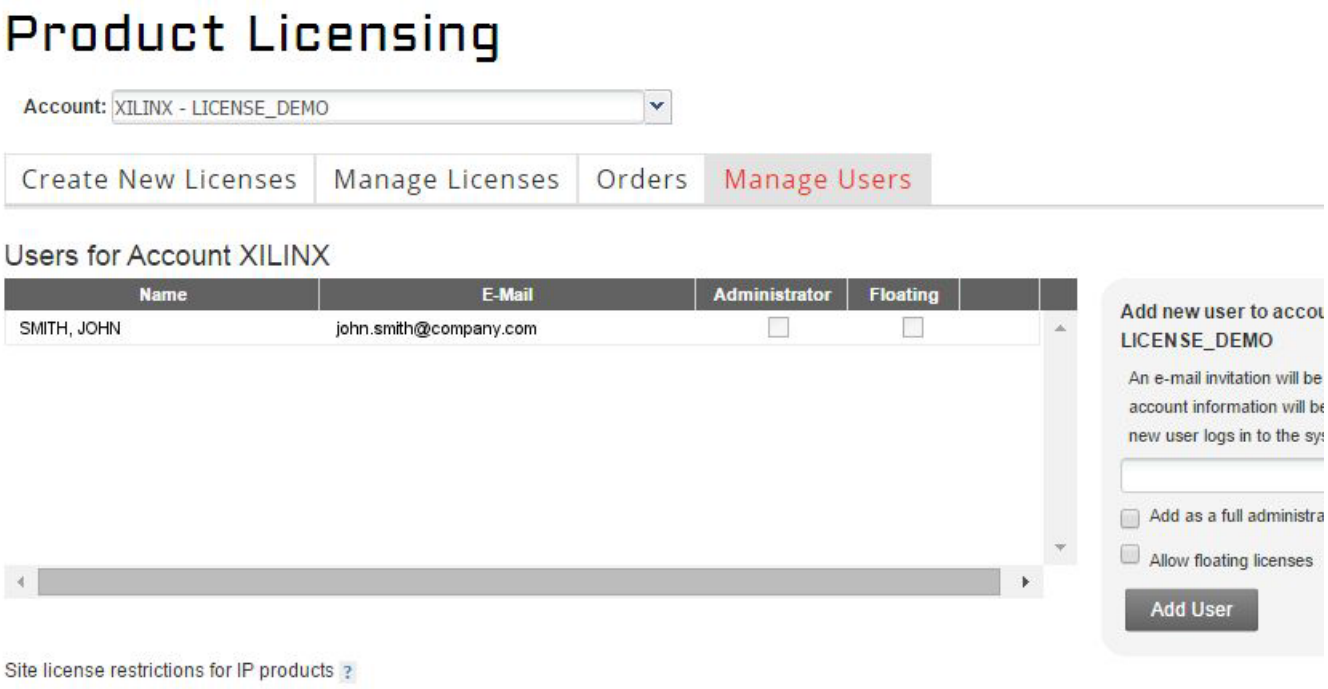

Figure 5-11: **Manage Users**

Adding Users

To add a user to your product licensing account:

- Type in the corporate email address of the new user.
- Check **Add as a full administrator**, to grant the new user customer account administrative privileges. Check **Allow Floating Licenses**, to grant the new user the ability to generate Floating Licenses, but not have full administrative privileges.

Note: The email address you provide must be the same email address the user supplied or supplies when creating their Xilinx account. If not, you might not be properly recognized when logging in.

If added users have already logged into the Product Licensing Site, their name appears in the user list. If they have never been to the site, the words Not Yet Registered appears in the space for their name. After they registered, their name is filled in.

In some instances, a customer account administrator might wish to have design team members administer license key files for their own use. By leaving both Add as full administrator and Allow Floating Licenses check boxes unchecked, you grant the user the following restricted privileges:

- User can generate node-locked license keys only.
- User can view and modify only those license key files they generated for themselves.
- User cannot manage users.

If you check Allow Floating Licenses only, the restriction on node-locked keys is lifted, but the others remain. You cannot check both boxes because it is not allowed. Full administrators already have floating license generation capability.

Removing Users

To remove administrative or floating license generation privileges from a user, uncheck the **Administrator** or **Floating** check box for that user.

To remove a user from a product licensing account, click the **Delete** button for that user.

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Chapter 6

Older Release Notes

Release Notes 2018.1

What's New

Vivado® 2018.1 introduces the new Zynq® UltraScale+™ RFSoC and Virtex® UltraScale+™ HBM devices. This release includes numerous advancements to improve quality of results and runtime reduction of UltraScale+ devices. Vivado 2018.1 also has additional ease of use improvements to ensure you can increase your overall efficiency and get your products to market faster.

The following devices and features are also updated in this release.

Device Support

This release of Vivado introduces the Zynq UltraScale+ RFSoC and Virtex UltraScale+ HBM devices. Additional devices are also enabled for the XA Spartan®-7 Family.

New devices introduced in this release:

- Virtex UltraScale+ HBM:
  - XCVU37P ES1
  - XCVU33P ES1
  - XCVU35P ES1
  - XCVU31P ES1
- Zynq UltraScale+ RFSoC:
  - XCZU21DR
  - XCZU25DR
  - XCZU27DR
  - XCZU28DR
  - XCZU29DR

- XA Spartan-7:
  - XA7S6
  - XA7S15
- XC Spartan-7:
  - XC7S6
  - XC7S15

The following devices are in production:

- Zynq UltraScale+ MPSoC:
  - XCZU11EG (-3)
  - XCZU15EG (-3)
  - XCZU17EG (-3)
  - XCZU19EG (-3)
- Kintex® UltraScale+:
  - XCKU3P (-3)
  - XCKU5P (-3)
  - XCKU11P (-3)
  - XCKU13P (-3)
  - XCKU15P (-3)
- Virtex UltraScale+:
  - XCVU3P (-3)
  - XCVU5P (-3)
  - XCVU7P (-3)
  - XCVU9P (-3)
- Artix®-7 and Spartan-7:
  - XC7A25T (-2LE (0.9V))
  - XC7A12T (-2LE (0.9V))
  - XC7S100 (-1,-2)
  - XC7S75 (-1,-2)
  - XC7S25 (-1Q)
  - XA7S25 (-1I, -2I, -1Q)

  - XA7A25T (-1I, -2I, -1Q)
  - XA7A12T (-1I, -2I, -1Q)

The following devices are enabled in Vivado WebPack:

- Artix-7:
  - XC7A12T
  - XC7A25T
- XA Artix-7:
  - XA7A12T
  - XA7A25T
- XA Spartan-7:
  - XA7S25

Vivado Tools

System Generator for DSP

- FFT/IFFT blocks updated to use new FFT/IFFT LogiCORE IP v9.1

Model Composer

- **View, Analyze and Compare Fixed-point Signals**: Leverage Simulink's data logging and visualization features like Signal Logging, Simulation Data Inspector, Scope, Displays, To Workspace blocks and Port value displays to log, visualize and compare arbitrary precision HLS fixed point data types in the design.
- **New Computer Vision blocks**: 5 additional reVISION xfOpenCV functions added into the Computer Vision library - Dense Non-Pyramidal LK Optical Flow, Histogram Equalization, Erosion, Dilation, Otsu Thresholding.
- **New Example Design**: Lucas-Kanade (LK) Dense Optical Flow for motion detection, showcases the use of blocks from Model Composer library as well as the custom C/C++ code import feature for building synthesizable designs.
- **Integer Overflow Detection**: Enable detection of Saturation and Wrap on Integer Overflow for Sum, Subtract, Product, Gain and Data Type Conversion blocks in the design using Simulink's Data Validity Diagnostics.
- **Parameterization in C/C++ Code Import**: Create custom Model Composer blocks, through the C/C++ Code Import feature, that support scalar, vector and matrix parameters which enables flexible and rapid exploration of parameter space in simulation.

- **Function Template Support in C/C++ Code Import**: Create custom Model Composer blocks that support simulation with multiple data types through use of function templates in source code, enabling rapid exploration of data types, including fixed-point, in designs.
- **Enhancements for Trigonometric Blocks**: Expanded data types supported for Trigonometric blocks: atan, atan2, cos, cosh, sin, sinh, tan.
- For more details on the features above, please refer to the *Model Composer User Guide* (UG1262) [Ref 21] and the individual block documentation.

Vivado HLS

Up to 2017.4, FIFO depths requested by the designer by using e.g. the depth=N argument of the #pragma HLS stream, or the -fifo_depth argument of config_dataflow, were automatically incremented to N+1 in the RTL generation step. This caused a mismatch between the user request, the depth as displayed by the GUI (which was the same as what was requested by the user), and the actual depth in the RTL. With 2018.1 this increment of the depth no longer occurs. **This means that some designs may now deadlock**, if the designer had specified a depth on N in order to get a depth of N+1. These designs must now be changed, by modifying either the Tcl commands or the pragmas used to specify the FIFO depths, so that the requested depth is now N+1.

Integrated Design Environment

- Streamlined and organized menus will improve your Vivado experience. Subcategories were added to the File menu to shorten the menu. A new Reports menu categorizes and consolidates all Vivado reports under a single menu.
- Set up and configure custom command toolbars using Tcl. Include these Tcl commands in your Tcl App install and uninstall procs, and execute your Tcl App with a single button click.

Power Analysis and Xilinx Power Estimator (XPE)

- Analyze power for Zynq UltraScale+ RFSoC devices with new, intuitive interfaces for the RFADC-DAC and SD-FEC cores.
- Analyze power for Virtex UltraScale+ HBM devices. XPE provides separate power totals for the FPGA and HBM device portions.

Vivado IP Integrator

- Ports and Block Diagram elements can now be pinned onto the canvas to prevent them from moving during schematic re-draws. Now user diagrams can accurately represent data flow through the design.

- Selectively upgrade IP on your BD canvas. Choose which IP to upgrade and when to do it dependent on your design schedule.
- Enhanced Find dialog lets you perform detailed searches on your Block Design. Use basic search or advanced regular expressions to help traverse designs.
- IP Packager can now archive all sources used in creating packaged IP.
- Can package designs that include RTL module referencing.
- Preliminary support for VHDL-2008 and SystemVerilog in IP Packager.

Board Flows and Example Designs

- FMC connector support added to reference boards.

Simulation Flows and Verification IP

- Accelerate your verification by utilizing clock & reset VIPs to generate different clocks and reset signals in your design.
- Simulation flow in Vivado has added support for Cadence's Xcelium Parallel Simulator.

Vivado Simulator

- Improve your verification time by visualizing the call stack, the stack frame and scoped variables with three new windows available in Vivado Simulator.

RTL Synthesis

- User encoded states will now persist even if there are DONT_TOUCH or MARK_DEBUG attributes present.
- Reduce DSP utilization in MACs by applying attributes in the RTL or constraints in the XDC file by using the new DSP folding feature.
- Automatically infer Read-Write Address collision glue logic by applying attributes to BRAMs.

Implementation

- Better UltraScale+™ performance with 2018.1, average Fmax is roughly 5% higher than 2017.4.
- Improved performance from using report_qor_suggestions, average 4% Fmax gain when following suggestions.
- Vivado 2018.1 has new techniques for improving UltraScale and UltraScale+ SSI designs.

    - It is now possible to use Laguna TX_REG registers to directly drive RX_REG registers for UltraScale+ devices only but not UltraScale. Prior to 2018.1 this was not permitted due to possibility of un-fixable hold violations but the router now has the ability to adjust clock delays on Laguna registers. Usage must be restricted to single-clock crossings, not intended for CDCs.
    - Prevent SLR-crossing violations using the USER_SLR_ASSIGNMENT cell property which assigns hierarchical cells to SLRs and prevents them from being partitioned across SLRs. This is a soft constraint which gives both the placer and physical optimization greater flexibility to replicate and improve performance.
- For faster design closure, direct opt_design to target specific timing failures and netlist complexity. New fine-grained controls are provided for small LUT collapsing (fewer logic levels), SRLs, register chains, and control sets. Also new in opt_design are optimizations to balance DSP pipeline registers.
- If you do not require repeatable results, you can use the route_design -ultrathreads option to speed up the router. This option causes small variations in routing between subsequent identical runs. Runtime savings are dependent on design and device size.

Static Timing Analysis

- Ensure all timing exceptions are valid and have been appropriately applied. Track your process using Report Exceptions in the GUI by cross-probing to the constraints in the XDC file.
- Simplify huge reports by waiving known safe DRCs, CDCs, and Methodology Violations.

Vivado Debug

- Vivado flow now generates and synthesizes debug IPs in parallel. This feature enhances the existing process by reducing the time it takes for implementing debug IPs when no-cache is available.
- Multiple/Separate Debug Networks - allows users to create physically separate debug networks in their design to block or allow access to specific debug cores.
    - Useful for datacenter applications to control access of debug cores by making specific debug IPs only visible to certain users while hiding the rest from others.
    - Supports the setup of independent debug networks both in a standalone and partial reconfiguration design.
    - Support for Xilinx Virtual Cable (XVC) communication used for remote debugging.

Hierarchical Design Flows

- Two new IP are available for Partial Reconfiguration solutions.

  - PR AXI Shutdown Manager IP – safely handles AXI4MM and AXI4Lite interfaces on a Reconfigurable Partition when it is undergoing PR, preventing system deadlock that can occur if AXI transactions are interrupted by PR.
  - PR Bitstream Monitor IP – can be used to identify partial bitstreams as they flow through the design. This information can be used for debugging or system applications such as blocking bitstream loads.
- Additional device support added for Partial Reconfiguration.
  - Full range of Zynq UltraScale+ RFSoC devices supported.
  - Virtex UltraScale+ HBM VU37P is available as beta, bitstreams gated by default.

Xilinx Parameterized Macro

- AXI Stream support is now native in XPM_FIFO.
- XPM_FIFO reset sequence is improved, to work under noisy clock/reset conditions.
- XPM_MEMORY max size increased to 192Mb.

Intellectual Property (IP)

- New capability (write_ip_tcl) XCI-based IP into a Tcl script which can be sourced to re-create the XCIs. This helps in difference IP versions and tracking parameterization changes more easily.
- New AXI Sideband Utility, used to automatically add/recover parity and/or Master ID bits on the USER fields.
- AXI SmartConnect, area-optimized for smaller switches.
- AXI DMA and CDMA now support larger than 8MB transfer sizes.
- HBM flow now supported in both IPI and RTL flows.
- New 10G Time Sensitive Networking with 10G Ethernet MAC and PCS Subsystem. Implements 802.1 CM profile for 5G wireless applications. Includes 802.1Qbu (preemption) and 802.3br (interspersed express traffic) specifications.
- New 100G KP4 RS(544, 518) Reed-Solomon Forward Error Correction (RS-FEC) supporting 100GAUI-4 Interface used for 100GBASE-KP4 implementations. Allows for connection to PAM-4 signaling with external Bitmux chip. Included with IEEE 802.3j 100G KR4 FEC.
- New 10G clause 74 Forward Error Correction used with Ethernet MAC and PCS for backplanes and copper cabling applications.
- New dynamically switchable 1G/10G Ethernet PCS/PMA IP.

Xilinx Embedded Software and Tools

- SDK Infrastructure Updates
- Cable Support
- OS Hypervisor Aware Debugging
- BootGen
- MicroBlaze
- Tools Support
  - PetaLinux/Vivado/SDK BSP support for ZCU104, enabling this low-cost VCU evaluation board.
- U-Boot
- Linux
- Yocto
- PetaLinux

Table 6-1: **Components and New Features**

Component	Version/New-features
Compiler Toolchain (gcc)	• GCC 7.2, GLIBC 2.26, Binutils 2.29
FreeRTOS	• Upgraded to Version 10.0
Linux Kernel	• Upgraded to V4.14 Kernel • 4.14 Rebase Tree • Drivers ◦ DDR EDAC (ECC) support for 16 bit RAM devices ◦ QSPI QUAD PAGE PROGRAM (QSPI x4 Writes MTD driver) ◦ 10G/25G Ethernet 1588 MCDMA Linux driver • FPGA Manager ◦ Xilinx HW Security enforced boot flow. ◦ NIST Sha3 Authentication support. ◦ "Encrypted & Authenticated" bitstream loading support

Table 6-1: **Components and New Features *(Cont'd)***

Component	Version/New-features
U-Boot	• Upgradeed to 2017.11 • Security Enhancements ◦ Xilinx HW Security enforced boot flow. ◦ PPK/SPK revocation check for Images and bitsteam. ◦ Authenticated and Encrypted Images/bitstream loading support. • Drivers ◦ Ethernet Fixed link feature ◦ U-Boot Drivers wiki page added • New Flash devices support added
Yocto	• Upgraded to 2.4 (Rocko)
PetaLinux	• Host OS support: RHEL/Cent OS - 7.2, 7.3, 7.4 • Yocto 2.4 based Rootfs • Re-factored the packagegroup and added new package groups • PetaLinux BSP's are now updated with meta-xilinx machines • device-tree-generation recipe is deprecated. ◦ device-tree recipe upgraded to use DTG. ◦ device-tree-generation_%.bbappend recipe is renamed to device-tree.bbappend. • Sysroot generation option PetaLinx ◦ Can be used for Linux application development.

- Xen
- OpenAMP
- LibMetal
- FSBL
- PMU Firmware
  - PMU support for Ultra96, enabling this low-cost, small form-factor evaluation board.
  - PMUFW support for ZCU1275, enabling the Caher characterization board.
  - Watchdog recovery mechanism for PMU, recovery in addition to triple-redundancy.
- Power Management
  - Power Off Suspend to RAM support for Zynq UltraScale+ MPSoC, enabling an extremely low power state.

  - Wake from LAN/USB support for Zynq UltraScale+ MPSoC, enabling additional low power designs.
  - RPU restart support for xpm_ForcePowerdown, enabling additional RPU resume options.
  - Config Object support for RPU, allowing RPU to be Power Management “aware”
- System Software
  - 200 MHz SD support for FSBL, u-boot, and Linux, broadening the mode support.
  - x1 and x2 mode support in QSPI, broadening the mode support.
  - IV and AES key reuse avoided, in conformance to specs.

Important Information

Licensing

The Vivado 2017.3 and beyond releases introduces the following changes in licensing that are listed below:

- Starting with Vivado 2017.3, activation licensing is no longer supported. Existing activation licenses have been replaced with certificate based license that can be accessed from www.xilinx.com/getlicense.
- Flexera version for license management tool has been upgraded to 11.14.1. Vivado 2017.3 is the last release that will support Solaris operating system for Flex license management tools. Xilinx will continue to support Window and Linux operating systems for Flex license management tools.
- Anyone using floating license will require to upgrade licensing utilities to Flex 11.14.1. These new licensing utilities are available on download page of www.xilinx.com.
- Please note that Flex version upgrade does not affect valid license files, in other words, existing valid license files will work just fine with Vivado 2017.3 release after you upgrade licensing utilities.

Vivado Naming Conventions

The following are the required naming conventions when working with the Vivado Design Suite. Failing to follow these naming conventions might introduce potential risk to the design or the tool, and cause unpredictable behavior in the design flow.

- Source files names must start with a letter (A-Z, a-z) and must contain only alphanumeric characters (A-Z, a-z, 0-9) and underscores (_).

- Output files names must start with a letter (A-Z, a-z) and must contain only alphanumeric characters (A-Z, a-z, 0-9) and underscores (_).
- Project names must start with a letter (A-Z, a-z) and must contain only alphanumeric characters (A-Z, a-z, 0-9) and underscores (_).
- Project directory names must start with a letter (A-Z, a-z) and should contain only alphanumeric characters (A-Z, a-z, 0-9), tilde (~) and underscores (_).

CAUTION! *The Windows operating system has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use the shortest possible names and directory locations when creating projects, defining IP or managed IP projects, or creating block designs.*

The following characters are not supported for project, file, or directory names:

- ! # $ % ^ & * ( ) ` ; < > ? , [ ] { } ' " |
- tab (\t)
- return (\r)
- new line (\n)
- / or \ (As part of the directory or file name rather than as a path delimiter)

The following character is not supported for directory names:

- . (dot as terminal character)

The following character is not supported for file or project names:

- @

Note: In the Vivado IDE, the @ character is not supported for new file or project names. The Vivado IDE does allow an existing file on disk that uses the @ character to be added to a project. The Vivado IDE can open a project that includes the @ character in the project name. Using the Tcl Console, you can create a project with a name that contains the @ character.

IMPORTANT: *Spaces in directory and file names are supported by the Windows operating system. However, you should avoid using spaces in order to preserve portability of the project or files between the Windows and Linux operating systems.*

The Vivado Design Suite supports the use of forward slashes (/) as path delimiters for both Windows and Linux platforms. Backslashes (\) are allowed as path delimiters on the Windows platform only.

Any characters not explicitly mentioned above are not supported for project, file, or directory names.

Vivado Design Suite Documentation Update

In the 2018.1 Vivado Design Suite Documentation release, not all documentation will be available at first customer ship. Use the **Update Catalog** button in DocNav to stay up-to-date with the 2018.1 documentation suite.

Known Issues

Vivado Design Suite Tools Known Issues can be found at Answer Record 70860.

Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

Licenses and End User License Agreements

The third-party licenses govern the use of certain third-party technology included in and/or distributed in connection with the Xilinx design tools. Each license applies only to the applicable technology expressly governed by such license and not to any other technology. You must accept the terms of the End User License Agreements (EULAs) for Xilinx design tools and third-party products before license files can be generated.

To view the third-party license details and EULA, see End User License Agreement.

To view the Xilinx design tools license details and EULA, see https://www.xilinx.com/cgi-bin/docs/rdoc?v=2018.2;d=end-user-license-agreement.pdf.

Registered Guest Resources

To view source packages which may be referenced in the Xilinx 3rd party licenses EULA, see https://www.xilinx.com/products/design-tools/guest-resources.html.

References

1. *UltraFast Design Methodology Guide for the Vivado Design Suite* (UG949)
2. *UltraFast™ High-Level Productivity Design Methodology Guide* (UG1197)
3. *UltraFast Embedded Design Methodology Guide* (UG1046)
4. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
5. *Vivado Design Suite User Guide: High-Level Synthesis* (UG902)
6. *Vivado Design Suite User Guide: Partial Reconfiguration* (UG909)
7. *Vivado Design Suite Tutorial: Partial Reconfiguration* (UG947)
8. *Vivado Design Suite User Guide: Hierarchical Design* (UG905)
9. *Vivado Design Suite User Guide: Model-Based DSP Design Using System Generator* (UG897)
10. *Vivado Design Suite User Guide: Implementation* (UG904)
11. *Vivado Design Suite User Guide: Power Analysis and Optimization* (UG907)
12. *IP Release Notes Guide* (XTP025)
13. *Platform Cable USB II Data Sheet* (DS593)

14. *Parallel Cable IV Data Sheet* (DS097)
15. Xilinx Download Center
16. Xilinx Design Tools WebTalk page
17. Vivado Design Suite QuickTake Video Tutorials
18. Vivado Design Suite Documentation
19. *PS and PL-Based 1G/10G Ethernet Solution* (XAPP1305)
20. *Secure Boot of Zynq-7000* SoC (XAPP1175)
21. *Model Composer User Guide* (UG1262)
22. *PetaLinux Tools Documentation: Reference Guide* (UG1144)

Training Resources

Xilinx provides a variety of training courses and QuickTake videos to help you learn more about the concepts presented in this document. Use these links to explore related training resources:

1. Designing FPGAs Using the Vivado Design Suite

Please Read: Important Legal Notices