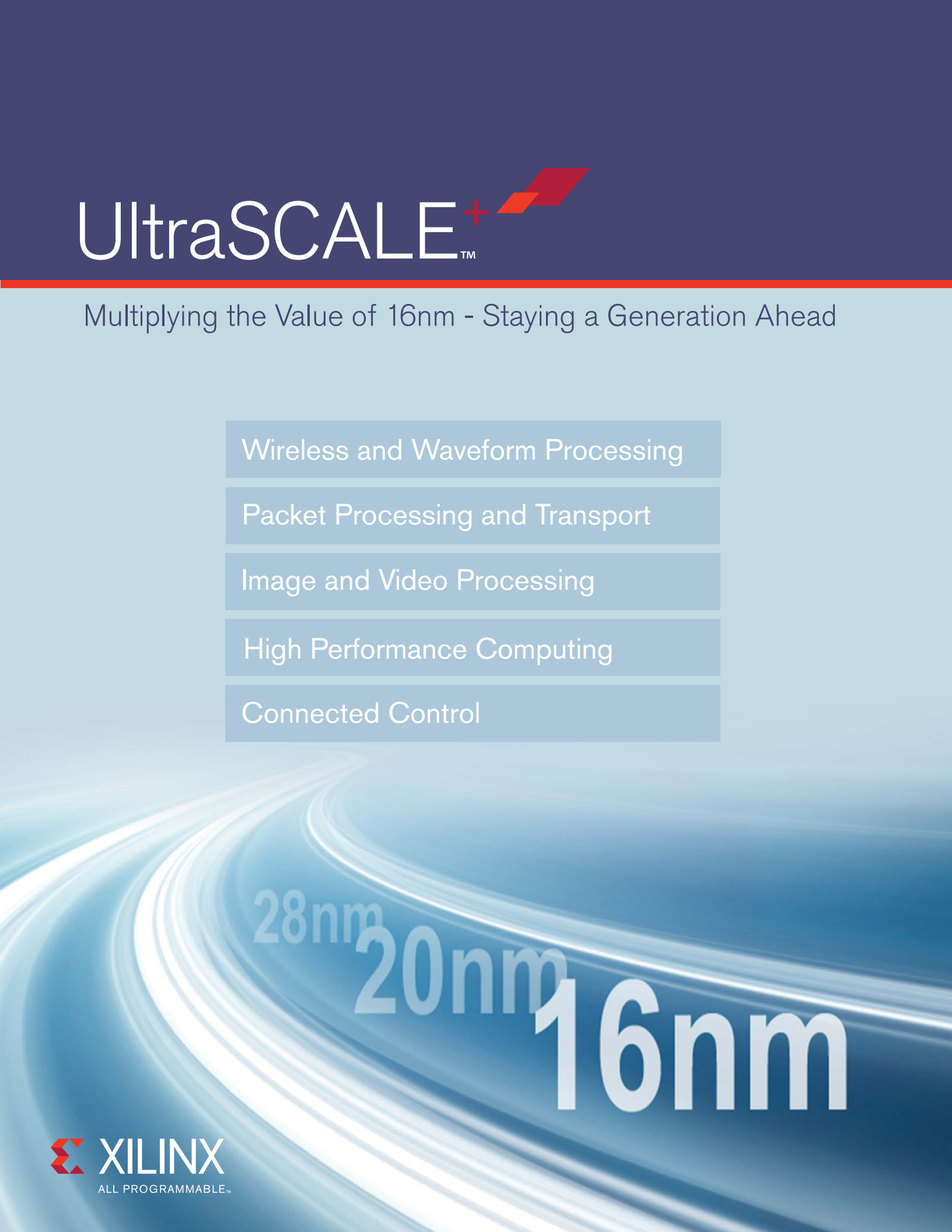
UltraSCALE+™

Multiplying the Value of 16nm - Staying a Generation Ahead

- Wireless and Waveform Processing
- Packet Processing and Transport
- Image and Video Processing
- High Performance Computing
- Connected Control



XILINX
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	Wireless and Waveform Processing	Value Multipliers	Key Applications
FPGA	**Domain-Optimized Integrated Blocks** ▪ Enhanced DSP performance with over 20 TMACS ▪ VCXO for external clock clean up ▪ Tx phase interpolator and fractional PLL ▪ UltraRAM and cascadable block RAM for deep buffers and configuration **Domain-Optimized Capabilities** ▪ 491MHz pushbutton timing closure in low-power speed grade and up to 825MHz in normal speed grade ▪ SRL for efficient filter implementation ▪ W-Mux DSP48 for efficient complex filter implementation ▪ UltraRAM for fiber length delay compensation **Key I/O & Connectivity Interfaces** ▪ Support for 12.5G transceivers in low-power speed grade (CPRI, JESD204B) ▪ Up to 128 transceivers with 33G support (25G Ethernet, 16/25G CPRI, 25G JESD204B/C, 28G backplane) ▪ Transceivers are interface agnostic and clock independent (X2/bank) ▪ 2666Mb/s DDR4 and HMC 1.0/2.0 memory interfaces	▪ Up to 2.5X greater system performance/watt ▪ Up to 60% fabric performance improvement ▪ Up to 86% increased DSP capability ▪ Up to 50% power reduction 4.5X more transceiver lanes ▪ 2X increased bandwidth ▪ Up to 20% BOM cost reduction ▪ Up to 25% smaller devices through integrated IP ▪ 2X efficient realization from Vivado® Design Suite w/ Vivado HLS & SDx™ Design Environment during algorithm development	**Wireless** ▪ Multi-standard, multi-antenna radio ▪ AAS, DAS, repeaters ▪ Microwave modem eBand modem Switching and aggregation (C-RAN/V-RAN) ▪ C-RAN **Aerospace and Defense** ▪ RADAR ▪ Electronic warfare (EW) ▪ Intelligence, surveillance, reconnaissance (ISR) **Test and Measurement** ▪ Instrumentation
MPSoC	**Key Processing Elements** ▪ Quad-core ARM® Cortex®-A53 + NEON for application, OAM, and control plane ▪ Power management unit to dynamically optimize power ▪ Dedicated configuration security unit (CSU) for IP, waveform, and tamper protection ▪ Dual-core ARM Cortex-R5 real-time coprocessor for wireless protocol software ▪ ARM Mali™-400MP GPU cores for radio GUI **Processing Ecosystem** ▪ 64-bit Linux, MVL, WL, and OSE support ▪ Processor-based DPD estimation engine ▪ OpenGL ES 2.0 for GUI development **Domain-Optimized Integrated Blocks** ▪ Enhanced DSP/transceiver capability ▪ Integrated radio control peripherals (SPI, I2C, and UART) ▪ USB3.0 ▪ Enhanced DSP for efficient digital voice compression	▪ Up to 5X system performance/watt ▪ 4.5X more transceiver lanes ▪ 2X DDR memory bandwidth ▪ Up to 50% BOM cost reduction ▪ Radio scalability with maximum software reuse ▪ 2X efficient realization from Vivado Design Suite w/ Vivado HLS & SDx Design Environment during algorithm development	**Wireless** ▪ Multi-standard, multi-antenna radio ▪ AAS, DAS, repeaters ▪ Microwave modem ▪ eBand modem ▪ Switching and aggregation (C-RAN/V-RAN) ▪ C-RAN **Aerospace and Defense** ▪ Public safety radio ▪ Military mobile radio ▪ Dual-channel, battery-powered radio ▪ Airborne radio

Wireless and Waveform Processing

Xilinx UltraScale+™ FPGAs and Zynq® UltraScale+ MPSoCs address next-generation waveform processing applications by delivering up to 20 TeraMACs of processing in a cost-optimized footprint, requiring less than half the power of previous generations. By focusing on system-level performance, power, and cost requirements, the UltraScale™ architecture delivers the ideal balance of digital signal processing (DSP) performance, optimized connectivity, and memory for next-generation wireless and waveform processing applications.

At their foundation, UltraScale+ devices are based on the UltraScale architecture, production proven at 20nm. The UltraScale architecture features a number of innovations, including re-architected routing, clocking, and logic fabric. Combined with SmartConnect technology, only UltraScale devices can support datapaths that exceed 2,048 bits for high bandwidth at high device utilization, without any degradation in performance.

Wireless carriers continuously look to drive down both OPEX and CAPEX through cost and power-optimized solutions for next-generation heterogeneous wireless networks. Leveraging the TSMC 16FinFET+ process technology, UltraScale+ devices continue Xilinx's relentless drive to increase power efficiency with a 2-5X increase in performance per watt compared to our 28nm devices. In addition, Zynq UltraScale+ MPSoCs offer high-performance processing combined with integrated fine-grained power management—delivering efficient implementation of radio processing algorithms and 50% power savings allows more integration for wideband multi-antenna radios while also meeting thermal and dissipation budgets with passive cooling.

Wireless and Waveform Processing Continued

UltraScale+ devices offer several enhancements geared toward wireless applications. Having dedicated pre-add functionality, an additional operand to the accumulator, and higher clock rate capabilities, the enhanced DSP block is unmatched in allowing high-throughput LTE radio systems to run up to 825MHz in the faster speed grade, or pushbutton 491MHz in a low-power speed grade, all with efficient device utilization, enabling more efficient filter implementation for radio designs.

These enhancements also make complex multiplication for high order QAM providing efficient modems that eases migration toward QAM4096. Extended support for double-precision floating point math delivers 1.5X to 2X improved system-level performance for complex data flow machines at power levels that set new standards for GFLOPs/watt. Massive on-chip UltraRAM provides extra deep on-chip buffering for capture, buffering, and processing functions. This combination enables scalability of up to multiple TeraMACs of performance in a fully programmable architecture, requiring 66% less power while being customizable to meet the specific needs of even the most demanding waveform processing application.

With world-class transceivers, Xilinx has consistently delivered IP and silicon solutions that support the latest leading-edge line rate and features of various connectivity standards. As the CPRI, SRIO, GbE, and JESD204B/C connectivity standards evolve towards 25Gb/s line rates, and multi-gigabit Ethernet transport expands out to the radio, UltraScale+ devices are ideally positioned to address the full range of connectivity protocols and line rates required on emerging CPRI aggregators, 10 GbE/CPRI gateways, and CPRI over OTN schemes.

Zynq UltraScale+ MPSoCs build on the success of the Zynq-7000 AP SoC to deliver even greater processing system (PS) performance per watt for customers seeking a single-chip solution for their advanced radio systems. Zynq UltraScale+ MPSoC, with its Quad-core ARM Cortex®-A53 processor, can leverage one processor core for operations and maintenance while another is used to implement a digital pre-distortion (DPD) estimation engine. The remaining processor cores can be used to split the DPD software processing amongst multiple antennas, thus improving the update rate and reducing power.

For backhaul applications, UltraScale+ FPGAs offer advanced algorithm mapping, and unsurpassed integration. DSP and logic content that historically is split among the modem, L2 switch, timing, and synchronization ICs, can be integrated on a single FPGA. Zynq UltraScale+ MPSoC's Cortex-A53 processor together with SDNet™ Specification Environment enable innovative packet processing from intuitive high-level specification code. UltraScale+ MPSoCs are ideally suited to address the full range backhaul solution.

For Aerospace and Defense, UltraScale+ devices are optimized for software-defined radio (SDR) applications requiring wideband communications and advanced features like spectrum agility, spectral situational awareness, and integration of complete wireless protocol stacks in a single chip solution. Support for Hybrid Memory Cube (HMC) offers higher bandwidth memory interfacing beyond the limits of traditional DDR. Zynq UltraScale+ MPSoC's dedicated PMU offers dynamic power management and power gating of individual regions and processing engines, enabling low-power sleep modes and extending battery life. Zynq UltraScale+ MPSoC with its PMU, integrated processor cores, Mali™-400MP GPU, and H.264/265 codecs, brings new levels of performance per watt and a new level of interactivity with wireless MILCOM, public safety radio, and spectrum-sensing applications, allowing a re-imagination of what is possible.

3D-on-3D technology combines the power of 3D FinFET transistors and third-generation Xilinx 3D ICs to enable a non-linear improvement in systems integration, performance/watt, and bandwidth/watt over monolithic, planar-transistor devices.

Tooling for success with the UltraScale+ portfolio, Xilinx offers the Vivado® Design Suite, The SDx™ Design Environments, and the UltraFast™ design methodology for ASIC-strength design capabilities and the fastest time to differentiation and integration. Using Vivado HLS, designers can accelerate various packet processing, traffic management, and RADAR processing functions. Advanced SDx Design Environments enable developers to easily perform a trade-off exploration between implementing an algorithm using the processor(s) vs. the programmable logic to determine the optimal solution.

Whether the task is to support texting with friends in the movie theater or tracking foes in a theater of operations, UltraScale+ FPGAs and MPSoCs deliver up to 20 TeraMACs of processing in a cost-optimized footprint. UltraScale+ devices require less than half the power of previous generations, and are customizable to meet the specific needs of even the most demanding wireless and waveform processing applications. The winning combination of UltraScale devices with the Vivado Design Suite, the SDx Design Environments, and the UltraFast design methodology enables a model-based design approach, bringing system-level design for next-generation waveform processing applications to new and more efficient levels of performance and productivity. ■

	Packet Processing and Transport	Value Multipliers	Key Applications
FPGA	**Domain-Optimized Integrated Blocks** ▪ Integrated 100G Ethernet MAC w/ RS-FEC and OTN modes ▪ Integrated 150G Interlaken w/ 300G lane logic ▪ Enhanced DSP floating and fixed-point performance ▪ SmartConnect for wide-bus optimized interconnect ▪ Integrated PCIe® Gen4x8 w/ SR-IOV (252 VFs, 4 PFs) **Domain-Optimized Capabilities** ▪ 491 MHz capable pushbutton timing closure at low-power speed grade ▪ 30% lower transceiver latency and ASIC-like clocking structures ▪ UltraRAM for fiber length delay compensation and packet buffers ▪ W-Mux DSP48 for greater complexity DSP functions and filtering ▪ Fractional PLL for flexible reference clock generation from the recovered clock **Key I/O and Connectivity Interfaces** ▪ Increased independent memory channels w/ DDR4 up to 2666 Mb/s ▪ PCIe Gen3/4 x8, Serial Rapid I/O ▪ Support for 12.5 Gb/s transceivers in low-power speed grade (CPRI, JESD204B) ▪ Up to 128 transceivers with 33G support (25G Ethernet, 16/25G CPRI, 25G JESD204B/C, 28G backplane) ▪ Low-cost CFP2/4 interfacing	▪ Up to 2.5X greater system performance/watt ▪ Up to 86% increased DSP capability ▪ Up to 60% fabric performance improvement ▪ Up to 50% power reduction ▪ Up to 4.5X more transceiver lanes ▪ 2X increased high-speed bandwidth ▪ 4X memory bandwidth with DDR4 and HMC ▪ Up to 20% BOM cost reduction ▪ Up to 25% smaller devices through integrated IP ▪ 2X efficient realization from Vivado® Design Suite with Vivado HLS and SDx™ Design Environment during algorithm development	**Wireless** ▪ 1Tb MuxSAR OTN switch ▪ 8x100G MAC to Interlaken bridge ▪ 500G OTN switch ▪ 500G OTN transponders ▪ 200G PP/TM **Wireless Communications** ▪ CPRI aggregator ▪ IQ compression ▪ Scalable MxN port IQ switch ▪ 25G/10GE to CPRI bridging ▪ C-RAN Layer 1 acceleration **Data Center** ▪ Data Center Acceleration ▪ Programmable NIC ▪ Software Defined Network (SDN) NIC ▪ Software Defined Network (SDN) TOR switch ▪ 800G Data Center Interconnect (DCI)
MPSoC	**Key Processing Elements** ▪ Key Processing Elements ▪ Quad-core ARM® Cortex™-A53 processor + NEON for applications, OAM, control plane, acceleration, and line card processing ▪ Dual-core ARM Cortex-R5 real-time coprocessor for wireless protocol software and IEEE Std 1533 timing control ▪ ARM Mali™-400MP GPU cores for OpenGL2.0 support ▪ Power management unit to dynamically optimize the processing system (PS) for power ▪ Dedicated configuration security unit for IP protection **Processing Ecosystem** ▪ Commercial-grade 64-bit Linux support ▪ MVL, WRL and OSE ▪ Processor-based configuration security unit (CSU) ▪ Integrated radio control peripherals (SPI, I2C and UART) ▪ Enhanced DSP/transceiver capability ▪ USB3.0, PCIe Gen2x4 ▪ Enhanced DSP48 for efficient digital voice compression	▪ Up to 5X system performance/watt ▪ 2X increased high-speed bandwidth ▪ 4.5X more transceiver lanes ▪ 2X dedicated PS DDR memory bandwidth ▪ Up to 50% BOM cost reduction and smaller board footprint ▪ 2X efficient realization from Vivado® Design Suite with Vivado HLS and SDx Design Environment during algorithm development ▪ 5X productivity with A53, R5, GPU, VENC integrated blocks ▪ MPSoC family range allows scalability with maximum software reuse	**Wireless** ▪ Up to 200G Access PP/TM/Switching ▪ NGPON2 **Wireless Communications** ▪ CPRI aggregator and control plane ▪ IQ compression ▪ Scalable MxN port IQ switch ▪ 25G/10GE to CPRI bridging ▪ C-RAN Layer 1 acceleration **Data Center** ▪ Storage acceleration ▪ Software Defined Network (SDN) Ethernet switch ▪ Solid State Drive (SSD)

The Value of UltraScale+

Packet Processing and Transport

Xilinx UltraScale+™ devices provide an ASIC-class advantage that addresses next-generation packet processing and transport applications. Leveraging the TSMC 16FinFET+ process and 3D-on-3D technology, they deliver 2-5X greater system-level performance per watt over 28nm devices. Through increased systems integration, UltraScale+ FPGAs and MPSoCs deliver value far beyond a traditional process node migration—with ASIC-class performance, heterogeneous multiprocessing, memory, and optimized connectivity for next-generation packet processing and transport applications. At their foundation, UltraScale+ devices are based on the UltraScale™ architecture, production proven at 20nm. The UltraScale architecture features a number of innovations including re-architected routing, clocking, and logic fabric. Combined with SmartConnect technology, only UltraScale devices can support datapaths that exceed 2,048 bits for high bandwidth at high device utilization, without any degradation in performance.

UltraScale+ FPGAs offer new capabilities for networking and packet processing applications, including UltraRAM, SEU mitigation, partial reconfiguration, high-speed interfacing, and connectivity, that provide compelling value versus traditional ASICs or ASSPs. UltraRAM on-chip memory improves density and performance per watt, by providing ASIC-like memory in an FPGA. With up to 432 Mb of on-chip capacity, UltraRAM eliminates the need for external SRAMs and low-latency DRAMs. UltraRAM allows for ample packet descriptor databases, on-chip statistics, and local caches for efficient packet processing, as well as significant cost reduction and simplified system design. Major innovation in SEU

Packet Processing and Transport Continued

mitigation at multiple levels—silicon, IP, and design methodology, results in failure in time (FIT) rates that are significantly lower than ASICs or ASSPs, thus enabling a five-nines class of system availability. Virtualized functions that need to be managed dynamically can benefit from Partial Reconfiguration in UltraScale+ devices, offering superior flexibility compared to fixed-function ASICs or ASSPs. This flexibility is essential for software-defined networking (SDN) and network function virtualization (NFV). Lastly, integrated 100G Ethernet MAC and PCIe® Gen3x16/ Gen4x8 interfaces with single root I/O virtualization (SR-IOV) enable unmatched levels of integration, cost, and power efficiencies.

Xilinx UltraScale+ devices are architected for highly efficient Nx10G, Nx100G, and up to terabit networking implementations in a single chip. Integrated Ethernet MAC, Interlaken IP, and PCIe Gen3x16/Gen4x8 enable the highest level of integration. An increased number of independent DDR3 and DDR4 channels, with data rates of up to 2133 Mb/s and 2666 Mb/s respectively, assure highest bandwidth and density for payload buffering. Low-latency transceivers enable seamless support of emerging serial memories for even higher bandwidth and density. These enhancements in conjunction with 3X logic density and higher fabric performance open up new horizons for implementing next-generation networking architectures.

C-RAN fronthaul and connectivity applications benefit from multi-port transceivers for high density switching functions such as CPRI and Ethernet, with line rates up to 25 Gb/s. High-performance programmable fabric and block RAM allow implementing multi-port IQ switching at up to 825 MHz with high device utilization for an extremely small footprint. Radio Access Networks are experiencing densification, which is placing considerable demands on fronthaul fiber business models, resulting in a desire for operators to maximize bandwidth and efficiency. UltraScale+ devices offer a rich programmable platform, capable of implementing proprietary IQ compression engines in close proximity to the CPRI endpoints configured on the device. Being at both ends of the CPRI link in radios and modem/controllers, Xilinx All Programmable devices are ideally suited to deploy compression schemes on a per operator and per network basis, even after field deployment.

Zynq UltraScale+ MPSoC's Quad-core ARM Cortex™-A53 processor along with the Xilinx SDNet™ Specification Environment enable the implementation of innovative packet processing offload engines to accelerate virtualized functions for Layer 1 baseband processing. This co-location of the offload engine improves efficiency while reducing power and latency. The ample processing bandwidth of Zynq UltraScale+ MPSoC, tightly integrated with the hardware fabric, enables innovative solutions around the OpenFlow initiative allowing a decoupling of specific hardware from the higher software layers above. Collectively these features deliver substantially higher levels of system performance and integration within a fully programmable platform ideally positioned to address the emerging needs of an IP-centric packet processing and transport systems.

3D-on-3D technology combines the power of 3D transistors and third-generation Xilinx 3D ICs to enable a non-linear improvement in systems integration, performance/watt, and bandwidth/watt over monolithic, planar-transistor devices.

Tooling for success with the UltraScale+ portfolio, Xilinx offers the Vivado® Design Suite and UltraFast™ design methodology to enable ASIC-strength design capabilities and the fastest time to differentiation. The SDNet Specification Environment allows for the creation of 'Softly' Defined Networks, a disruptive innovation that goes well beyond today's SDN architectures.

UltraScale+ FPGAs and MPSoCs deliver ASIC-class performance capable of supporting throughput at line rates from hundreds of gigabits up to terabits per second. The Vivado Design Suite, SDx Design Environment, and the UltraFast design methodology enable ASIC-strength design capabilities and the fastest time to differentiation. This winning combination removes system-level design and productivity bottlenecks for next-generation packet processing and transport applications. ■

	Image and Video Processing	Value Multipliers	Key Applications
FPGA	**Domain-Optimized Integrated Blocks** ▪ Enhanced DSP for efficient FEC and CRC ▪ VCXO for external clock clean up **Domain-Optimized Capabilities** ▪ SmartConnect for wide bus optimized interconnect ▪ UltraRAM for stream buffering ▪ ASIC-like clocking for low skew clocks **Key I/O & Connectivity Interfaces** ▪ UHD-SDI (SD/HD/3G/6G/12G-SDI) ▪ SMPTE ST 2022 Video over IP ▪ HDMI 2.0 ▪ Native MIPI ▪ GE controllers supporting IEEE Std 1588 and AVB ▪ Flexible memory support with DDR4/3 and LPDDR4/3	▪ 2X logic cell throughput ▪ 2.5X serial bandwidth ▪ 2X DDR memory bandwidth ▪ 30% lower power at increased performance ▪ Up to 3X system performance improvement ▪ Up to 2.5X greater system performance/watt ▪ Up to 50% BOM cost reduction	**Broadcast / Pro A/V** ▪ High density video transcoding ▪ Advanced 4K video pre/post processing algorithms ▪ Motion-compensated frame rate conversion ▪ 3D noise reduction ▪ Ultra HD video compositing and analysis ▪ 128+ frame rate processing for applications like slow motion playback ▪ Multi-Streaming Control Unit **Industrial** ▪ Surveillance ▪ Machine Vision
MPSoC	**Key Processing Elements** ▪ Quad-core ARM® Cortex®-A53 for real-time vision analytics, streaming, and automated metadata ▪ ARM Mali™-400MP GPU for HMI with OpenGL2.0 support ▪ Dual-core ARM Cortex-R5 for real-time peripheral interfaces ▪ Functional safety support with lock-step mode on Dual-core ARM Cortex-R5 and Advanced Power Management Unit **Processing Ecosystem** ▪ Windows embedded compact ▪ 64-bit Linux support ▪ Baremetal and RTOS support for real-time coprocessor ▪ Functional safety & AUTOSAR/MCAL package **Domain-Optimized Integrated Blocks** ▪ Video encoder supporting H.265/H.264 for up to 4K2Kp60 or 8K4Kp15, IPB frame 4:2:2, 10-bit ▪ DisplayPort 1.2 monitor output ▪ USB3.0 & SATA for storage/logging ▪ CAN2.0B, PCIe® Gen4x8/3x16, and Gigabit Ethernet supporting IEEE Std 1588 and AVB ▪ DDR3/4 & LPDDR3/4 memory support	▪ Up to 5X system performance/watt ▪ Up to 50% system BOM reduction ▪ Up to 40% power savings ▪ 5X productivity with A53, R5, GPU, VENC integrated blocks	**Video Infrastructure** ▪ Pro A/V encompasses video conferencing ▪ Enterprise video switches ▪ 4K conversion products ▪ Video Over IP bridging ▪ IP multi-viewers ▪ Broadcast cameras ▪ High density video transcoding **Automotive** ▪ Camera-based advanced driver assistance systems ▪ DA central processing platform **Industrial** ▪ Surveillance ▪ Machine Vision

Image and Video Processing

Xilinx UltraScale+™ devices address next-generation 8K and 4K broadcast, video processing, video conferencing, and advanced driver assistance system (ADAS) applications. Leveraging the TSMC 16FinFET+ process and 3D-on-3D technology, UltraScale+ devices deliver a 5X improvement in system-level performance per watt over 28 nm devices. UltraScale+ FPGAs and Zynq® UltraScale+ MPSoCs provide an ASIC-class advantage with gigapixel and terabit per second system throughputs, faster time to market, and lower system-level BOM costs.

At their foundation, UltraScale+ devices are based on the UltraScale architecture, production proven at 20nm. The UltraScale architecture features a number of innovations including re-architected routing, clocking, and logic fabric. Combined with SmartConnect technology, only UltraScale devices can support high bandwidth datapaths at high device utilization, without any degradation in performance.

With a host of domain-specific functionality, the Zynq UltraScale+ MPSoC is a powerful, single-chip audio / video and broadcast platform. At the heart of its processing system is the 64-bit Quad-core ARM® Cortex®-A53, providing greater than 2X performance over its A9 predecessor in the Zynq-7000 AP SoC—ideal for vision analytics, streaming, and automated metadata. Also integrated is a dual-core ARM Cortex-R5 real-time processor for real-time peripheral interfaces. For graphics acceleration, video compression and decompression, the Zynq UltraScale+ MPSoC incorporates an ARM Mali™-400MP as well as a H.265 video codec unit embedded in the programmable logic, capable for up to 8K4K support. In addition, the Zynq UltraScale MPSoC boasts tightly integrated interconnect, linking the processing system and

Image and Video
Continued

programmable logic blocks, yielding throughput and performance simply not achievable with a multi-chip, ASSP+FPGA system architecture. These integrated multi-processing engines are complemented by massive on-chip UltraRAM, providing extra deep on-chip buffering for frame capture and processing functions. UltraScale+ devices support interfacing standards HDMI1.4/2.0, 3G/UHD-SDI, and DisplayPort1.2, with memory bandwidth with DDR4 up to 2400Mb/s, and versatile I/O interfacing. To meet ever-tightening power budgets, Zynq UltraScale+ MPSoCs include a dedicated power management unit (PMU) that provides system monitoring, system management, and dynamic power gating of individual regions and processing engines. With proven 4K processing performance, and a commitment to 4K video connectivity, UltraScale+ MPSoCs lead the industry in integration of ISP and video analytics for a single chip implementation.

For automotive systems, the Zynq UltraScale+ MPSoC offers a lock-step configuration for the dual-core ARM Cortex-R5 real-time processor for real-time response and low latency in safety critical and high reliability applications. The PMU is implemented with built-in triple mode redundancy for reliable on-chip monitoring, and the MPSoC also offers a configuration security unit (CSU) for assurance of device configuration and anti-tamper functions.

Major innovation in SEU mitigation at multiple levels—silicon, IP, and design methodology, results in failure in time (FIT) rates that are significantly lower than ASICs or ASSPs, thus enabling a five-nines class of system availability.

3D-on-3D technology combines the power of 3D FinFET transistors and third-generation Xilinx 3D ICs to enable a non-linear improvement in systems integration, performance/watt, and bandwidth/watt over monolithic, planar-transistor devices.

The Vivado® Design Suite, Vivado HLS, and the SDx™ Design Environments allow creation of programmable logic based hardware accelerators at higher levels of abstraction; the UltraFast™ design methodology enhances productivity for ADAS designers. Xilinx also provides an extensive ecosystem for Zynq UltraScale+ MPSoCs, including SDK, baremetal drivers, operating systems, and tools.

Based on a thorough, system-level understanding of requirements and constraints, the UltraScale+ portfolio has been optimized for next-generation video-processing applications, to address the bottlenecks associated with media/system control, image processing, and analytics for high-quality 8K and 4K video, at high frame rates. The winning combination of UltraScale devices, the Vivado Design Suite, Vivado HLS, the SDx Design Environments, and the UltraFast design methodology enables 5X higher system performance per watt and integration in a fully programmable architecture that can be tailored to match the specific needs of even the most demanding image and video processing applications. ■

	High Performance Computing	Value Multipliers	Key Applications
FPGA	**Domain-Optimized Integrated Blocks** ▪ High-speed, high quality transceivers with 2D-EyeScan ▪ Integrated PCIe® Gen4x8, Gen3x16 with SR-IOV ▪ VCXO for external clock clean up ▪ Enhanced DSP for algorithm acceleration **Domain-Optimized Capabilities** ▪ W-Mux DSP48 for complex DSP functions ▪ SRL for efficient filter implementation ▪ 491MHz capable pushbutton timing closure in slowest speed grade ▪ 6X more cascadable block RAM for packet buffers ▪ UltraRAM for fiber length delay compensation in baseband **Key I/O & Connectivity Interfaces** ▪ Increased independent memory channels ▪ Low latency DMA engines ▪ Support for 12.165G CPRI in slow speed grade ▪ Support for 25G Ethernet and 16G/25G CPRI	▪ Up to 3X system performance ▪ 86% increased DSP capability ▪ Up to 60% fabric performance ▪ 3X serial bandwidth ▪ 4X memory bandwidth with DDR4 and HMC ▪ Up to 40% system BOM cost reduction	**Data Center** ▪ Compute acceleration ▪ Flash Controller and Storage bridging ▪ Programmable NIC **Wireless Communications** ▪ C-RAN/HD-BTS ▪ 5G Baseband L2 acceleration ▪ Evolved packet core - SDN/NFV acceleration
MPSoC	**Key Processing Elements** ▪ Quad-core ARM® Cortex®-A53 processor for OAM, control plane, compute, and storage acceleration ▪ Dedicated configuration security unit (CSU) for IP protection ▪ Power management unit to optimize processing system power **Processing Ecosystem** ▪ MVL, WRL, and OSE ▪ 64-bit Linux support ▪ Vivado® Design Suite, Vivado HSL & SDx™ Design Environments for efficient realization for hardware and software algorithms **Domain-Optimized Integrated Blocks** ▪ Enhanced DSP/transceiver capability ▪ Integrated control peripherals for board management (SPI, I2C, and UART) ▪ Integrated block for PCIe® Gen2x4	▪ Up to 5X system performance/watt ▪ 2X dedicated PS DDR memory bandwidth ▪ Up to 50% power reduction ▪ Up to 50% system BOM cost reduction	**Video Infrastructure** ▪ Compute acceleration ▪ Flash Controller and Storage bridging ▪ Programmable NIC **Wireless Communications** ▪ C-RAN Layer 1 acceleration

High Performance Computing

Xilinx UltraScale+™ devices provide an ASIC-class advantage that addresses next-generation high-performance computing and data center applications. Leveraging the TSMC 16FinFET+ process and 3D-on-3D technology, the UltraScale+ devices deliver 2-5X greater system-level performance per watt over 28nm devices. Through increased system integration, UltraScale+ FPGAs and Zynq® UltraScale+ MPSoCs deliver value far beyond a traditional process node migration with ASIC-class performance, heterogeneous multiprocessors, optimized connectivity, memory, logic, and other engines for complex algorithm implementation.

At their foundation, UltraScale+ devices are based on the UltraScale™ architecture, production proven at 20nm. The UltraScale architecture features a number of innovations including re-architected routing, clocking, and logic fabric. Combined with SmartConnect technology, only UltraScale devices can support datapaths that exceed 2,048 bits for high bandwidth at high device utilization, without any degradation in performance.

UltraScale+ FPGAs offer new capabilities for high-performance computing and data center applications including UltraRAM, SEU mitigation, partial reconfiguration, high-speed interfacing, and connectivity, that provide compelling value versus traditional ASICs or ASSPs. UltraRAM on-chip memory improves density and performance per watt, by providing ASIC-like memory in an FPGA. With up to 432Mb of on-chip memory capacity, UltraRAM eliminates the need for external SRAMs and low-latency DRAMs. Thus UltraRAM offers unprecedented power efficiency, as well as significant cost reduction and simplified system design.

High Performance Computing Continued

Major innovation in SEU mitigation at multiple levels—silicon, IP, and design methodology, results in failure in time (FIT) rates that are significantly lower than ASICs or ASSPs, thus enabling a five-nines class of system availability. Virtualized functions that need to be managed dynamically can benefit from Partial Reconfiguration in UltraScale+ devices, offering superior flexibility compared to fixed-function ASICs or ASSPs. This flexibility is essential for software-defined networking (SDN) and network function virtualization (NFV). Lastly, integrated 100G Ethernet MAC and PCIe® Gen3x16 and Gen4x8 interfaces with single root I/O virtualization (SR-IOV) enable unmatched levels of integration, cost, and power efficiencies.

Beyond data center applications, DSP-intensive 5G baseband applications benefit from enhanced DSP integrated blocks with pre-add functionality, an additional operand to the accumulator, and higher clock rate capabilities, allowing for pushbutton 491MHz LTE in the low-power speed grade at high device utilization, without performance degradation. The enhancements make complex multiplication and filtering more efficient, and ease migration to QAM4096. Extended support for double-precision floating point math delivers 1.5X to 2X improved system-level performance for complex data flow machines at power levels that set new standards for GFLOPs/watt. Fully programmable I/O are capable of DDR3 and 2133 Mb/s and DDR4 at 2666 Mb/s respectively. World-class transceiver connectivity is capable of enabling 25 Gb/s line rates for CPRI, SRIO, and GbE, and the evolving JESD204B/C interface standard, and offers Gen3 Hybrid Memory Cube (HMC2.0) interfacing. The Zynq UltraScale+ MPSoC's Quad-core ARM Cortex™-A53 processor, with the Xilinx SDNet™ Specification Environment, enables implementing innovative packet processing offload engines to accelerate virtualized functions for Layer 1 baseband processing. This co-location of the offload engine improves efficiency while reducing power and latency. The ample processing bandwidth of Zynq UltraScale+ MPSoC, tightly integrated with the hardware fabric, enables innovative solutions around the OpenFlow initiative, allowing a decoupling of specific hardware from the higher software layers above. Thus, the UltraScale architecture is a potent platform to secure first to market advantage on many of the evolving solutions for HetNet, C-RAN, network virtualization, and 5G air interface proposals.

Data center and enterprise-class SSDs use FPGAs to meet tough performance and data-integrity requirements that cannot be met with ASSPs; enterprise-class SSD controllers must implement significantly more complex wear-leveling, ECC, and error-management algorithms. SSD designers also need high-speed, low-latency interfaces to flash memory, and support for the many standard interfaces used in the storage. Xilinx All Programmable devices and Smarter Solutions encompass the IP support and devices needed to implement sophisticated storage algorithms for rapid design and deployment of new storage architectures. UltraScale+ devices offer unprecedented levels of system integration to enable next-generation storage designs with significant power and cost savings.

3D-on-3D technology combines the power of 3D FinFET transistors and third-generation Xilinx 3D ICs to enable a non-linear improvement in systems integration, performance/watt, and bandwidth/watt over monolithic, planar-transistor devices. Tooling for success with the UltraScale+ portfolio, Xilinx offers the Vivado® Design Suite and UltraFast™ design methodology to enable ASIC-strength design capabilities and the fastest time to differentiation. The SDAccel Design Environments (OpenCL) makes UltraScale+ devices accessible to software developers and domain experts, and allows for high-performance implementation of complex algorithms. The SDNet Specification Environment allows for the creation of 'Softly' Defined Networks, a disruptive innovation that goes well beyond today's SDN architectures.

Whether the task requires accelerated processing of large datasets, computing investment value and risk in real time, or responding to financial market events in nanoseconds, the UltraScale+ portfolio enables scalability up to 5X performance per watt in a fully programmable architecture, with up to 60% less power, customizable to meet the specific needs of even the most demanding high performance computing or data center applications. The winning combination of UltraScale+ devices, the Vivado Design Suite, and the UltraFast design methodology removes system-level design and productivity bottlenecks for next-generation high performance computing and data center applications. ■

MPSoC

Connected Control	Value Multipliers	Key Applications
Key Processing Elements ▪ Quad-core ARM® Cortex®-A53 processor for high- performance PLC runtime ▪ Dual-core ARM Cortex-R5 real-time coprocessor for safety critical, real-time I/O, and functions ▪ ARM Mali™-400MP GPU for HMI **Domain-Optimized Capabilities** ▪ Enhanced DSP for efficient algorithm acceleration ▪ Cascading block RAM and UltraRAM for deep buffers ▪ ASIC-like low skew clocking **Domain-Optimized Integrated Blocks** ▪ Lock-step real-time processor configuration for high-availability safe systems (SIL3 safety) ▪ Dedicated configuration security unit (CSU) for enhanced safety and cyber security ▪ Up to 128-bit-wide AXI processing system (PS) to programmable logic (PL) interconnect ports ▪ USB3.0 and SATA for storage ▪ Integrated PCIe® Gen3 for system expansion ▪ XADC for analog input and system monitoring & safety **Key I/O & Connectivity Interfaces** ▪ DDR4 to extend system memory bandwidth ▪ PCIe® Gen3 in slowest speed grade ▪ Flexible display connectivity – DP, HDMI, MIPI DSI2, LVDS Zynq UltraScale+ MPSoC prodcuts are best suited for Connected Control.	▪ Up to 5X system performance/watt ▪ Up to 25% smaller devices through integrated IP ▪ 4X memory bandwidth with DDR4 and HMC ▪ Up to 50% power reduction ▪ 86% increased DSP capability ▪ Up to 3X system performance ▪ Up to 50% BOM cost reduction	**Industrial Internet of Things (IoT)** **Programmable Logic Control** ▪ M2M fast database ▪ IEC61131-3 fast interpreters ▪ Multi-gateway network ▪ Safety diversity ▪ High-end PCIe-based PLC **Motion Control** ▪ Control systems ▪ MIMO robot controllers ▪ Multi-axis motion control ▪ Drive systems ▪ Diagnostic algorithms ▪ Safety diversity **Robotics** ▪ Real-time observer and estimators ▪ Real-time profiles and protocols ▪ Real-time motion planner ▪ M2M, B2B, and B2M communication ▪ Autonomous controllers ▪ Diagnostic algorithms

Connected Control

Xilinx UltraScale+™ MPSoCs bring a technological breakthrough to robotic, industrial drive, power conversion, and programmable logic controller (PLC) applications. Leveraging TSMC's 16FinFET+ process for Zynq® UltraScale+ MPSoCs enables greater than 5X system-level performance per watt advantage over traditional connected control platforms, while providing up to a 65% system-level BOM cost reduction. For safety-conscious applications, the Zynq UltraScale+ MPSoC offers a dual-core ARM® Cortex®-R5 real-time processor with support for lock-step configuration, a power management unit (PMU), and a configuration security unit (CSU) to provide assurance of device configuration, anti-tamper functions, as well as on-chip safety monitoring.

At their foundation, UltraScale+ devices are based on the UltraScale™ architecture, production proven at 20nm. The UltraScale architecture features a number of innovations including re-architected routing, clocking, and logic fabric. UltraScale+ FPGAs offer new capabilities for robotics, industrial drive, power conversion and PLC applications including UltraRAM, SEU mitigation, partial reconfiguration, high-speed processing and connectivity, that provide compelling value versus traditional ASICs or ASSPs. UltraRAM on-chip memory improves density and performance per watt, by providing ASIC-like memory in an FPGA. Combined with SmartConnect technology, only UltraScale devices can support high bandwidth datapaths at high device utilization, without any degradation in performance.

Today's high-performance PLCs are cost-sensitive and require highly sophisticated multi-core processing systems in the smallest form factor consuming the lowest possible power.

Connected Control
Continued

Zynq UltraScale+ MPSoCs are architected to deliver the highest performance per watt with a Quad-core ARM Cortex-A53 application processing unit (APU), a dual-core ARM Cortex-R5 real-time processing unit (RPU), and ASIC-class programmable logic to deliver and service multiple communication paths in and out of the PLC. To meet ever-tightening power budgets, Zynq UltraScale+ MPSoC includes a dedicated power management unit (PMU) that provides system monitoring, system management, dynamic power management, and power gating of individual regions and processing engines, allowing you to develop small form factor, high-reliability PLC designs for high-performance industrial control systems.

For industrial drive applications, Zynq UltraScale+ MPSoCs are the ideal platform to integrate data acquisition, diagnostics, local decision-making, energy-aware, and self-aware control systems. Zynq UltraScale+ MPSoCs support wide, parallel processing at high device utilization, without performance degradation. Enhanced block RAM, UltraRAM, DSP, and logic capacity allows for better mapping of algorithmic calculations, such as those used in high-performance motion planning in robotics, or sub-microsecond synchronization between a PLC and electric drives. The Xilinx SDx™ Design Environments provide high-level implementation tools that support the use of advanced algorithms for diagnostic, estimation, control, and vision analysis being more widely used in next-generation industrial products. The multicore processors benefit from DDR4 memory at 2666 Mb/s and high performance AXI interfaces for higher bandwidth and data sharing with the programmable logic. This higher bandwidth coupled with integrated Ethernet MAC and PCIe® Gen3/4 interfaces enable unmatched levels of integration, interfacing, cost, and power efficiencies—yielding a step-function in system-level capabilities. Zynq UltraScale+ MPSoCs enable a first to market advantage for many of the evolving applications that apply intelligent drive technology to mechanical systems using the Internet of Things.

To support the Zynq UltraScale+ MPSoC, Xilinx offers the Vivado® Design Suite and the SDx Design Environments to create software accelerators in the programmable logic using higher levels of abstraction. These higher levels of abstraction, such as C, C++, or Open-CL, ease the programming model for multicore heterogeneous systems. Further, the UltraFast™ embedded design methodology enhances productivity for designers, reduces development iteration cycles, improves design visibility and testability, and ensures timely implementation of the final system. Xilinx also provides an extensive ecosystem, including various operating systems to meet the needs of embedded system developers for real-time software and hardware applications.

Whether the task requires precision motion planning, self-aware control, or intelligent drive, the UltraScale+ portfolio enables scalability with greater than 5X performance per watt in a fully programmable architecture, with up to 65% system-level cost reduction, customizable to meet the specific needs of next- generation connected control applications. The winning combination of UltraScale+ devices, the Vivado Design Suite, the SDx Design Environments, and the UltraFast embedded design methodology removes system-level design and productivity bottlenecks, and enables new end product capabilities for next-generation connected control applications. ■