Integrated Bit Error Ratio Tester 7 Series GTZ Transceivers v3.1

LogiCORE IP Product Guide

Vivado Design Suite

PG171 June 8, 2016

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Appendix C: Additional Resources and Legal Notices

Introduction

The LogiCORE™ IP Integrated Bit Error Ratio Tester (IBERT) core for 7 series FPGA GTZ transceivers is designed for evaluating and monitoring the GTZ transceivers. This core includes pattern generators and checkers that are implemented in FPGA logic, and access to ports and the dynamic reconfiguration port attributes of the GTZ transceivers. Communication logic is also included to allow the design to be run time accessible through JTAG. This core can be used as a self-contained or open design, based on customer configuration, and as described in this document.

Features

- Provides a communication path to the Vivado® Serial I/O Analyzer feature
- Provides a user-selectable number of 7 series FPGA GTZ transceivers
- Transceivers can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width
- Requires a system clock that can be sourced from a pin or one of the enabled GTZ transceivers

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Virtex®-7
Supported User Interfaces	N/A
Resources	Performance and Resource Utilization webpage
Provided with Core	
Design Files	Register Transfer Level (RTL)
Example Design	Verilog
Test Bench	Not Provided
Constraints File	Xilinx Design Constraints (XDC)
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	Not Provided
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page.	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The IBERT core provides a broad-based Physical Medium Attachment (PMA) evaluation and demonstration platform for 7 series FPGA GTZ transceivers. Parameterizable to use different GTZ transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and logic widths. Data pattern generators and checkers are included for each GTZ transceiver desired, giving several different Pseudo-random binary sequence (PRBS) and clock patterns to be sent over the channels.

In addition, the configuration and tuning of the GTZ transceivers is accessible though logic that communicates to the Dynamic Reconfiguration Port (DRP) port of the GTZ transceiver, to change attribute settings, as well as registers that control the values on the ports. At run time, the Vivado® serial I/O analyzer communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

Feature Summary

The IBERT core is designed for PMA evaluation and demonstration. All the major physical medium attachment (PMA) features of the GTZ transceiver are supported and controllable, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- Phase-Locked Loop (PLL) divider settings

Some of the Physical Coding Sublayer (PCS) features offered by the transceiver are outside the scope of IBERT, including:

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

PLL Configuration

For each serial transceiver, two LC tank PLLs are present, one for RX, and one for TX. There are no shared PLLs amongst channels in the OCTAL.

Figure 1-1 shows a GTZ OCTAL in a 7 series device. The GTZ channels has the serial transceiver and CPLL units.

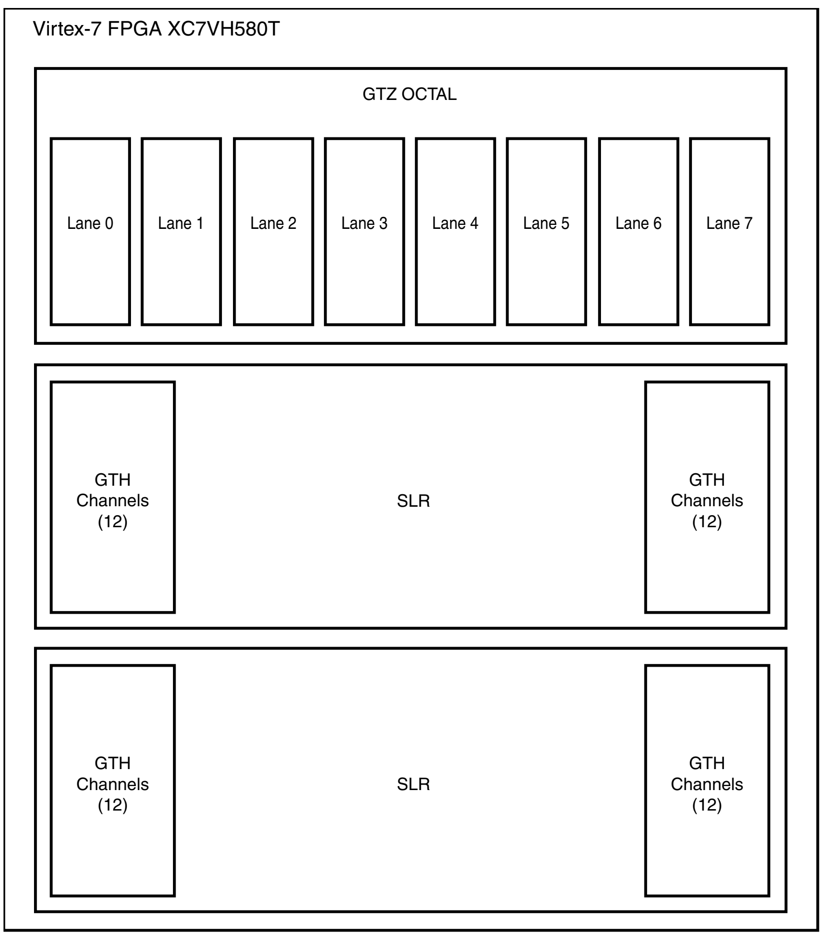

Figure 1-1: **GTZ OCTAL in a Virtex-7 FPGA XC7VH580T**

The serial transceiver REFCLK can be sourced from either of two inputs, with a multiplexer as shown in Figure 1-2. This can be selected from the 7 series FPGA IBERT Vivado IP Catalog.

Each OCTAL has two REFCLK inputs and attributes control which REFCLK is used for each channel. The IBERT 7 series GTZ core only supports one line rate per OCTAL.

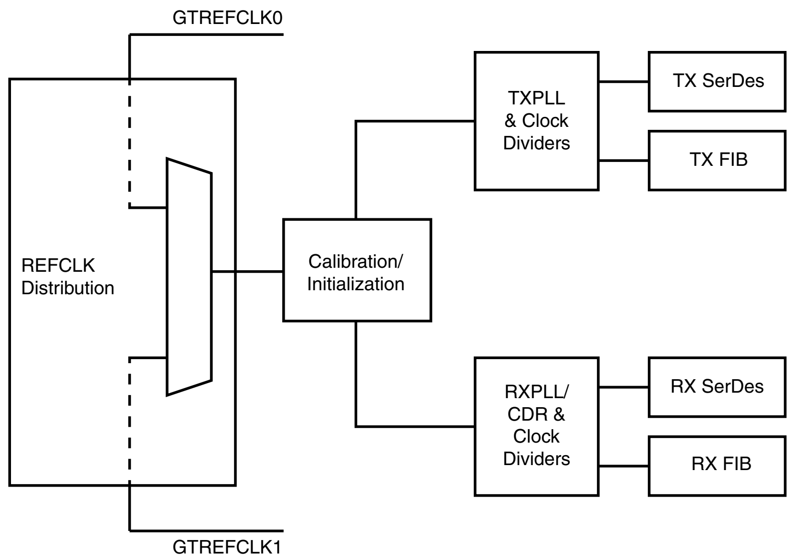

Figure 1-2: **GTZ Internal Clocking Architecture**

Pattern Generation and Checking

Each GTZ transceiver enabled in the IBERT design has a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker accepts data through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS 31-bit, Clk 2x (101010...), and Clk 10x (11111111110000000000...) patterns.

These patterns are optimized for the logic width that was selected at run time. The TX and RX patterns are individually selected.

Using the pattern checker logic, the incoming data is compared against a pattern that is internally generated. When the checker receives five consecutive cycles of data with no errors, the `LINK` signal is asserted. If the `LINK` signal is asserted and the checker receives five consecutive cycles with data errors, the `LINK` signal is deasserted. Internal counters accumulate the number of words and errors received.

DRP and Port Access

You can change GTZ transceiver ports and attributes. The DRP interface logic allows the run time software to monitor and change any attribute of the GTZ OCTAL. When applicable, readable and writable registers are also included that are connected to the various ports of the GTZ OCTAL. All are accessible at run time using the Vivado serial I/O analyzer.

Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of 7 series FPGA GTZ transceivers.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado design tools: Vivado synthesis
- Vivado implementation
- write_bitstream (Tcl command)

IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Product Specification

Performance

The core can be configured to run any of the allowable line rates for the GTZ transceivers. See the *7 Series FPGAs Overview* (DS180) [Ref 1] for the line rates supported by speed grade.

Maximum Frequencies

The core can operate at the maximum user clock frequencies for the FPGA logic width/ speed grade selected. The maximum system clock rate is 100 MHz and the generated design divides any incoming system clock to adhere to this constraint.

Resource Utilization

For full details about performance and resource utilization, visit the Performance and Resource Utilization web page.

Port Descriptions

The core ports are shown in Table 2-1.

Table 2-1: **IBERT I/O Signals**

Signal Name	I/O	Description
sysclk_i	I	Clocks all communication logic. This port is present only when an external clock is selected in the generator.
txp_o[n – 1:0] txn_o[n – 1:0]	O	Transmit differential pairs for each of the n GTZ transceivers used.
rxn_i[n – 1:0] rxp_i[n – 1:0]	I	Receive differential pairs for each of the n GTZ transceivers used.
gtrefclk0_i[n – 1:0] gtrefclk1_i[n – 1:0]	I	GTZ transceiver reference clocks used. The number of MGTREFCLK ports can be equal to or less than the number of transmit and receive ports because some GTZ transceivers can share clock inputs.

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

Line Rate Support

The IBERT core supports one line rate per OCTAL. A list of the supported line rates is available, and for each line rate, one or more reference clock rates are supported. The proper divider settings is specified for each line rate/reference clock rate combination.

Serial Transceiver Location

Based on the total number of serial transceivers selected, provide the specific location of each serial transceiver that you intend to use. The region shown in the panel indicates the location of serial transceivers in the tile. This demarcation of region is based on the physical placement of serial transceivers with respect to median of BUFGs available for each device. Depending on the device selected, one or two OCTALs are available. The region shown in the panel indicates the location of the OCTAL in the device.

Clocking

System Clock

When you choose different system clock locations while customizing the IBERT GTZ IP, you have to modify the `local.xdc` file to update the `BUFGTCTRL LOC` for the constraint and the cell `u_bufg_dclk` to match the System Package Pin location (making sure the `SYSCLK` location and BUFG (compatible to GTZ `DRPCLK` only) are both in top/bottom region of an SLR region).

The IBERT core requires a free-running system clock for communication and other logic that is included in the core. This clock can be chosen at generation time to originate from an FPGA pin, or to be driven from the `TXOUTCLK` port of one of the GTZ transceivers. In order for the core to operate properly, this system clock source must remain operational and stable when the FPGA is configured with the IBERT core design.

If the system clock is running faster than 100 MHz, it is divided down internally using a Mixed-Mode Clock Manager (MMCM) to satisfy timing constraints. The clock source selected must be stable and free running after the FPGA is configured with the IBERT design. The system clock is used for core communication and as a reference for system measurements. Therefore, the clock source selected must remain operational and stable when using the IBERT core.

Receiver Output Clock

The receiver clock probe enable is provided to pull out a recovered clock from any serial transceiver, if desired. When enabled, a new panel appears just before the summary page where you can fill in the serial transceiver source and probe pin standards.

Reference Clock

The reference clock source should be provided for all the serial transceivers selected. The drop-down list provides you with possible sources based on local clocks in the same quad.

Resets

Run time resets are available for the BERT counters and all GT resets are available.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 2]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 4]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 5]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 2] for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the Vivado IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 4].

Note: Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Figure 4-1 to Figure 4-5 show the IBERT Customize IP dialog boxes with information about customizing ports.

Entering the Component Name

The Component Name field can consist of any combination of alpha-numeric characters including the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

Design Options

- **Board Configuration Settings (BCS)** – Generates bit file for Super Clock II along with IBERT design to set the `REFCLK` frequencies on GTZ boards.
- **System Clock** – Options to set the frequency, input standard, and P/N pin locations.
    - **Frequency** – Range of 50 to 500.
    - **Input Standard** – BLVDS 25.
    - **P Pin Location** – Specify a valid pin location, such as Unconstrained.
    - **N Pin Location** – Specify a valid pin location, such as Unconstrained.
- **Add RXOUTCLK Probe Check Box** – Enables the `RXOUTCLK` panel for entering the output pin locations for `RXOUTCLK`.
- **Silicon Version** – Only Initial ES is supported.

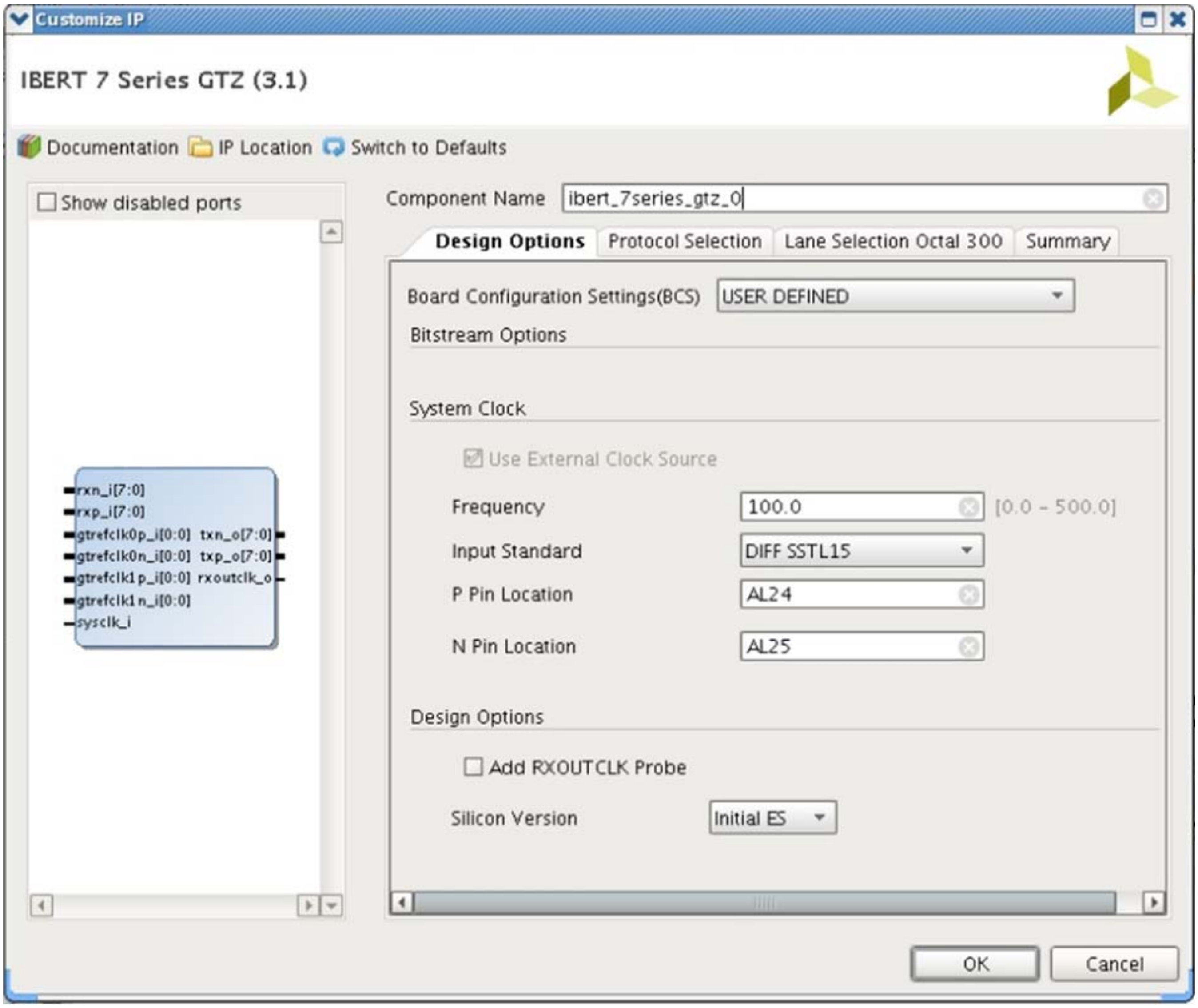

Figure 4-1: **Vivado Customize IP Dialog Box – Design Options**

Protocol Selection

A protocol is a line rate, data width, reference clock rate, lane count, and reference clock source. For an IBERT GTZ core, the transceiver selection is on a lane basis. For each protocol, eight or 16 lanes are allowed (one OCTAL or two OCTALs).

1. Choose the number of protocols desired.
2. In the Protocol combination box, select a Pre-defined protocol.
    a. Select the line rate and data width. IBERT supports one line rate per OCTAL.
    b. Choose the `REFCLK` rate and lane count of 8 or 16.
3. Select the `REFCLK` source.

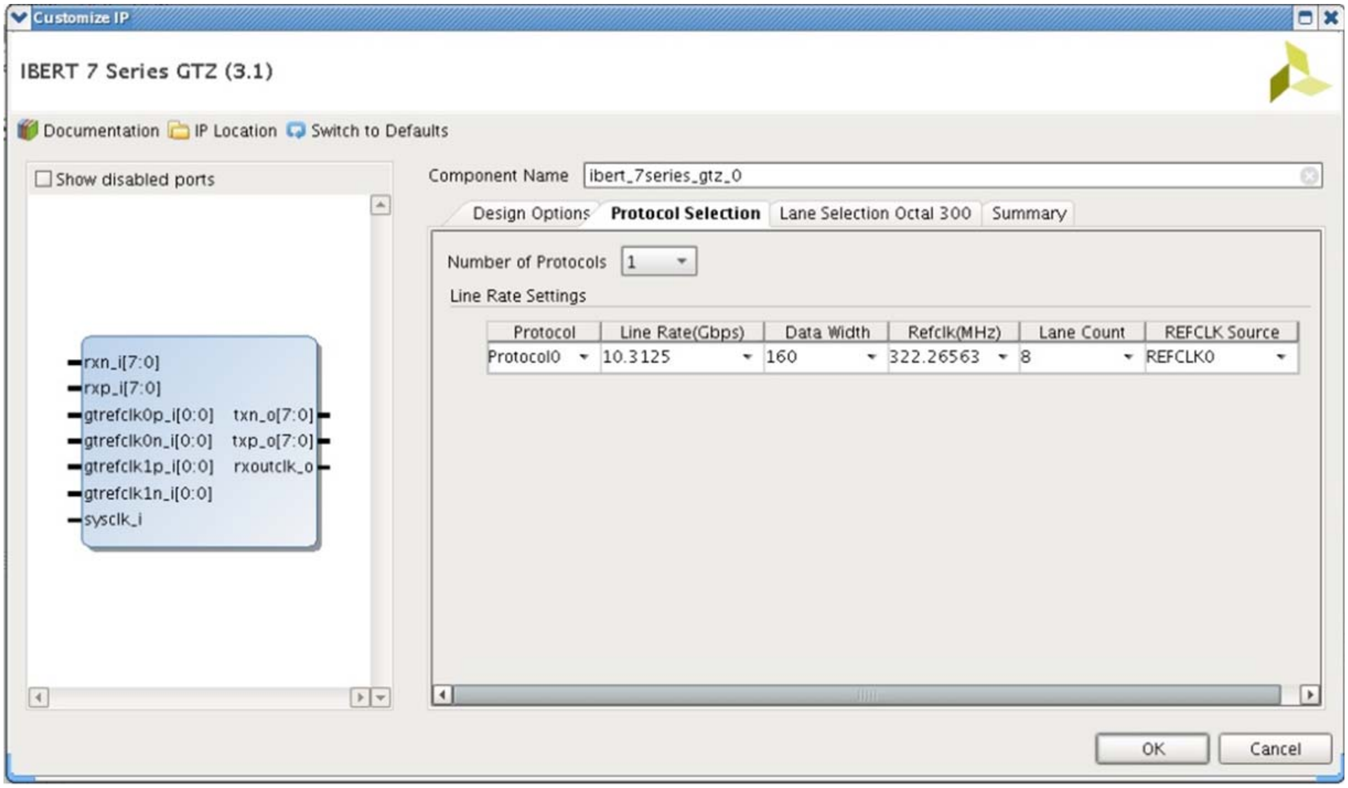

Figure 4-2: **Vivado Customize IP Dialog Box – Protocol Selection**

Lane Selection OCTAL 300

- **Location** – Specifies the lane location.
- **Protocol** – Specification for the OCTAL based on availability in the part.
- **Power Down for Each Lane** – This option powers down the specific transceiver while the design is running on hardware.
- **Resource Usage** – BUFG count is at 2.

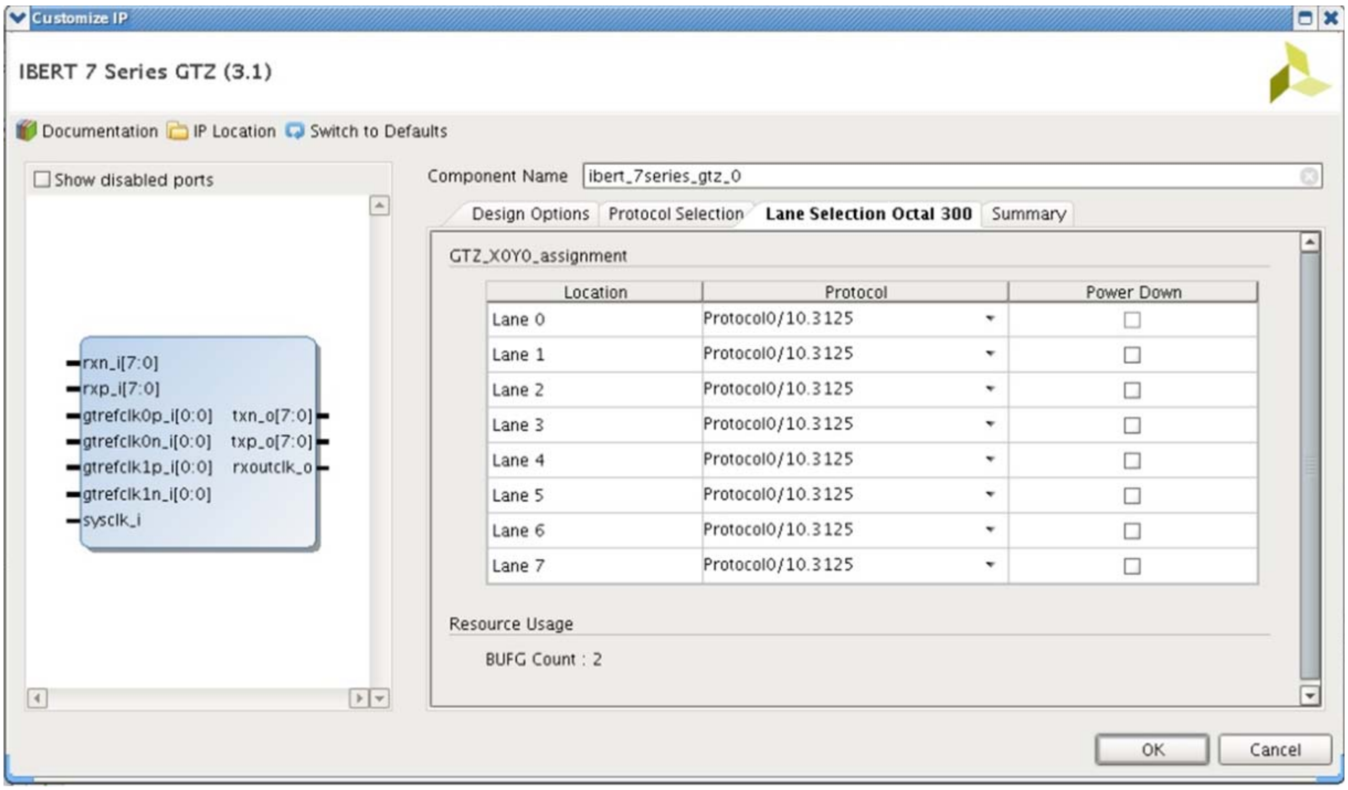

Figure 4-3: **Vivado Customize IP Dialog Box – Lane Selection OCTAL 300**

RXOUTCLK Source Selection

When the check box **Add RXOUTCLK Probe** is enabled, this panel is shown (hidden if disabled). This page allows you to provide the I/O pin locations for `RXOUTCLK` that is given in the design.

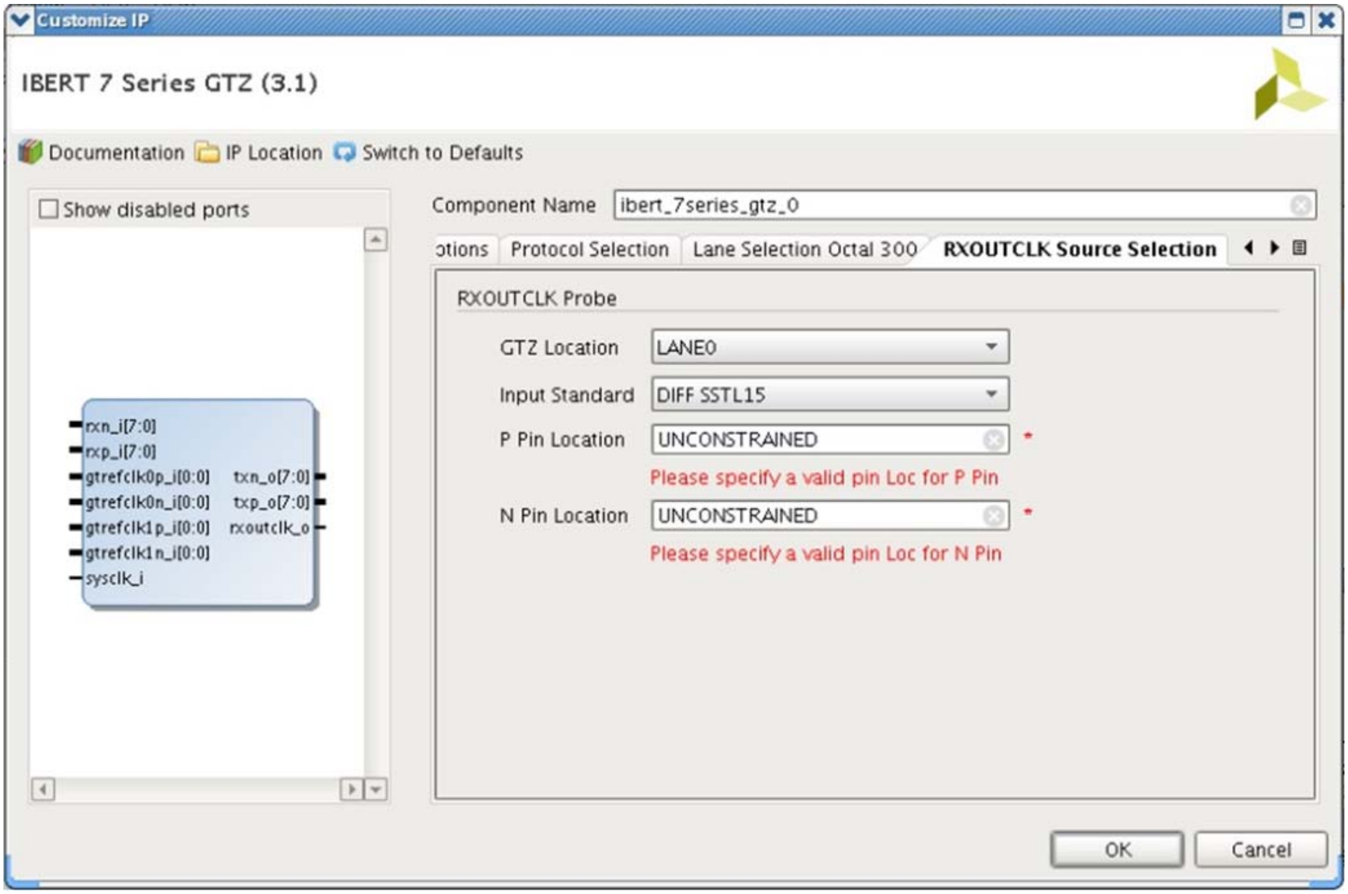

Figure 4-4: **Vivado Customize IP Dialog Box – RXOUTCLK Source Selection**

Summary

Review the settings chosen in the summary page and if they are satisfactory, click **OK** to generate the IBERT core.

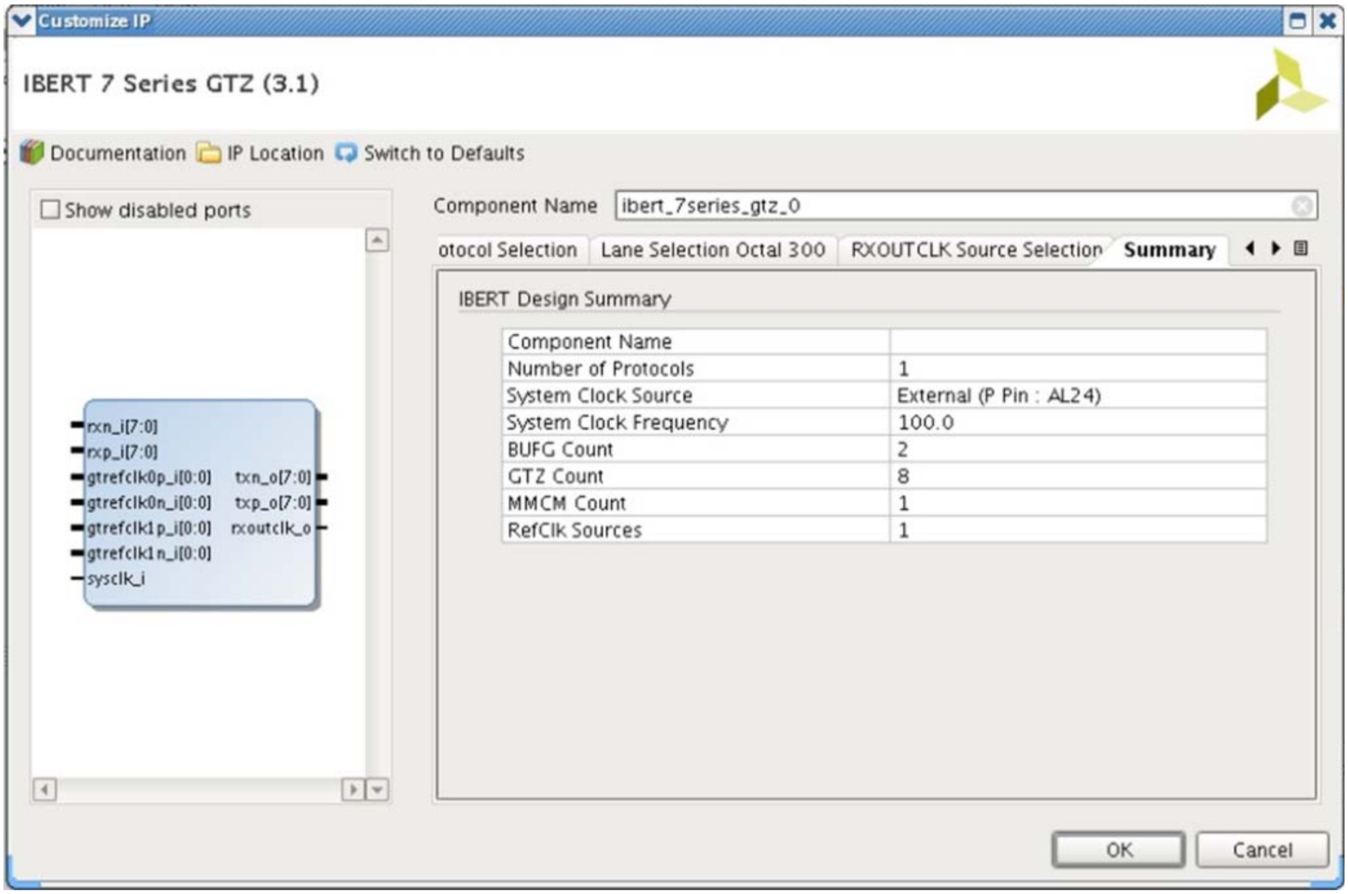

Figure 4-5: **Vivado Customize IP Dialog Box – Summary**

User Parameters

Table 4-1 shows the relationship between the fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl Console).

Table 4-1: **Vivado IDE Parameter to User Parameter Relationship**

Vivado IDE Parameter/Value	User Parameter/Value	Default Value
Frequency	C_SYSCLK_FREQUENCY	100.00
Input Standard	C_SYSCLK_IO_PIN_STD	DIFF_SSTL15
P Pin Location	C_SYSCLK_IO_PIN_LOC_P	AL24
N Pin Location	C_SYSCLK_IO_PIN_LOC_N	AL25
Add RXOUTCLK Probe	C_ADD_RXOUTCLK_PROBES	FALSE
Silicon Version	C_SILICON_VERSION	Initial_ES

Table 4-1: **Vivado IDE Parameter to User Parameter Relationship *(Cont'd)***

Vivado IDE Parameter/Value	User Parameter/Value	Default Value
Number of Protocols	C_PROTOCOL_COUNT	1
Protocol	C_PROTOCOL0	Protocol0
Line Rate (Gb/s)	C_LINERATE0	10.3125
Data Width	C_DATAWIDTH0	160
Refclk (MHz)	C_REFCLK0	322.26563
Lane Count	C_PROTOCOL0_LANE_COUNT	8
REFCLK Source	C_REFCLK_SOURCE0	REFCLK0
GTZ Location	C_RXOUTCLK0_LANE_SEL	LANE0
Input Standard	C_RXOUTCLK_IO_PIN_STD	DIFF_SSTL15
P Pin Location	C_RXOUTCLK_IO_PIN_LOC_P	Unconstrained
N Pin Location	C_RXOUTCLK_IO_PIN_LOC_N	Unconstrained

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3].

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

The IBERT GTZ core is generated with its own timing and location constraints, based on the choices the user made when customizing the core. No additional constraints are required.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

This core does not support simulation.

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3].

Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

Purpose of the Example Design

An example design can be generated for any customization of the 7 series IBERT core. After you have customized and generated a core instance, right-click the generated core and select **Open IP Example Design** in the Vivado IDE for that instance. A separate Vivado project opens with the IBERT example design as the top-level module. The example design instantiates the customized core. The recommended and supported flow is to use the example design as-is, without modifications outside the Vivado IDE.

The purpose of the IBERT IP example design is to:

- Provide a quick demonstration of the customized core instance operating in hardware through the use of a link status indicator based on PRBS generators and checkers which are part of core and generated during IP generation.
- Provide a system which includes reference clock buffers and example system-level constraints.
- Speed up hardware bring-up and debug through the inclusion of a pattern generator and checker.

The example design contains configurable PRBS generator and checker modules per transceiver channel that enable simple data integrity testing, and resulting link status reporting. The example design is also synthesizable so it can be used to check for data integrity and hardware links, either through loopback or connection to a suitable link partner. All key status signals, driving basic control signals, and hardware I/O interaction can be done using the Serial I/O Analyzer from the Vivado Hardware Manager after downloading the example design generated bit file.

Directory Structure and File Contents

<component_name>_example/<component_name>_example.srcs/
Top-level project directory; name is user-defined

- constrs_1/imports/<component name>/
  - ibert_7series_gtz.xdc
  - local.xdc
  - timing.xdc
- sources_1/imports/<component name>/
  - example_<component name>.v
- sources_1/ip/<component name>

Note: Only Verilog is supported.

<component_name>_example/<component_name>_example.srcs/

This directory contains the source files needed to synthesize the IBERT GTZ core whose name is `<component_name>`.

Table 5-1: **IBERT GTZ Example Design Source Files**

Name	Description
constrs_1/imports/<component_name>/	
Ibert_7series_gtz.xdc	Constraint file for example design
local.xdc	Constraint file for example design
timing.xdc	Constraint file for example design
sources_1/imports/<component_name>/	
example_<component_name>.v	Verilog (.v) source file for the example design

Implementation

To implement the example design, select **Run Implementation** in the **Vivado Project Manager** window. For further details on setting up the implementation, see the *Vivado Design Suite User Guide: Implementation* (UG904) [Ref 6].

Appendix A

Migrating and Upgrading

This appendix contains information about upgrading to a more recent version of the IP core.

Upgrading in the Vivado Design Suite

This section provides information about any changes to the user logic or port designations between core versions.

Changes from v1.0 to v3.0

Example Design added.

Parameter Changes

No change.

Port Changes

No change.

Other Changes

No change.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

TIP: *If the IP generation halts with an error, there might be a license issue. See License Checkers in Chapter 1 for more details.*

Finding Help on Xilinx.com

To help in the design and debug process when using the IBERT 7 series GTZ transceivers, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the IBERT 7 series GTZ transceivers. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the IBERT 7 Series GTZ Transceivers Core

AR 54607

Contacting Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Debug Tools

There are many tools available to address IBERT 7 series GTZ transceivers design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used with the logic debug IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 8].

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

References

These documents provide supplemental material useful with this product guide:

1. *7 Series FPGAs Overview* (DS180)
2. *Vivado® Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
3. *Vivado Design Suite User Guide: Designing with IP* (UG896)
4. *Vivado Design Suite User Guide: Getting Started* (UG910)
5. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
6. *Vivado Design Suite User Guide: Implementation* (UG904)
7. *ISE® to Vivado Design Suite Migration Guide* (UG911)
8. *Vivado Design Suite User Guide, Programming and Debugging* (UG908)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/08/2016	3.1	Example Design added.
06/24/2015	3.1	• Updated Resource Utilization section. • Updated Fig. 4-1 to 4-5. • Added User Parameters section. • Added descriptions in Example Design and Migration chapters.
06/19/2013	3.0	• Initial Xilinx public release of document in product guide format. Replaces DS878. • Revision number advanced to 3.0 to align with core version number.

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