Integrated Bit Error Ratio Tester 7 Series GTX Transceivers v3.0

LogiCORE IP Product Guide

Vivado Design Suite

PG132 June 8, 2016

XILINX
ALL PROGRAMMABLE™

Table of Contents

Chapter 1: Overview

Chapter 2: Product Specification

Chapter 3: Designing with the Core

Chapter 4: Design Flow Steps

Chapter 5: Example Design

Appendix A: Migrating and Upgrading

Appendix B: Debugging

Appendix C: Additional Resources and Legal Notices

Introduction

The LogiCORE™ IP Integrated Bit Error Ratio Tester (IBERT) core for 7 series FPGA GTX transceivers is designed for evaluating and monitoring the GTX transceivers. This core includes pattern generators and checkers that are implemented in FPGA logic, and access to ports and the dynamic reconfiguration port attributes of the GTX transceivers. Communication logic is also included to allow the design to be run time accessible through JTAG. This core can be used as a self-contained or open design, based on customer configuration, and as described in this document.

Features

- Provides a communication path to the Vivado® Serial I/O Analyzer feature
- Provides a user-selectable number of 7 series FPGA GTX transceivers
- Transceivers can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width
- Requires a system clock that can be sourced from a pin or one of the enabled GTX transceivers

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Zynq®-7000 All Programmable SoC Virtex®-7 Kintex®-7
Supported User Interfaces	N/A
Resources	Performance and Resource Utilization webpage
Provided with Core	
Design Files	register transfer level (RTL)
Example Design	Verilog
Test Bench	Not Provided
Constraints File	Xilinx Design Constraints (XDC)
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	Not Provided
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page.	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Chapter 1

Overview

Functional Description

The IBERT core provides a broad-based Physical Medium Attachment (PMA) evaluation and demonstration platform for 7 series FPGA GTX transceivers. Parameterizable to use different GTX transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and logic widths. Data pattern generators and checkers are included for each GTX transceiver desired, giving several different Pseudo-random binary sequence (PRBS) and clock patterns to be sent over the channels.

In addition, the configuration and tuning of the GTX transceivers is accessible though logic that communicates to the Dynamic Reconfiguration Port (DRP) port of the GTX transceiver, to change attribute settings, as well as registers that control the values on the ports. At run time, the Vivado® serial I/O analyzer communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

Feature Summary

The IBERT core is designed for PMA evaluation and demonstration. All the major physical medium attachment (PMA) features of the GTX transceiver are supported and controllable, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- Decision Feedback Equalizer (DFE)
- Phase-Locked Loop (PLL) divider settings

Some of the Physical Coding Sublayer (PCS) features offered by the transceiver are outside the scope of IBERT, including:

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

PLL Configuration

For each serial transceiver channel, there is a ring PLL called Channel PLL (CPLL). The GTX in the 7 series FPGA has an additional shared PLL per quad, Quad PLL (QPLL). This QPLL is shared LC PLL to support high speed, high performance, and low power multi-lane applications.

Figure 1-1 shows a Quad in a 7 series device. The GTXE2_CHANNEL component has the serial transceiver and CPLL units and the GTXE2_COMMON has the QPLL unit.

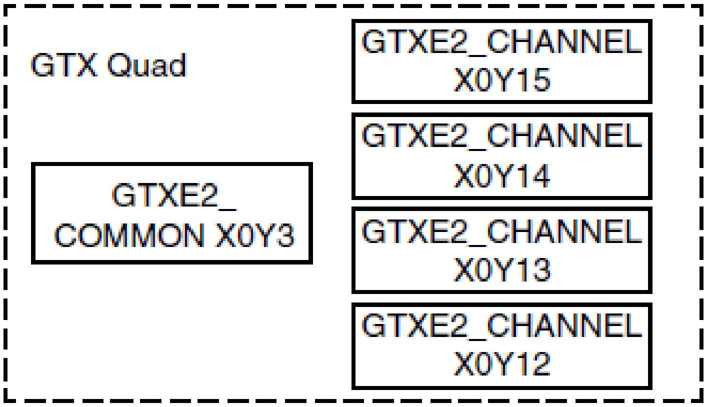


Figure 1-1: **Quad in a 7 Series Device**

The serial transceiver REFCLK can be sourced from either CPLL or QPLL based on multiplexers as shown in Figure 1-2.

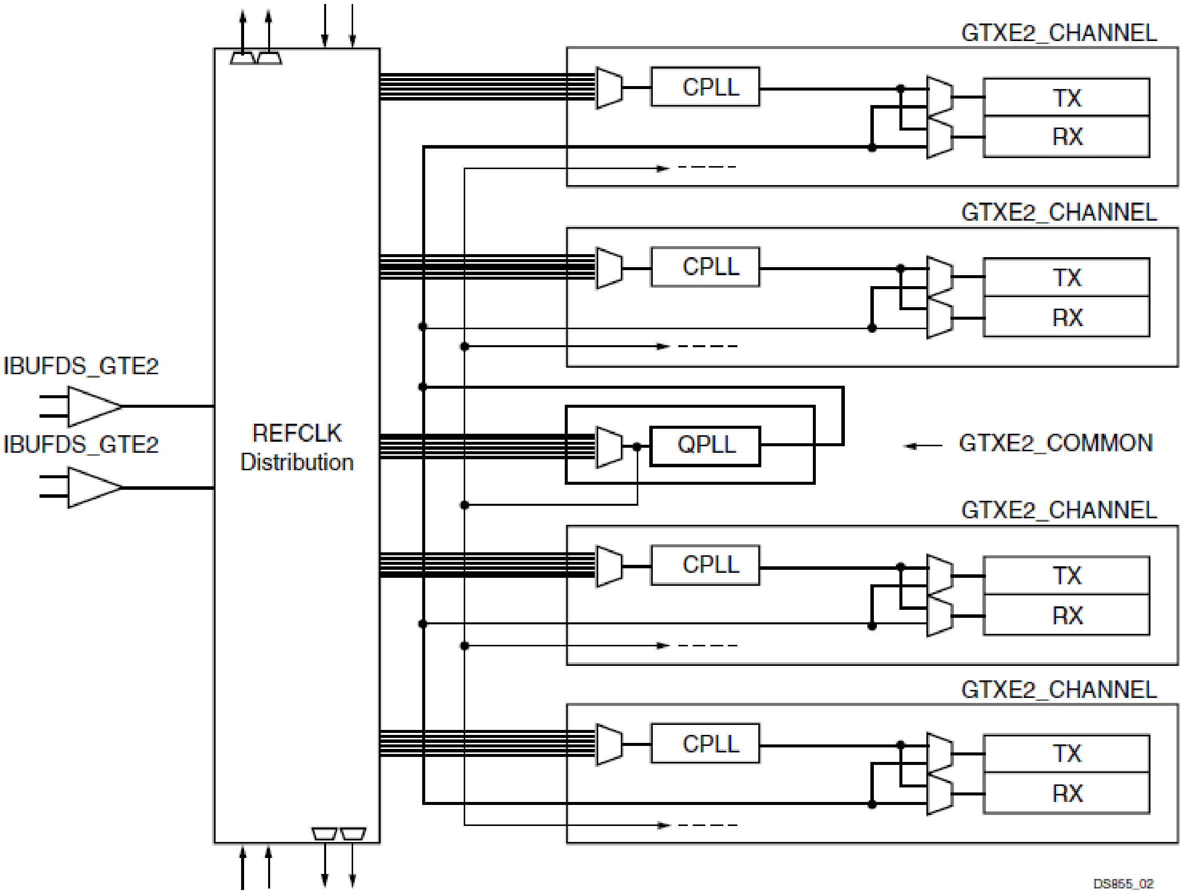


Figure 1-2: **Serial Transceiver REFCLK Sourcing**

Pattern Generation and Checking

Each GTX transceiver enabled in the IBERT design has a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker accepts data through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS 31-bit, Clk 2x (101010...), and Clk 10x (11111111110000000000...) patterns.

These patterns are optimized for the logic width that was selected at run time. The TX and RX patterns are individually selected.

Using the pattern checker logic, the incoming data is compared against a pattern that is internally generated. When the checker receives five consecutive cycles of data with no errors, the `LINK` signal is asserted. If the `LINK` signal is asserted and the checker receives five consecutive cycles with data errors, the `LINK` signal is deasserted. Internal counters accumulate the number of words and errors received.

DRP and Port Access

You can change GTX transceiver ports and attributes. The DRP interface logic allows the run time software to monitor and change any attribute of the GTX transceivers and the corresponding CPLL/QPLL. When applicable, readable and writable registers are also included that are connected to the various ports of the GTX transceiver. All are accessible at run time using the Vivado serial I/O analyzer.

Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of 7 series FPGA GTX transceivers.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Performance

The core can be configured to run any of the allowable line rates for the GTX transceivers. See the *7 Series FPGAs Overview* (DS180) [Ref 1] for the line rates supported by speed grade.

Maximum Frequencies

The core can operate at the maximum user clock frequencies for the FPGA logic width/ speed grade selected. The maximum system clock rate is 125 MHz and the generated design divides any incoming system clock to adhere to this constraint.

Resource Utilization

For full details about performance and resource utilization, visit the Performance and Resource Utilization web page.

Port Descriptions

The core ports are shown in Table 2-1.

Table 2-1: **Core Ports**

Signal Name	I/O	Description
SYSCLK_I	I	Clock that clocks all communication logic. This port is present only when an external clock is selected in the generator.
TXP_O[n - 1:0]	O	Transmit differential pairs for each of the n GTX transceivers used.
TXN_O[n - 1:0]		
RXN_I[n - 1:0]	I	Receive differential pairs for each of the n GTX transceivers used.
RXP_I[n - 1:0]		
GTREFCLK0_I[n - 1:0]	I	GTX transceiver reference clocks used. The number of MGTREFCLK ports can be equal to or less than the number of TX and RX ports because some GTX transceivers can share clock inputs.
GTREFCLK1_I[n - 1:0]		
RXOUTCLK_O	O	Quad based RX output clock.

Chapter 3

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

Line Rate Support

The core supports a maximum of three different line rates in a single design. For each of these line rates, you can select a custom value based on your requirements, or you can choose from pre-provided industry standard protocols (for example, CPRI™, Gigabit Ethernet, or XAUI). Specify the number of serial transceivers for each line rate that is programmed with these settings. Because usage of QPLL is recommended for line rates above 6.5 Gb/s, you can select QPLL/CPLL for each line rate falling in the range 0.6 Gb/s to 6.5 Gb/s.

Serial Transceiver Location

Based on the total number of serial transceivers selected, provide the specific location of each serial transceiver that you intend to use. The region shown in the panel indicates the location of serial transceivers in the tile. This demarcation of region is based on the physical placement of serial transceivers with respect to median of BUFGs available for each device.

Clocking

System Clock

The IBERT core requires a free-running system clock for communication and other logic that is included in the core. This clock can be chosen at generation time to originate from an FPGA pin, or from a dedicated REFCLK input of one of the GTX transceivers. In order for the core to operate properly, this system clock source must remain operational and stable when the FPGA is configured with the IBERT core design.

If the system clock is running faster than 150 MHz, it is divided down internally using a Mixed-Mode Clock Manager (MMCM) to satisfy timing constraints. The clock source selected must be stable and free running after the FPGA is configured with the IBERT design. The system clock is used for core communication and as a reference for system measurements. Therefore, the clock source selected must remain operational and stable when using the IBERT core.

Receiver Output Clock

The receiver clock probe enable is provided to pull out a recovered clock from any serial transceiver, if desired. When enabled, a new panel appears just before the summary page where you can fill in the serial transceiver source and probe pin standards.

Reference Clock

The reference clock source should be provided for all the serial transceivers selected. The drop-down list provides you with possible sources based on local clocks in the same quad and shared clocks from north/south quads.

Resets

Run time resets are available for the BERT counters and all GT resets are available.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 4]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 6]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 7]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 8]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 4] for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the Vivado IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 6] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 7].

Note: Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Figure 4-1 to Figure 4-4 show the IBERT Customize IP dialog boxes with information about customizing ports.

Entering the Component Name

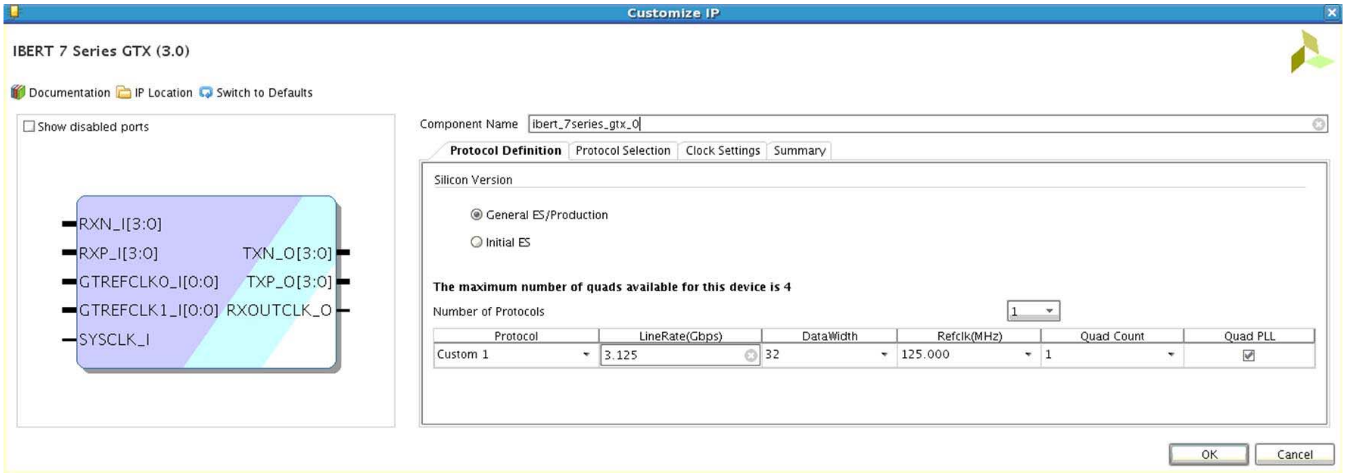
The Component Name field can consist of any combination of alpha-numeric characters including the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

Silicon Version

Choose either the **General ES/Production** or **Initial ES** radio button to match the silicon targeted.

Protocol Definition

A protocol is a line rate/data width/reference clock rate combination. Up to three protocols can be defined for an IBERT core, and any number of available Quads can be designated as any protocol defined.



□ Show disabled ports

Component Name: ibert_7series_gtx_0

Silicon Version

● General ES/Production

○ Initial ES

The maximum number of quads available for this device is 4

Number of Protocols: 1

Protocol	LineRate(Gbps)	DataWidth	Refclk(MHz)	Quad Count	Quad PLL
Custom 1	3.125	32	125.000	1	☑

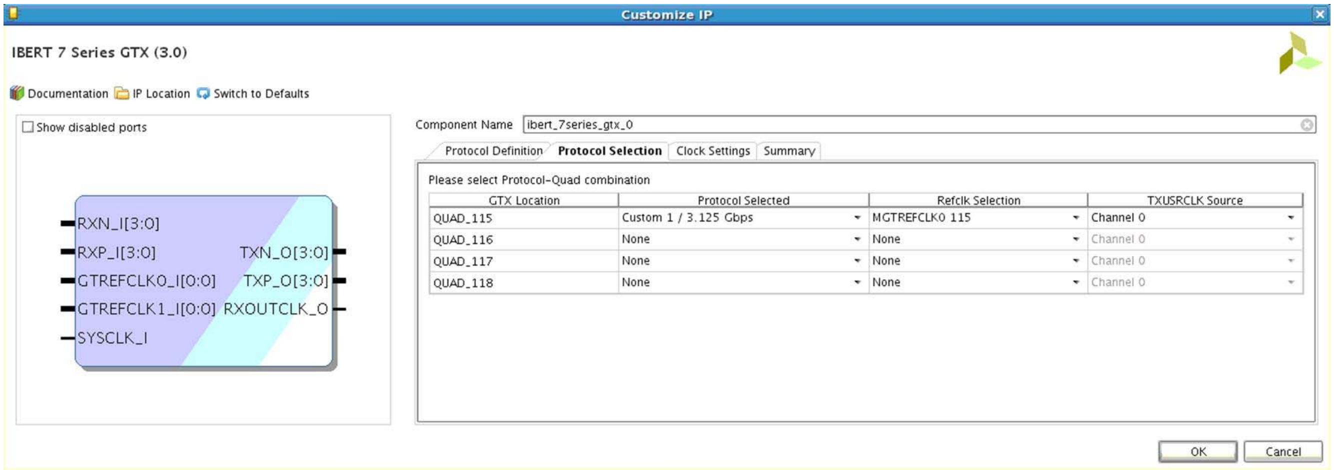
Figure 4-1: **Vivado Customize IP Dialog Box – Protocol Definition**

1. Choose the number of protocols desired.
2. In the Protocol combination box, select either Custom or a Pre-defined protocol. If Custom, type in the line rate (the rate appears in red text if outside the range allowed).
   a. Select the data width.
   b. Choose the REFCLK rate and the number of Quads running at this rate.

   Changing the line rate entered changes the choices in the REFCLK combination box.
3. The Quad PLL is selected by default. To select CPLL instead, uncheck the QPLL checkbox.

Protocol Selection

In the **Protocol Selection** tab, the Quads available in the device/package combination are shown. To allocate a Quad to a specific protocol, select it in the **Protocol Selected** combination. The legal choices for the reference clock input are listed in the `REFCLK` selection combination. After a Quad is allocated to a protocol, the `TXUSRCLK` source combination is enabled. The `TXUSRCLKs` are shared among all four channels in the Quad, so use this combination to select which of the four lanes `TXOUTCLK` should be used for the user clocks.



☐ Show disabled ports

Component Name: ibert_7series_gtx_0

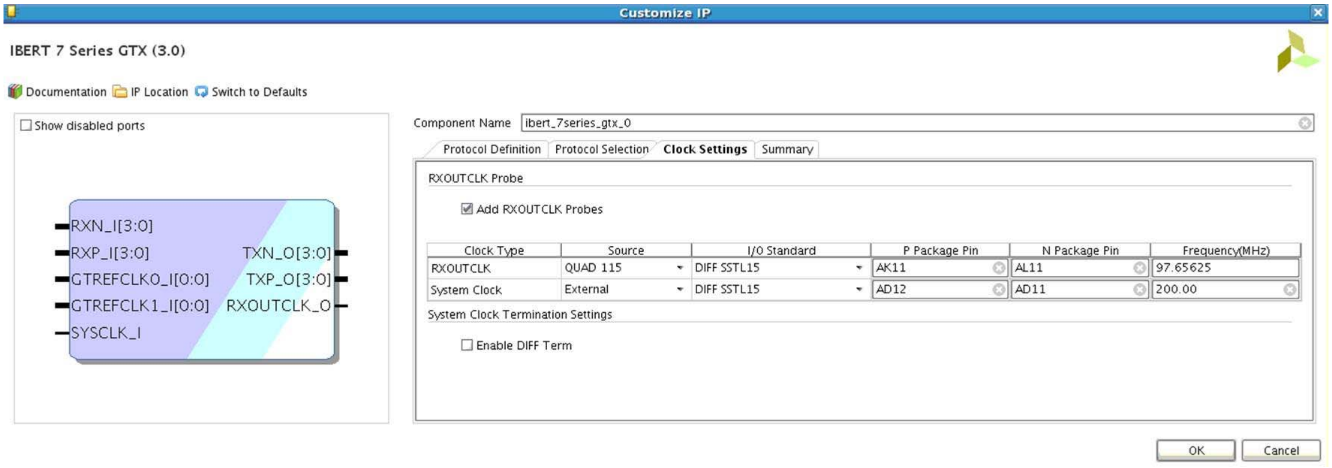
Please select Protocol-Quad combination

GTX Location	Protocol Selected	Refclk Selection	TXUSRCLK Source
QUAD_115	Custom 1 / 3.125 Gbps	MGTREFCLK0 115	Channel 0
QUAD_116	None	None	Channel 0
QUAD_117	None	None	Channel 0
QUAD_118	None	None	Channel 0

Figure 4-2: **Vivado Customize IP Dialog Box – Protocol Selection**

Clock Settings

In the **Clock Settings** tab, click the **Add RXOUTCLK Probes** to drive an output pin or pin pair with the RXOUTCLK of lane 0 of the Quad. Select the **I/O Standard** from the list and assign valid pin locations.



☐ Show disabled ports

Component Name: ibert_7series_gtx_0

RXOUTCLK Probe

☑ Add RXOUTCLK Probes

Clock Type	Source	I/O Standard	P Package Pin	N Package Pin	Frequency(MHz)
RXOUTCLK	QUAD 115	DIFF SSTL15	AK11	AL11	97.65625
System Clock	External	DIFF SSTL15	AD12	AD11	200.00

System Clock Termination Settings

☐ Enable DIFF Term

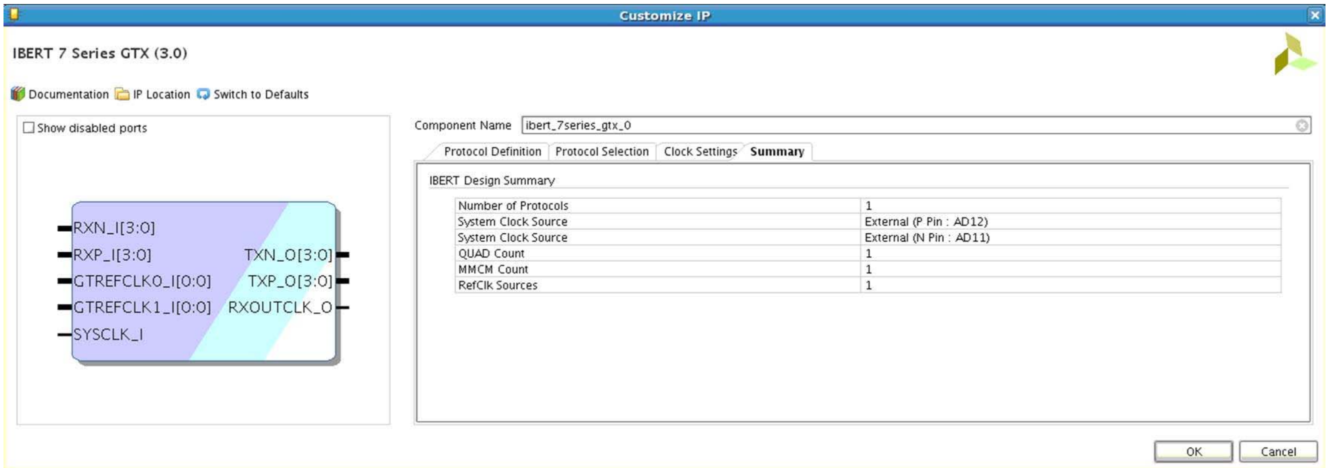
Figure 4-3: **Vivado Customize IP Dialog Box – Clock Settings**

RECOMMENDED: *For the system clock, select an external clock source to drive the system clock of the IBERT design.*

Select an **I/O Standard**, valid pin locations, and frequency to complete the system clock settings. Alternatively, any enabled Quad reference clock can be chosen instead.

Summary

Review the settings chosen in the summary page and if they are satisfactory, click **OK** to generate the IBERT core.



Component Name ibert_7series_gtx_0

IBERT Design Summary

Number of Protocols	1
System Clock Source	External (P Pin : AD12)
System Clock Source	External (N Pin : AD11)
QUAD Count	1
MMCM Count	1
RefClk Sources	1

Figure 4-4: **Vivado Customize IP Dialog Box –Summary**

User Parameters

Table 4-1 shows the relationship between the GUI fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl Console).

Table 4-1: **Vivado IDE Parameter to User Parameter Relationship**

Vivado IDE Parameter/Value	User Parameter/Value	Default Value
Component name	Component_Name	ibert_7series_gtx_v3_0
Silicon Version	C_SI_VER	General ES/Production
Number of Protocols	C_PROTOCOL_COUNT	1
Protocol	C_PROTOCOL_1	Custom_1
Line Rate (Gb/s)	C_PROTOCOL_MAXLINERATE_1	3.125
Data Width	C_PROTOCOL_DATAWIDTH_1	32
Refclk (MHz)	C_PROTOCOL_RXREFCLK_FREQUENCY_1	125
Quad Count	C_PROTOCOL_GT_COUNT_1	1
PLL Used	C_PROTOCOL_USE_QUAD_PLL_1	QPLL

Table 4-1: **Vivado IDE Parameter to User Parameter Relationship *(Cont'd)***

Vivado IDE Parameter/Value	User Parameter/Value	Default Value
Protocol Selected	C_PROTOCOL_QUAD0	Custom_1/3.125_Gbps
REFCLK Source	C_REFCLK_SOURCE_QUAD_0	REFCLK0
TXUSRCLK Source	C_CHANNEL_QUAD_0	Channel 0
Add RXOUTCLK Probe	C_ADD_RXOUTCLK_PROBES	False
Frequency	C_SYSCLK_FREQUENCY	200.00
Input Standard	C_SYSCLK_IO_PIN_STD	DIFF_SSTL15
P Pin Location	C_SYSCLK_IO_PIN_LOC_P	UNASSIGNED
N Pin Location	C_SYSCLK_IO_PIN_LOC_N	UNASSIGNED
Enable DIFF Term	C_ENABLE_DIFF_TERM	False

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 6].

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

The IBERT GTX core is generated with its own timing and location constraints, based on the choices the user made when customizing the core. No additional constraints are required.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

This core does not support simulation.

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 6].

Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

An example design can be generated for any customization of the 7 series IBERT core. After you have customized and generated a core instance, right-click the generated core and select **Open IP Example Design** in the Vivado IDE for that instance. A separate Vivado project opens with the IBERT example design as the top-level module. The example design instantiates the customized core. The recommended and supported flow is to use the example design as-is, without modifications outside the Vivado IDE.

The purpose of the IBERT IP example design is to:

- Provide a quick demonstration of the customized core instance operating in hardware through the use of a link status indicator based on PRBS generators and checkers which are part of core and generated during IP generation.
- Provide a system which includes reference clock buffers and example system-level constraints.
- Speed up hardware bring-up and debug through the inclusion of a pattern generator and checker.

The example design contains configurable PRBS generator and checker modules per transceiver channel that enable simple data integrity testing and resulting link status reporting. The example design is also synthesizable so it can be used to check for data integrity and hardware links, either through loopback or connection to a suitable link partner. All key status signals, driving basic control signals, and hardware I/O interaction can be done using the Serial I/O Analyzer from the Vivado Hardware Manager after downloading the example design generated bit file.

Appendix A

Migrating and Upgrading

This appendix contains information about upgrading to a more recent version of the IP core.

Upgrading in the Vivado Design Suite

This section provides information about any changes to the user logic or port designations between core versions.

Changes from v1.0 to v3.0

Example Design added.

Parameter Changes

No change.

Port Changes

No change.

Other Changes

No change.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the IBERT 7 series GTX transceivers, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the IBERT 7 series GTX transceivers. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the IBERT 7 Series GTX Transceivers

AR 54607

Contacting Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Debug Tools

There are many tools available to address IBERT 7 series GTX transceivers design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used with the logic debug IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 8].

License Checkers

If the IP requires a license key, the key must be verified. The Vivado design tools have several license check points for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

References

These documents provide supplemental material useful with this product guide:

1. *Vivado Design Suite User Guide, Programming and Debugging* (UG908)
2. 7 Series FPGAs GTX/GTH Transceivers User Guide (UG476)
3. *7 Series FPGAs Overview* (DS180)
4. *Vivado® Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
5. *ISE to Vivado Design Suite Migration Guide* (UG911)
6. *Vivado Design Suite User Guide: Designing with IP* (UG896)
7. *Vivado Design Suite User Guide: Getting Started* (UG910)
8. *Vivado Design Suite User Guide: Implementation* (UG904)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/08/2016	3.0	• Example Design added • User Parameters section added
03/20/2013	1.0	Initial Xilinx release of the product guide and replaces DS872.

Please Read: Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at http://www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at http://www.xilinx.com/legal.htm#tos.