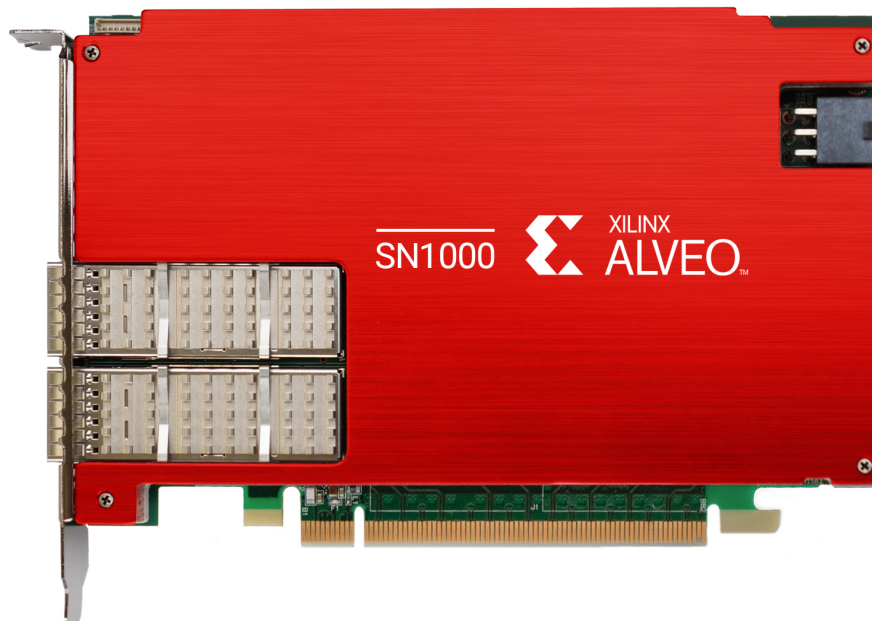


Summary

The Xilinx® Alveo™ SN1000 SmartNICs bring true convergence of network, compute, and storage acceleration to a single platform. As shown in the following figure, the Alveo SN1000 SmartNICs are offered in a single slot, half-length, full height form factor. The card consists of an XCU26 FPGA (XCU26-L2VSVA1365E) and an NXP Layerscape LX2162A processor featuring 16 Arm® v8 Cortex®-A72 cores. The card is passively-cooled, and has two QSFP28 network connections and a x16 PCI Express® Gen 3/Gen 4 x8 interface connected to the XCU26. The card currently supports a 1×100GbE network configuration via Port 1 only. The card has a maximum electrical power limit of 75W. The SN1000 SmartNICs integrate the XCU26 FPGA with the LX2162A processor, enabling hardware accelerated networking, compute, and storage applications to process data with maximum efficiency while avoiding unnecessary data movements and CPU processing. The SN1000 SmartNICs enable cloud service providers to maximize CPU savings by offloading infrastructure workloads to the SmartNIC and enabling deployment of bare-metal services.

Figure 1: Alveo SN1000 SmartNICs



X24615-022421

Xilinx is creating an environment where employees, customers, and partners feel welcome and included. To that end, we're removing non-inclusive language from our products and related collateral. We've launched an internal initiative to remove language that could exclude people or reinforce historical biases, including terms embedded in our software and IPs. You may still find examples of non-inclusive language in our older products as we work to make these changes and align with evolving industry standards. Follow this [link](#) for more information.

Product Details

Table 1: Alveo SN1000 SmartNICs Product Details

Specification	Alveo SN1000 SmartNICs
Production product SKU	A-SN1022-P4N-PQ (2x100G, encryption disabled) A-SN1022-P4E-PQ (2x100G, encryption enabled)
Total electrical card load	75W
Thermal design power (TDP)	70W
Thermal cooling solution	Passive
Form factor	Full height, half length
Network interface	2 x QSFP28 (currently supports a 1x100GbE network configuration via Port 1 only)
PCIe interface	Gen 3 x16/Gen 4 x8 to host system and Gen 3 x8 to communications processor
FPGA	
FPGA DDR	Two 4 GB DDR4 component interface 72b with ECC operating at 2400 MT/s
LUTs/Registers/DSP slices	1030K/2059K/1320
Maximum distributed RAM/block Ram/UltraRAM	14.2 Mb/74.3 Mb/99 Mb
Communications Processor	
Arm processor	NXP Layerscape LX2162A
Cores	16 Arm v8 Cortex-A72 CPU cores, running up to 2.0 GHz
Cache buffer	16 MB cache
Packet buffer	2 MB packet caching buffer
Connection to FPGA	PCIe Gen 3 x8
DDR	4 GB DDR4 component x72 up to 2400 MT/s
System storage	Flash: NAND 128 Gb (16G x 8) eMMC for root file system
	Flash: NOR 512 Mb SERIAL MT35X OSPI for boot

Table 1: Alveo SN1000 SmartNICs Product Details (cont'd)

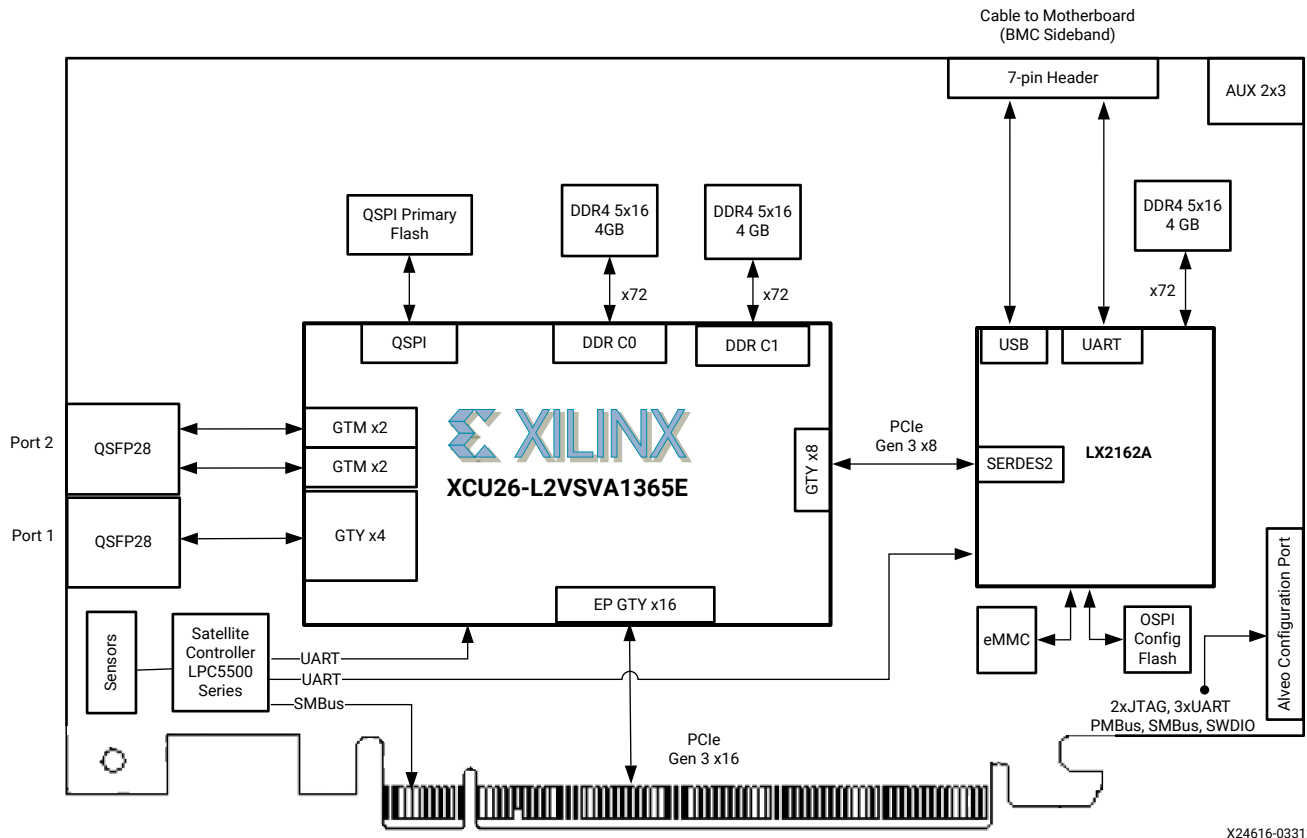
Specification	Alveo SN1000 SmartNICs
Feature summary ¹	<ul style="list-style-type: none"> • Stateless offloads • Linux multi-queue • SR-IOV • Tunneling offloads • Accelerated receive flow steering • Transmit packet steering • Open virtual switching (OvS) • Hardware-based virtualization (match/action engine) • Hardware offloaded Virtio-net: <ul style="list-style-type: none"> ◦ Virtual datapath acceleration • Hardware offloaded Virtio-blk • Ceph RBD client offload • Support for custom plug-ins to enable new functionality programmed via P4, HLS, or RTL • PXE and UEFI boot support • NC-SI/PLDM over MCTP SMBus • MCTP PCIe VDM • DPDK support • Onload support • Secure firmware upgrade and hardware root of trust • OS support: <ul style="list-style-type: none"> ◦ Red Hat Enterprise Linux (RHEL), CentOS, and Ubuntu for host CPU ◦ Debian-based package for on-board Arm processor

Notes:

1. Feature availability is software release dependent. Check the release notes or contact [Xilinx Support](#) for more information.

The following figure shows the components within the Alveo SN1000 SmartNICs.

Figure 2: Alveo SN1000 Block Diagram



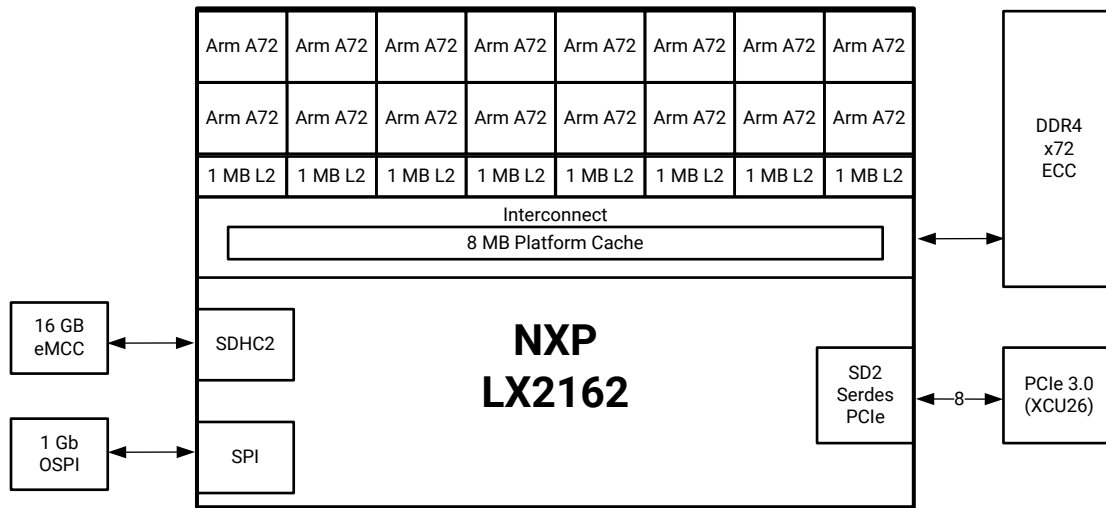
X24616-033121

The XCU26 is based on the Xilinx 16 nm UltraScale architecture. The programmable logic (PL) region is connected to two QSFP28 cages, but currently supports a 1x100GbE network configuration via Port 1 only. The XCU26 also has two 4 GB x72 of DDR4 memory component interfaces and a PCIe CEM 3.0 compliant x16 edge-finger interface.

The XCU26 is connected to an NXP Layerscape LX2162A Arm processor through a PCIe 3.0 compliant x8 interface. The LX2162A supports 16 Cortex-A72 cores, a 46 Gb/s security engine and an 88 Gb/s data compression engine. For system applications, the LX2162A has a dedicated DDR4 memory interface with 4 GB x72 DDR4, a dedicated 32 GB eMMC NAND, and a 1 Gb OSPI NOR flash. The Arm processor on the SN1000 SmartNICs helps to increase the server CPU efficiency and lower total costs by offloading workloads from the host.

Typical examples of offloaded services include virtual switching (OVS), software-defined storage, and data and network encryption. This SmartNIC offloading capability also allows cloud service providers to maximize CPU savings by offloading infrastructure workloads to the SmartNIC and enabling deployment of bare-metal services.

Figure 3: XCU26 Communication Processor Floorplan



X24618-102320

Card Specifications

Dimensions

The Alveo SN1000 SmartNICs are compliant with the PCIe CEM rev. 3.0 specification as single slot, full height, half length cards. The dimensions in the following table do not include the bracket.

Table 2: Card Dimensions

Parameter	Dimension
Height	0.72 inch (18.3 mm)
Width	4.38 inch (111.15 mm)
Length	6.59 inch (167.5 mm)

Network Interfaces and Manageability

Alveo SN1000 SmartNICs support both in-band and out-of-band communication with the host. In-band communication is provided by PCIe bus with sixteen lanes allocated to the XCU26. In addition, in-band communication with the management subsystem, particularly reading any sensor values, is done via the satellite microcontroller on board the SN1000 SmartNICs. The sensor values can be read via the standard Linux mechanisms using the sensors command from the lm_sensors package in your Linux distribution.

For out-of-band communications, the platform management subsystem on the Alveo SN1000 SmartNIC uses Platform Management Components Intercommunication (PMCI) conformance standards and command implementations. Adapter manageability is supported through the platform level data model (PLDM) and network controller sideband interface (NC-SI) specifications. Limited manageability is also available through the unified extensible firmware interface (UEFI) and command line processing (CLP) interfaces.

The Alveo SN1000 SmartNICs support the following manageability protocols:

- PLDM
- NC-SI

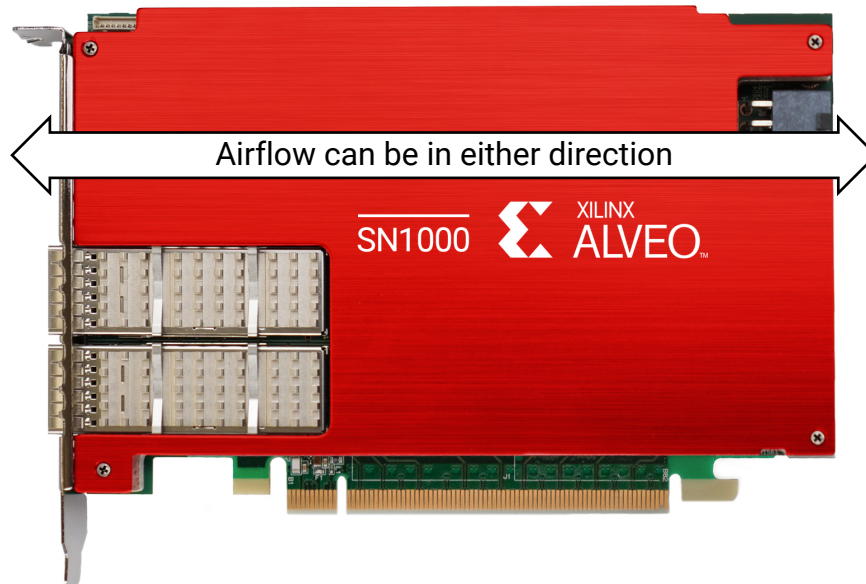
The Alveo SN1000 SmartNICs support the following manageability transports:

- MCTP SMBus
- MCTP PCIe VDM

Thermal Specifications

The Alveo SN1000 SmartNICs support airflow in either direction.

Figure 4: Airflow Direction for SN1000 SmartNICs



X24623-022421

The following table shows requirements for Alveo SN1000 SmartNICs that are dependent on airflow direction.

Table 3: Airflow Direction Dependent Requirements

Specification	Requirements
QSFP case temperature for airflow entering PCIe bracket	QSFP($\leq 2.5W$) case should be rated 70°C
QSFP case temperature for airflow exiting PCIe bracket	QSFP ($\leq 2.5W$) case should be rated 85°C
Airflow entering PCIe bracket area	104.6 mm x 13.2 mm
Airflow exiting PCIe bracket area	98.4 mm x 20.3 mm

Inlet Temperature versus Airflow Requirement in Server

The following tables provide the required airflow rate and airflow speed to SN1000 SmartNICs under various operating conditions.

Table 4: Normal Flow (Exhaust Air from I/O Bracket) at Sea Level

Inlet Temperature vs Airflow Requirement of PCIe Card Slot (98.4 mm x 20.33 mm) at Sea Level for 70W Total Card Power						
Inlet Temperature to the Card (°C)	I/O Bracket (70°C) with QSFP Optical Module (85°C)			I/O Bracket (70°C) without QSFP ¹		
	CFM	LFM	Static Pressure	CFM	LFM	Static Pressure
25	3.9	181	0.10	2.5	118	0.05
30	4.6	212	0.12	2.9	137	0.06
35	5.5	254	0.16	3.4	160	0.07
40	6.8	314	0.21	4.1	189	0.09
45	8.7	404	0.32	4.9	228	0.12
50	11.9	554	0.52	6.0	279	0.17
55	18.1	842	1.06	7.6	351	0.24

Notes:

1. A card without QSFP allocates more power in the FPGA than one with QSFP.

Table 5: Normal Flow (Exhaust Air from I/O Bracket) at 1200m Above Sea Level

Inlet Temperature vs Airflow Requirement of PCIe Card Slot (98.4 mm x 20.33 mm) at 1200m Above Sea Level for 70W Total Card Power						
Inlet Temperature to the Card (°C)	I/O Bracket (70°C) with QSFP Optical Module (85°C)			I/O Bracket (70°C) without QSFP ¹		
	CFM	LFM	Static Pressure	CFM	LFM	Static Pressure
25	4.2	193	0.11	2.7	127	0.05
30	4.9	227	0.13	3.2	146	0.07
35	5.9	273	0.17	3.7	171	0.08
40	7.3	337	0.24	4.4	203	0.10
45	9.4	435	0.35	5.3	245	0.14
50	12.9	597	0.59	6.5	301	0.19
55	19.6	909	1.21	8.2	379	0.27

Notes:

1. A card without QSFP allocates more power in the FPGA than one with QSFP.

Table 6: Reverse Flow (Inlet Air from I/O Bracket) at Sea Level

Inlet Temperature vs Airflow Requirement of PCIe Card Slot (104.57 mm x 13.18 mm) at Sea Level for 70W Total Card Power						
Inlet Temperature to the Card (°C)	I/O Bracket (70°C) with QSFP Optical Module (85°C)			I/O Bracket (70°C) without QSFP ¹		
	CFM	LFM	Static Pressure	CFM	LFM	Static Pressure
25	2.8	129	0.12	2.9	135	0.09
30	3.2	149	0.15	3.4	156	0.11
35	3.7	174	0.19	3.9	182	0.14
40	4.5	207	0.24	4.7	217	0.18
45	5.4	251	0.33	5.7	263	0.24
50	6.7	312	0.47	7.0	327	0.34
55	8.6	401	0.72	9.1	421	0.52

Notes:

1. A card without QSFP allocates more power in the FPGA than one with QSFP.

Table 7: Reverse Flow (Inlet Air from I/O Bracket) at 1200m Above Sea Level

Inlet Temperature vs Airflow Requirement of PCIe Card Slot (104.57 mm x 13.18 mm) at 1200m Above Sea Level for 70W Total Card Power						
Inlet Temperature to the Card (°C)	I/O Bracket (70°C) with QSFP Optical Module (85°C)			I/O Bracket (70°C) without QSFP ¹		
	CFM	LFM	Static Pressure	CFM	LFM	Static Pressure
25	3.0	138	0.13	3.1	145	0.10
30	3.4	160	0.16	3.6	167	0.12
35	4.0	187	0.21	4.2	196	0.15
40	4.8	222	0.27	5.0	233	0.20
45	5.8	270	0.37	6.1	283	0.27
50	7.2	336	0.53	7.6	353	0.39
55	9.3	433	0.82	9.8	455	0.59

Notes:

1. A card without QSFP allocates more power in the FPGA than one with QSFP.

Operating and Storage Conditions

Table 8: Operating and Storage Environmental Conditions

Specification	Requirements
Storage temperature	-40°C to 75°C
Storage humidity, non-condensing	5% to 95%
Operating temperature gradient	15°C/hour
Operating temperature	≤ 30°C
Operating humidity, non-condensing	8% to 90%, and a dew point of -12°C

Notes:

1. The above operating conditions are based on preliminary data. SN1000 SmartNICs are targeted to operate between an inlet ambient from 5°C to 55°C. For more information, contact your Xilinx sales representative.

Regulatory Compliance Statements

FCC Class A Products

Note: These devices are for use with UL Listed Servers or I.T.E.

Safety Compliance

The following safety standards apply to all products listed above.

- IEC 62368-1:2014 +A11:2017
- EU LVD Directive 2014/35/EU

EMC Compliance

The following standards apply.

Class A Products

- FCC Part 15 – Radiated & Conducted Emissions (USA)
- CAN ICES-3(A)/NMB-3(A) – Radiated & Conducted Emissions (Canada)
- CISPR 32 – Radiated & Conducted Emissions (International)
- EN55032: 2015 – Radiated & Conducted Emissions (European Union)
- EN55035:2017 – Immunity (European Union)
- EMC Directive 2014/30/EU
- VCCI (Class A)– Radiated & Conducted Emissions (Japan)
- CNS13438 – Radiated & Conducted Emissions (Taiwan)
- CNS 15663 - RoHS (Taiwan)

- AS/NZS CISPR 32 – Radiated and Conducted Emissions (Australia/New Zealand)
- Article 58-2 of Radio Waves Act, Clause 3 (Korea)

Regulatory Compliance Markings


When required, these products are provided with the following Product Certification Markings:


- UL Listed Accessories Mark for the USA and Canada
- CE mark
- FCC markings
- VCCI marking
- Australian C-Tick mark
- Korea MSIP mark
- Taiwan BSMI mark


FCC Class A User Information


The Class A products listed above comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

 **IMPORTANT!** *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.*

 **IMPORTANT!** *Cet équipement a été testé et jugé conforme à la Class A digital device, conformément à la règle 15 du standard FCC. Ces limites sont conçues pour fournir des protections contre des interférences nuisibles lorsque l'équipement est utilisé dans un environnement commercial. Cet équipement génère, utilise et peut émettre des énergies de radio-fréquence et, s'il n'est pas installé et utilisé conformément aux instructions, peut nuire aux communications radio. L'exploitation de cet équipement dans une zone résidentielle est susceptible de causer des interférences nuisibles, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates à ses propres frais.*

 **WICHTIG!** *Dieses Gerät wurde getestet und entspricht den Grenzwerten für digitale Geräte der Klasse A gemäß Teil 15 der FCC-Bestimmungen. Diese Grenzwerte bieten einen angemessenen Schutz gegen schädliche Interferenzen, wenn das Gerät in einer gewerblichen Umgebung betrieben wird. Dieses Gerät erzeugt und verwendet Hochfrequenzenergie und kann diese abstrahlen. Wenn es nicht gemäß den Anweisungen installiert und verwendet wird, kann dies Funkstörungen verursachen. Der Betrieb dieses Geräts in einem Wohngebiet kann schädliche Interferenzen verursachen. In diesem Fall muss der Benutzer die Interferenz auf eigene Kosten beheben.*

 **CAUTION!** *If the device is changed or modified without permission from Xilinx, the user may void his or her authority to operate the equipment.*



ATTENTION! Si l'appareil est modifié sans l'autorisation de Xilinx, l'utilisateur peut annuler son habilité à utiliser l'équipement.



VORSICHT! Wenn das Gerät ohne Erlaubnis von Xilinx geändert wird, kann der Benutzer seine Berechtigung zum Betrieb des Geräts verlieren.

Canadian Compliance (Industry Canada)

CAN ICES-3(A)/NMB-3(A)

China RoHS Compliance

- SJ/T 11363-2006, 11364-2006, and GB/T 26572-2011
- RoHS 3 directive 2015/863
- EU 2015/863

VCCI Class A Statement

この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を構ずるよう要求されることがあります。

VCCI-A

KCC Notice Class A (Republic of Korea Only)

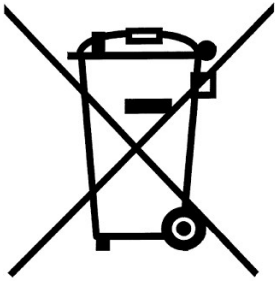
<p>A급 기기 (업무용 방송통신기기)</p> <p>CLASS A device (commercial broadcasting and communication equipment)</p>	<p>이 기기는 업무용(A급)으로 전자파적합등록을 한 기기이오니 판매자 또는 사용자는 이 점을 주의하시기 바라며, 가정외의 지역에서 사용하는 것을 목적으로 합니다.</p> <p>This device has been approved by EMC registration. Distributors or users pay attention to this point. This device is usually aimed to be used in other area except at home</p>
--	---

BSMI Class A Notice (Taiwan)

警告使用者:

此為甲類資訊技術設備，於居住環境中使用時，可能會造成射頻擾動，在此種情況下，使用者會被要求採取某些適對的對策。

EU WEEE Logo



Manufacturer Declaration European Community



Manufacturer Declaration

Xilinx declares that the equipment described in this document is in conformance with the requirements of the European Council Directive listed below:

- Low Voltage Directive 2014/35/EU
- EMC Directive 2014/30/EU

These products follow the provisions of the European Directive 2014/53/EU.

Dette produkt er i overensstemmelse med det europæiske direktiv 2014/53/EU.

Dit product is in navolging van de bepalingen van Europees Directief 2014/53/EU.

Tämä tuote noudattaa EU-direktiivin 2014/53/EU määräyksiä.

Ce produit est conforme aux exigences de la Directive Européenne 2014/53/EU.

Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2014/53/EU.

Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2014/53/EU.

Questo prodotto è conforme alla Direttiva Europea 2014/53/EU.

Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2014/53/EU.

Este produto cumpre com as normas da Diretiva Europeia 2014/53/EU.

Este producto cumple con las normas del Directivo Europeo 2014/53/EU.

Denna produkt har tillverkats i enlighet med EG-direktiv 2014/53/EU.


This declaration is based upon compliance of the Class A products listed above to the following standards:


EN 55032 (CISPR 32 Class A) RF Emissions Control.


EN 55024:2010 (CISPR 24) Immunity to Electromagnetic Disturbance.

IEC 62368-1:2014 +A11:2017 Information Technology Equipment- Safety-Part 1: General Requirements.

EN 50581:2012 - Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances.

 **CAUTION!** *In a domestic environment, Class A products may cause radio interference, in which case the user may be required to take adequate measures.*

 **ATTENTION!** *Dans un environnement domestique, les produits de Classe A peuvent causer des interférences radio, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates.*

 **VORSICHT!** *In einer häuslichen Umgebung können Produkte der Klasse A Funkstörungen verursachen. In diesem Fall muss der Benutzer möglicherweise geeignete Maßnahmen ergreifen.*

Responsible Party

Xilinx, Inc.
2100 Logic Drive, San Jose, CA 95124
United States of America
Phone: (408) 559-7778

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
04/22/2022 Version 1.4	
Table 4	<ul style="list-style-type: none"> Added 70°C requirement for I/O bracket. Updated values for use with QSFP.
Table 5	
Table 6	Added 70°C requirement for I/O bracket.
Table 7	
06/30/2021 Version 1.3	
Summary	Added information about supported configuration.
Product Details	
06/14/2021 Version 1.2	
Table 4	Updated with measured values.
Table 5	
Table 6	
Table 7	
03/17/2021 Version 1.1.1	
Figure 2	Updated image.

Section	Revision Summary
03/01/2021 Version 1.1	
Figure 1	Updated image.
Table 1	<ul style="list-style-type: none"> Updated row for DDR. Updated OS support in row for feature support.
Figure 4	Updated image.
02/23/2021 Version 1.0	
Initial release.	N/A

Please Read: Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at <https://www.xilinx.com/legal.htm#tos>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at <https://www.xilinx.com/legal.htm#tos>.

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

Copyright

© Copyright 2022 Xilinx, Inc. Xilinx, the Xilinx logo, Alveo, Artix, Kintex, Kria, Spartan, Versal, Vitis, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. AMBA, AMBA Designer, Arm, ARM1176JZ-S, CoreSight, Cortex, PrimeCell, Mali, and MPCore are trademarks of Arm Limited in the EU and other countries. PCI, PCIe, and PCI Express are trademarks of PCI-SIG and used under license. All other trademarks are the property of their respective owners.