CLK104 RF Clock Add-on Card

User Guide

UG1437 (v1.1) August 25, 2022

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Chapter 1

Introduction

Overview

The CLK104 RF clock add-on card is designed for use with Zynq® UltraScale+™ RFSoC Gen3 ZCU216 and ZCU208 evaluation boards. It provides an ultra low-noise, wideband RF clock source for the analog-to-digital and digital-to-ananlog converters (ADCs and DACs).

The clock distribution PLL provides the low frequency reference clock for integrated PLL of RFSoC devices. RFSoC devices accept one RF sampling clock for all ADC channels and one RF sampling clock for all DAC channels. ADCs and DACs have dedicated RF PLLs physically located close to them. The CLK104 supports multi-tile and multi-board synchronization.

Module Features

The CLK104 provides the following features:

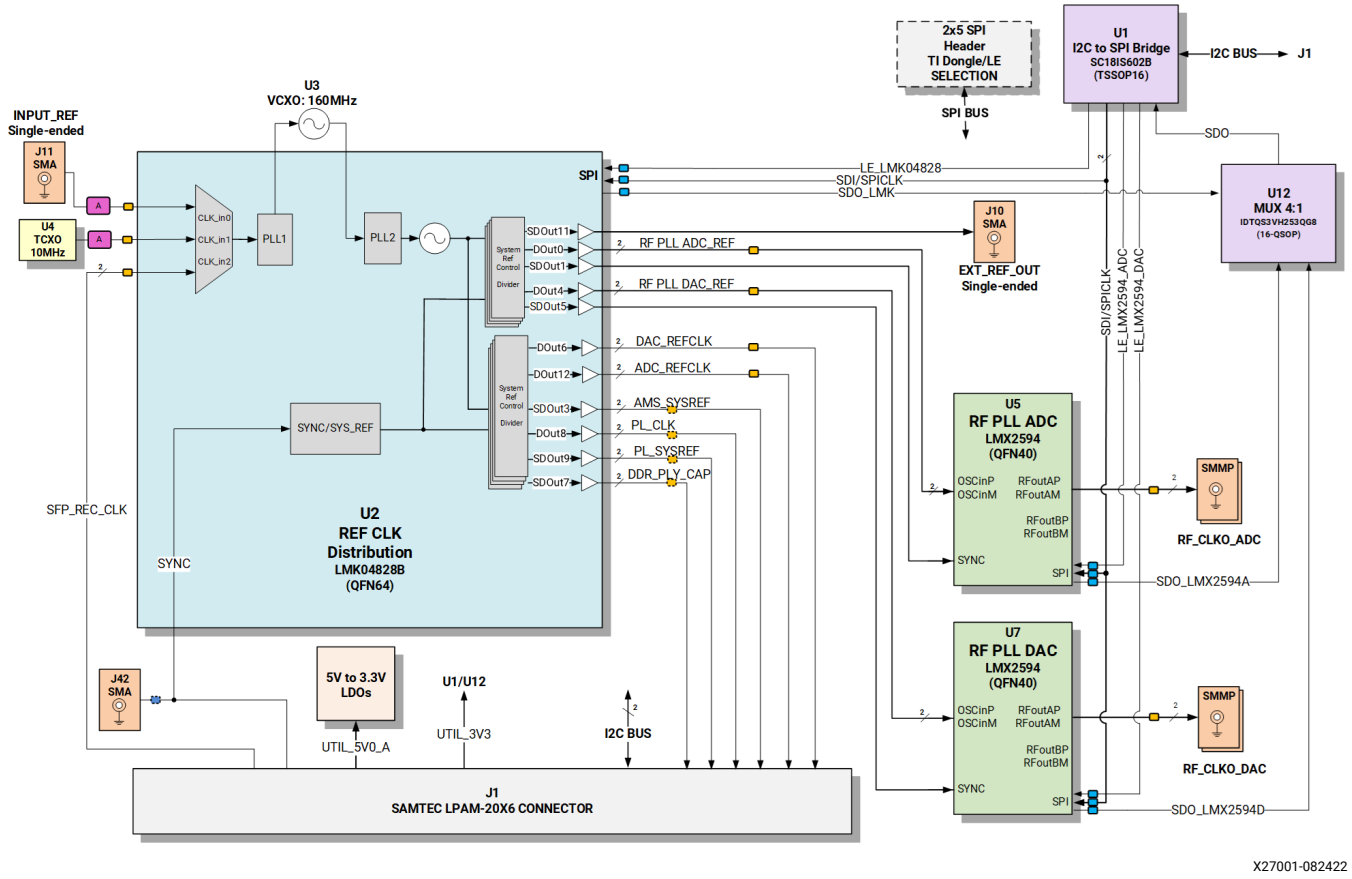
- On-module dedicated low noise LDO regulators supply 3.3V power to the GP PLL and RF PLLs.
- I2C serial interface
- TI USB2ANY interface (customized adapter/cable is required)
- LEDs indicate lock status of GP PLL and RF PLLs
- Programmable tracking on-module TCXO clock (10 MHz), or an external reference clock through SMA or a recovered clock from the PL bank
- Clock distribution PLL reference clock options
    - External reference clock
        - Single-ended clock through SMA connector
        - 3 dB attenuation
        - AC coupled

    - Free running on-module reference clock
        - 10.0 MHz TCXO
        - Manual mute option
    - Recovered clock
        - Differential clock through interface connector
        - Routed to RFSoC PL bank on evaluation board
- Clock distribution PLL output clock options
    - ADC RF PLL and DAC RF PLL differential reference clock signals (two pairs)
    - Two single-ended SYNC signals for the ADC RF PLL and DAC RF PLL
    - RFSoC ADC and DAC differential reference clock signals (two pairs)
    - SYSREF differential clock signal (one pair)
    - RFSoC differential clocks for PL banks (three pairs)
    - Single-ended external reference clock to SMA connector
- RF clock options
    - ADC RF clocks (two pairs)
        - Programmable to any frequency up to 10 GHz
        - Programmable output power level, typical > 4 dBm
        - Phase noise performance: -131 dBc/Hz at 1 MHz offset with 4 GHz carrier
    - DAC clock options (two pairs)
        - Programmable to any frequency up to 10 GHz
        - Programmable output power level, typical > 4 dBm
        - Phase noise performance: -124 dBc/Hz at 1 MHz offset with 10 GHz carrier

Block Diagram

The block diagram for the CLK104 is shown in the following figure.

Figure 1: **CLK104 RF Clock Add-on Card Block Diagram**



Module Specifications

Specifications for the CLK104 RF clock add-on card are as follows:

- Dimensions
  - Height: 2.0 inches (50.8 cm)
  - Width: 8.0 inches (203.2 cm)
  - Thickness: 0.068 inches (0.173 cm)
- Environmental
  - Temperature
    - Operating: 0°C to +45°C
    - Storage: -25°C to +60°C
  - Humidity: 10% to 90% non-condensing

Setup and Configuration

Component Location

The following figure shows the CLK104 RF clock add-on card and its components. Each numbered component referenced in the figure is described in the table and sections that follow.

CAUTION! *The CLK104 add-on card must be secured to the evaluation board with three screws before operation. The mounting holes are shown in the figure.*

IMPORTANT! *The figure is for reference only and might not reflect the current revision of the board.*

Figure 2: **CLK104 Component Locations**

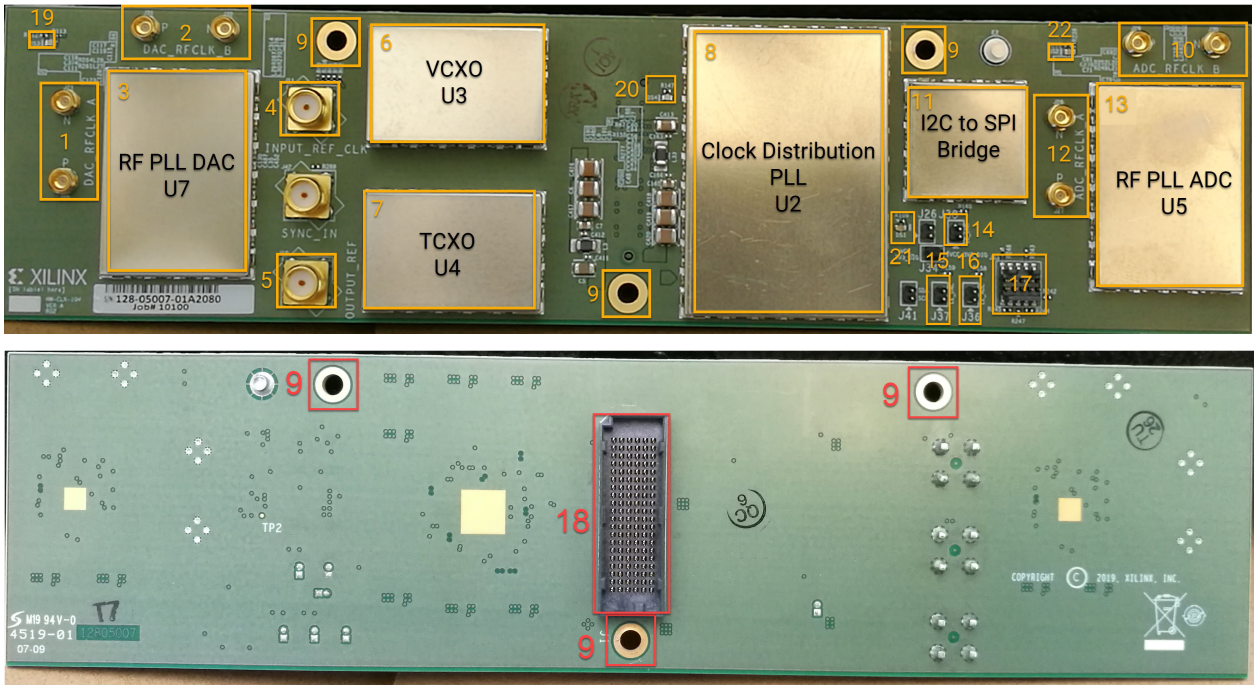


Table 1: **CLK104 Component Locations (Back)**

Callout	Reference Designation	Description
1	J20, J21	DAC_RFCLK_A, DAC RF PLL output A
2	J31, J32	DAC_RFCLK_B, DAC RF PLL output B
3	U7	RF PLL for DAC (LMX2594) with RF cage
4	J11	INPUT_REF_CLK, (U2 external reference clock)
5	J10	OUTPUT_REF (U2 output reference clock)
6	U3	VCXO 160.00MHz, VX-501-0245-160M0
7	U4	TCXO 10.0MHz, DOT050F-010.0M
8	U2	Clock distribution PLL (LMK04828B) with RF cage
9	MH1, MH2, MH3	Mounting holes
10	J29, J30	ADC_RFCLK_B, ADC RF PLL output B
11	U1, U12	I2C to SPI bridge and multiplexer
12	J27, J28	ADC_RFCLK_A, ADC RF PLL output A
13	U5	RF PLL for ADC (LMX2594) with RF cage
14	J38*	LE_LMK04828 selection, NPB02SVAN-RC
15	J37*	LE_2594_DAC selection, NPB02SVAN-RC
16	J36*	LE_2594_ADC selection, NPB02SVAN-RC
17	J33*	TI USB2ANY interface connector (customized adapter/cables required)
18	J1	Host interface connector (LPAM-20-01.0-L-06-2-K-TR)
19	DS3	U7 PLL lock LED (DAC RF PLL)
20	DS4	5.0V power supply LED
21	DS1	U2 PLL lock LED (clock distribution PLL)
22	DS2	U5 PLL lock LED (ADC RF PLL)

Note: J38, J37, J36, and J33 headers are only needed for use with the USB2ANY interface. If using I2C programming, shunts are not required.

PLL Mode Configuration

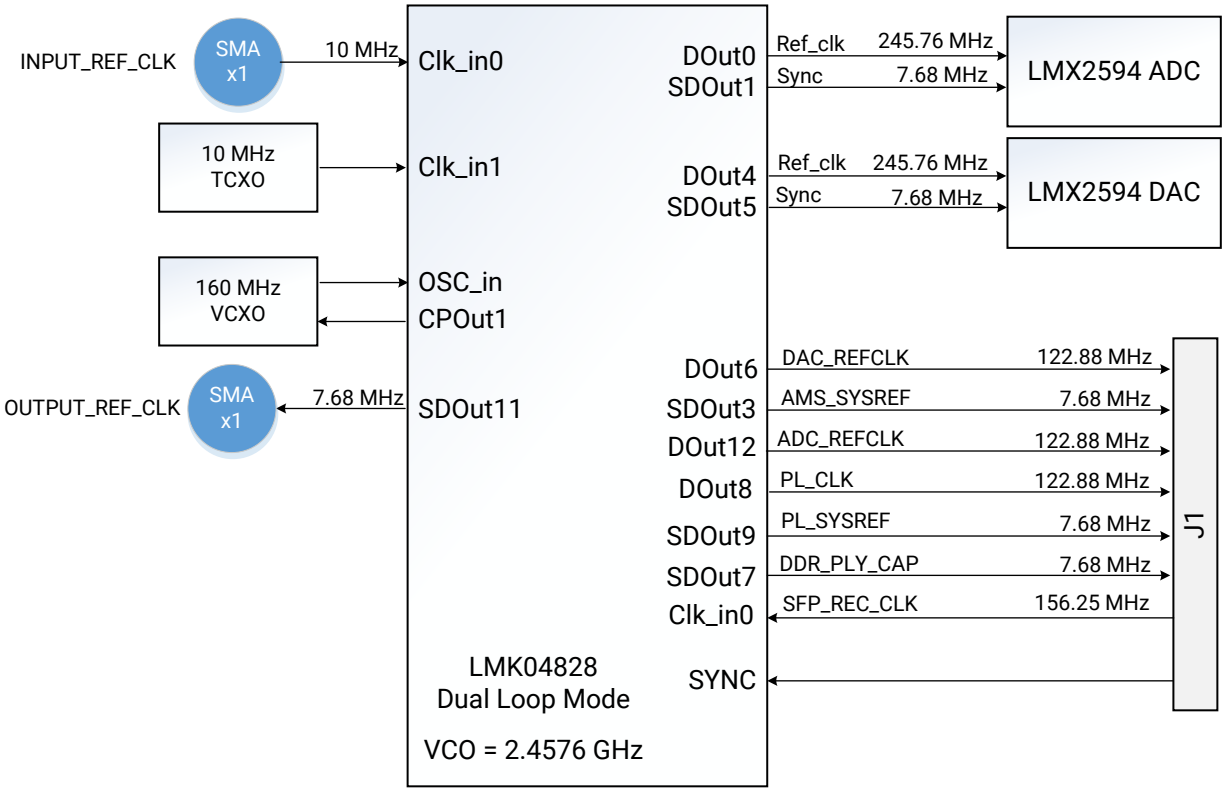
LMK04828B

LMK04828B (U2) is a dual loop jitter cleaner and clock generator. The first stage PLL (PLL1) is driven by either an external reference clock, the on-module TCXO reference clock (10.0 MHz), or the recovered reference clock from the RFSoC. An external 160.00 MHz VCXO provides a frequency-accurate, low-phase noise reference clock for the second stage PLL (PLL2). PLL2 operates with a wide-loop bandwidth and generates the input references and SYNC signal for the ADC/DAC RF PLLs (U5 and U7), the PLL reference clocks, the SYSREF signal for the RFSoC ADC/DAC, the reference clocks for the RFSoC PL banks, and the output reference clock for multi-tile and multi-board synchronization.

U2 can be configured in dual-loop mode if synchronization is not required between the outputs and reference input. If it is configured in nested 0-delay mode, either DCLKout6 or DCLKout8 needs to be selected by the feedback multiplexer, as it establishes a fixed deterministic phase relationship of the phase of PLL1 input reference to the phase of outputs. DCLKoutX can be driven from either the internal VCO or the output divider. The internal PLL2 VCO frequency range is 2,370 to 2,630 MHz and 2,920 to 3,080 MHz. Each DCLKoutX has a single clock output divider (from 2 to 32). The output of this divider can also be directed to SDCLKoutY, where Y=X +1. SDCLKoutY can be driven from either output divider or a common SYSREF divider (from 8 to 8,191).

The following figure shows an example of a typical LMK04828B configuration. Note that no external cables are required.

Figure 3: **LMK04828B (U2) Configuration Example**



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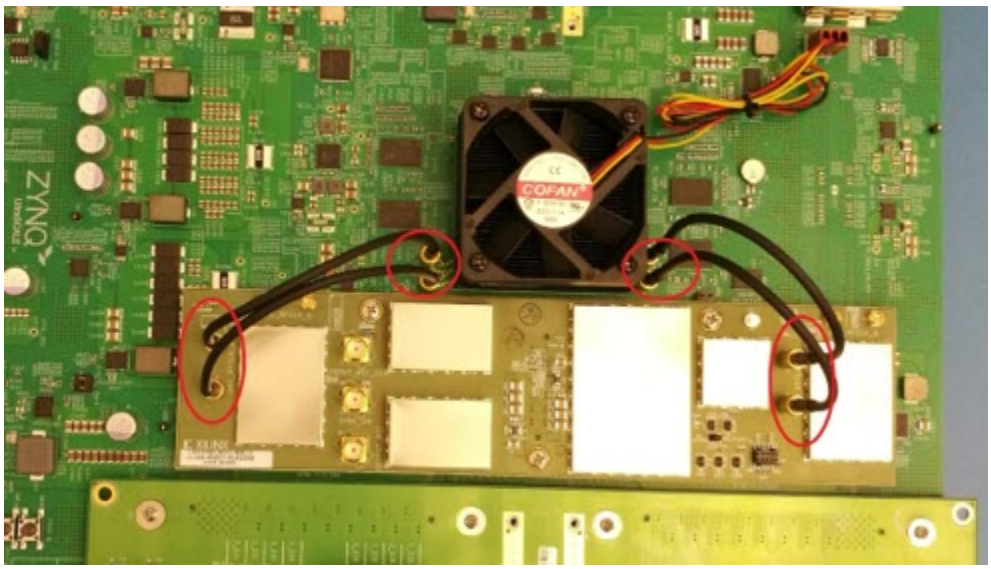
LMX2594

LMX2594 ADC (U5) and LMX2594 DAC (U7) provide dedicated RF PLLs for the RFSoC ADC RFSoC DAC. RF output port A is usually the main RF output, and uses the Carlisle SSMP loopback cable (TM40-0153) to connect it to the RF sampling clock connector on the RFSoC EVM. The following figure shows the RF clock connections between the CLK104 and the ZCU216.

Figure 4: **RF Clock Connections using SSMP Loopback Cables**



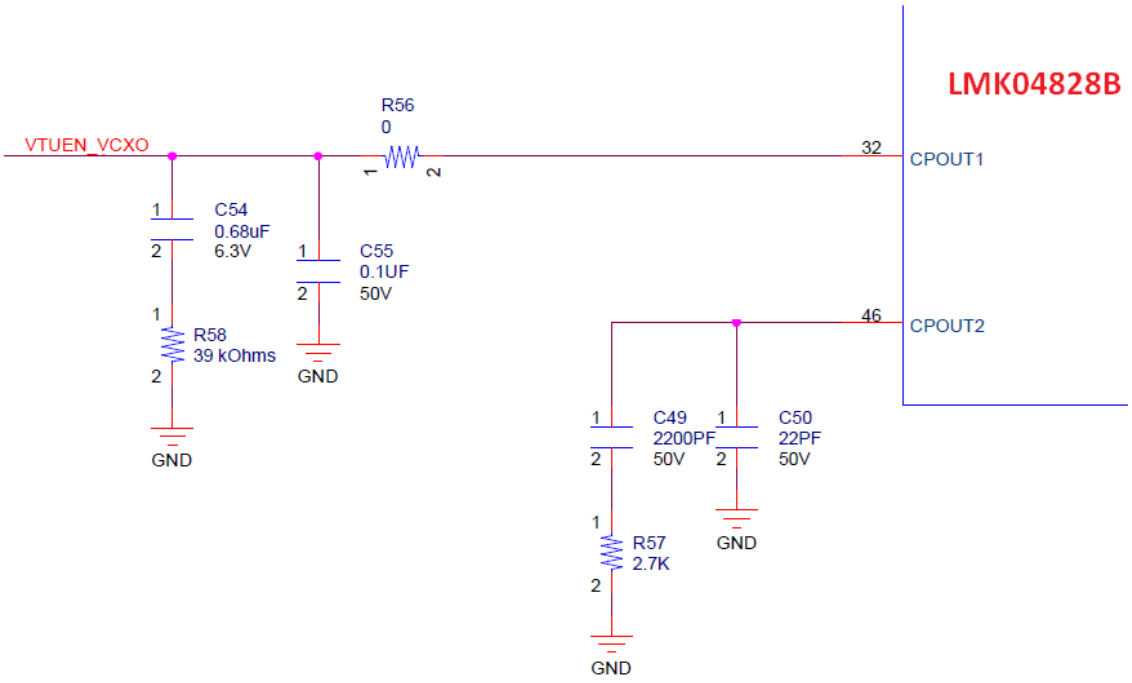
As a part of frequency planning, you need to select the proper input frequency for the LMX2594. If possible, use the integer mode as it is preferred to avoid fractional spurs. For example, for a 3.93216 GHz output, select the input frequency at 245.76 MHz. For an 8 GHz output, select the input frequency at 300.00 MHz. New configuration designs should be assessed on the spectrum analyzer before use.

PLL Loop Filters and Parameters

LMK04828B

The following figure shows the external loop filter design for LMK04828B (U2) PLL1 and PLL2.

Figure 5: **LMK04828B (U2) PLL1 and PLL2 External Loop Filter Schematic**



The following two tables identify typical U2 loop filter configurations for PLL1 in both dual-loop and nested 0-delay modes.

Table 2: **Typical U2 PLL1 Loop Filter Configuration in Dual-Loop Mode**

Parameter	Value
VCO Gain	8 KHz/V
Loop Bandwidth	29 Hz
Phase Margin	46 deg
C55 (C1_LF)	100 nF
C54 (C2_LF)	680 nF
R58 (R2_LF)	39 KΩ
Effective Charge Pump Gain	150 uA
Phase Detector Frequency (MHz)	1.25 MHz
External VCXO Frequency	160 MHz

Table 3: **Typical U2 PLL1 Loop Filter Configuration in Nested 0-Delay Mode**

Parameter	Value
VCO Gain	8 KHz/V
Loop Bandwidth	21 Hz
Phase Margin	50 deg
C55 (C1_LF)	100 nF
C54 (C2_LF)	680 nF
R58 (R2_LF)	39 KΩ
Effective Charge Pump Gain	1,050 uA
Phase Detector Frequency (MHz)	0.08 MHz
External VCXO Frequency	160 MHz

The following table identifies a typical U2 loop filter configuration for PLL2.

Table 4: **Typical U2 PLL2 Loop Filter Configuration**

Parameter	Value
VCO Gain	21 MHz/V
Loop Bandwidth	79 KHz
Phase Margin	68 deg
C50 (C1_LF)	22 pF
C49 (C2_LF)	2,200 pF
R57 (R2_LF)	2.7 KΩ
Internal Loop Filter R3	200 Ω
Internal Loop Filter C3	10 pF
Internal Loop Filter R4	200 Ω
Internal Loop Filter C4	10 pF
Effective Charge Pump Gain	3,200 uA
Phase Detector Frequency (MHz)	6.4 MHz
VCXO Frequency	2,457.6 MHz

LMX2594

The following figures show the external loop filter design for LMX2594 ADC (U5) and DAC (U7).

Figure 6: **LMX2594 ADC (U5) External Loop Filter Schematic**

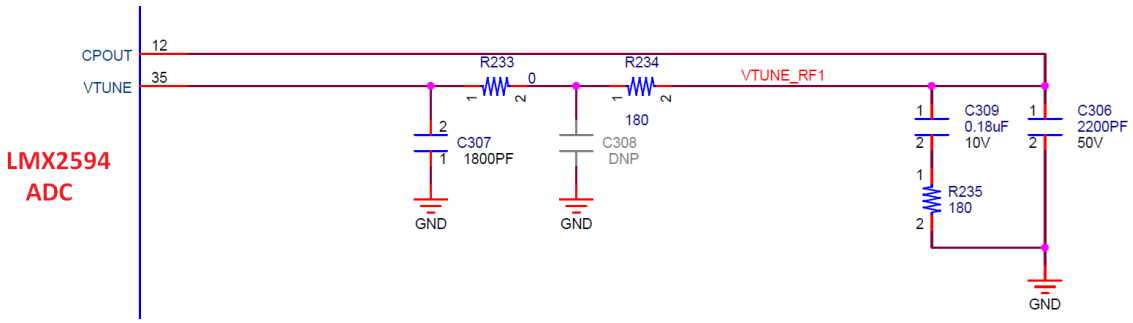
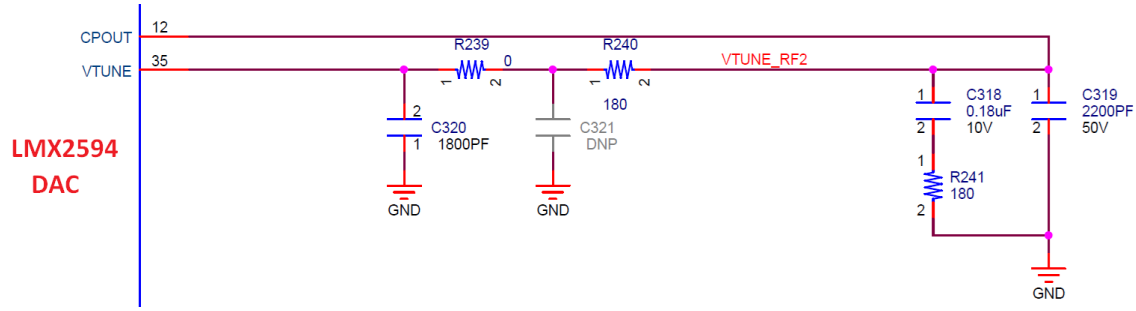


Figure 7: **LMX2594 DAC (U7) External Loop Filter Schematic**



The following table identifies a typical LMX2594 loop filter configuration.

Table 5: **Typical LMX2594 Loop Filter Configuration**

Parameter	Value
VCO Gain	239 MHz/V
Loop Bandwidth	32.7 kHz
Phase Margin	69 deg
C306, C319 (C1_LF)	2200 pF
C309, C318 (C2_LF)	180 nF
C307, C320 (R2_LF)	1800 pF
R235, R241 (R2)	180 Ω
R234, R240 (R3_LF)	180 Ω
Effective Charge Pump Gain	3 mA
Phase Detector Frequency (MHz)	24.576 MHz
VCXO Frequency	Designed for 15 GHz, but works over the whole frequency range

SAMTEC LPAM Host Interface Connector

The CLK104 RF clock add-on card mates with RFSoC evaluation boards using a low profile, 120-pin, high-speed SAMTEC LPA connector. The following figure shows the mezzanine module connector pin-out and the table that follows identifies the pins.

Figure 8: **LPA Connector Pin-out**

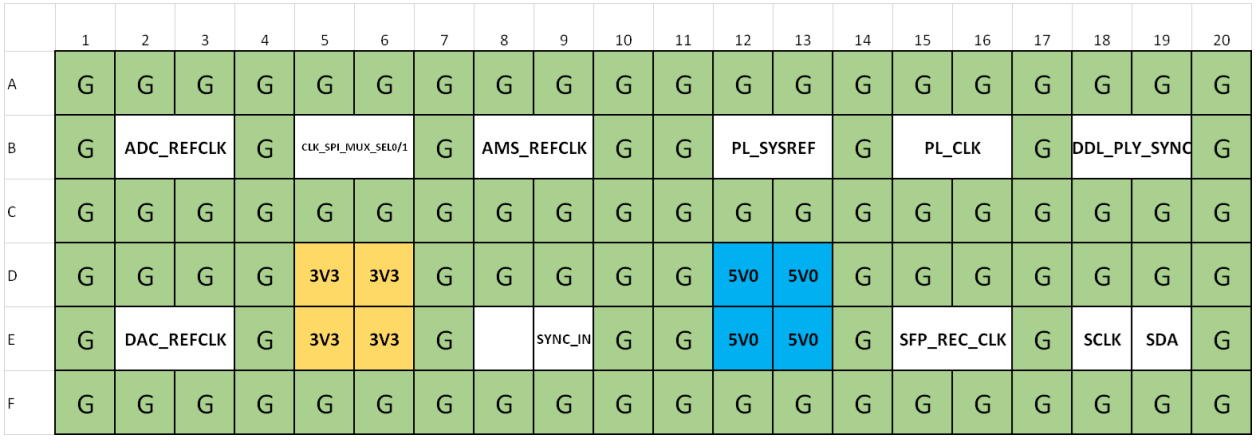


Table 6: **LPA Connector Pin Descriptions**

Pin	Signal Name	Description	LMK04828 Pin
E2	DAC_REFCLK_P	DAC REFCLK, routed to RFSoC DAC on board	DCLKout6*
E3	DAC_REFCLK_N		
B2	ADC_REFCLK_P	ADC REFCLK, routed to RFSoC ADC on board	DCLKout12*
B3	ADC_REFCLK_N		
B8	AMS_SYSREF_P	AMS SYSREF, routed to RFSoC SYSREF on board	SDCLKout3*
B9	AMS_SYSREF_N		
B15	PL_CLK_P	PL CLK, routed to PL bank on board	DCLKout8*
B16	PL_CLK_N		
B12	PL_SYSREF_P	PL_SYSREF, routed to PL bank on board	SDCLKout9*
B13	PL_SYSREF_N		
B18	DDR_PLY_CAP_SYNC_P	DDR Playback/Capture Sync, routed to PL bank on board	SDCLKout7*
B19	DDR_PLY_CAP_SYNC_N		

Table 6: **LPA Connector Pin Descriptions** *(cont'd)*

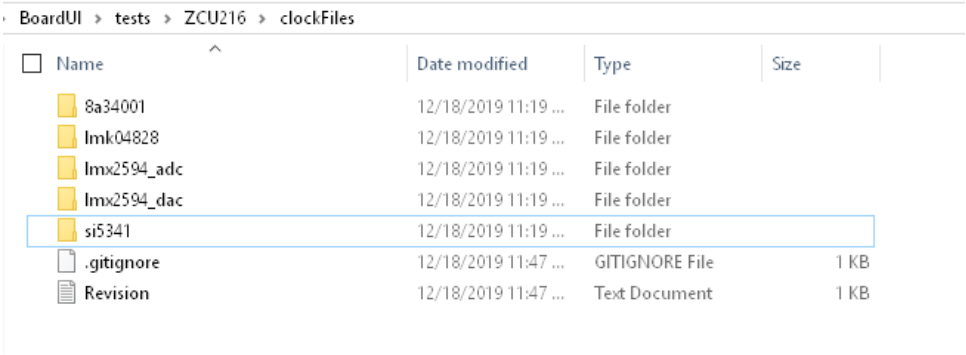
Pin	Signal Name	Description	LMK04828 Pin
E15	SFP_REC_CLK_P	Recovered clock from RFSoC PL banks	CLKin0
E16	SFP_REC_CLK_N		
E9	SYNC_IN	SYNC signal routed to PL bank on board	SYNC
E18	CLK104_SCL	I2C bus SCL	--
E19	CLK104_SDA	I2C bus SDA	--
B5	CLK_SPI_MUX_SEL0	PLL SPI MUX SEL0	--
B6	CLK_SPI_MUX_SEL1	PLL SPI MUX SEL0	--

***Note*:** The output frequency, power level, and enable/disable of each LMK04828B output are subject to change as determined by the configuration files.

CLK104 RF Clock Add-on Card Configuration with the ZCU216 SCUI

Clock Configuration Files

The PLL configuration files are included with the ZCU216 SCUI. New PLL configuration files can be added to the corresponding clock files folder before launching the SCUI as shown in the following screen capture.



The naming convention of the LMK04828B (U2) configuration files are as follows:

- Example: `LMK04828B_BxxxxMx_DualLoop_C0in10M_C1in10M_C2in156M25_DATECODE.txt`
  - `BxxxxMx`: PLL2 internal VCO frequency
  - `DualLoop` or `Nested`: LMK mode
  - `C0in_xxM`: Cin0 input reference frequency
  - `C1in_yyM`: Cin1 input reference frequency
  - `C2inzzMzz`: Cin2 input reference frequency

The naming convention of the LMK2594 ADC/DAC RF PLL (U5/U7) configuration files are as follows:

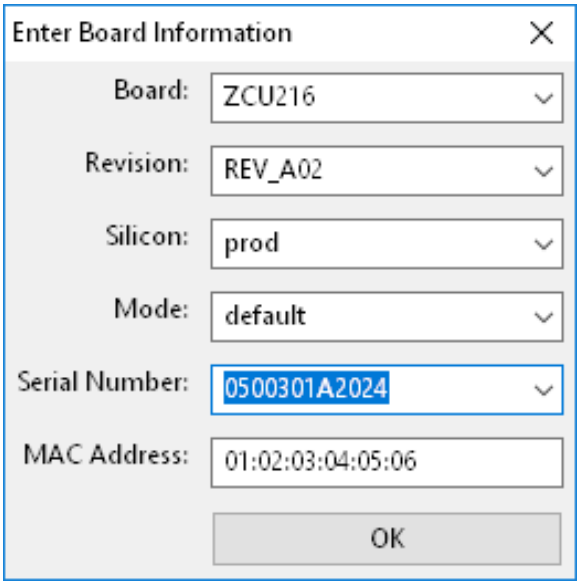
- Example: `LMX2594_REF-xxxMxx__OUT-xxxxMxx_DATECODE.txt`
  - `REF-xxxMxx`: Expected input reference frequency
  - `OUT-xxxxMxx`: RF output frequency

Note: PLL configuration files that do not follow the naming conventions do not affect the configuration content, but will result in incorrect information in the SCUI.

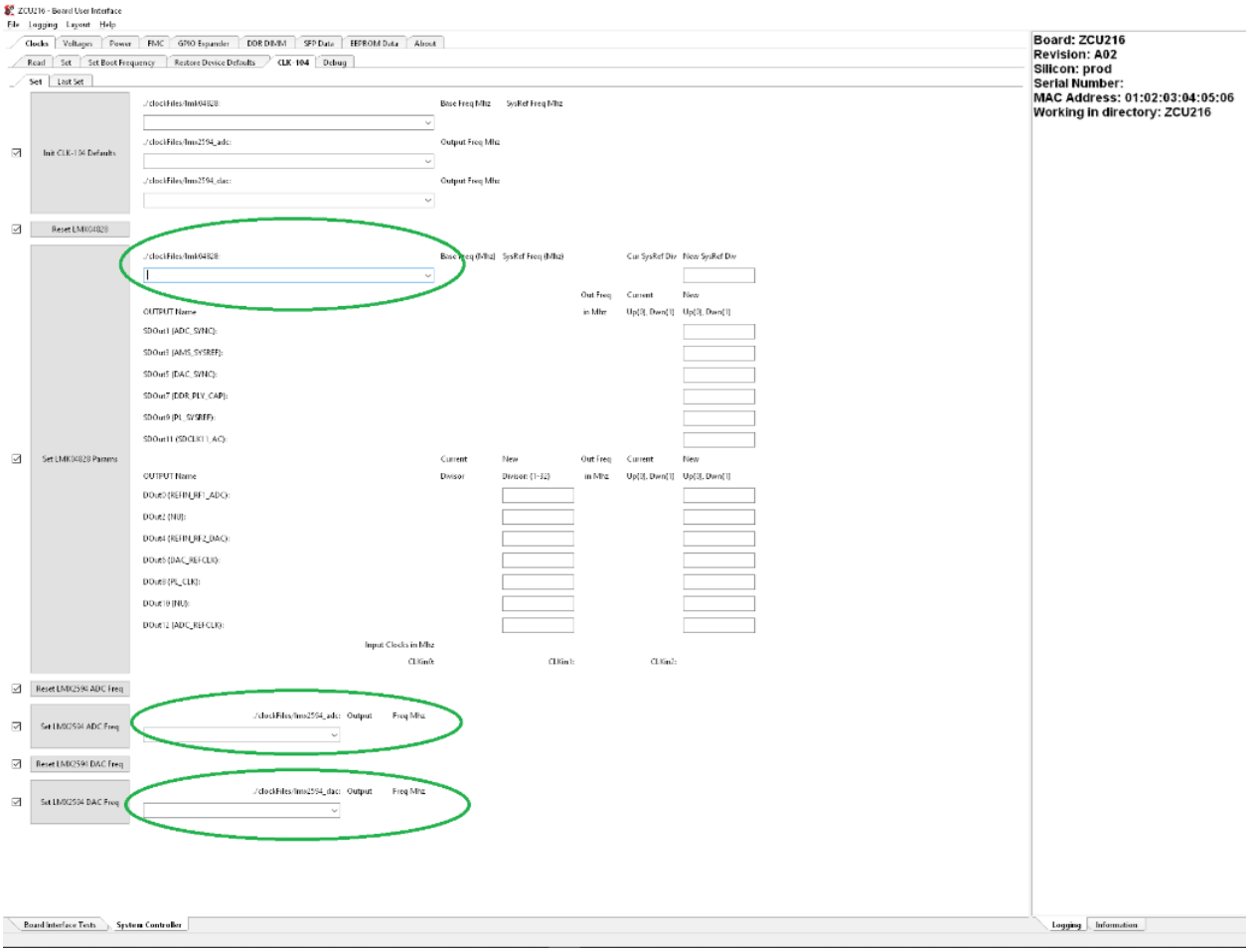
Configuring Clock PLLs

Proceed as follows to configure the clock PLLs:

1. From the \BoardUI\ working directory, double-click BoardUI.exe. The following is displayed:



2. Click **OK**.
3. Select the *System_Controller* tab, then the *Clocks* tab, followed by the *CLK-104* tab.
4. Select the expected clock file from the pull-down menu adjacent to the *Set LMK04828 Params* button. Click **Set LMK04828 Params** button and wait until the DS1 LED illuminates (green).
5. Select the expected clock file from the pull-down menu adjacent to the *Set LMX2594 ADC freq* button. Click **Set LMX2594 ADC freq** button and wait until the DS2 LED illuminates (green).
6. Select the expected clock file from the pull-down menu adjacent to the *Set LMX2594 DAC freq* button. Click **LMX2594 DAC freq** button and wait until the DS2 LED illuminates (green).


ZCU216 - Board User Interface
File Logging Layout Help
Clocks Voltages Power FMC GPIO Expander DDR DIMM SFP Data EEPROM Data About
Read Set Set Boot Frequency Restore Device Defaults CLK-104 Debug
Set Last Set
Init CLK-104 Defaults
Reset LMK04828
Set LMK04828 Params
Reset LMX2594 ADC Freq
Set LMX2594 ADC Freq
Reset LMX2594 DAC Freq
Set LMX2594 DAC Freq
Board: ZCU216
Revision: A02
Silicon: prod
Serial Number:
MAC Address: 01:02:03:04:05:06
Working in directory: ZCU216
Board Interface Tests
System Controller
Logging
Information

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Appendix C

CLK104 RF Clock Add-on Card Configuration with the ZCU216 APU

The CLK104 RF clock add-on card can be programmed and controlled by the RFCLK driver implemented in the Linux/baremetal application of the APU on the ZCU216 evaluation board. This excludes the external programming dongle. An example demonstrating how the RFCLK driver can control the CLK104 is provided in the Zynq® UltraScale+™ RFSoC RF data converter evaluation tool (see *Zynq UltraScale+ RFSoC ZCU208 and ZCU216 RF Data Converter Evaluation Tool User Guide* (UG1433)). The example code with a simple application that controls the CLK104 is available at: https://github.com/Xilinx/embeddedsw/tree/master/XilinxProcessorIPLib/drivers/board_common/src/rfclk.

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Appendix D

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

***Note*:** For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *ZCU208 Evaluation Board User Guide* (UG1410)
2. *ZCU216 Evaluation Board User Guide* (UG1390)

These websites provide supplemental material useful with this guide:

1. Texas Instruments: https://www.ti.com/
2. Carlisle Interconnect Technologies: https://www.carlisleit.com/

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
08/25/2022 Version 1.1	
Appendix C: CLK104 RF Clock Add-on Card Configuration with the ZCU216 APU	Added link to example code.
03/19/2020 Version 1.0	
Initial release.	N/A

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