Virtex-7 XT VC709 Connectivity Kit

Getting Started Guide

Vivado Design Suite 2014.3

UG966 (v4.0) December 3, 2014

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/08/2013	1.0	Initial Xilinx release.
02/22/2013	1.0.1	Changed XPN number on title page to 0402950-01.

Date	Version	Revision
06/20/2013	1.1	Revised DDR3 description in the first paragraph of the Introduction, page 15. Revised DDR3 transfer rate on page 15. Added ISE design suite to list in Requirements. Added step 6 through step 9 on page 17. Updated screen captures in Figure 2-12, Figure 2-15, and Figure 2-19. Updated links in References, page 37.
07/29/2013	2.0	Revised all references to the FPGA part number from commercial engineering sample (CES) to commercial (C). Replaced direct links in the text with indirect links referenced in Appendix A. Revised the list under Requirements, page 17 to indicate a board programmed with the BIST and TRD is required. Added note on page 17 referring to UG962 for programming instructions. Removed programming instructions from VC709 Board Setup, page 18. Added ZIP file download instructions under Driver Installation and Modes of Operation, page 22.
06/10/2014	3.0	Added SW11 dip switch to Figure 1-2. Updated VC709 Board Setup, including Figure 1-3. Updated Hardware Test Setup. Updated Run the BIST Application. Updated Figure 2-1, Figure 2-14, Figure 2-18, and Figure 2-22. Removed references to ISE software.
06/30/2014	3.0.1	Changed TRD file name to the correct name: rdf0285-vc709-connectivity-trd-2014-1.zip.
12/03/2014	4.0	Updated for the Vivado Design Suite 2014.3 release. Added device driver to Requirements in Chapter 2.

Table of Contents

Chapter 1

Introduction

Overview

The VC709 evaluation kit is based on the XC7VX690T-2FFG1761C FPGA. For additional information, see the Virtex®-7 FPGAs product table. A built-in self-test (BIST) and a Connectivity Targeted Reference Design (TRD) are provided with the VC709 evaluation kit. The BIST provides a convenient way to test many of the features of the board on power-up and upon reconfiguration. This guide describes how to run the BIST and the Connectivity TRD. For more designs targeting the VC709 board, and the most up to date information on the tutorial or documentation, visit the Virtex-7 FPGA VC709 Connectivity Kit website.

Figure 1-1 is a photograph of the VC709 evaluation kit.

Figure 1-1: **VC709 Evaluation Kit**

VC709 Evaluation Kit Contents

The VC709 evaluation kit includes:

- VC709 evaluation board featuring the XC7VX690T-2FFG1761C FPGA with cooling fan
- Vivado® Design Suite DVD and License Voucher
  - Node-locked, device-locked to the Virtex-7 690T FPGA
- Documentation
  - Getting Started Guide
- 12V AC-adapter power supply
- Four 10 Gb Ethernet SFP+ transceivers
- Fedora 16 LiveDVD (v2.0)
- Cables
  - USB-to-Mini-B cable (for UART)
  - USB-to-Micro-B cable (for JTAG)
  - Two fiber optic patch cables

Software and reference designs, demos, and documents to get started, including the BIST files (RDF0230), can be found at the Virtex-7 FPGA VC709 Connectivity Kit website.

Virtex-7 FPGA Base Platform Built-In Self-Test

The built-in self-test (BIST) of the Virtex-7 FPGA tests many of the features offered by the Virtex-7 FPGA VC709 evaluation kit. The test is an available reference design for the VC709 evaluation kit and can be programmed into the FPGA by way of JTAG.

Figure 1-2 provides an overview of the board features utilized by the BIST.

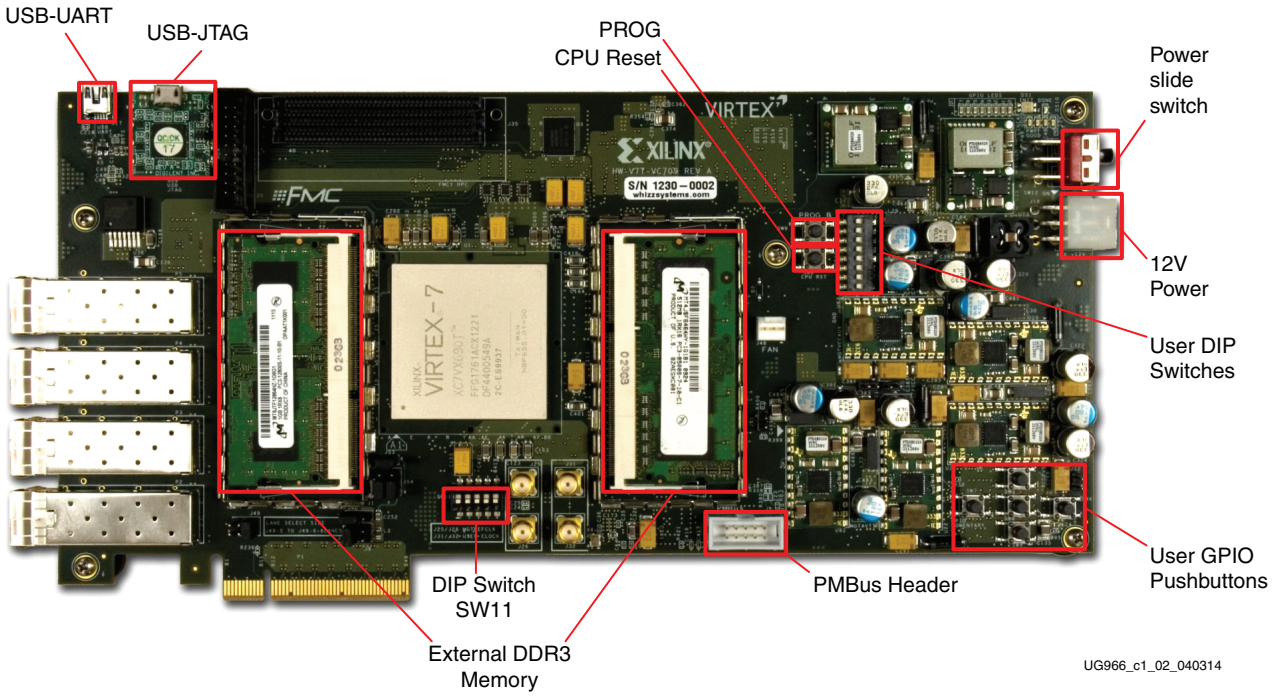

Figure 1-2: **VC709 Board Features**

Note: For a diagram of all the features on the VC709, see the *VC709 Evaluation Board for the Virtex-7 FPGA User Guide* [Ref 1].

Prerequisites

The prerequisites include:

- VC709 evaluation board with Virtex-7 FPGA
- USB-to-Mini-B cable (for UART)
- USB-to-Micro-B cable (for JTAG)
- 12V AC power adapter
- Tera Term Pro (terminal emulation program)
- Silicon Labs USB-UART driver
- A PC and display monitor (not included with kit)

Hardware Setup

This section details the hardware setup and use of the terminal program for running the BIST application. Also included are step-by-step instructions for board bring-up.

VC709 Board Setup

Set SW11, the configuration mode and flash address switch as shown in Figure 1-3 to set up the VC709 evaluation board.

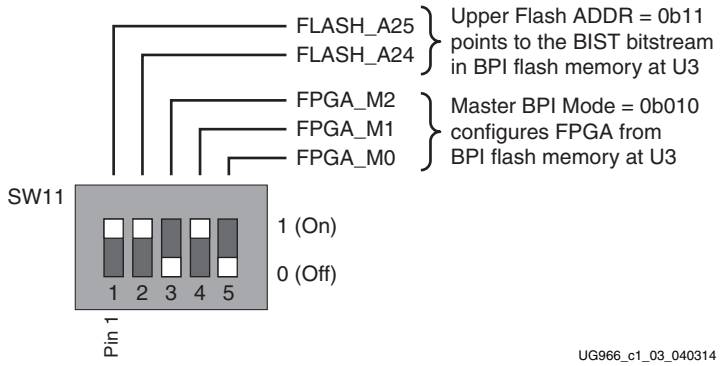

Figure 1-3: **SW11 BIST Settings**

Note: For this application, set the board up as a standalone system powered with the AC power adapter provided with the VC709 evaluation kit.

Hardware Bring-Up

Figure 1-2 is a photograph of the setup for the VC709 board.

To prepare the VC709 board for hardware bring-up:

1. With the VC709 board switched off, connect a USB-to-Mini-B cable to the UART port of the VC709 board and to the host PC (USB-UART in Figure 1-2).
2. Connect the 12V_AC adapter cable to the VC709 board (12V Power in Figure 1-2).
3. Connect the Digilent JTAG cable to the VC709 board (USB-JTAG in Figure 1-2).
4. Switch on the power to the VC709 board.

Install Silicon Labs UART Device Driver

The UART device driver is required for UART-USB communications with the host computer.

Note: The steps described here refer to a host PC running Windows XP or Windows 7.

To install the UART device driver and set the COM port:

1. Download and run the executable file for the Silicon Labs UART-USB driver.

Figure 1-4 shows the Silicon Labs InstallShield Wizard.

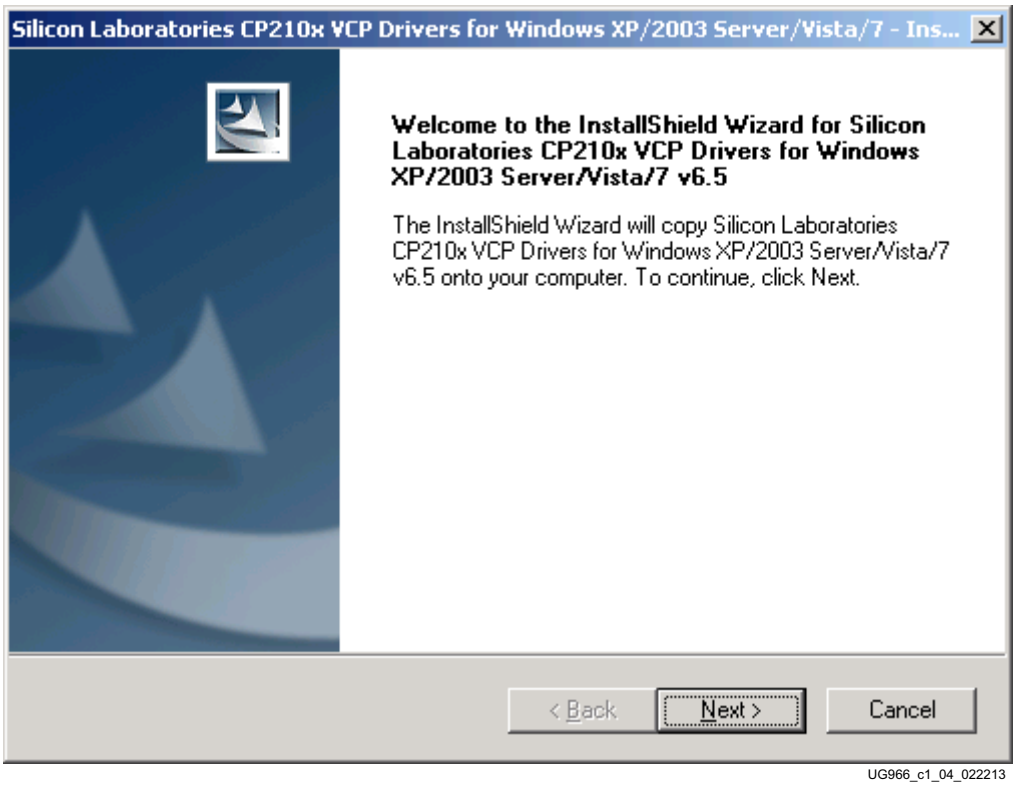

Figure 1-4: **Silicon Labs UART Installation Window**

2. On the host PC, right-click on **My Computer** and select **Properties**.
3. Click the **Hardware** tab.
4. Click the **Device Manager** button.

5. Locate the Silicon Labs device, right-click on it and select **Properties** (see Figure 1-5).

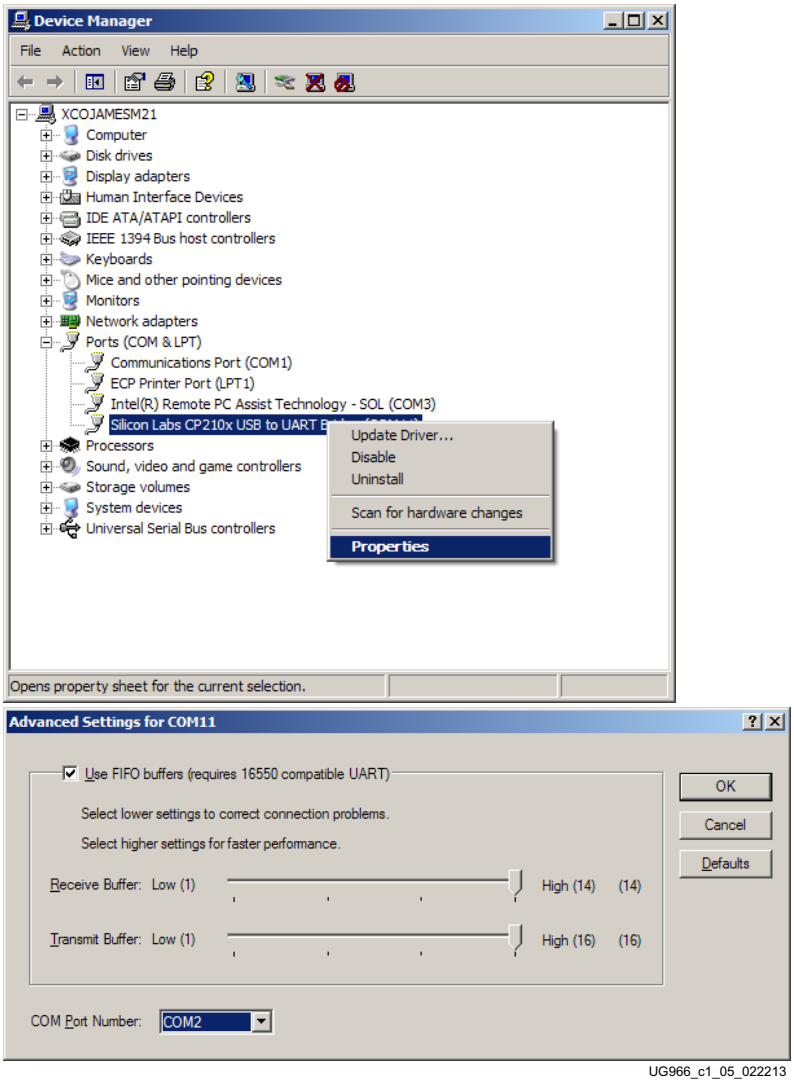

Figure 1-5: **Screenshots of Device Manager Window**

6. Click the **Port Settings** tab.
7. Click the **Advanced** button.
8. Select an open COM port between COM1 and COM4.
9. Click **OK**.
10. Under **Setup > Serial Port . . .** ensure that the settings match Figure 1-6:
    - **Port**: COM2 (the COM port set in the Install Silicon Labs UART Device Driver, page 11 section)
    - **Baud Rate**: 9600
    - **Data**: 8-bit
    - **Parity**: none
    - **Stop**: 1-bit
    - **Flow control**: None

Figure 1-6 shows the serial port setup window.

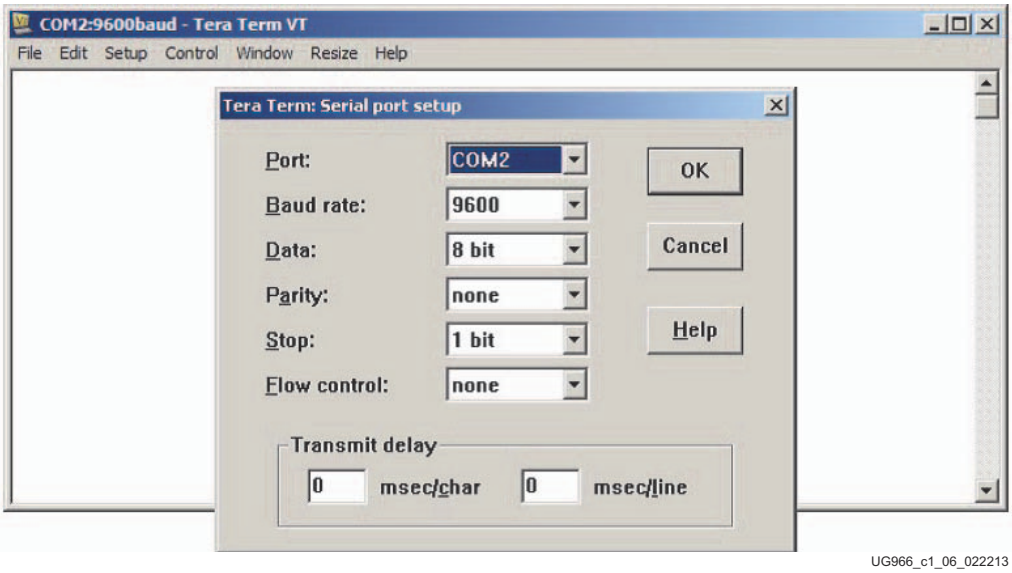

Figure 1-6: **Serial Port Setup Window**

Run the BIST Application

To run the BIST application:

1. Complete the tasks in Hardware Setup, page 10.
2. Switch on the power to the VC709 board.
3. Set DIP switch SW11 as shown in Figure 1-3, page 10.
4. Press and release the PROG button SW9 (Figure 1-2, page 9). The BIST bitstream configures the FPGA and then runs BIST. The terminal program displays the BIST menu shown in Figure 1-7.

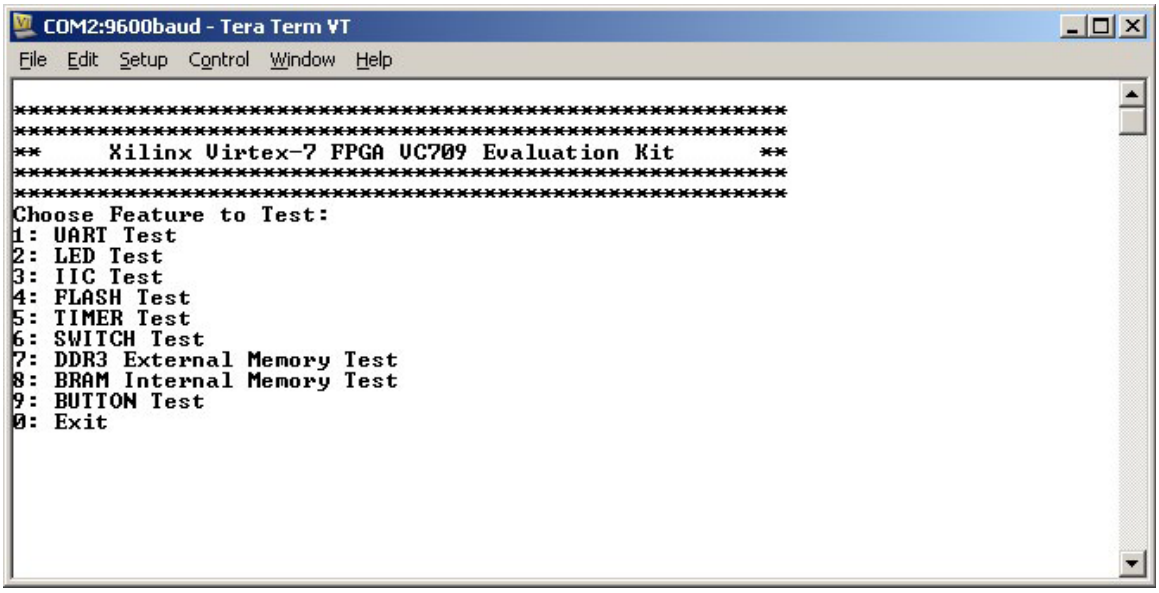

Figure 1-7: **BIST Main Menu**

5. Select the desired tests to run (see Figure 1-7) and observe the results.

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard nonvolatile storage, see the Virtex-7 FPGA VC709 Connectivity Kit website.

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Chapter 2

Connectivity System Setup with Targeted Reference Design

Introduction

The Virtex®-7 XT Targeted Reference Design (TRD) targets a VC709 evaluation board containing a Xilinx XC7VX690T-2FFG1761C device (see Figure 2-1). The intent of this design is to demonstrate a high performance data transfer system using x8 PCIe® Gen3 endpoint with a high performance scatter gather DMA. Two DDR3 SODIMM memories are used as a packet buffer. Data is transferred over Quad 10G BASE-R links.

The TRD demonstrates high speed data transfers between the host system memory and the FPGA card. The software driver (the data source) generates packets in the user space for the performance demonstration and also connects to the TCP/IP stack for the networking application demonstration.

Features of the TRD include:

- PCIe Gen3 Endpoint operating at 8 Gb/s, per lane, per direction
  - PCIe transaction interface utilization engine
  - MSI and Legacy interrupt support
- Bus mastering Scatter-gather DMA
  - Multichannel DMA
  - AXI4 streaming interface for data
  - AXI4 interface for register space access
  - DMA performance engine
  - Full duplex operation
  - Independent transmit and receive channels
- Two 64-bit wide DDR3 SODIMMs
  - Use of AXI stream interconnect and AXI Virtual FIFO controller IP to make DDR3 a packet FIFO
- 10 Gigabit Ethernet MAC with 10GBASE-R PHY
  - Address filtering
  - Inter-frame gap control
  - Jumbo frame support up to 16,383 bytes
  - Ethernet statistics engine
  - Management interface for physical interface configuration (MDIO)

- PicoBlaze™ processor-based PVT monitoring
  - Engine in hardware to monitor power consumption by reading the TI UCD9248 Power controller devices on the VC709 board
  - Engine in hardware to monitor die temperature and voltage rails using Xilinx Analog-to-Digital Converter (XADC)

PicoBlaze processor-based I2C programming of SI5324 clock multiplier or a jitter attenuator device on the VC709 board

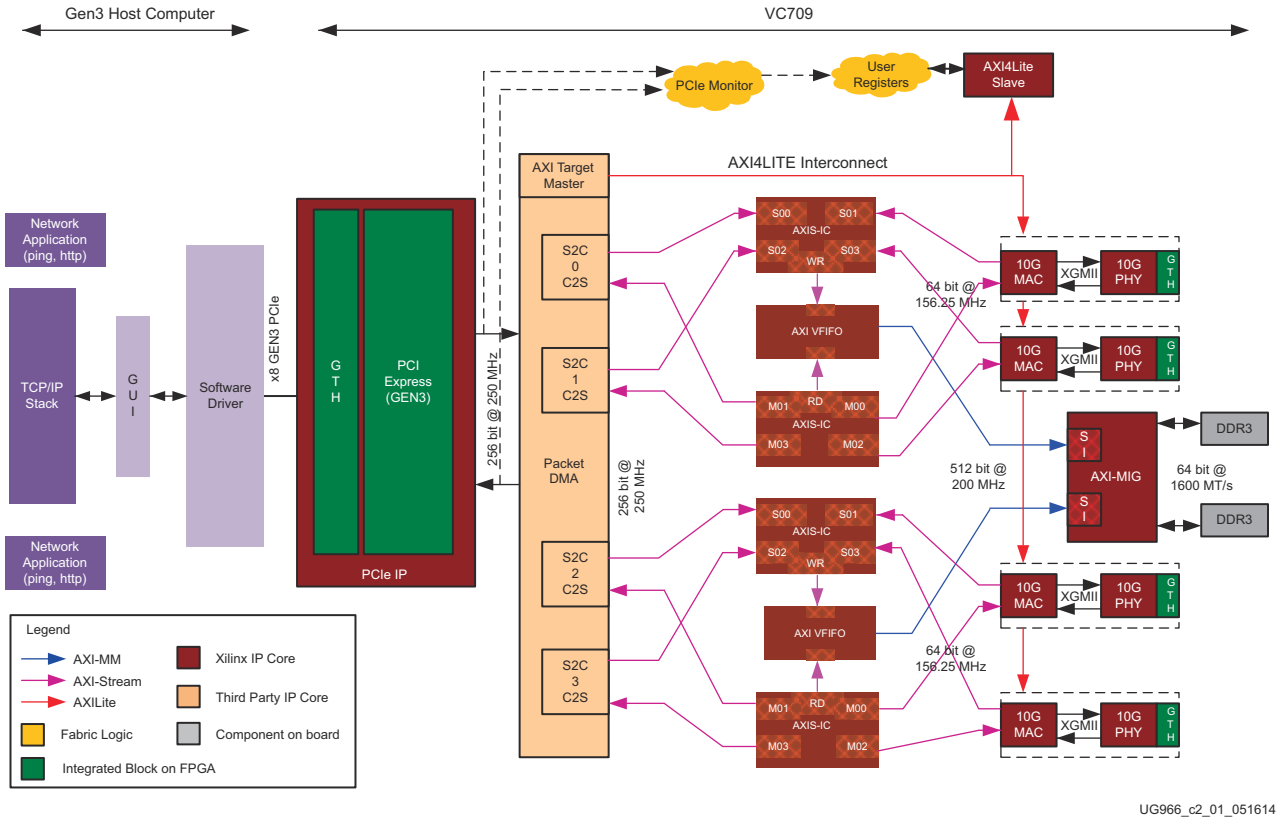

Figure 2-1: **Virtex-7 XT TRD Block Diagram**

Requirements

A host PC with a PCIe v3.0 slot and a monitor is required for testing the VC709 evaluation kit TRD.

Requirements for testing the design in hardware include:

- VC709 evaluation board with XC7VX690T-2FFG1761C FPGA programmed with the XT Connectivity TRD.

  Note: The VC709 evaluation board is delivered pre-programmed with the XT Connectivity TRD and a BIST. Programming instructions for the XT Connectivity TRD are provided in the *Virtex-7 FPGA XT Connectivity Targeted Reference Design for the VC709 Board User Guide* [Ref 2].
- Vivado® Design Suite: Design Edition
- USB cable, standard-A plug to micro-B plug
- Four Avago SFP+ connector modules with two fiber optic cables
- ATX power supply adapter cable (4-pin to 6-pin adapter)
- Fedora 16 LiveDVD
- Device driver files from `rdf0285-vc709-connectivity-trd-2014-3.zip`
- USB Memory device for transferring TRD drivers and GUI files to PCIe host PC (not included in kit)

Note: Due to the presence of four SFP+ cages on the side of VC709 evaluation board, a full-sized chassis is needed to test the TRD in its entirety because a rack-sized chassis makes two of the four SFP+ cages inaccessible.

For a list of all known issues, refer to the Virtex-7 XT Connectivity TRD release notes and the Known Issues and Release Notes Master Answer Record. The same information is available in the `readme.txt` file included with the design files.

Hardware Test Setup

This section describes hardware bring-up, software bring-up, and use of the application GUI.

All procedures listed in the following sections require Linux super user permissions for access. When using Fedora 16 LiveDVD provided with the kit, super user access is granted by default due to the way the kernel image is built. If not using LiveCD, contact your system administrator for super user access.

These instructions assume that the VC709 board has the TRD pre-programmed into the flash. If using a board that does not have the TRD pre-programmed, see the Programming the VC709 Board section in *Virtex-7 FPGA XT Connectivity Targeted Reference Design for the VC709 Board User Guide* [Ref 2] to program the flash before continuing.

See Driver Installation and Modes of Operation for information on how to download the TRD zip file.

VC709 Board Setup

To set up the VC709 evaluation board:

1. Turn off the host computer.
2. Insert the VC709 board into a PCIe slot.
3. Insert SFP+ connectors into the SFP+ cage positions as shown in Figure 2-2.

Note: The cage connector P2 is connected to P3 and P4 to P5 (cage P2 is the bottom one nearer to PCIe finger) to provide loopback capability. The photos in Figure 2-2 show the board outside of the PC chassis for clarity.

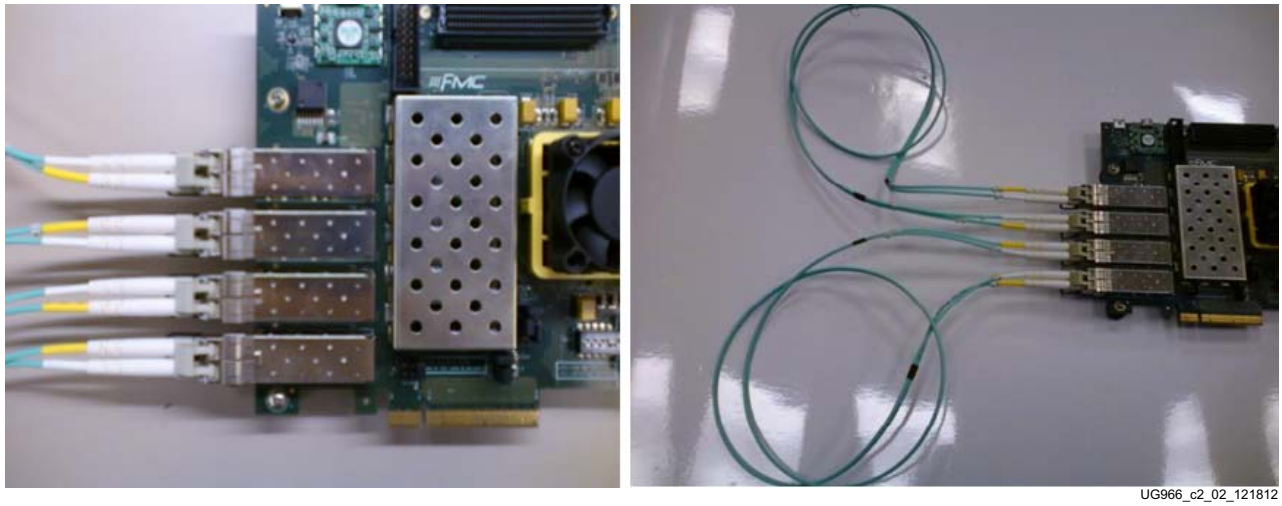

Figure 2-2: **SFP+ Connector Locations on VC709 Board (Left) and Cables Showing Loopback Configuration (Right)**

Figure 2-3 shows the setup with fiber optic cables installed in the PC chassis.

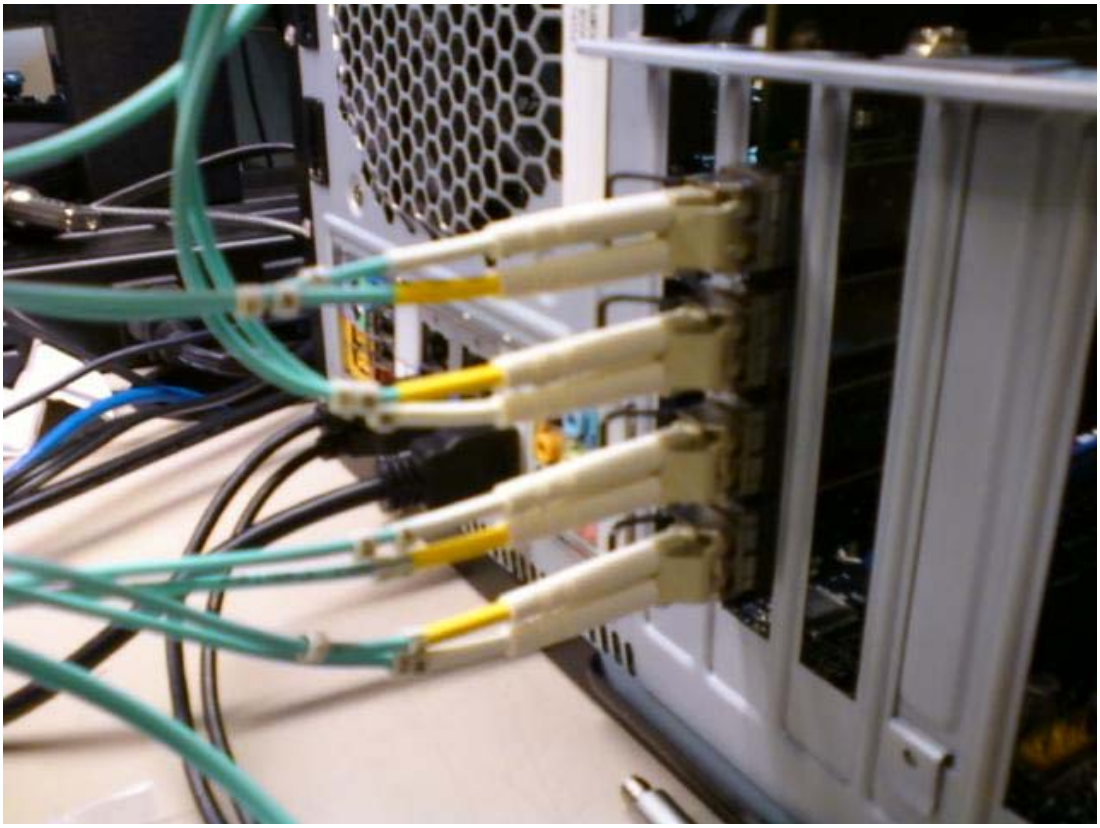

Figure 2-3: **Setup with Fiber Optic Cable Installed in PC Chassis**

4. Connect the 12V ATX power supply adapter cable (6-pin side) to the board at connector J18, and the other side (4-pin) to the ATX power supply. Cable is shown in Figure 2-4.

Figure 2-4: **12V ATX Power Supply Adapter Cable**

5. Ensure the connections are secure.

Note: The ATX Power Supply Adapter Cable is needed because the 4-pin ATX supply cannot be connected directly to the VC709 board.

6. On SW11, set the mode pins and the BPI upper address pins to configure the FPGA (see the settings in Figure 2-5). A25 and A24 are to 00 and the mode pins are set to 010.

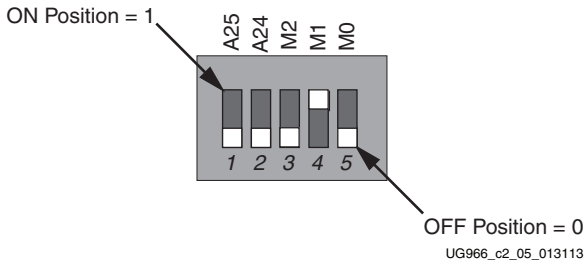

Figure 2-5: **SW11 Switch Settings for Mode Pins and BPI Upper Addresses**

7. Power on the system.

The LED indicators on the VC709 board provide the indications listed in Table 2-1. LED positions are marked on the board starting from 7 on the left to 0 on the right.

Table 2-1: **LED Indicators on VC709 Evaluation Board**

LED	Description	Proper Behavior	If Something Wrong
0	PCIe link up	On (after a few seconds)	Off after BIOS loads (no link)
1	PCIe 250 MHz clock heart beat	Blinks slowly	Off (no clock)
2	PCIe linked at x8	On	Blinking fast (not x8)
3	PCIe linked at Gen3	On	Blinking fast (not Gen3)
4	Ethernet 156.25 clock heart beats	Blinks slowly	Off (no clock)
5	10GBASE-R links ready (for all four links)	On	Off (one or more links down)
6	DDR3 calibration done (both SODIMMs)	On	Off (calibration failed on at least one SODIMM)
7	unused		

LED positions are shown in Figure 2-6. If the LEDs are not exhibiting the proper behavior, refer to the Virtex-7 XT Connectivity TRD release notes and the Known Issues and Release Notes Master Answer Record.

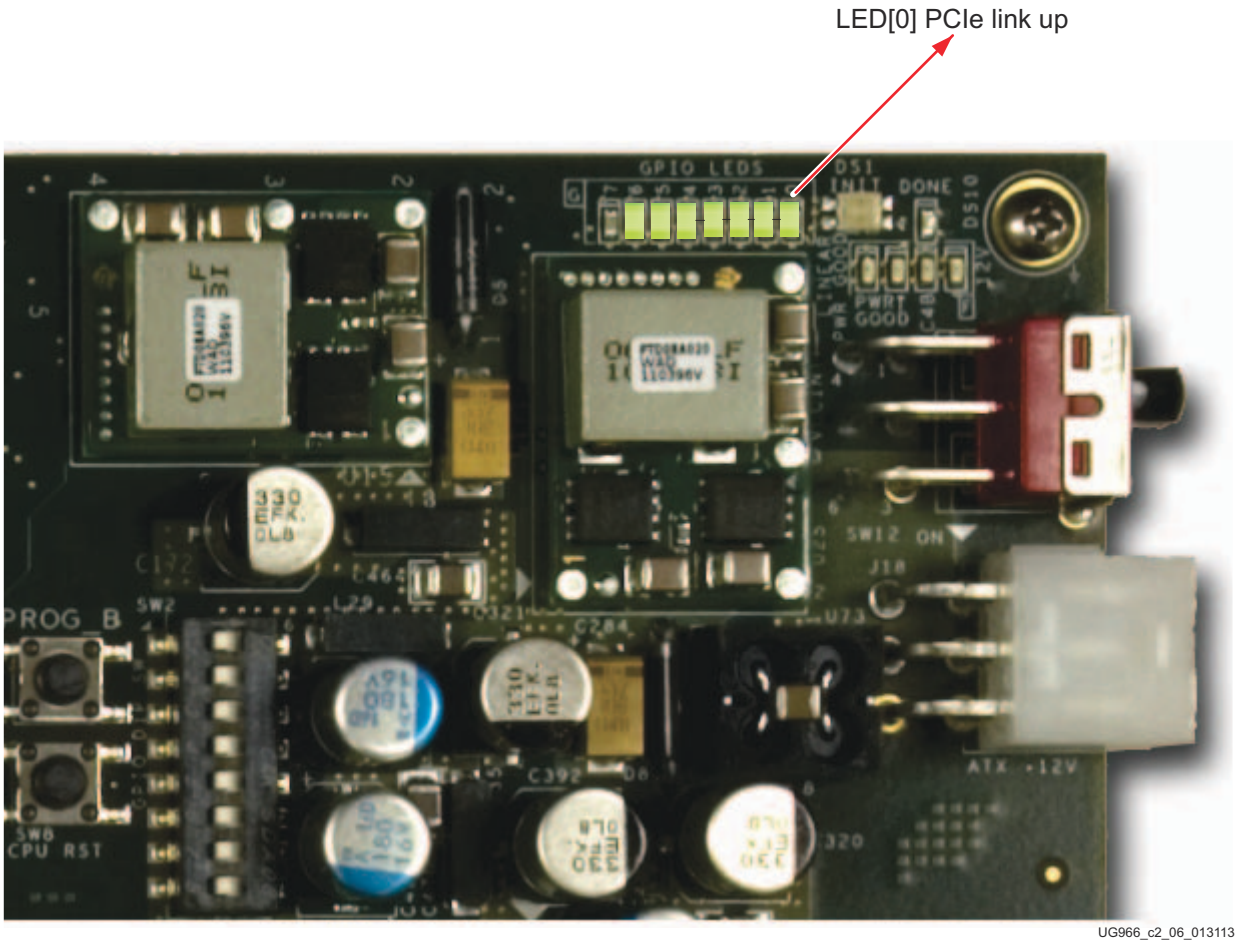

Figure 2-6: **LED Positions on the VC709 Evaluation Board**

Driver Installation and Modes of Operation

The following steps describe the installation of the device drivers for the Virtex-7 XT Connectivity TRD after the hardware is set up. The steps that follow demonstrate all modes of test operation by installing and uninstalling various drivers.

Note: If Fedora 16 is currently installed on the hard drive of the host PC, reboot the PC as a user with root privileges. After reboot, proceed to step 2.

1. Place the Fedora 16 LiveDVD in the CD-ROM drive of the host PC. The PC should boot automatically from the CD-ROM drive.

   The Fedora 16 LiveDVD Media is for Intel-compatible PCs. The DVD contains a complete, bootable 32-bit Fedora 16 environment with the proper packages installed for the TRD demonstration environment. The PC boots from the CD-ROM drive and logs into a live user account. This account has kernel development root privileges required to install and remove device driver modules.

   Note: Users might have to adjust BIOS boot order settings to ensure that the CD-ROM drive is the first drive in the boot order. To enter the BIOS menu to set the boot order, press the Delete or F2 key when the system is powered on. Set the boot order and save the changes.

   The screen images shown in Figure 2-7 are displayed on the monitor during boot-up.

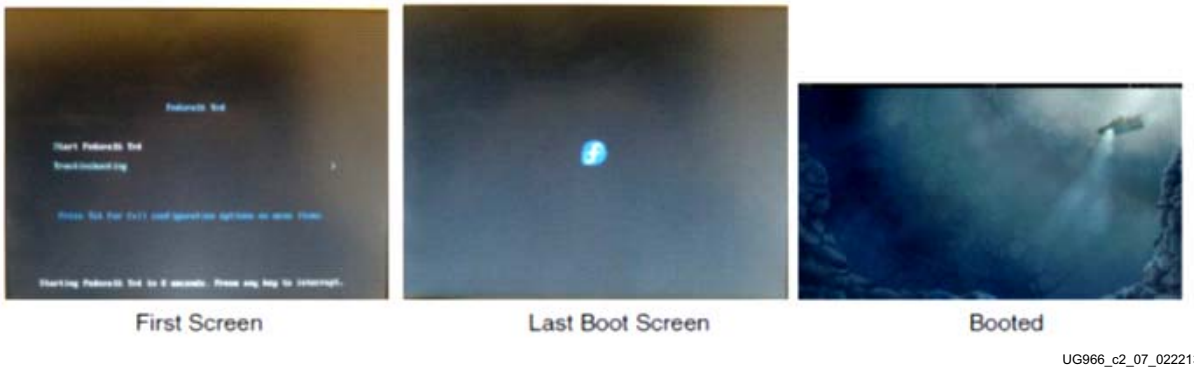

Figure 2-7: **Screen Images of Fedora 16 LiveDVD Boot Sequence**

2. Browse to the Virtex-7 FPGA VC709 Connectivity Kit website.
3. Under the **Documentation** heading, expand by clicking **Virtex-7 FPGA VC709 Connectivity Kit – (<Software Version>)** where **Software Version** equals the appropriate design suite software version.
4. Under the **By Document Type** heading, click **Targeted Reference Designs**.
5. Click **Virtex-7 FPGA VC709 Connectivity Kit Targeted Reference Design** and save `rdf0285-vc709-connectivity-trd-2014-3.zip` to a working directory on the host computer.

6. Use a USB Flash memory to copy `v7_xt_conn_trd.tar.gz` from the `rdf0285-vc709-connectivity-trd-2014-3.zip` to the `Home` directory on the host computer (Figure 2-8).

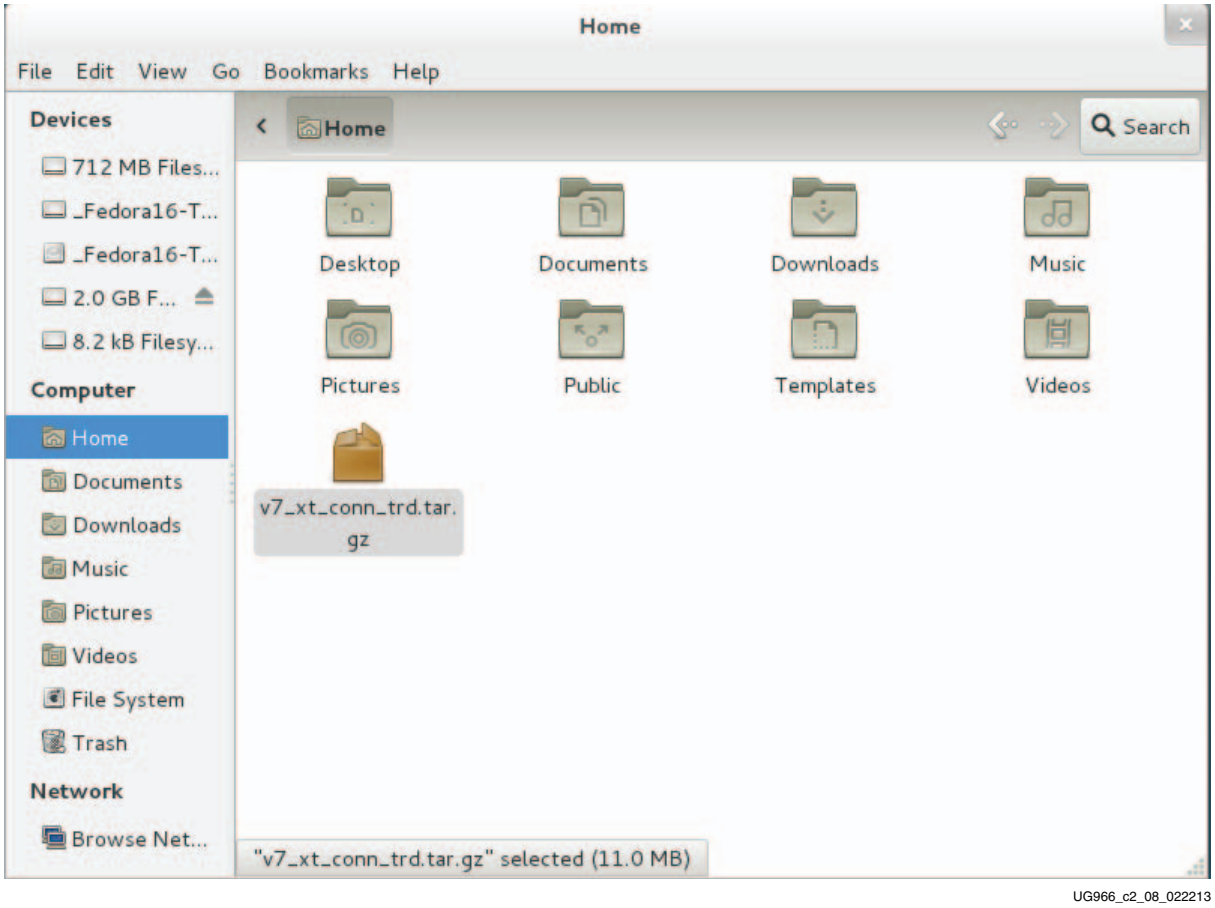

Figure 2-8: **TAR File in Home Directory**

7. Right-click `v7_xt_conn_trd.tar.gz` and select **Extract Here**. Double-click the **`v7_xt_conn_trd`** folder. Figure 2-9 shows the contents of the `v7_xt_conn_trd` folder.

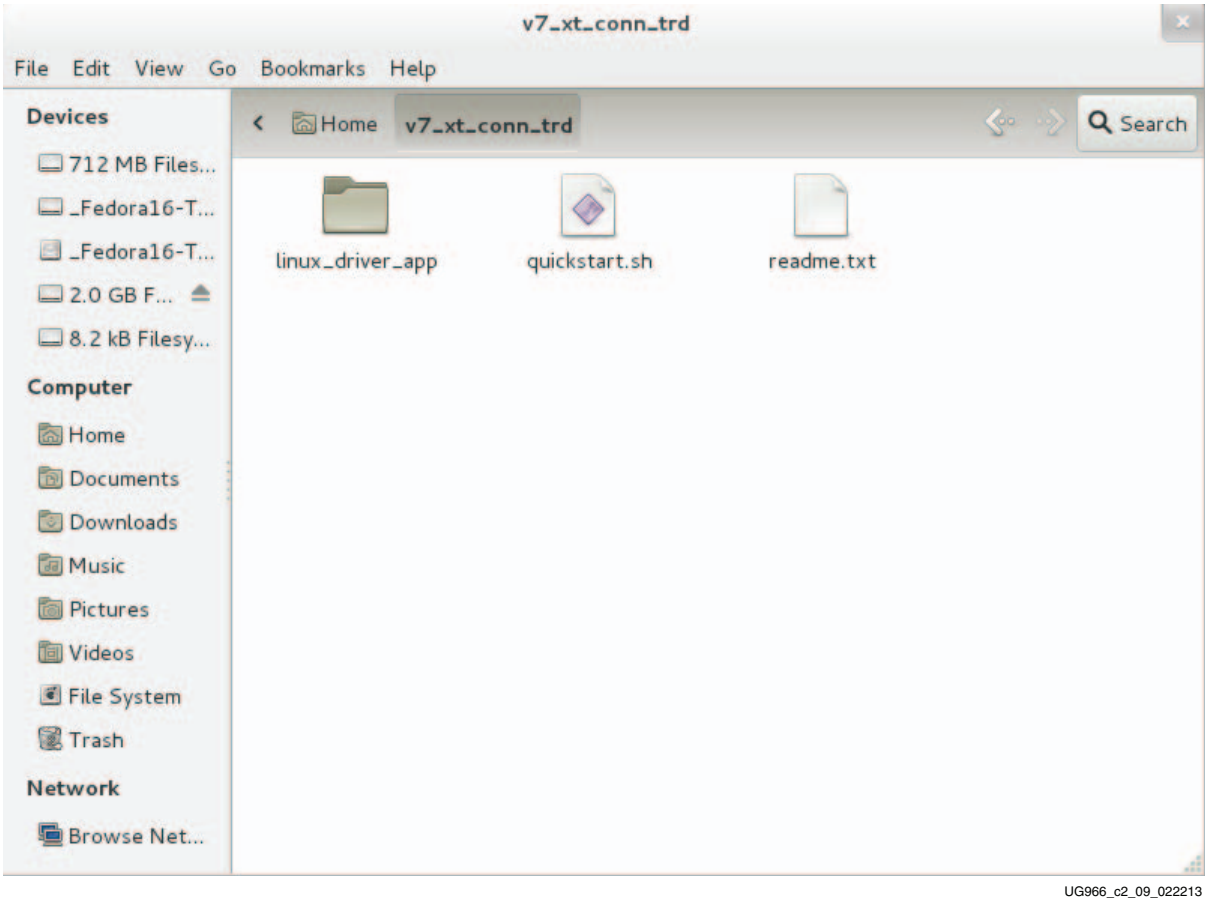

Figure 2-9: **Contents of v7_xt_conn_trd Folder**

8. Double-click the `quickstart.sh` file. This script sets the proper permissions and a pop-up window is displayed to control the running of the script (see Figure 2-10).

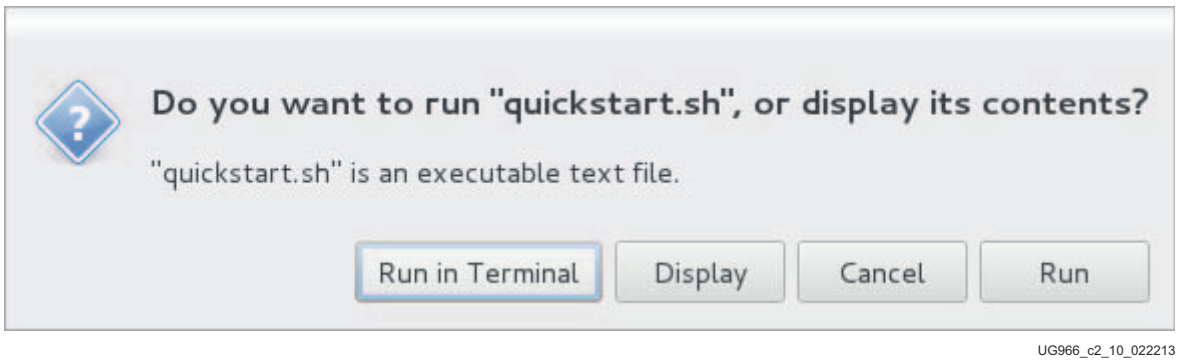

Figure 2-10: **Running QuickStart Script**

9. Click **Run in Terminal**. The TRD Setup window is displayed as shown in Figure 2-11.

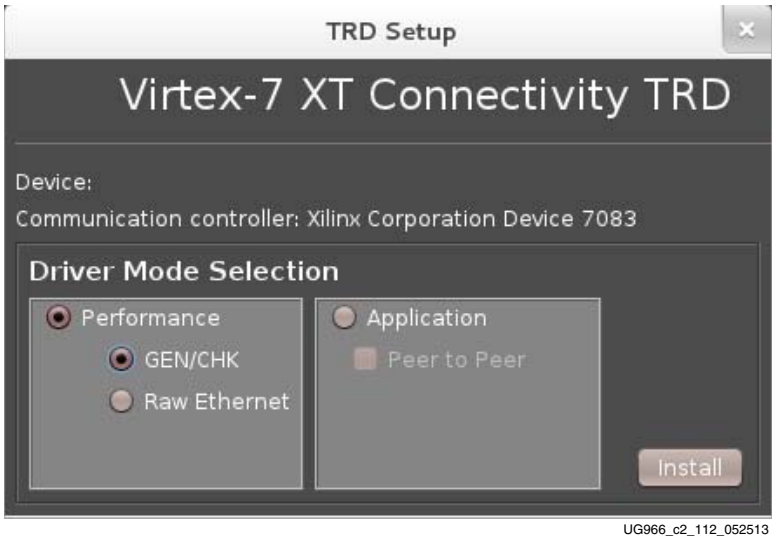

Figure 2-11: **TRD Setup**

As described in the following sections, this window is used to install the drivers for testing the different modes of operation. Hovering the mouse pointer over the choices brings up a short description. The available tests are:

- **GEN/CHK**—Selects PCIe-DMA driver with Generator and Checker in hardware or Loopback for maximum PCIe-DMA performance
- **Raw Ethernet**—Selects the Raw Ethernet drivers exercising the Quad 10G links in hardware for maximum Ethernet performance
- **Application**—Selects the Application mode drivers that connect to the networking (TCP/IP) stack for demonstrating a real networking application.

These modes are further explained in the following sections.

GEN/CHK Performance Mode

With the TRD Setup window displayed:

1. In the Driver Mode Selection area select **GEN/CHK** (Figure 2-11).
2. Click the **Install** button.

   After installation of the GEN/CHK performance mode driver is complete, the Virtex-7 XT Connectivity TRD Control and Monitoring Interface is displayed (Figure 2-12). This interface includes control parameters such as test mode (loopback, generator, or checker) and packet length. The **System Monitor** tab displays system power consumption and die temperature.

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Figure 2-12: **GEN/CHK Performance Mode**

Note: This interface also provides LED indicators for DDR3 memory calibration and 10G PHY link status.

Note: Only Data Path-0 is enabled in Performance mode GEN/CHK flow.

3. In the Data Path-0 field, with **Loopback** selected by default, click **Start**.

   The Virtex-7 XT Connectivity TRD Control and Monitoring Interface is updated.

4. Click the **Performance Plots** tab.

   The **Performance Plots** tab (Figure 2-13) shows the system-to-card and card-to-system performance numbers for a specific packet size. The packet size and view performance variations can be varied accordingly.

Figure 2-13: **GEN/CHK Performance Mode Plots**

5. Stop the Gen/Chk test by clicking **Stop** for Data Path 0.

6. Click the **Block Diagram** tab on the right side of the GUI to bring up the block diagram of the TRD with the datapath highlighted for the selected mode. See Figure 2-14.

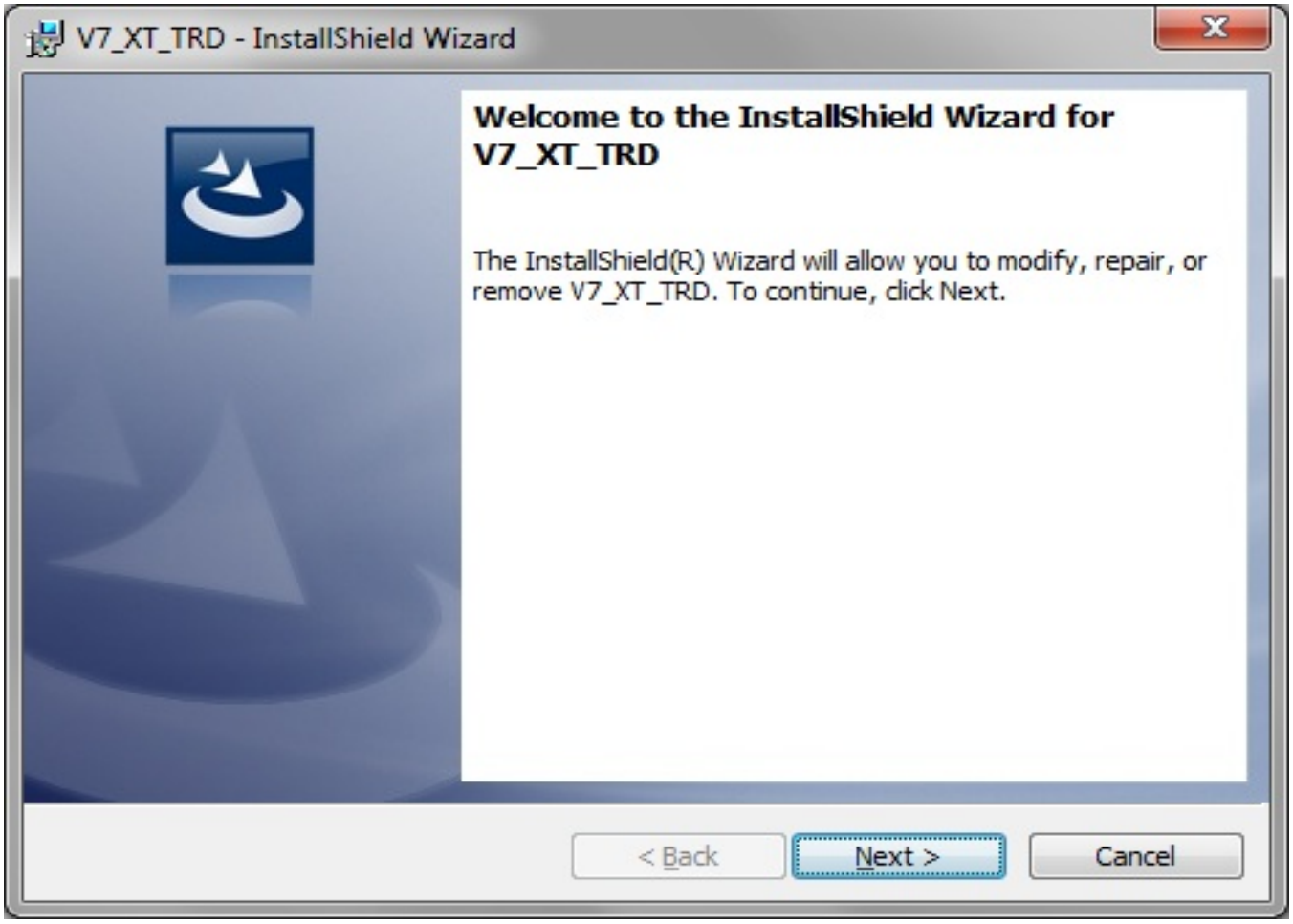

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Figure 2-14: **Performance Mode (GEN/CHK) Block Diagram**

7. Close the Virtex-7 XT Connectivity TRD Control and Monitoring Interface by clicking **X** in the upper right corner. Closing the interface stops any running test, uninstalls the driver, and returns to the TRD Setup window.

Raw Ethernet Performance Mode

With the TRD Setup window displayed:

1. In the Driver Mode Selection area select **Raw Ethernet** (Figure 2-15).

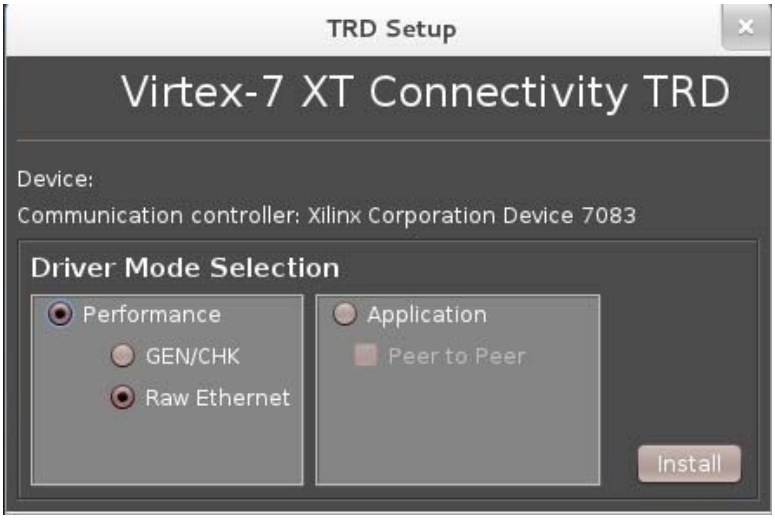

Figure 2-15: **Raw Ethernet Driver Installation**

2. Click the **Install** button. The Virtex-7 XT Connectivity TRD Control and Monitoring Interface starts with Performance Mode (Raw Ethernet) displayed by default (Figure 2-16). The packet size can be configured in this mode. The **System Monitor** tab monitors system power consumption and die temperature.
3. Click **Start All** to start tests on all channels at once or **Start** for each datapath to start each channel separately.

Figure 2-16: **Raw Ethernet Driver Interface**

4. Click the **Plots** tab to see performance on system-to-card and card-to-system (Figure 2-17).

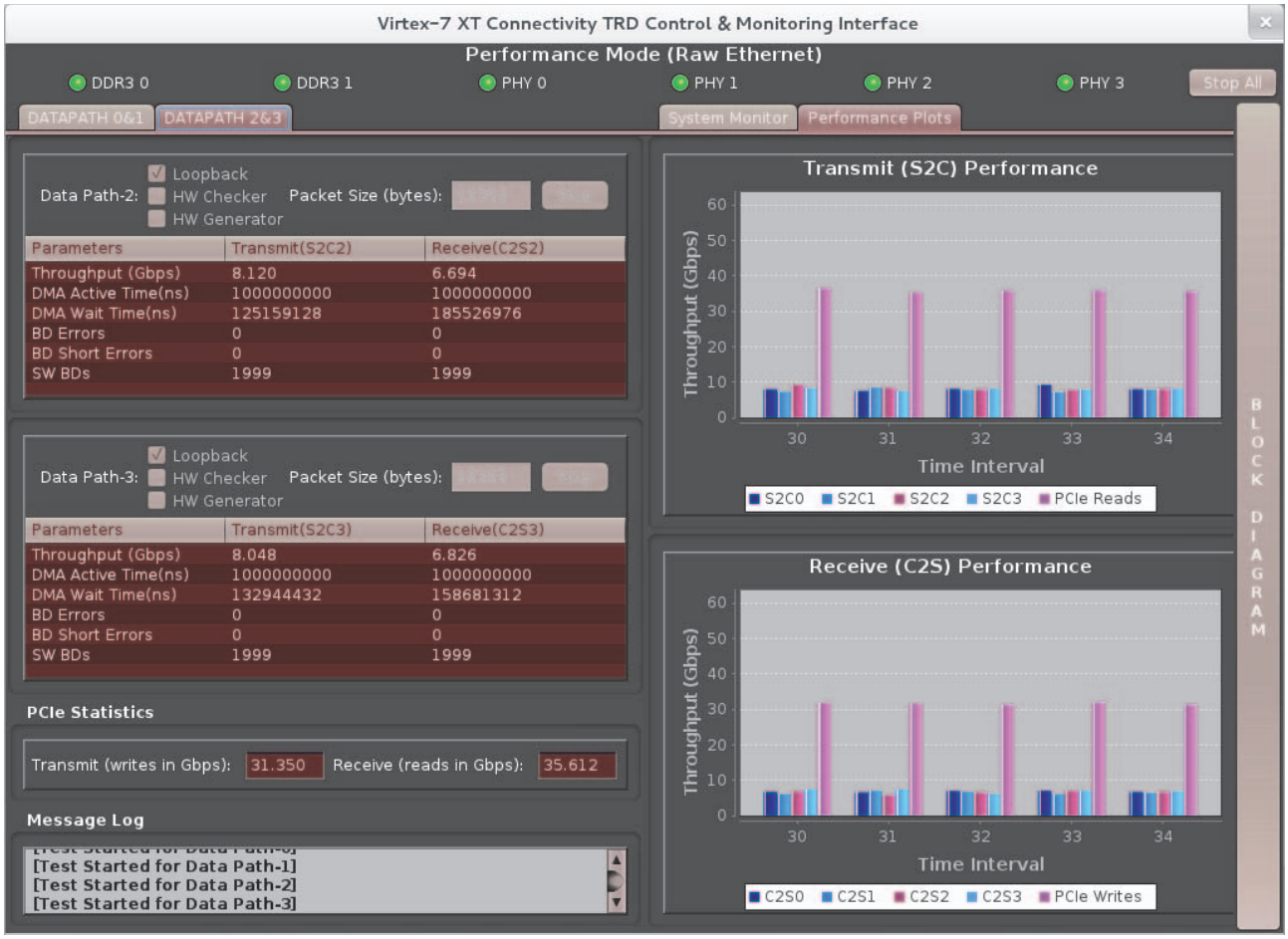

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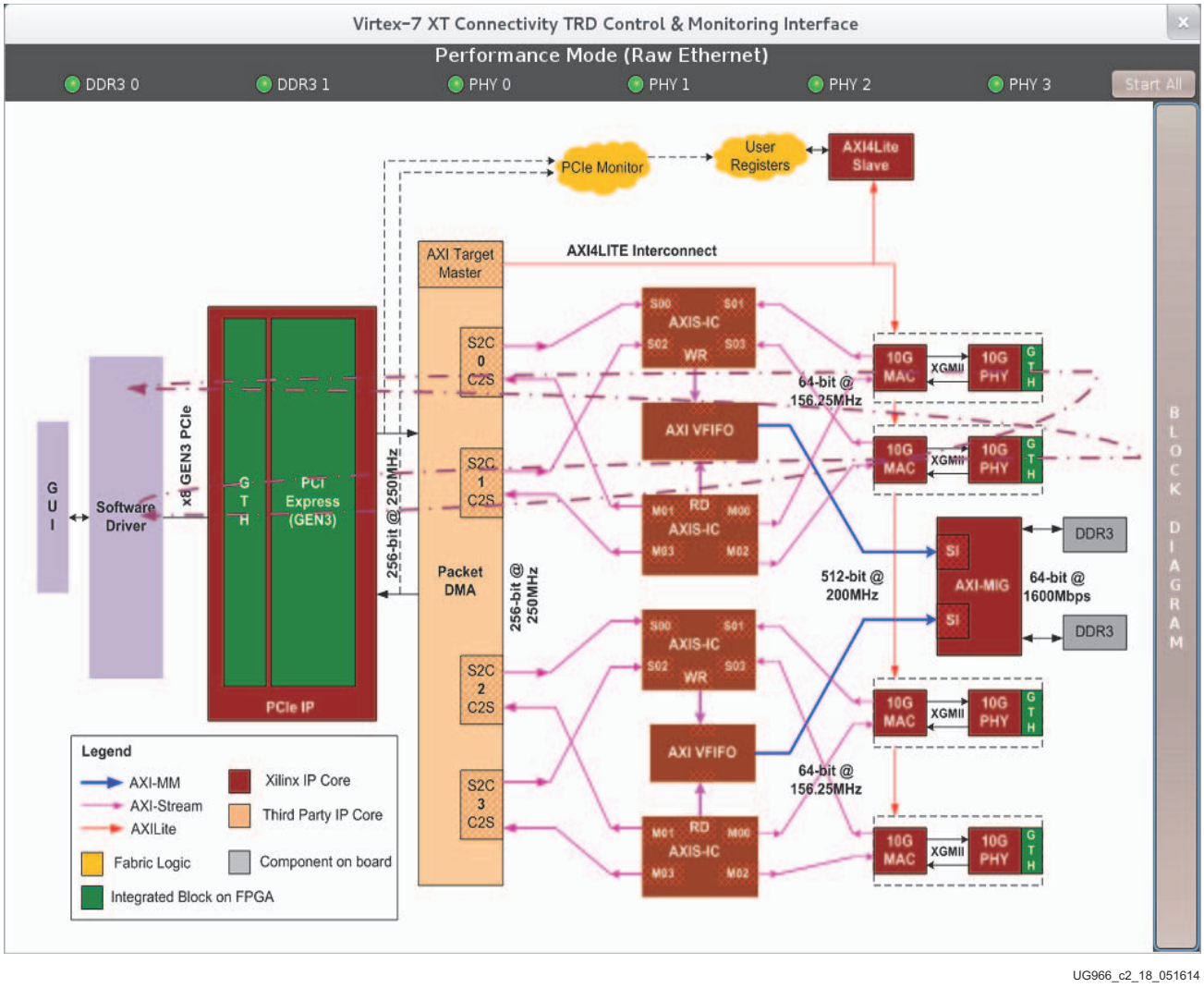
Figure 2-17: **Raw Ethernet Driver Interface**

5. Stop the raw ethernet test by clicking **Stop All** or stop an individual datapath by clicking **Stop** associated with the individual datapath.

6. Click the **Block Diagram** tab on the right side of the GUI to bring up the block diagram of the TRD with the datapath highlighted for the selected mode (Figure 2-18).



UG966_c2_18_051614

Figure 2-18: **Performance Mode (Raw Ethernet) Block Diagram**

7. Close the Virtex-7 XT Connectivity TRD Control and Monitoring Interface by clicking **X** in the upper right corner. Closing the interface stops any running test, uninstalls the driver, and returns to the TRD Setup window.

Application Mode

With the TRD Setup window displayed:

1. In the Driver Mode Selection area select **Application** (Figure 2-19).

Note: Do not select the Peer-to-Peer option if a peer machine is not available with 10G NIC or an identical VC709 setup.

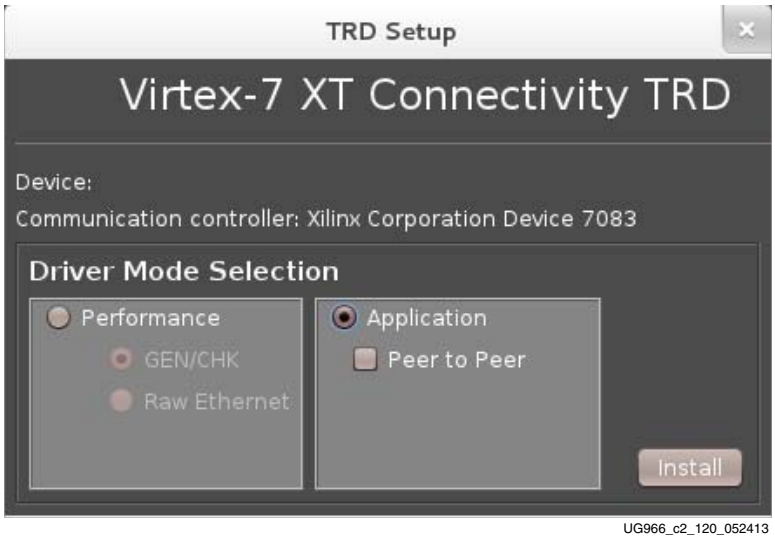


Figure 2-19: **Application Mode Driver Installation**

2. Click **Install**. After installing the application mode driver the Virtex-7 XT Connectivity TRD Control and Monitoring Interface starts (see Figure 2-20). However, in application mode, a test cannot be started or stopped because the traffic is generated by the networking stack.

UG966_c2_20_022213

Figure 2-20: **Application Driver Interface**

3. Open a command prompt on the host PC and ping the four network interfaces by entering:

   % ping 10.60.0.1

   % ping 10.60.1.1

   % ping 10.60.2.1

   % ping 10.60.3.1

The results should be similar to the output shown in Figure 2-21.

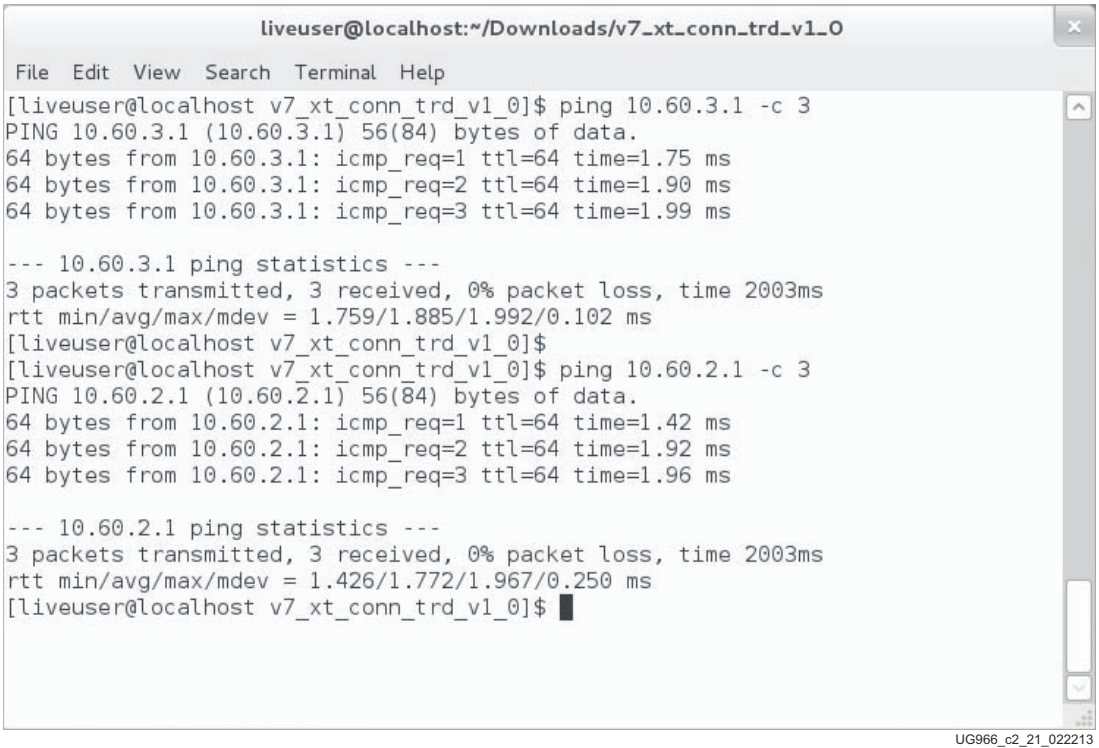
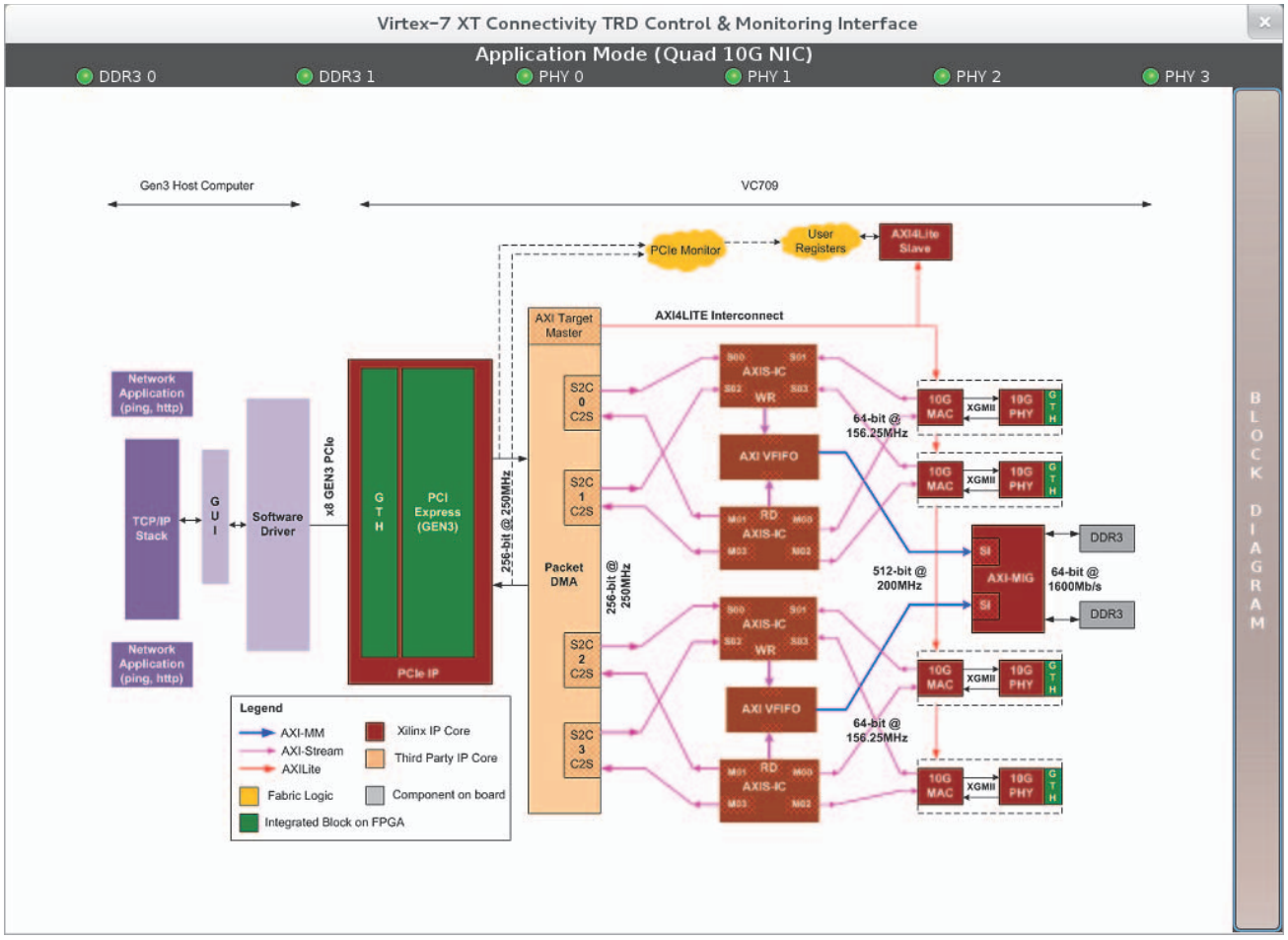


Figure 2-21: **System Output from Ping of Network Interfaces**

4. Click the **Block Diagram** tab on the right side of the GUI to bring up the block diagram of the TRD with the datapath highlighted for the selected mode. See Figure 2-22.



UG966_c2_22_051614

Figure 2-22: **Access the Block Diagram**

5. Close the Virtex-7 XT Connectivity TRD Control and Monitoring Interface by clicking **X** in the upper right corner. Closing the interface stops any running test, uninstalls the driver, and returns to the TRD setup window.

Conclusion

This completes the demonstration of the three modes of operation provided by the design. Refer to the *Virtex-7 FPGA XT Connectivity Targeted Reference Design for the VC709 Board User Guide* [Ref 2] for testing application mode when connecting to a peer machine.

This getting started guide describes how to gain initial hands-on experience with the connectivity kit by performing a simple hardware bring-up of the Virtex-7 XT Connectivity TRD in three different modes.

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Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website

For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the VC709 board and its documentation is available on these websites.

Virtex-7 VC709 Evaluation Kit

Virtex-7 VC709 Evaluation Kit Master Answer Record (AR 51901)

These Xilinx documents and sites provide supplemental material useful with this guide:

1. *VC709 Evaluation Board for the Virtex-7 FPGA User Guide* (UG887)
2. *Virtex-7 FPGA XT Connectivity Targeted Reference Design for the VC709 Board User Guide* (UG962)
3. *Virtex-7 FPGA Gen3 Integrated Block for PCI Express* (PG023)
4. *Understanding Performance of PCI Express Systems* (WP350)
5. *LogiCORE IP AXI Stream Interconnect* (PG035)
6. *LogiCORE IP AXI Virtual FIFO Controller: Product guide for Vivado Design Suite* (PG038)
7. *Xilinx Memory Interface Generator User Guide* (UG586)
8. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
9. *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072)
10. *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide for Vivado Design Suite* (PG068)
11. *PicoBlaze 8-bit Embedded Microcontroller User Guide* (UG129)
12. Northwest Logic DMA Backend core
    nwlogic.com/products/docs/DMA_Back-End_Core.pdf
13. Fedora project
    fedoraproject.org
    Fedora is a Linux-based operating system used in the development of this TRD.

14. 10G MMF SFP+ SR Optical Transceivers: Avago AFBR-703SDZ
www.avagotech.com/pages/en/fiber_optics/ethernet/10_gbe/afbr-703sdz
15. LC to LC OM3 10G fiber optic patch cable:
Amphenol Cables on Demand™ (ACD) FO-10GGBLCX20-001
http://www.cablesondemand.com/category/FO10GGBMM/URvars/Catalog/Library/InfoManage/10-GIGABIT_MULTIMODE_CABLES_...htm
16. Tera Term home page
en.sourceforge.jp/projects/ttssh2/releases
17. Silicon Labs USB-UART drivers:
www.silabs.com/Support%20Documents/Software/CP210x_VCP_Windows.zip
18. Virtex-7 family FPGA Product Table:
www.xilinx.com/publications/prod_mktg/Virtex7-Product-Table.pdf
19. VC709 product page:
http://www.xilinx.com/vc709
20. Silicon Labs CP210x USB to UART Bridge VCP Drivers:
http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx
21. Master Answer Record:
www.xilinx.com/support/answers/51901.htm

Appendix B

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx ("Development Systems"). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes:
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(iii) Development Systems procured through unauthorized third parties; and
(iv) Development Systems that have been subject to misuse, mishandling, accident, alteration, neglect, unauthorized repair or installation. Furthermore, this limited warranty shall not apply to the use of covered products in an application or environment that is not within Xilinx specifications or in the event of any act, error, neglect or default of Customer. For any breach by Xilinx of this limited warranty, the exclusive remedy of Customer and the sole liability of Xilinx shall be, at the option of Xilinx, to replace or repair the affected products, or to refund to Customer the price of the affected products. The availability of replacement products is subject to product discontinuation policies at Xilinx. Customer may not return product without first obtaining a customer return material authorization (RMA) number from Xilinx.

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