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Ethernet Cores Hardware Demonstration Platform

Summary

The Ethernet Cores Hardware Demonstration Platform application note describes the functionality of Ethernet cores in Xilinx FPGA hardware. The development board requirements, setup, and MAC core-specific design components are provided, as well as a description of the graphical user interface (GUI) used to control the demonstration platform.

Introduction

The Ethernet Hardware Demonstration Platform demonstrates the functionality of the following Xilinx LogiCORE™ and embedded Ethernet products:

- 10-Gigabit Ethernet MAC (XGMAC) core
- XAUI core (as part of the XGMAC demonstration)
- 1-Gigabit Ethernet MAC (GEMAC) core
- Ethernet 1000 Base-X PCS/PMA or SGMII core (as part of the GEMAC demonstration)
- Tri-Mode Ethernet MAC (TEMAC) core
- Embedded Tri-Mode Ethernet MAC (EMAC) core
- Ethernet Statistics core (as part of the TEMAC and EMAC demonstrations)

The platform demonstrates how to integrate these cores into a system, interface the Ethernet cores to a microprocessor, generate the required clock resources, handle the Ethernet data flow using packet FIFOs and flow control, and connect to a physical interface.

A GUI is provided to enable the user to control the platform, using a standard RS-232 serial cable, and also allows the user to experiment with different configurations of the MAC, monitor frame information, and observe the MAC statistics.

Requirements

Development Boards

Table 1 describes the development boards supported by the demonstration platform.

Table 1: **Supported Hardware**

Demonstration	ML310 (2VP30)	ML323 (2VP20 & 2VP50)	ML401 (4LX25)	ML403 (4FX12)
10-Gigabit Ethernet MAC with XAUI Interface	Not Supported	Supported	Not Supported	Not Supported
10-Gigabit Ethernet MAC with 10GBaseSR Physical Interface	Requires PM101	Not Supported	Not Supported	Not Supported
10-Gigabit Ethernet MAC without Physical Interface	Supported	Supported	Not Supported	Not Supported
1-Gigabit Ethernet MAC with 1000 Base-X Physical Interface	Requires PM102	Requires SMA to SFP Conversion Module	Not Supported	Not Supported
1-Gigabit Ethernet MAC without Physical Interface	Supported	Supported	Not Supported	Not Supported

Table 1: **Supported Hardware *(Continued)***

Demonstration	ML310 (2VP30)	ML323 (2VP20 & 2VP50)	ML401 (4LX25)	ML403 (4FX12)
Tri-Mode Ethernet MAC with 1000/100/10 Base-T Physical Interface	Requires PM102	Requires PHY Daughter Card	Supported	Supported
Tri-Mode Ethernet MAC without Physical Interface	Supported	Supported	Supported	Supported
Embedded Tri-Mode Ethernet MAC with 1000/100/10 Base-T Physical interface	Not Supported	Not Supported	Not Supported	Supported

Various board attachments are required to achieve connection to a physical interface, as shown in Table 1. Board attachments are described below.

PM101

A 10-Gigabit fibre-optic Personality Module for the ML310 board. This must have an XPAK module fitted in the XPAK socket. The 10-Gigabit Ethernet demo design has been tested with an Infineon 10GBase-SR XPAK 850nm module (V23833-G6005-A101).

PM102

A Gigabit Ethernet Personality Module for the ML310 board. This board has a Broadcom Tri-speed Ethernet PHY that is used to provide a 1000/100/10 Base-T connection to the demonstration platform.

PHY Daughter Card

The PHY Daughter card (HW-AFX-BERG-EPHY) for use with ML323 board, has a Marvell Tri-speed Ethernet PHY, that is used to provide 1000/100/10 Base-T connection to the demonstration platform.

SMA to SFP Conversion Module

The SMA to SFP Conversion Module (HW-AFX-SMA-SFP) for use with the ML323 board, contains a socket for an SFP optical module and connects to a board via 4 SMA connectors. This provides a 1000 Base-X connection to the demonstration platform.

PC

The demonstration platform requires a PC on which to run the GUI, a standard Windows® 2000/XP application that can be run on most PCs. A spare serial port is required to connect the GUI to the development board.

Demonstration Platform System Design

Overview

The demonstration platform consists of the following

- A development board with a Xilinx FPGA loaded with the hardware design
- A PC used to control the hardware design using a RS-232 serial cable
- A physical interface connection (optional)

All demonstration designs share a common microprocessor system and frame generation logic. The microprocessor used is either the embedded PowerPC on ML310 and ML323 boards, or a microblaze soft processor on ML401 and ML403 boards. Equivalent hardware components are used in all Ethernet MAC designs, however, the implementation details are different for each core.

10-Gigabit Ethernet MAC Hardware Design

Figure 1 illustrates the design for the 10-Gigabit Ethernet MAC (XGMAC) hardware design. The design, including the microprocessor system, uses approximately 9000 slices of the FPGA. A XAUI core is used to provide a physical interface to the MAC, and a FIFO is used on the client side of the MAC to provide frame buffering. The microprocessor system connects to the MAC host interface to control the MAC configuration, and connects to the FIFO to read/write frame data.

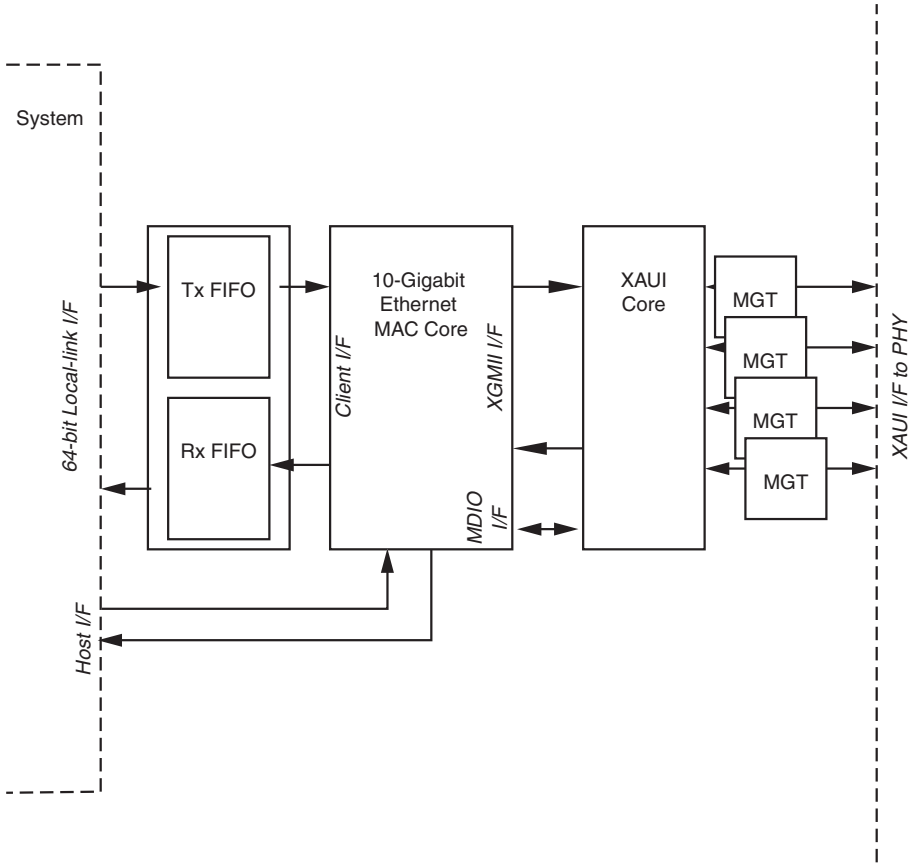

Figure 1: **10-Gigabit Ethernet MAC FPGA Block Diagram**

10-Gigabit Ethernet MAC Core

The XGMAC core is a CORE Generator™ instance of the XGMAC v6.0, generated with the following XCO parameters:

```
component_name = xgm6
physical_interface = none
management_interface = true
statistics_gathering = true
simplex_split = none
```

The core has been generated with a full-system hardware evaluation license, which operates for approximately 8 hours. After the core ceases to function, the board must be reconfigured.

XAUI Core

The XAUI core, used to connect to a PHY or an external device with a XAUI interface, is a CORE Generator instance of the XAUI v6.0, generated with the following XCO parameters:

```
component_name = xaui6
physical_interface = none
management_interface = true
statistics_gathering = true
simplex_split = none
```

Ethernet FIFO

The FIFO used in the demonstration platform is taken from the XGMAC example design, which is provided with the core.

Physical Interface

Any compatible PHY device can be connected to the XAUI interface. The PM101 provides a suitable XPAK socket which has XAUI signals and has been tested with a 10 GBase-SR optical module.

Clock Management

The XGMAC core uses a 156.25 MHz reference clock. The same 156.25 MHz reference is required for the XAUI interface.

Chipscope

Chipscope probes in the hardware design allow the user to look at data passing through the MAC core. The chipscope probes are placed on the transmitter XGMII and receiver XGMII interfaces, the transmitter client and receiver client interfaces and the MAC statistics vector. A chipscope project file is provided for the XGMAC demonstration.

1-Gigabit Ethernet MAC Hardware Design

Figure 2 illustrates the 1-Gigabit Ethernet MAC (GEMAC) hardware design. The entire design, including the microprocessor system, uses approximately 4500 slices of the FPGA. The 1000 Base-X PCS PMA core is used to provide an external 1000 Base-X interface to the core, and a FIFO is used on the client side of the MAC to provide frame buffering. The microprocessor system connects to the MAC host interface to control the MAC configuration, and connects to the FIFO to read/write frame data.

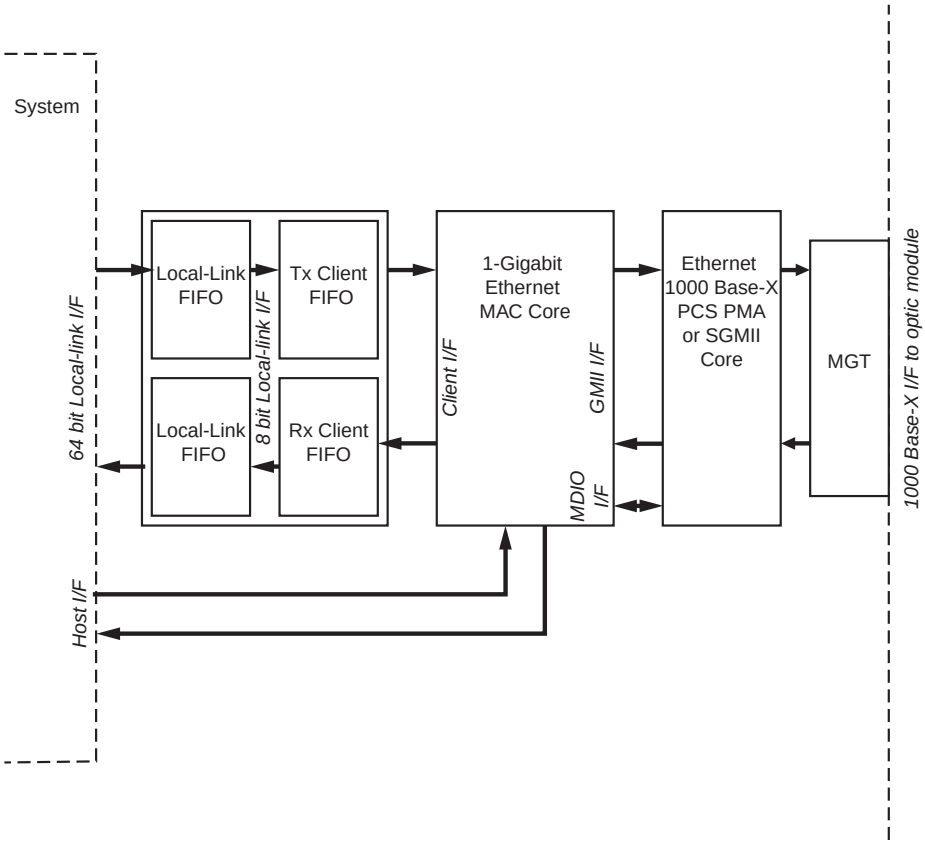

Figure 2: **1-Gigabit Ethernet MAC FPGA Block Diagram**

1-Gigabit Ethernet MAC Core

The GEMAC core is a CORE Generator™ instance of the GEMAC v6.0 and was generated using the following XCO parameters:

```
component_name = gig_mac60
physical_interface = gmii
management_interface = true
statistics_gathering = true
```

The core has been generated with a full-system hardware evaluation license, which operates for approximately 8 hours. When the core ceases to function, the board must be reconfigured.

Ethernet 1000 Base-X PCS PMA or SGMII Core

The Ethernet 1000 Base-X PCS PMA core, used to connect to the physical interface through MGTs to an optical module, is a CORE Generator instance of v6.0 of the core and was generated using the following XCO parameters:

```
component_name = gig_pcspma60
management_interface = true
auto_negotiation = true
```

```
physical_interface = RocketIO
mgt_crc_enabled = false
standard = 1000BASEX
```

Ethernet FIFO

The FIFO used in the demonstration platform consists of the local link FIFO design XAPP691 (http://direct.xilinx.com/bvdocs/appnotes/xapp691.pdf) and the FIFO components **tx_client_fifo**, **rx_client_fifo**, which are supplied with the GEMAC core as part of the example design.

The local link FIFO from XAPP691 connects to the 64-bit local link interface of the microprocessor system. This FIFO is used to convert the data width from 64-bit to 8-bit. The client side FIFOs from the example design connect directly to the 8-bit local link interface of the XAPP691 FIFO. The client side FIFOs have a client interface that connects directly to the GEMAC core and provides all the necessary functionality to drive the client interface appropriately.

Clock Management

The GEMAC core uses a 125 MHz input clock. The 1000 Base-X PCS PMA requires a high quality 62.5MHz reference clock to drive the MGT.

Chipscope

Chipscope probes in the hardware design allow the user to look at data passing through the MAC core. The chipscope probes are placed on the transmitter GMII and receiver GMII interfaces, the transmitter client and receiver client interfaces and the MAC host interface. A chipscope project file is provided for the GEMAC demonstration.

Tri-Mode Ethernet MAC Hardware Design

Figure 3 illustrates the Tri-Mode Ethernet MAC (TEMAC) hardware design. The entire design, including the microprocessor system, uses approximately 6700 slices of the FPGA. IOB logic is used to provide an interface from the MAC to an external PHY, and a FIFO is used on the client side of the MAC to provide frame buffering. The Ethernet Statistics core collects statistics information from the TEMAC core. The microprocessor system connects to the MAC host interface to control the MAC configuration, and connects to the FIFO to read/write frame data.

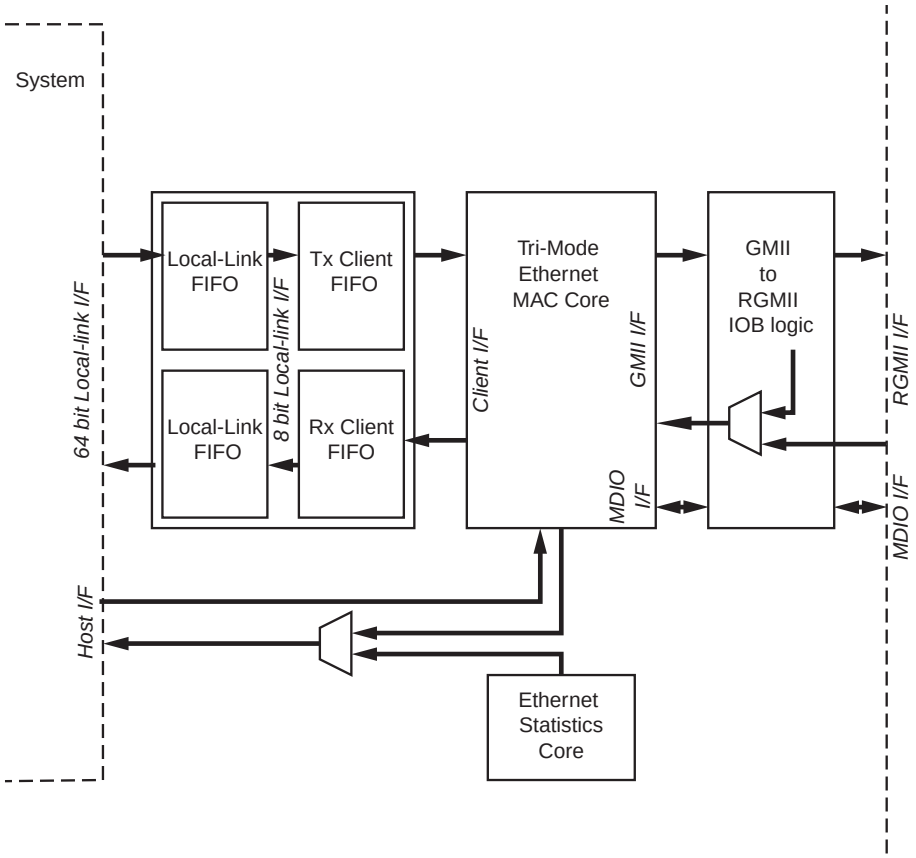

Figure 3: **Tri-Mode Ethernet MAC FPGA Block Diagram**

Tri-Mode Ethernet MAC Core

The TEMAC core is a CORE Generator instance of the TEMAC v2.1 and was generated using the following XCO parameters:

```
component_name = tri_mac21
physical_interface = GMII
management_interface = true
clock_enables = true
address_filter = true
number_of_address_table_entries = 4
```

The core has been generated with a full-system hardware evaluation license, which operates for approximately 8 hours. When the core ceases to function, the board must be reconfigured.

Ethernet Statistics Core

The Ethernet Statistics core, used to provide statistical counters for the TEMAC core, is a CORE Generator instance of the Ethernet Statistics core v1.1 and was generated using the following XCO parameters:

```
component_name = ethernet_statistics
statisticswidth = 64bit
numberofstatistics = 42
mactype = TEMAC
```

Ethernet FIFO

The FIFO used in the demonstration platform consists of the local link FIFO design XAPP691 (http://direct.xilinx.com/bvdocs/appnotes/xapp691.pdf) and the FIFO components **tx_client_fifo**, **rx_client_fifo** (supplied with the TEMAC core as part of the example design).

The local link FIFO from XAPP691 connects to the 64-bit local link interface of the microprocessor system. This FIFO is used to convert the data width from 64-bit to 8-bit. The client side FIFOs from the example design connect directly to the 8-bit local link interface of the XAPP691 FIFO. The client side FIFOs have a client interface that connects directly to the TEMAC core and provides all the necessary functionality to drive the client interface appropriately.

Physical Interface

Logic is used at the physical interface to convert the GMII interface of the MAC into an RGMII interface, which is then connected to the external Base-T PHY. The physical interface logic uses double-data rate IO registers and is based on logic provided in the TEMAC example design. The logic also provides functionality to loopback the GMII interface from transmitter to receiver. The MDIO interface from the MAC core is passed through a tri-state buffer to connect to the PHY.

Clock Management

Clock generation for the TEMAC core is based on logic provided in the TEMAC example design. A 125 MHz input clock is provided to the clock management logic, either directly from an onboard oscillator or generated from a DCM. This generates an output clock for the MAC transmitter logic at 125 MHz, 25 MHz, or 2.5 MHz given the MAC operating speed. The clocking management logic also provides phase shifting abilities to correct the receiver clock from the PHY, to adjust for delays across the receiver interface. When the physical interface is put into loopback, the clock management logic sets the receiver clock input to the transmitter clock.

Chipscope

Chipscope probes in the hardware design allow the user to look at data passing through the MAC core. The chipscope probes are placed on the transmitter GMII and receiver GMII interfaces, the transmitter client and receiver client interfaces and the MAC host interface. A chipscope project file is provided for the TEMAC demonstration.

Embedded Tri-Mode Ethernet MAC Hardware Design

Figure 4 illustrates the Embedded Tri-Mode Ethernet MAC (EMAC) hardware design. The entire design, including the microprocessor system, uses approximately 3300 slices of the FPGA. IOB logic is used to provide a GMII interface from the MAC to an external PHY, and a FIFO is used on the client side of the MAC to provide frame buffering. The Ethernet Statistics core collects statistics information from the EMAC core. The microprocessor system connects to the MAC host interface to control the MAC configuration, and connects to the FIFO to read/write frame data.

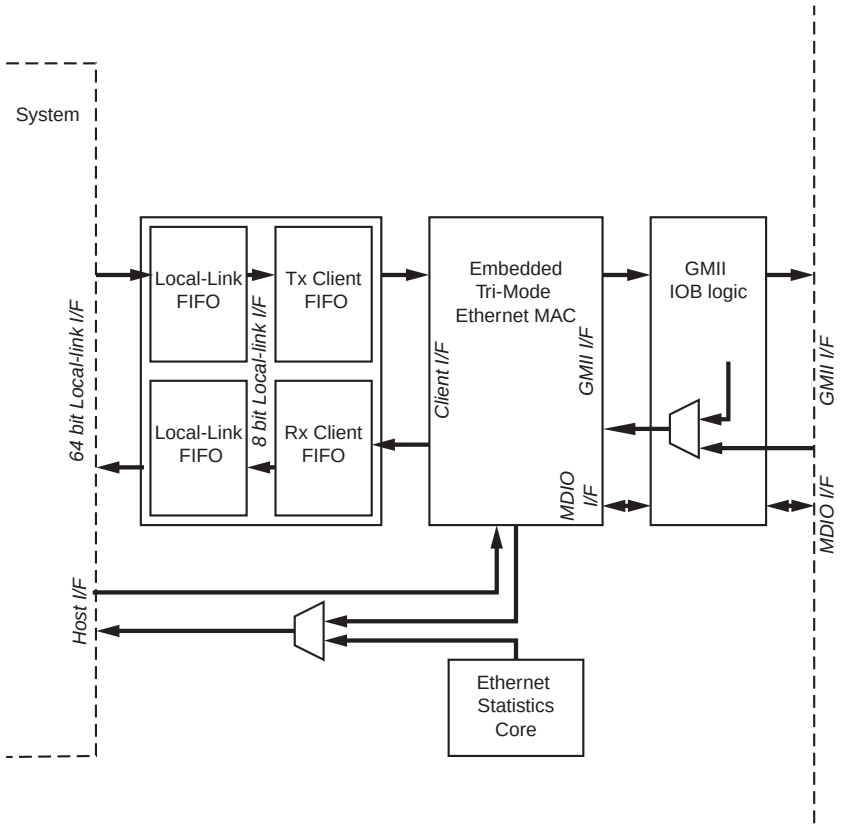

Figure 4: **Embedded Tri-Mode Ethernet MAC FPGA Block Diagram**

Embedded Tri-Mode Ethernet MAC

The EMAC is available in all Virtex-4 FX parts. The MAC is instantiated in the HDL design, from a wrapper file, based on the CORE Generator EMAC wrapper.

Ethernet Statistics Core

The Ethernet Statistics core, used to provide statistical counters for the EMAC core, is a CORE Generator instance of the Ethernet Statistics core v1.1 and was generated using the following XCO parameters:

```
component_name = ethernet_statistics
statisticswidth = 64bit
numberofstatistics = 41
mactype = V4EMAC
```

Ethernet FIFO

The FIFO used in the demonstration platform consists of the local link FIFO design XAPP691 (http://direct.xilinx.com/bvdocs/appnotes/xapp691.pdf) and the FIFO components **tx_client_fifo**, **rx_client_fifo**, which are supplied with the TEMAC and GEMAC cores as part of their example designs.

The local link FIFO from XAPP691 connects to the 64-bit local link interface of the microprocessor system. This FIFO is used to convert the data width from 64-bit to 8-bit. The client side FIFOs from the example design connect directly to the 8-bit local link interface of the XAPP691 FIFO. The client side FIFOs have a client interface that connects directly to the EMAC core and provides all the necessary functionality to drive the client interface appropriately.

Physical Interface

IOB registers are used at the physical interface to connect the GMII interface of the MAC onto IO pins, which are then connected to the external Base-T PHY. The logic also provides functionality to loopback the GMII interface from transmitter to receiver. The MDIO interface from the MAC core is passed through a tri-state buffer to connect to the PHY.

Chipscope

No chipscope probes are used in this design due to insufficient Block RAM availability.

Common Microprocessor System

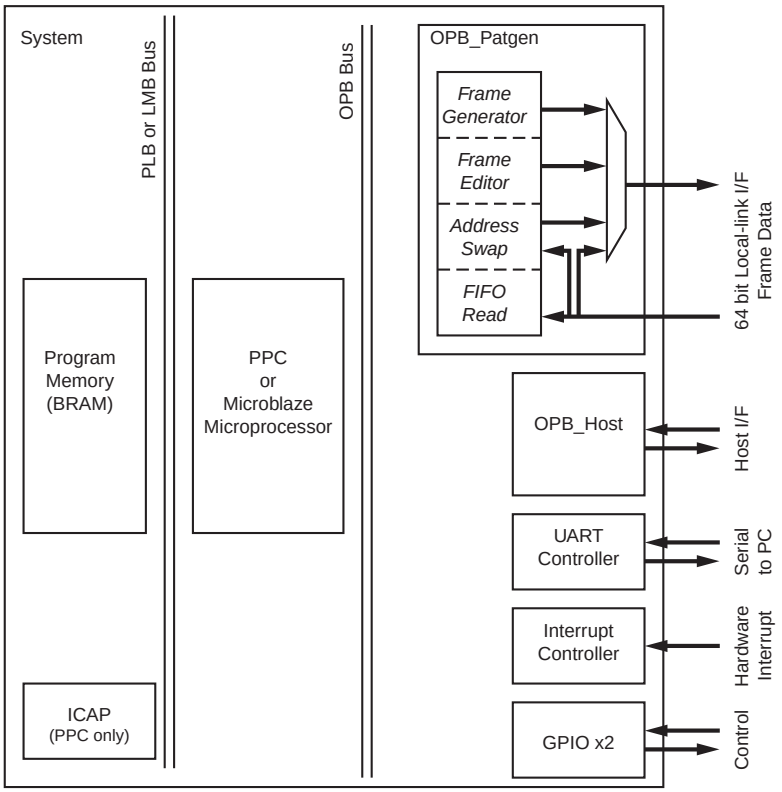

Figure 5: **Microprocessor System Block Diagram**

The microprocessor system, as shown in Figure 5, is either based on an embedded PowerPC CPU (PPC) or a soft MicroBlaze processor. These have both been created using the Xilinx Platform Studio, as a separate module. They share common standard OPB peripherals and two peripherals designed specifically for the demonstration platform, the Pattern Generator, and the Host cores.

PPC System

This block is a complete PowerPC CPU subsystem containing PPC405, 32k RAM, UART (uartlite), interrupt controller, PLB, and OPB buses.

MicroBlaze System

This is a MicroBlaze v3.0 CPU subsystem containing 16k RAM, UART (uartlite), interrupt controller, LMB, and OPB buses.

Pattern Generator (OPB_Patgen)

The Pattern Generator peripheral holds all the logic required to access the client side data stream of the MAC core, allowing data to be written to the transmitter side FIFO, or read from the receiver side FIFO. This peripheral is made up of the following components:

- **The frame editor**

  This uses a block RAM to store user defined frames for the transmitter. There is 16 kBytes of RAM available for frame storage.

- **The frame generator**

  This component can generate fixed pattern test frames and transmit these individually or continuously.

- **The loopback multiplexer**

  This is included in the pattern generator and allows the transmitter (Tx) and receiver (Rx) FIFOs to be connected. This allows external test equipment or Ethernet devices to stimulate the MAC core and receive frames back. There is an option to switch the source address and destination address fields of each frame passing through the multiplexer which allows external equipment to stimulate the design and receive valid addressed frames from the demonstration platform.

- **The receive FIFO reader**

  This logic reads the contents of the receiver side FIFO. The captured frame data can be read from the peripheral by the microprocessor, which formats the frames and makes them available to the GUI for display, by transmitting them over the serial link.

Host (OPB_Host)

The Host peripheral allows the Management Interface of the MAC core to be accessed. Through this interface, the MAC configuration can be read and modified, the statistics counters can be read, and the MDIO transactions can be made to control the physical layer.

Microprocessor Firmware

The microprocessor runs firmware which monitors the serial interface and responds to commands issued by the GUI. On startup, the microprocessor detects what design is operating on the FPGA, configures the logic on the FPGA appropriately, and then waits for and processes commands from the PC.

Setting up the Demonstration Platform

ML310 Configuration for 10-Gigabit Ethernet MAC Demo

Power Supply

The ML310 should be connected to the ATX power supply provided with the board. Please check the ML310 documentation to ensure the power supply is configured correctly for the supply voltage.

Clock Selection

The demonstration platform uses the onboard 156.25 MHz differential oscillator as a master reference to generate all the clocks required for the design. To select the 156.25 MHz output from the differential oscillator, jumpers must be placed on J20 and J21 between pins 1 and 2 to select the 156.25 MHz clock.

Jumper Settings

The RocketIO voltage jumpers should be set to 1.8V. The jumpers labeled **BOT MGT VTT_RX** and **TOP MGT VTT_RX** should be set to 1.8V. No other jumpers should be fitted to the board.

RS-232

Connect a Null-Modem cable between the RS-232 port on the board and an additional serial port on the PC. The FPGA UART header is used for the serial link to the PC. The DIL header to D-Type connector cable must be fitted to the board. The cable is supplied with the board. Take care when fitting the cable, as the connector is not keyed and can be fitted two ways. See the ML310 documentation for details.

LEDs

The LEDs on the boards indicate the basic status of the platform at a glance. Detailed information is available using the GUI. Table 2 defines the LED functions.

Table 2: **LED Indications for ML310 10-Gigabit MAC Demo**

LED	10-Gigabit Function
DBG0	Lane0 Sync OK
DBG1	Lane1 Sync OK
DBG2	Lane2 Sync OK
DBG3	Lane3 Sync OK
DBG4	Lanes Aligned
DBG5	FIFO loopback selected
DBG6	Address swap enabled
DBG7	PHY/MGT loopback

Using the PM101

PM101 is a 10-Gigabit fibre optic PHY card. Only the XPAK connector (U9) is used and should be fitted with a suitable XPAK module. The 10-Gigabit design has been tested with an Infineon 10 GBase-SR XPAK 850nm module (V23833-G6005-A101). The CPLD on the PM101 must be programmed to drive the reset input on the XPAK socket. An example design and bitfile for the Infineon XPAK module is included in the PM101_CPLD folder. The Infineon XPAK module simply requires that the reset is not asserted at any time, the internal power on reset enables the module.

ML323 Configuration for 10-Gigabit Ethernet MAC Demo

Power Supply

The ML323 should be powered from the 5V jack input. See the ML323 documentation to configure the jumpers for this supply.

Clock Selection

The demonstration platform uses the on-board 156.25 MHz differential oscillator as a master reference to generate all the clocks required for the design. Only GCLK3P and GCLK2S (the top oscillator) inputs are used. J68 must be set to **ON** and J74 must be set to **VCCO**. The lower differential oscillator and both DIL oscillators can be disabled, removed, or left unchanged as these do not affect the demo design.

The SystemACE oscillator (X1) should be enabled (J63 set to **ON**) if the FPGA is configured using SystemACE (see the following section).

Jumper Settings

J52 (near the RS-232 Port) must be fitted and set to **ON** to enable the RS-232 transceiver. No additional jumpers are required.

The setting on the DIP switches other than the SystemACE address does not affect the operation of the designs.

RS-232

Connect a Null-Modem cable between the RS-232 port on the board and an additional serial port on the PC. There is only one serial port on the ML323. This is used to connect to the PC. J52 must be fitted and set to **ON** to enable the transceiver.

LEDs

The LEDs on the boards indicate the basic status of the platform at a glance. Detailed information is available using the GUI. Table 3 defines the LED functions.

Table 3: **LED Indications for ML323 10-Gigabit MAC Demo**

LED	10-Gigabit Function
DS29	Lane0 Sync OK
DS28	Lane1 Sync OK
DS23	Lane2 Sync OK
DS16	Lane3 Sync OK
DS17	Lanes Aligned
DS18	FIFO loopback selected
DS19	Address swap enabled
DS20	PHY/MGT loopback

Physical Interface

There are no 10-Gigabit PHY cards available for the ML323. SMA cables can be used to connect the MGT inputs and outputs to a suitable XAUI equipped PHY. 16 SMA cables are required for the 4-lane differential XAUI interface, the board connections are:

Lane0 = MGT4 (Out = J79,J83; In = J78,J80)

Lane1 = MGT6 (Out = J18,J17; In = J15,J14)

Lane2 = MGT7 (Out = J31,J38; In = J32,J29)

Lane3 = MGT9 (Out = J90,J91; In = J89,J88)

ML310 Configuration for 1-Gigabit Ethernet MAC Demo

Power Supply

The ML310 should be connected to the ATX power supply provided with the board. Please check the ML310 documentation to ensure the power supply is configured correctly for the supply voltage.

Clock Selection

The demonstration platform can be run from one of two possible input clock sources. For full demonstration functionality a plug-in 62.5 MHz single-ended oscillator should be used. This 62.5 MHz oscillator should be inserted into the socket X6. The oscillator will be detected by the demonstration design. When using the 62.5MHz oscillator, the on-board 125MHz oscillator should also be enabled as below.

If a 62.5 MHz external oscillator is not available, the demonstration platform will run from the on-board 125 MHz oscillator. To select the 125 MHz output from the differential oscillator,

jumpers must be placed on J20 and 21 between pins 2 and 3 to select the 125 MHz clock. Using the 125 MHz oscillator will allow the demonstration platform to be run with the physical interface in loopback, but there will be no 62.5MHz reference clock to the MGT and the physical interface will not function.

Jumper Settings

No further jumpers are required.

RS-232

Connect a Null-Modem cable between the RS-232 port on the board and a spare serial port on the PC. The FPGA UART header is used for the serial link to the PC. The DIL header to D-Type connector cable must be fitted to the board. The cable is supplied with the board. Take care when fitting the cable, as the connector is not keyed and can be fitted in two ways. See the ML310 documentation for details.

LEDs

The LEDs on the boards indicate the basic status of the platform at a glance. Detailed information is available using the GUI. Table 6 defines the LED functions.

Table 4: **LED Indications for ML310 1-Gigabit Ethernet MAC Demo**

LED	1-Gigabit MAC Function
DBG0	Design running from 125MHz oscillator
DBG1	Design running from 62.5MHz oscillator
DBG2	MAC speed is 1 Gbps
DBG5	FIFO loopback selected
DBG6	Address swap enabled
DBG7	GMII loopback

Using the PM102

The PM102 is a copper and fibre optic PHY card for 10/100/1000 operation. The GEMAC design uses an SFP cage on the board to enable a fibre optic connection to be made. Ensure that the Personality Module is connected to the board before configuration of the FPGA. The active SFP cage on the board is U7. The CPLD on the PM102 must be programmed to drive the reset input on the SFP socket. A bitfile for the CPLD module is included in the PM102_CPLD folder.

ML323 Configuration for 1-Gigabit Ethernet MAC Demo

Power Supply

The ML323 should be powered from the 5V jack input. See the ML323 documentation to configure the jumpers for this supply.

Clock Selection

The demonstration platform can be run from one of two possible input clock sources. For full demonstration functionality a plug-in 62.5 MHz single-ended oscillator should be used. This 62.5 MHz oscillator should be inserted into the socket X3. J71must be set to **ON** and J73 must be set to **VCCO**. The oscillator will be detected by the demonstration design. When using the 62.5MHz oscillator, the on-board 156.25MHz oscillator should also be enabled as below.

If a 62.5 MHz external oscillator is not available, the demonstration platform will run from the on-board 156.25 MHz oscillator. Only GCLK3P and GCLK2S (the top oscillator) inputs are used. J68 must be set to **ON** and J74 must be set to **VCCO**. Using the 156.25 MHz oscillator

will allow the demonstration platform to be run with the physical interface in loopback, but there will be no 62.5MHz reference clock to the MGT and a physical connection will not function.

The SystemACE oscillator (X1) should be enabled (J63 set to **ON**) if the FPGA is configured using SystemACE (see "SystemACE," page 20).

Jumper Settings

J52 (near the RS-232 Port) must be fitted and set to **ON** to enable the RS-232 transceiver. No additional jumpers are required.

RS-232

Connect a Null-Modem cable between the RS-232 port on the board and an additional serial port on the PC. There is only one serial port on the ML323. This is used to connect to the PC. J52 must be fitted and set to **ON** to enable the transceiver.

LEDs

The LEDs on the boards indicate the basic status of the platform at a glance. Detailed information is available using the GUI. Table 7 defines the LED functions.

Table 5: **LED Indications for ML323 1-Gigabit Ethernet MAC Demo**

LED	1-Gigabit MAC Function
DS29	Design running from 156.25MHz oscillator
DS28	Design running from 62.5MHz oscillator
DS23	MAC Speed 1 Gbps
DS18	FIFO loopback selected
DS19	Address swap enabled
DS20	GMII loopback

Physical Interface

SMA cables can be used to connect the MGT inputs and outputs to the SMA to SFP conversion module, or any other suitable SFP/GBIC optical daughter card. 4 SMA cables are required for the 1000 Base-X interface. These should connect to MGT 7, where rxp=J32, rxn=J29, txp=J31, txn=J38. The SFP conversion module should be supplied with a 3.3 volt power supply and a jumper should set on header J5 to configure TX ENABLE.

For more information on the SMA to SFP Conversion Module, see:

http://www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=HW-AFX-SMA-SFP

ML310 Configuration for Tri-Mode Ethernet MAC Demo

Power Supply

The ML310 should be connected to the ATX power supply provided with the board. Please check the ML310 documentation to ensure the power supply is configured correctly for the supply voltage.

Clock Selection

The demonstration platform uses the on-board 125 MHz differential oscillator as a master reference to generate all the clocks required for the design. To select the 125 MHz output from the differential oscillator, jumpers must be placed on J20 and 21 between pins 2 and 3 to select the 125 MHz clock.

Jumper Settings

No other jumpers should be fitted to the board.

RS-232

Connect a Null-Modem cable between the RS-232 port on the board and a spare serial port on the PC. The FPGA UART header is used for the serial link to the PC. The DIL header to D-Type connector cable must be fitted to the board. The cable is supplied with the board. Take care when fitting the cable, as the connector is not keyed and can be fitted in two ways. See the ML310 documentation for details.

LEDs

The LEDs on the boards indicate the basic status of the platform at a glance. Detailed information is available using the GUI. Table 6 defines the LED functions.

Table 6: **LED Indications for ML310 Tri-Mode Ethernet MAC Demo**

LED	Tri Mode Function
DBG0	MAC speed is 10 Mbps
DBG1	MAC speed is 100 Mbps
DBG2	MAC speed is 1 Gbps
DBG5	FIFO loopback selected
DBG6	Address swap enabled
DBG7	GMII loopback

Using the PM102

The PM102 is a copper and fibre optic PHY card for 10/100/1000 operation. The Tri-Mode design uses the copper PHY in 1000/100/10BaseT mode only. Ensure that the Personality Module is connected to the board before configuration of the FPGA. A 1-Gigabit compatible RJ45 patch lead should be connected to the leftmost PHY (P2) on the Personality Module. A crossover cable is required for direct connection to another Gigabit Ethernet device, else a normal cable should be used for connection to a Gigabit Hub. Upon power-up of the board and before FPGA configuration, apply a hardware reset to the PHY by pressing push button SW2 on the Personality Module. If configuring the board from systemace, power-up the board, apply a hardware reset by pressing push button SW2 and then reprogram the board by pressing the systemace reset on the ML310 board, SW1.

ML323 Configuration for Tri-Mode Ethernet MAC Demo

Power Supply

The ML323 should be powered from the 5V jack input. See the ML323 documentation to configure the jumpers for this supply.

Clock Selection

The demonstration platform can be run from one of two possible input clock sources. It is recommended that a plug-in 62.5 MHz single-ended oscillator is used if available. This 62.5 MHz oscillator should be inserted into the socket X5. The oscillator will be detected by the demonstration design.

If a 62.5 MHz external oscillator is not available, the demonstration platform will run from the on-board 156.25 MHz oscillator. Only GCLK3P and GCLK2S (the top oscillator) inputs are used. J68 must be set to **ON** and J74 must be set to **VCCO**. Using the 156.25 MHz oscillator will allow the demonstration platform to be run with the physical interface in loopback, but the

125 MHz clock generated from the on-board oscillator is not accurate enough for Base-T operation. If a physical connection is provided, the MAC core will still be able to receive data, as the received clock is provided to the board from the PHY. However, the MAC core will not successfully transmit frames to an external device.

The SystemACE oscillator (X1) should be enabled (J63 set to **ON**) if the FPGA is configured using SystemACE (see "SystemACE," page 20).

Jumper Settings

J52 (near the RS-232 Port) must be fitted and set to **ON** to enable the RS-232 transceiver. No additional jumpers are required.

RS-232

Connect a Null-Modem cable between the RS-232 port on the board and an additional serial port on the PC. There is only one serial port on the ML323. This is used to connect to the PC. J52 must be fitted and set to **ON** to enable the transceiver.

LEDs

The LEDs on the boards indicate the basic status of the platform at a glance. Detailed information is available using the GUI. Table 7 defines the LED functions.

Table 7: **LED Indications for ML323 Tri-Mode MAC Demo**

LED	Tri-Mode Function
DS29	MAC Speed 10 Mbps
DS28	MAC Speed 100 Mbps
DS23	MAC Speed 1 Gbps
DS18	FIFO loopback selected
DS19	Address swap enabled
DS20	GMII loopback

Using the PHY Daughter Card

A PHY daughter card is available (HW-AFX-BERG-EPHY) for the ML323 board. The card contains a Marvell Tri-speed PHY. The leftmost PHY is the active device for the demonstration, that is, the PHY on the same side as the jumpers described below. The PHY should be configured to operate with an RGMII interface by setting jumper connections on the card as follows:

J5 = 1-2, 3-4, 7-8

J6 = 3-4, 7-8

J7 = 7-8

J10 = 1-2

This configures the device for RGMII operation as discussed in the PHY daughter card data sheet. For more information, see:

- http://www.xilinx.com/products/boards/ug_phy_daughter_card.pdf
- http://www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=HW-AFX-BERG-EPHY.

A 1-Gigabit compatible RJ45 patch lead should be connected to the leftmost PHY on the Daughter Card. A crossover cable is required for direct connection to another Gigabit Ethernet device, else a normal cable should be used for connection to a Gigabit Hub.

ML401 & ML403 Configuration for Tri-Mode Ethernet MAC Demo

Power Supply

The ML401/403 should be powered from the 5V jack input.

Clock Selection

The demonstration platform uses the on-board 100 MHz oscillator, X1 SYSCLK, as a master reference to generate all the clocks required for the design.

Jumper Settings

No jumpers are required on the board.

RS-232

Connect a Null-Modem cable between the RS-232 port on the board, labelled UART Host, and an additional serial port on the PC. This is used to connect to the PC.

LEDs

The LEDs on the boards indicate the basic status of the platform at a glance. Detailed information is available using the GUI. Table 8 defines the LED functions.

Table 8: **LED Indications for ML401 & ML403 Tri-Mode Demo**

LED	Tri-Mode Function
GPIO LED 0	MAC Speed 10 Mbps
GPIO LED 1	MAC Speed 100 Mbps
GPIO LED 2	MAC Speed 1 Gbps
LED East	FIFO loopback selected
LED South	Address swap enabled
LED West	GMII loopback

On-board Tri-Speed PHY

The ML401 and ML403 boards have a Marvell Tri-speed PHY built onto the boards. This is connected to the MAC in the demonstration platform. A 1-Gigabit compatible RJ45 patch lead should be connected to the PHY. A crossover cable is required for direct connection to another Gigabit Ethernet device, else a normal cable should be used for connection to a Gigabit Hub.

ML403 Configuration for the Embedded Tri-Mode Ethernet MAC Demo

Power Supply

The ML403 should be powered from the 5V jack input.

Clock Selection

The demonstration platform uses the on-board 100 MHz oscillator, X1 SYSCLK, as a master reference to generate all the clocks required for the design.

Jumper Settings

No jumpers are required on the board.

RS-232

Connect a Null-Modem cable between the RS-232 port on the board, labelled UART Host, and an additional serial port on the PC. This is used to connect to the PC.

LEDs

The LEDs on the boards indicate the basic status of the platform at a glance. Detailed information is available using the GUI. Table 9 defines the LED functions.

Table 9: **LED Indications for ML403 Embedded Tri-Mode Demo**

LED	Tri-Mode Function
GPIO LED 0	MAC Speed 10 Mbps
GPIO LED 1	MAC Speed 100 Mbps
GPIO LED 2	MAC Speed 1 Gbps
LED East	FIFO loopback selected
LED South	Address swap enabled
LED West	GMII loopback

On-board Tri-Speed PHY

The ML403 board has a Marvell Tri-speed PHY built onto the boards. This is connected to the MAC in the demonstration platform. A 1-Gigabit compatible RJ45 patch lead should be connected to the PHY. A crossover cable is required for direct connection to another Gigabit Ethernet device, else a normal cable should be used for connection to a Gigabit Hub.

FPGA Configuration

The FPGA must be configured with one of the bitfiles included with the Application Note source files. The following bitfiles can be found in the implement folder.

```
   xgm_hdp_top_ML310.bit  : 10-Gigabit design for ML310 board
xgm_hdp_top_ML323_20.bit  : 10-Gigabit design for ML323 fitted with xc2vp20 FPGA
xgm_hdp_top_ML323_50.bit  : 10-Gigabit design for ML323 fitted with xc2vp50 FPGA
   gig_hdp_top_ML310.bit  : 1-Gigabit design for ML310 board
gig_hdp_top_ML323_20.bit  : 1-Gigabit design for ML323 board fitted with xc2vp20 FPGA
gig_hdp_top_ML323_50.bit  : 1-Gigabit design for ML323 board fitted with xc2vp50 FPGA
   tri_hdp_top_ML310.bit  : Tri-Mode design for ML310 board
tri_hdp_top_ML323_20.bit  : Tri-Mode design for ML323 fitted with xc2vp20 FPGA
tri_hdp_top_ML323_50.bit  : Tri-Mode design for ML323 fitted with xc2vp50 FPGA
   tri_hdp_top_ML401.bit  : Tri-Mode design for ML401 board
   tri_hdp_top_ML403.bit  : Tri-Mode design for ML403 board
  emac_hdp_top_ML403.bit  : Embedded Tri-Mode design for ML403 board
```

The FPGA can be configured using the SystemACE or JTAG.

SystemACE

SystemAce files for each of the bitfiles listed above are included in the implement folder. Select the correct folder for the design using the same naming convention as above (for example, implement/systemace_tri_ML310 contains the Tri-Mode design for the ML310). Copy the contents of this folder onto a compact flash card and insert the card into the CF card slot. The SystemACE address DIP switches should be set to "000". The device will be configured from the SystemACE file on power-up.

JTAG

After connecting the appropriate cable to the JTAG header (see board documentation), the appropriate bitfile from the list above should be loaded onto the FPGA using Impact or Chipscope. These bitfiles can be found in the implement folder.

Graphical User Interface

The GUI application allows the user to control the Ethernet MAC core in the demonstration and the other components within the design. The GUI has three screens: the Serial Port Selection screen, displayed on startup; the Main screen, displayed after the Serial Port Selection screen; and the MAC Statistics Screen, which can be displayed alongside the main screen.

Installation

Extract the project files from the Application Note zip file into a new directory on the PC (for example, `c:\mac_hdp`).

Note: Do not download the demonstration platform to a directory path containing spaces. This will cause errors when running the GUI.

After loading the hardware design onto the FPGA, run the GUI by navigating to the directory `c:\mac_hdp\code\pc\rtf\` (if you saved the zip file contents to `c:\mac_hdp`) and double clicking on `mac_hdp.exe`.

Serial (COM) Port Selection

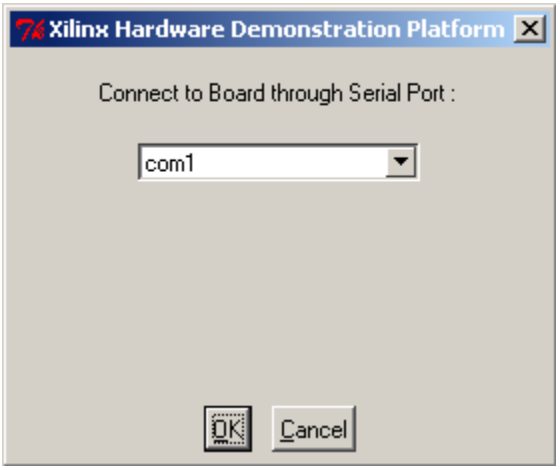

Figure 6: **Serial (COM) Port Selection Screen**

Figure 6 displays the Serial Port selection dialog box, the first screen displayed when the GUI is run. This option lets the user select the COM port used to communicate with the board. Select the correct COM port, click OK and wait for the link to be established with the board. After the connection, the main GUI screen is displayed.

If a link is established with the board, the board type and the MAC type are displayed at the bottom of the screen.

If a connection to the board cannot be established, an error message appears at the bottom of the main screen. Check that the board is switched on, the FPGA is configured with the correct bitfile, the serial cable is connected and is the correct type, and then restart the GUI.

If a link is established with the board then the board type and the MAC type are displayed at the bottom of the main GUI screen.

Main Screen

Figure 7 displays the primary GUI screen, which consists of four sections:

Main Menu Bar (Top of Main Screen)

A standard Windows menu.

Control Pane (Leftmost Pane)

The Control Pane provides several tabs that allow the user to control different parts of the design. The XGMAC and TEMAC cores have different configuration settings, reflected by different tabs on the Control pane.

Tabs common to all platforms:

- Welcome
- MAC Configuration
- Platform Configuration
- Read Rx FIFO
- Frame Editor

Tabs available for the TEMAC and EMAC demo only: Address Filtering

Tabs available for the XGMAC and GEMAC demo only: PHY Control

Help Pane (Rightmost Pane)

Displays context-sensitive help.

Message Pane (Bottom Pane)

Displays debug and status messages.

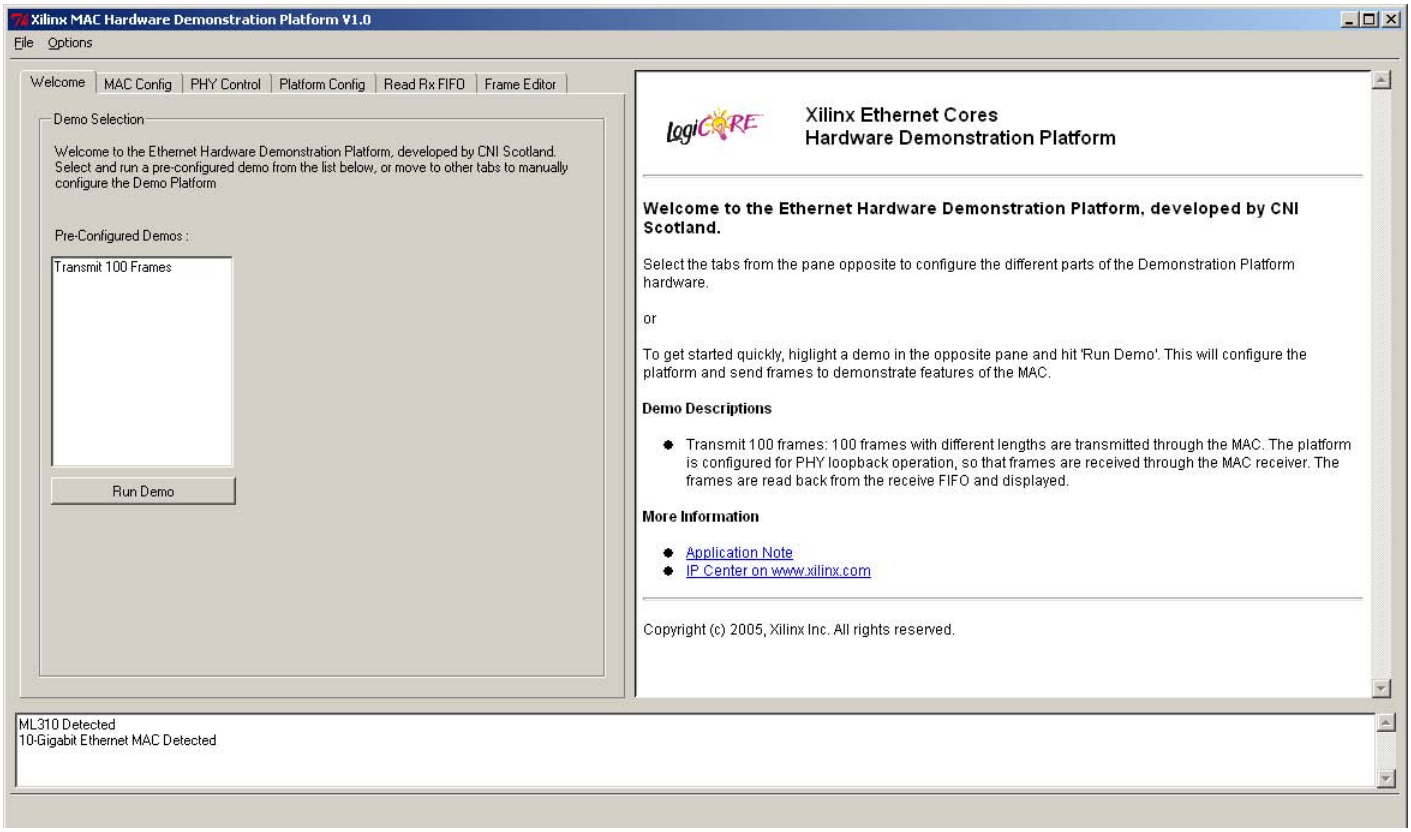

Figure 7: **Main GUI Window**

Welcome Tab

Figure 8 displays the Welcome tab, the first tab displayed when the application starts (after the COM port is selected). This tab can be used to run pre-configured demos. (Available pre-configured demos are determined by the hardware demo connected.)

To run a demo, select it from the list and click **Run Demo**. After the demo is complete a message appears in the message pane.

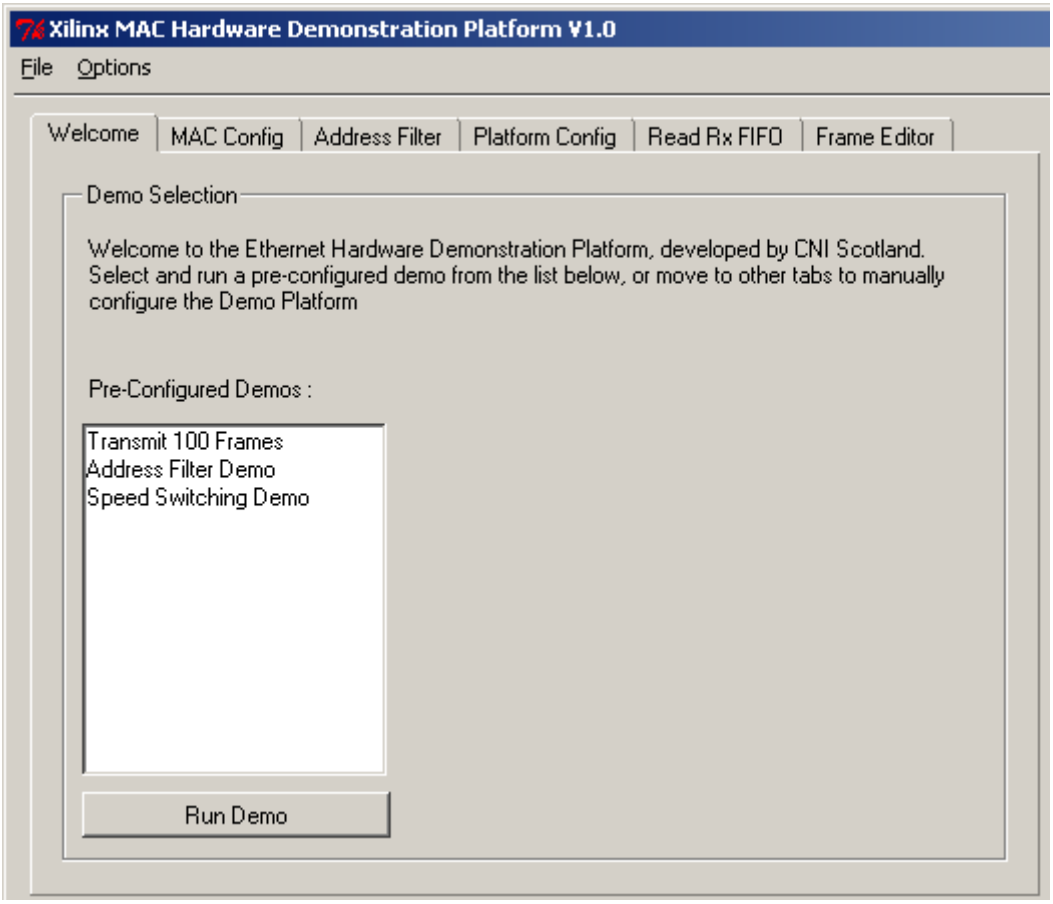

Figure 8: **Welcome Tab for TEMAC Demo**

Demos available for the TEMAC platform:

- Transmit 100 Frames
- Speed Switching Demo
- Address Filter Demo

Demos available for the EMAC platform:

- Transmit 100 Frames
- Address Filter Demo

Demo available for the XGMAC and GEMAC platform:

- Transmit 100 Frames

MAC Configuration Tab

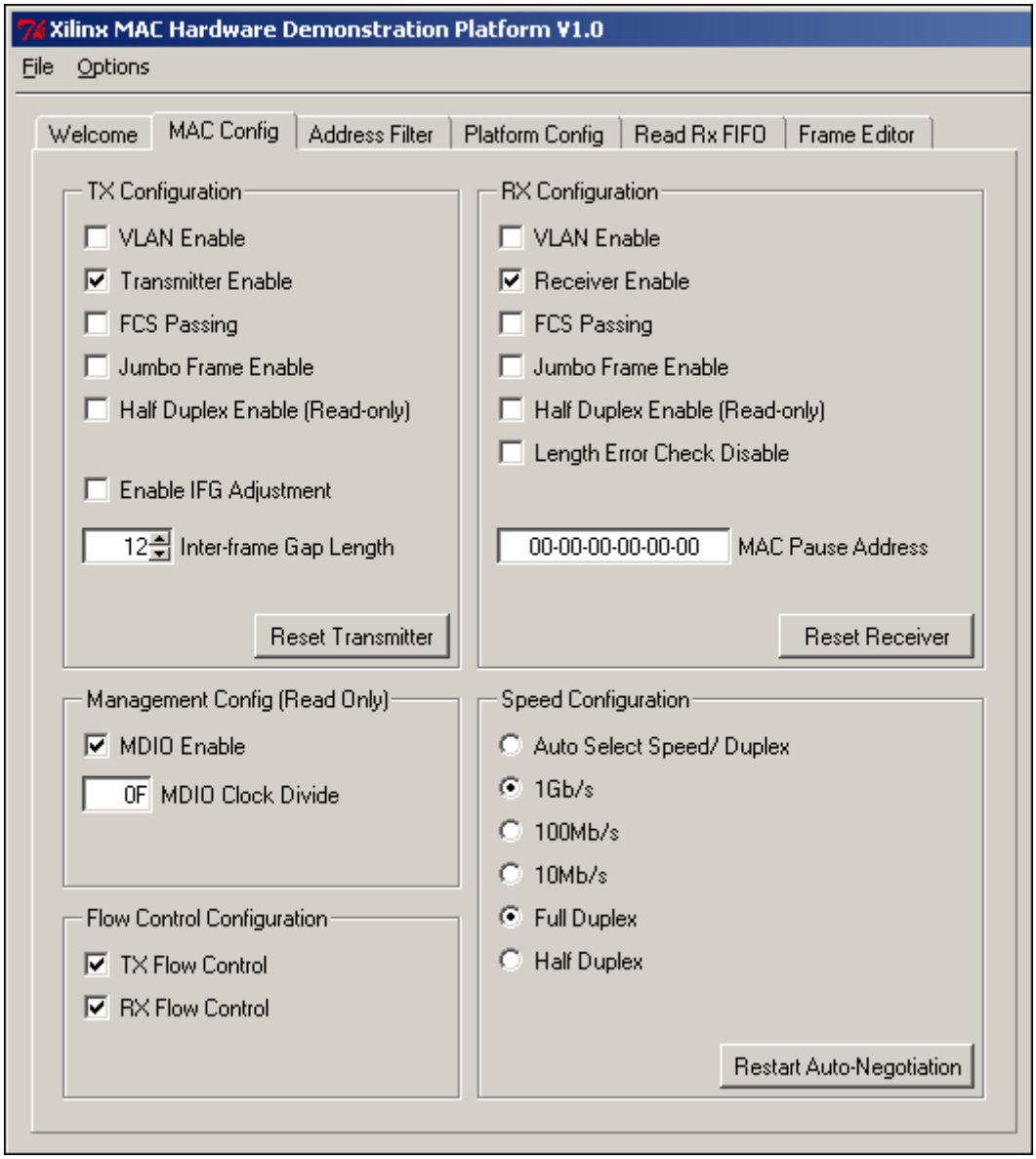

Figure 9: **MAC Configuration Tab for TEMAC Demo**

Figure 9 shows the MAC Configuration tab for the TEMAC demo. The MAC Configuration tab provides the user access to the configurable features of the MAC cores. When the FPGA is configured, this screen displays the default configuration for the MAC core.

The transmitter and receiver configurations can be modified by the user to observe different configuration behaviors. The MAC configuration for transmitter and receiver can be reset to the default values by using the **Reset Transmitter** and **Reset Receiver** buttons.

The management configuration for the MDIO interface cannot be modified from the GUI, as these settings are configured correctly to allow the hardware to control the PHY or MGT. The management configuration is set by the embedded processor software, which writes to the management configuration of the MAC on startup.

Flow Control configuration can be set by the user, allowing observation of the flow control functionality.

Speed Configuration: Tri-Mode Ethernet MAC Demo Only

The speed configuration for the TEMAC demonstration does not give direct access to the speed registers in the MAC core; the user selects different speeds for operation.

The method used to configure speed is dependent on whether a 1000/100/10BaseT PHY is being used.

Loopback Mode

When the GMII interface is set into loopback mode (see "Platform Configuration Tab," page 29), or no PHY is connected to the demonstration, do the following to configure speed.

1. Select either **Auto Select Speed/Duplex** to use the MAC core at the fastest speed, or select a specific speed and duplex combination.
2. Click **Restart Auto-Negotiation**. The GUI speed/duplex options will be deasserted until the MAC has been configured for the new speed.

As no PHY is in use, only the speed configuration registers in the MAC core are changed. Once the MAC is configured for the new speed, the GUI speed/duplex options will be reasserted to show the operating speed/duplex.

Note: As the physical side is being looped back, only full-duplex operation can be used. Any attempt to set the mode to half-duplex will fail.

External Device Mode

When an external PHY is being used and the physical interface is selected to use the external device, follow the steps below to configure speed:

1. Select either **Auto Select Speed/Duplex** to use the MAC core at the fastest speed, or select a specific speed and duplex combination.
2. Click **Restart Auto-Negotiation**. The GUI speed/duplex options will be deasserted until the MAC has been configured for the new speed.

The command forces the PHY to advertise all speed/duplex combinations, in the case of using **Auto-Select**; or to advertise only the requested speed/duplex combination. The PHY is then set to restart **Auto-Negotiation** with the external device.

After **Auto-Negotiation** is complete, the demonstration platform reads the PHY registers to determine the link speed/duplex and then appropriately configures the MAC core. The GUI speed/duplex options will be reasserted to show the operating speed/duplex.

If an error occurs in **Auto-Negotiation**, it will be reported in the message pane.

Note: If the link to the external device goes down at any time, the GUI speed/duplex options disappear from the speed configuration and return when the link is re-established.

Speed Configuration: Embedded Tri-Mode Ethernet MAC Demo Only

The speed configuration for the EMAC demonstration does not give direct access to the speed registers in the MAC core; the user selects different speeds for operation.

The method used to configure speed is dependent on whether a 1000/100/10BaseT PHY is being used.

Loopback Mode

When the GMII interface is set into loopback mode (see "Platform Configuration Tab," page 29), or no PHY is connected to the demonstration, the MAC will always operate in 1 Gpbs Full-Duplex mode. This is necessary as the PHY determines the mii_tx_clk input speed from the external line speed.

External Device Mode

When an external PHY is being used and the physical interface is selected to use the external device, do the following to configure speed:

1. Select either **Auto Select Speed/Duplex** to use the MAC core at the fastest speed, or select a specific speed and duplex combination.
2. Click **Restart Auto-Negotiation**. The GUI speed/duplex options will be deasserted until the MAC has been configured for the new speed.

The command forces the PHY to advertise all speed/duplex combinations, in the case of using **Auto-Select**; or to advertise only the requested speed/duplex combination. The PHY is then set to restart **Auto-Negotiation** with the external device.

After **Auto-Negotiation** is complete, the demonstration platform reads the PHY registers to determine the link speed/duplex and then appropriately configures the MAC core. The GUI speed/duplex options will be reasserted to show the operating speed/duplex.

If an error occurs in **Auto-Negotiation**, it will be reported in the message pane.

Note: If the link to the external device goes down at any time, the GUI speed/duplex options disappear from the speed configuration and return when the link is re-established.

Address Filter Tab (TEMAC Demo and EMAC Demo Only)

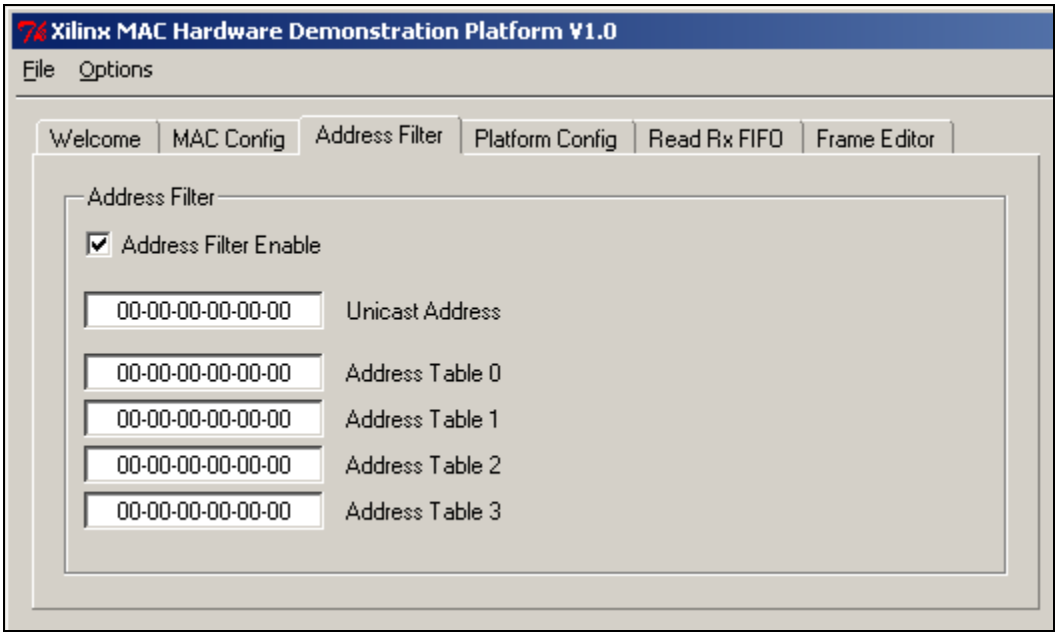

Figure 10: **Address Filter Tab**

Figure 10 displays the Address Filter tab, used to control address filtering on the receiver of the TEMAC or EMAC core. From this tab, address filtering can be enabled or disabled and addresses can be written into the table in Hex.

If an external device is connected to the demonstration platform, to receive frames from the device the address filter must be configured with the MAC address of that device, or address filtering should be disabled.

If loopback is selected, the address filter should be configured with the address set in the frame editor, the destination address used by the pattern generator (11-22-33-44-55-66) or disabled.

The statistics counters only count frames received with valid addresses, however, the counter **Bytes Received** increments for all frames, with or without valid addresses.

PHY Control Tab (10-Gigabit Ethernet MAC Demo)

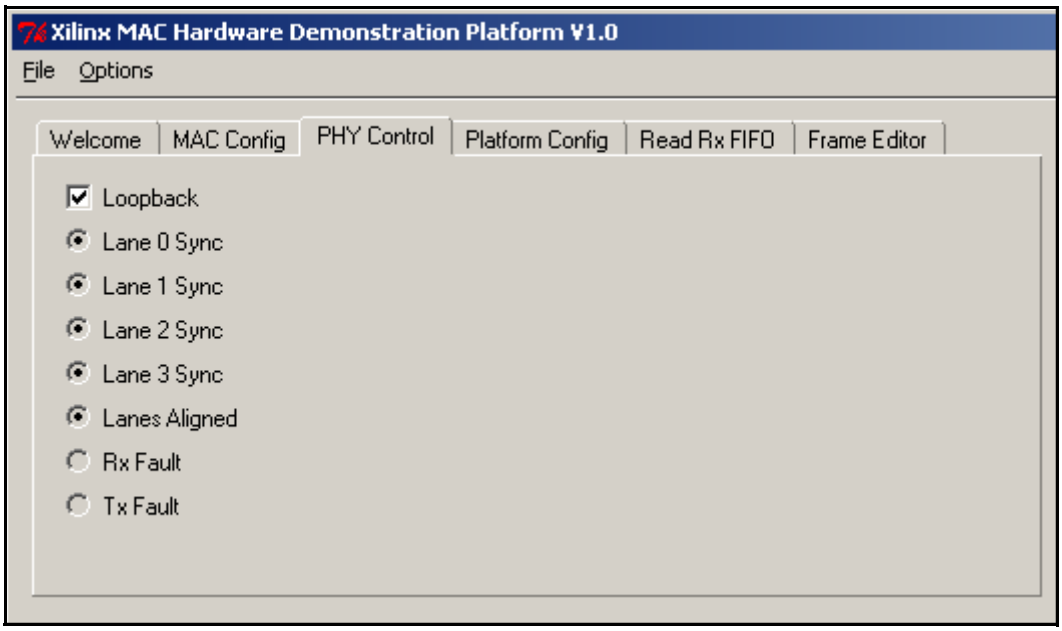

Figure 11: **PHY Control Tab for XGMAC Demo**

Figure 11 displays the PHY control tab, which is only available if the XGMAC core is detected. This tab displays the information gathered by the MAC core about the PHY (XAUI) using the MDIO. The only item that can be configured is loopback which sets the XAUI loopback register so the demo can be used without a PHY card. The other fields give status information about the four XAUI lanes. All lanes should be synchronized and the lanes should be aligned. If there is no PHY card connected to the board (or no SMA XAUI device connected to the ML323), the lanes will not synchronize and align until loopback is enabled. A Rx Fault condition will be indicated if the lanes do not align.

PHY Control Tab (1-Gigabit Ethernet MAC Demo)

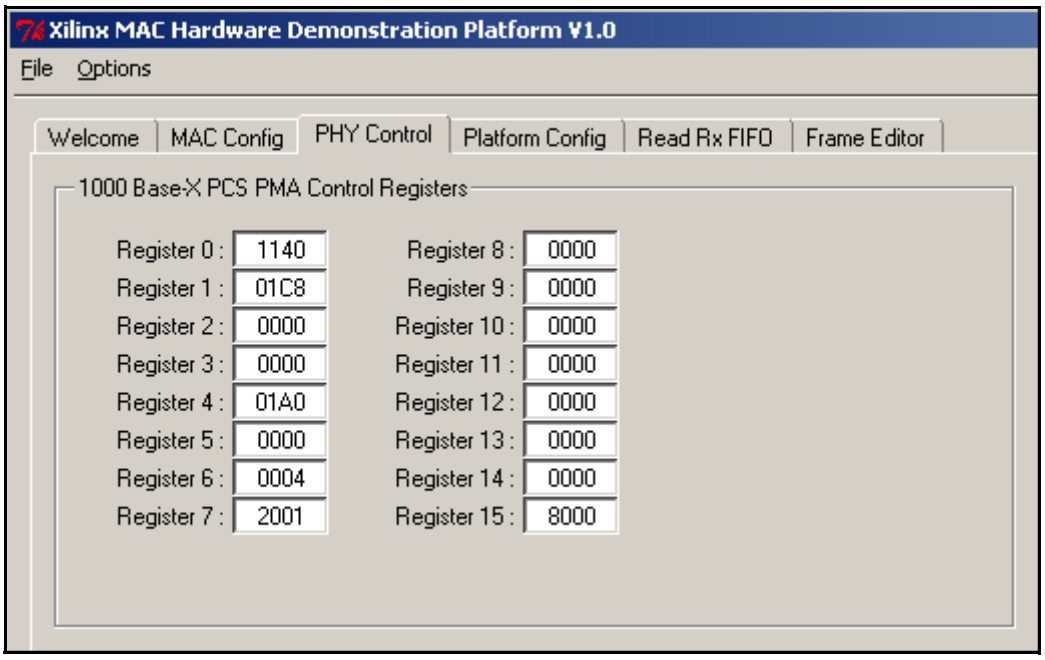

Figure 12: **PHY Control Tab for GEMAC Demo**

Figure 12 shows the PHY control tab, which is only available if the GEMAC core is detected. This tab displays the 1000 Base-X PCS PMA core register values [15:0] in hexadecimal. The register values are read through the MAC host interface using the MDIO. Register descriptions can be found in the 1000 Base-X PCS PMA core user guide.

Of most interest to the user in this demonstration are Register 0, the control register and Register 1, the status register. Register 0 bit 14 sets the PCS PMA core into loopback and this bit is set by the GUI when the platform is set to use loopback at the physical interface, see "Receiver Data Source," page 30. Register 1 bit 5 indicates when auto-negotiation is complete. When using the platform with external mode, this will indicate whether the optic link is ready to operate.

Platform Configuration Tab

Figure 13 shows the Platform Configuration tab, which controls the data sources in the demonstration platform.

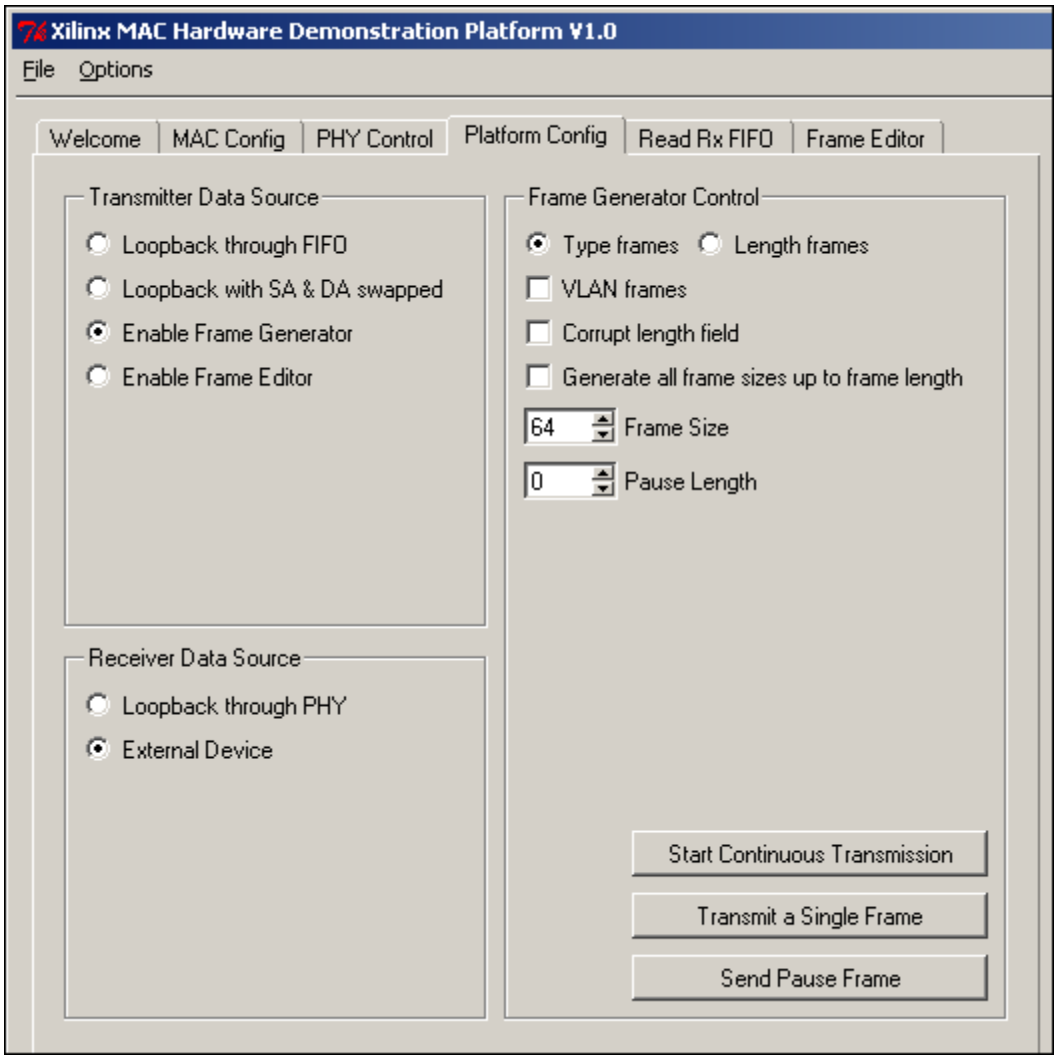

Figure 13: **Platform Configuration Tab**

Transmitter Data Source

The client side transmitter interface of the MAC can be connected to one of three data sources. Loopback (and Loopback with destination address (DA) and source address (SA) swapped) simply connects the data path from the MAC client side receiver to the transmit path. Data passes from the MAC receiver to the receive FIFO, then directly to the transmit FIFO and finally to the MAC transmitter. If SA and DA swapping is selected, the first 6 bytes of each frame are switched with the following 6 bytes, switching source and destination address. This allows an external device to send frames to the demonstration platform and receive correctly addressed frames back.

Enable Frame Generator connects the transmit FIFO to the hardware pattern generator. Options for controlling the pattern generator are also set in this tab and are described in "Frame Generator Control."

Enable Frame Editor connects the transmit FIFO to the RAM based frame editor, which allows the user to enter and transmit any frame using the GUI. The Frame Editor is controlled in the Frame Editor tab, see "Frame Editor Tab," page 32.

Receiver Data Source

The receiver can be configured for loopback at the physical interface or connected to an external device. If loopback through PHY or loopback at GMII interface is selected, the transmitter is connected to the receiver, through the PHY or physical interface logic. The method of connecting transmit to receive varies depending on the MAC type. If the TEMAC core is used, the GMII output of the transmitter is connected directly to the GMII input of the receiver. If the XGMAC core is used, the MDIO is used to request loopback at the MGT used by the XAUI (this has the same effect as setting loopback in the PHY control pane).

Frame Generator Control

The Frame Generator can generate various frame types and lengths, as described below.

Type frames: When checked, the pattern generator inserts hex 0800 in the length/type field of each frame.

Length frames: When checked, the pattern generator inserts the length of the data contained in each frame into the length/type field of each frame.

VLAN frames: When enabled, the pattern generator inserts a VLAN tag into each frame. The total length of each frame is unchanged but the length field is adjusted to indicate less data in each frame.

Corrupt length field: When selected, the length field is set incorrectly, giving an errored frame.

Generate all frame sizes up to frame length: When checked, the pattern generator will start transmitting 19-byte frames (padded by the MAC core) and increase the length of the frame by 1-byte. Once the length is equal to the length selected in the Frame Length box, the length is set back to 19 and the process repeats. Use this option when transmitting frames continuously.

Frame Size: Set the total size for frames sent to the transmitter. If this is less than 60, the MAC core will pad the frame unless configured for FCS passing.

Pause Length: Set the 16-bit pause length input to the MAC core, which is used if **Send Pause Frame** is selected. See the specific MAC user guide for a description of the pause transmission mechanism.

The buttons at the bottom of this section of the GUI are used to send frames to the MAC transmitter. These buttons trigger transmission by the pattern generator. **Transmit a Single Frame** enables one-shot mode in which a single frame is sent. **Start Continuous Transmission** sends frames to the MAC until the same button, now displaying **Stop Transmission** is clicked. A single pause frame can be sent from the MAC by clicking **Send Pause Frame**, which asserts the pause request input to the MAC. The Transmitter Data Source must be set to **Enable Frame Generator** to enable these buttons.

Read Rx FIFO Tab

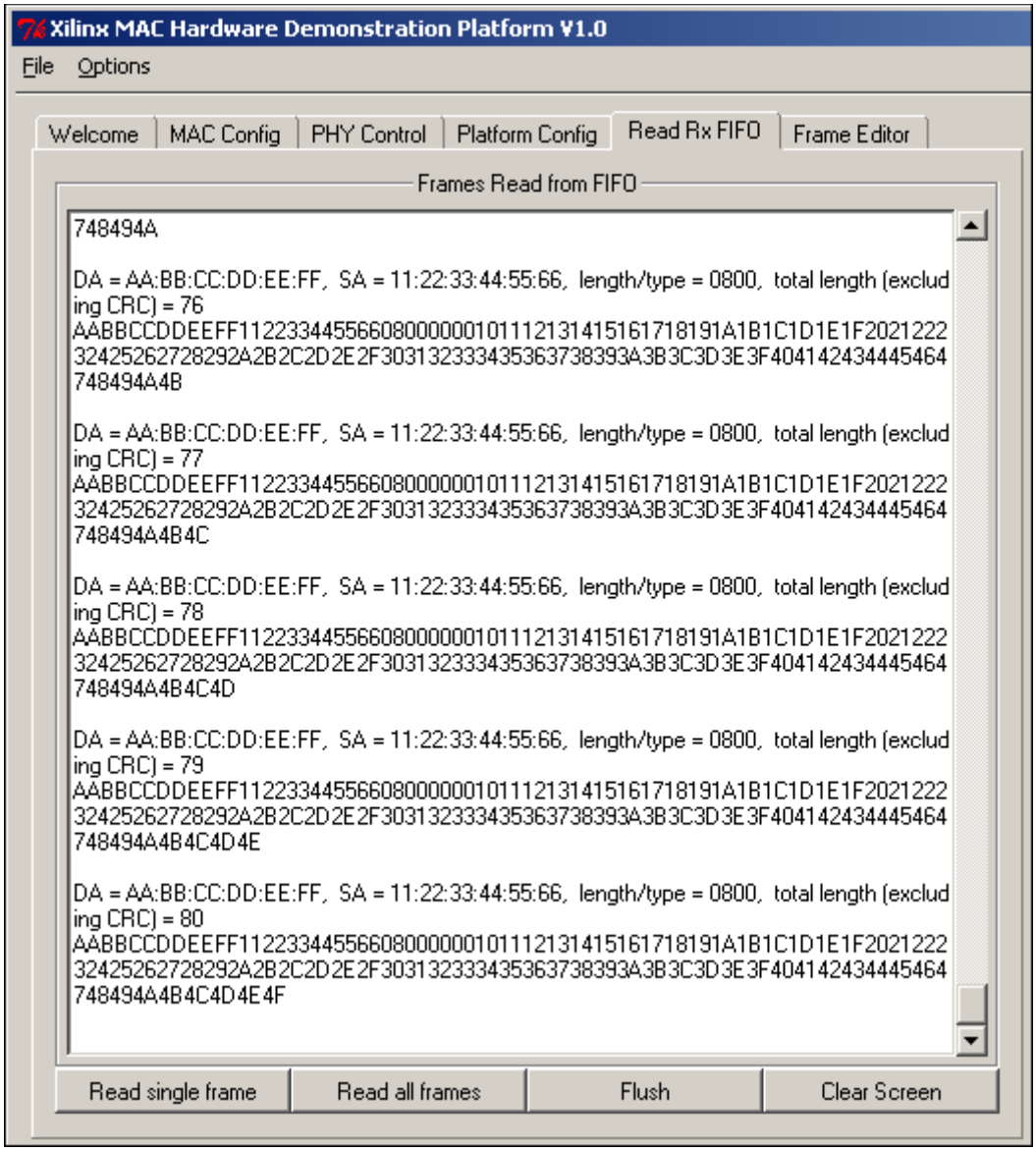

Figure 14: **Read Receive FIFO Tab**

Figure 14 shows the Read Rx FIFO tab, used to read frames from the receive side FIFO received by the MAC core. The FIFO cannot be read if the platform is configured for loopback through the FIFO.

The FIFO stores all frames received from the MAC core, until it is full. Once full, the FIFO will discard further incoming frames. The FIFO is 16 Kbytes deep so can store approximately 10 frames of 1518 bytes. The exception to this is the TEMAC demo on ML403 board, which has a much smaller receive side FIFO.

Care should be taken when mixing frame sizes. If the FIFO is nearing full and a frame larger than the remaining space is received, it will be discarded. If the next frame is smaller than the remaining space, it will be stored in the FIFO. This situation should not be confused with frame loss.

To read frames from the receive FIFO it is advisable to flush the FIFO before initiating transmission. This ensures that the FIFO has space to store the new frames. After transmission is started, the FIFO can be read. During continuous reception of frames, a snapshot of the data

can be captured by flushing the FIFO, which will cause it to discard any stored frames, and store the next 16 kBytes of frame data received. The user can read a single frame or all available frames.

During continuous reception, the FIFO is unlikely to empty because data can enter the FIFO at a much faster rate than can be transmitted across the serial link to the GUI. To prevent an endless upload of frames to the GUI, a maximum of 64 frames can be read at once. To read more frames, continue to use the **Read all frames** button.

Frame Editor Tab

The Frame Editor tab is used to load frames into the RAM in the Pattern Generator, which can then be sent to the MAC core for transmission. To enable this functionality, the Transmitter Data Source in the Platform Config tab should be set to **Enable Frame Editor**.

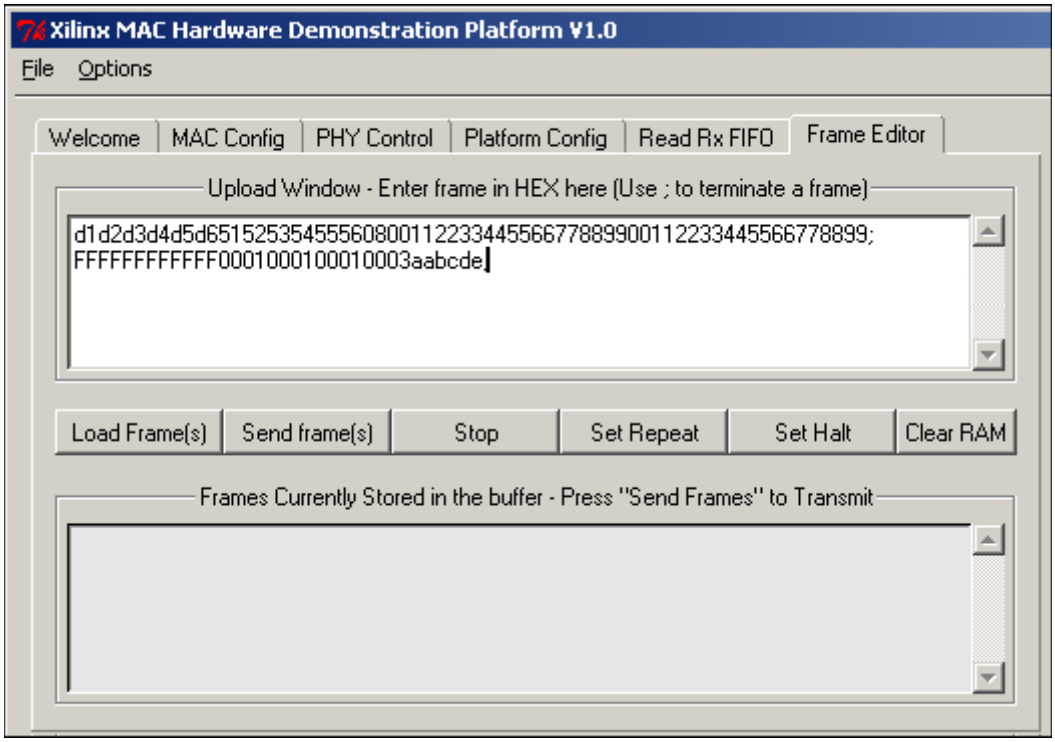

Figure 15: **Frame Edit Tab: Data Entry**

Frame data should be entered in hex in the top window as shown in Figure 15. Multiple frames can be entered and uploaded at the same time.

The syntax for entering frames is as follows:

a. White space and CR/LF characters are ignored
b. Data must only contain the characters 01234567890ABCDEFabcdef
c. Each frame must be terminated with a semicolon
d. Each frame must have an even number of characters (nibbles)

Example valid frames:

```
1122334455667788990OAAbbCCddEE;
1 2 3 4 5 6 7 8;11223344; 2 35556;
```

Example invalid frames:

```
123456789; - uneven number of nibbles will give a warning
11223344rt56; - invalid hex characters
```

Example mistakes:

```
1122334455667788990O
12345678123456789012;
```

The input will be treated as a single frame. The carriage return character is not treated as a frame terminate character.

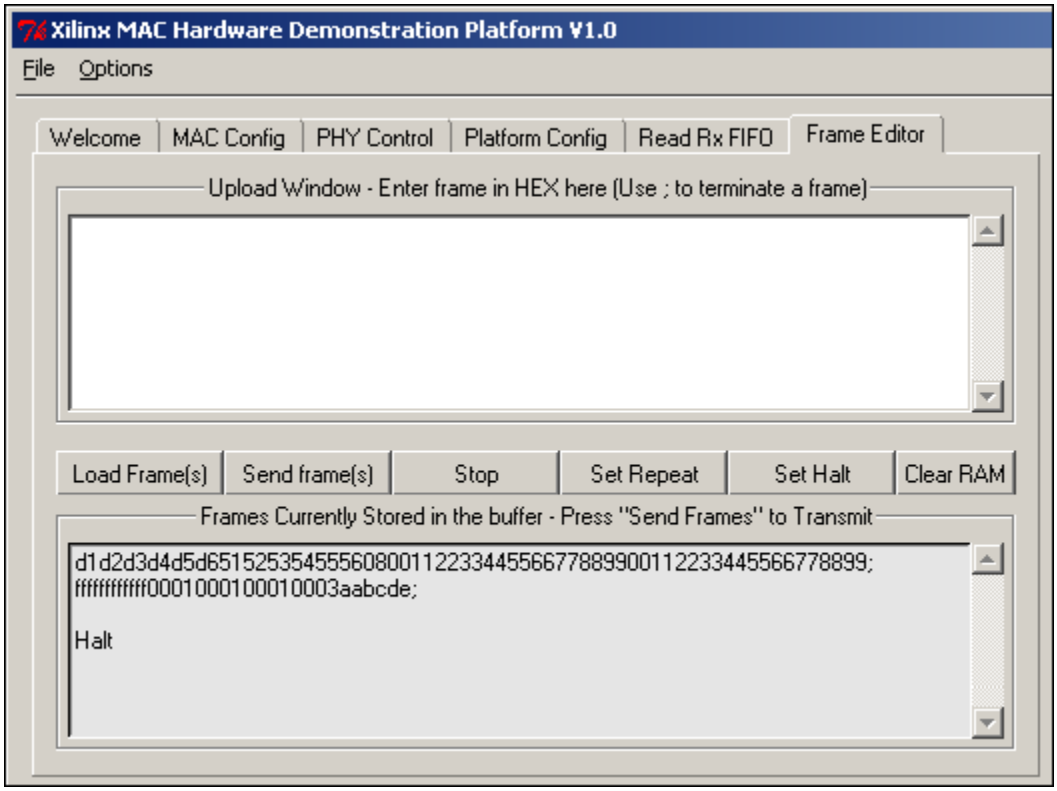

Figure 16: **Frame Edit Tab: Buffer Display**

Clicking on **Load Frames(s)** loads frames into the RAM as shown in Figure 16. When an error is detected on an entered frame, this will be highlighted to the user and the frame will remain in the upload window. If the user enters three frames and the first two are valid but the third is invalid, the first two will be uploaded and the third will remain in the edit window. If an error occurs in the first frame, all three frames will remain in the upload window.

The control **Set Repeat** can be used to request continuous transmission of frames, by continuously looping through all the frames in the RAM. The control **Set Halt** can be used to request that frames in the RAM are only sent once. The button **Send frames** is used to start sending frames to the MAC core and the **Stop** button is used to stop transmission of frames to the MAC core.

MAC Statistics

To view the statistics collected by the demonstration platform, select **Options -> Show Stats**. This option opens a new window displaying statistic counter values, collected either by the XGMAC statistic counters for XGMAC demo, the GEMAC statistic counters for GEMAC demo, or by the Ethernet Statistics core for the TEMAC and EMAC demos. Figure 17 shows this window for the TEMAC demo.

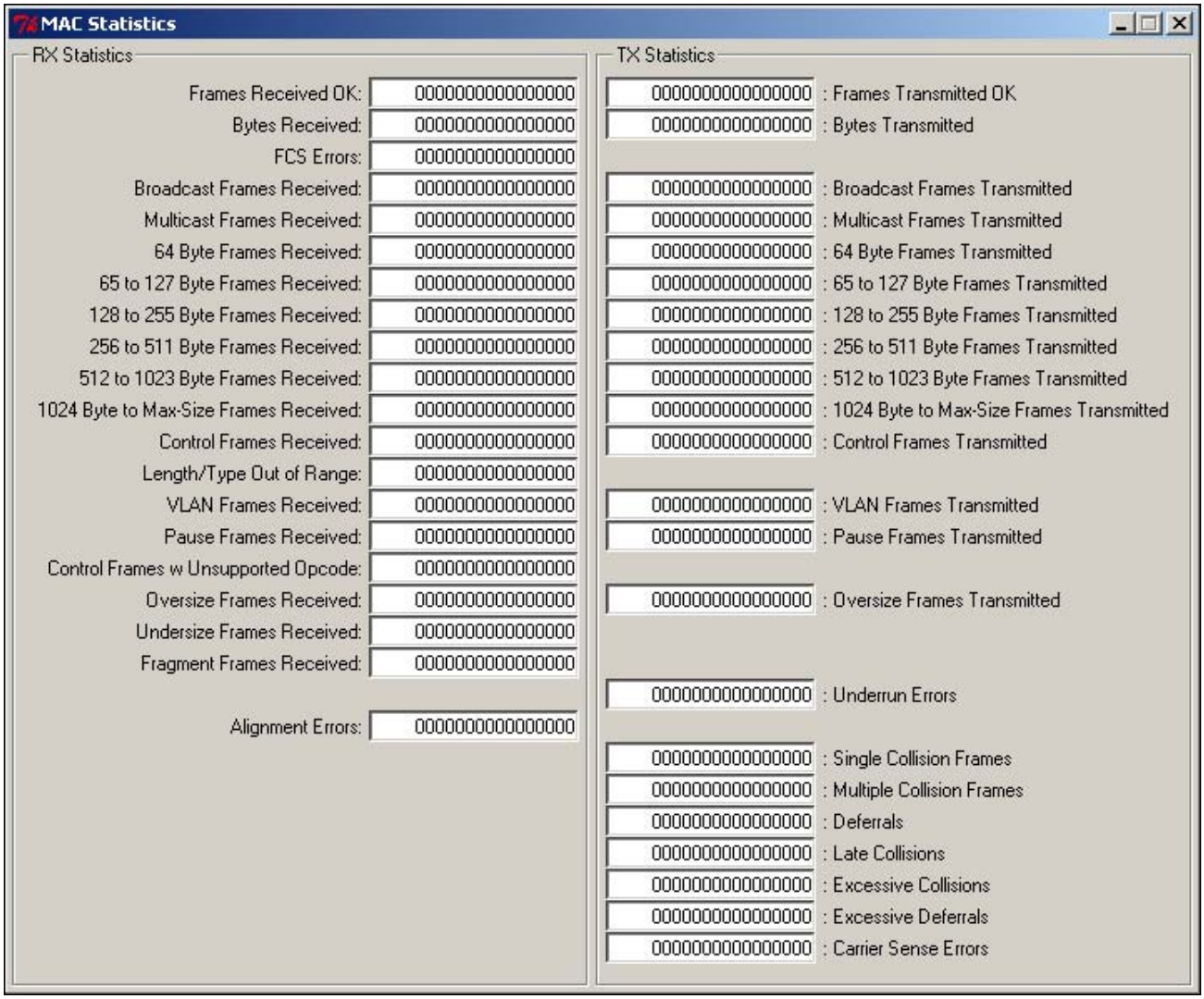

Figure 17: **Statistics Window for TEMAC Demo**

Building the Hardware

Ready-to-use bitfiles and SystemACE files are provided. HDL source code and support files are also provided for the project. This allows the user to regenerate programming files if changes are made to the hardware design. This section describes how to recreate the programming files for one or all board/MAC combinations.

Source Code Directory Structure

The two main components of the hardware design are

- An EDK subsystem containing the PowerPC/MicroBlaze peripherals and software.
- An RTL-based project containing the MAC core and board specific logic.

Figure 18 shows the organization of the source code directories. The EDK system is built using RTL from the `edk` directory. The libraries which are provided by the EDK installation are not included in the zip file. The top-level RTL is contained in the `hdl` directory and the MAC and ChipScope netlists are in the `netlist` directory.

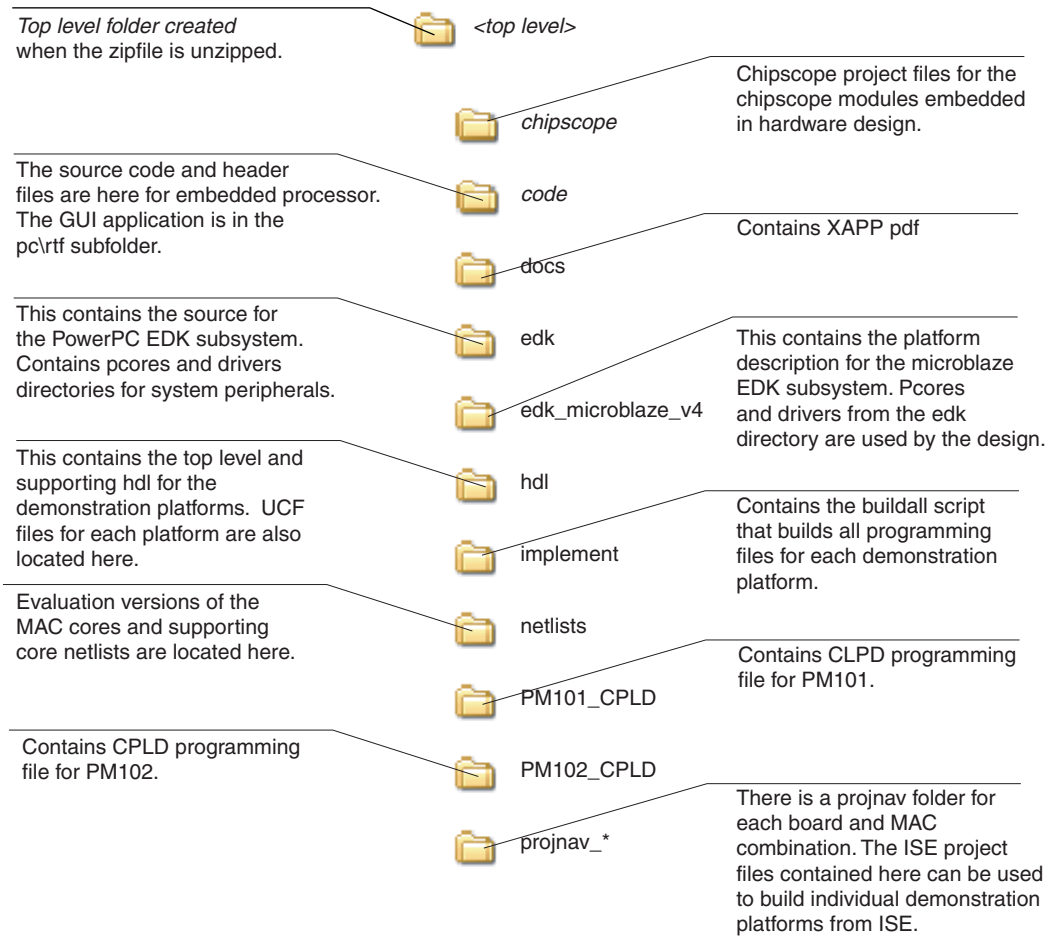

Figure 18: **Source Code Directories**

Building All Demonstration Platforms

A script is provided which builds all the demonstration bitfiles and SystemACE files without user intervention. First, the EDK system is built and then the Xilinx implementation tools are run for each MAC/board combination in turn. The output is created in the `implement` directory along with a logfile for each project. The SystemACE folders for each MAC/board combination are also created in the `implement` directory.

The script must be run on a Windows 2000/XP machine with Xilinx ISE 7.1i or later and Xilinx EDK 7.1 or later installed. Hardware Evaluation or bought licenses must be installed on the machine for each of the cores in the designs.

To run the script:

1) Open a Windows Command Prompt and navigate to the folder created when the .zip file is unzipped.

2) Change to the `implement` folder (`c:\mac_hdp> cd implement`)

3) Run `buildall.bat` script with required options

```
c:\mac_hdp\implement> buildall <edk_options> <platform_options>
```

<edk_options> for running the script are:

- `"noedk"`, to skip the edk implementation, (use only if the script has run previously) .

- "ppc", to build only the ppc based EDK project, (the XGMAC and GEMAC demos use only the ppc based project).
- "mb", to build only the microblaze based EDK project, (the EMAC demo uses only the microblaze based project).
- "all", to build both EDK projects, (the TEMAC demos use both EDK projects).

<platform_options> for running the script are:

- "xgm", to build all XGMAC demo platforms
- "gig", to build all GEMAC demo platforms
- "tri", to build all TEMAC demo platforms
- "emac", to build all EMAC
- "all", to build all demo platforms

Note: The script may take several hours to run depending on the speed of the PC.

Building Single Bitfiles

It is assumed that the user is familiar with both EDK and ISE project flows if this method is selected. Xilinx ISE 7.1i or later and Xilinx EDK 7.1 or later should be installed. Hardware Evaluation or bought licenses must be installed for each of the cores used in the design.

If using a Virtex-4 based demo for the ML401 or ML403 boards, the MicroBlaze system must be built. Open the XPS project, `system.xmp`, from the `edk_microblaze_v4` directory using EDK.

If using any other board, the PPC system must be built. Open the XPS project, `system.xmp`, from the `edk` directory using EDK.

From within XPS, build the netlist for the microprocessor system (`Tools ->Generate netlist`) followed by the embedded software (`Tools ->Build All User Applications`). When the build is complete, close the XPS.

There is a ISE project for each board/MAC combination. Each project is in an individual folder with the name `projnav_<MAC type>_<board type>`. Open ISE Project Navigator and open the project file (`system.ise`) from the appropriate folder. Once the project is open, select the top-level `<MAC type>_hdp_top.vhd` and build the platform by double-clicking on `Generate Programming file` in the Process view window. All search paths, including paths to the EDK components are already set in the project. When the build has finished, the new .bit file can be found in the `projnav_<MAC type>_<board type>` folder.

References

[1] *LogiCORE Tri-Mode Ethernet MAC User Guide*, UG138, April 28, 2005

[2] *LogiCORE 10-Gigabit Ethernet MAC User Guide*, UG148, April 28, 2005

[3] *LogiCORE XAUI User Guide*, UG150, September 30, 2004

[3] *LogiCORE 1-Gigabit Ethernet MAC User Guide*, UG144, April 28, 2005

[3] *LogiCORE 1000 Base-X PCS PMA or SGMII User Guide*, UG155, April 28, 2005

[3] *LogiCORE Ethernet Statistics User Guide*, UG170, April28, 2005

[3] *Virtex-4 Embedded Ethernet MAC User Guide*, UG074, November 11, 2004

[4] *ML323 Platform User Guide*, UG033 (v2.1) P/N 0402071, March 19, 2004

[5] *ML310 Overview Setup Guide* from ML310 CD

[6] *ML40x Evaluation Platform User Guide*, UG080, February 28, 2005

Revision History

Date	Version	Revision
07/11/05	1.0	Initial Xilinx release.