Mechanical and Thermal Design Guidelines for Lidless Flip-Chip Packages

Application Note

XAPP1301 (v1.6) February 23, 2021

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/23/2021	1.6	Updated Figure 1-18, Figure 1-19, and Figure 1-20.
09/22/2020	1.5.1	Refined pedestal dimensions in Figure 1-18, Figure 1-19, and Figure 1-20.
07/16/2020	1.5	Added support for lidless XCVU19P FSVA3824 and XCVU23P VSVA1365. Minor updates and modifications.
04/29/2019	1.4	Added support for floating-lid designs throughout document. Added figures, schematics, and relevant information for new devices.
07/02/2018	1.3.1	Updated web description. No technical content changes.
06/08/2018	1.3	Added figures, schematics, and relevant information for new devices. Added Appendix A, Recommended Thermal Solution Installation of Xilinx FCBGA Lidless Packages.
02/28/2018	1.2	Revised text and updated figures throughout document. Minor editorial updates and clarifications.
08/22/2017	1.1	Updated figures.
01/09/2017	1.0	Initial Xilinx release.

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Table of Contents

Revision History 2

Chapter 1: Mechanical and Thermal Design Guidelines

Summary 4
Introduction 4
Lidless Flip-Chip Packages 6
Package Mechanical Specifications 6
Mechanical Support for Testing 7
Thermal Management Strategy 19
Thermal Simulation and the Use of Thermal Models 35
Example Heat Sink Thermal Performance 54
Removing Heat Sink Phase Change Material 56
Measurement Debug 57
Reference Design Files 57
Conclusion 57

Appendix A: Recommended Thermal Solution Installation of Xilinx FCBGA Lidless Packages

Overview 58
Challenges 58
Installation Control 59

Appendix B: Additional Resources and Legal Notices

Xilinx Resources 86
Solution Centers 86
Documentation Navigator and Design Hubs 86
References 87
Please Read: Important Legal Notices 88

Chapter 1

Mechanical and Thermal Design Guidelines

Summary

This application note describes specifications, guidelines, and best practices for using the Virtex® UltraScale+™ and Zynq® UltraScale+ products with the lidless flip-chip device/package combinations listed in Table 1-1, page 5.

Introduction

Changes to the size, performance, and complexity of programmable logic designs and increases in power density warrant new approaches to system thermal management. Xilinx's investment in new packaging technology addresses the need to reduce device thermal resistance, allows for increased power dissipation while in the same thermal environment, without increasing junction temperature. The Virtex UltraScale+ and Zynq UltraScale+ device/package combinations in Table 1-1 have an innovative lidless packaging design that targets the largest Xilinx 16 nm FinFET technology devices, allowing for up to a 10°C cooler operation with the same power dissipation.

For these packages, component thermal management must be carefully designed to obtain optimum device performance and long-term component reliability. Due to the wide range of mechanical designs available for different applications, it is necessary to design system-level thermal simulations that analyze the thermal interaction of the devices using a specific chassis.

To facilitate system-level thermal design and analysis, this application note describes the thermal models of the device/package combinations listed in Table 1-1. These thermal models can be incorporated into system-level thermal models and analyzed using computational fluid dynamics (CFD) simulation software (e.g., Ansys IcePak and Mentor FloTHERM). This application note discusses how the thermal models are created using simulation software packages and how to use these models.

Precise mechanical design is vital to the optimum performance of programmable logic designs. Often, these devices must be subjected to severe mechanical shock and vibration tests. With good mechanical design, these devices can meet the performance stress requirements. In addition, to maintain good contact between heat sinks and the device, innovative designs are implemented for maximum thermal performance.

This application note presents the unique thermal and mechanical designs and requirements for these Virtex UltraScale+ and Zynq UltraScale+ device/package combinations. The reference designs are available in Reference Design Files.

Table 1-1: **Lidless Device/Package Combinations**

Device	Package	Heat Sink Design	Thermal Models			Floating Lid Design
			Two-Resistor	DELPHI Model	Simplified Model	
XCVU11P	FSGD2104	Figure 1-15	Figure 1-27	Table 1-6		Figure 1-2
XCVU9P	FSGD2104	Figure 1-16	Figure 1-28	Table 1-7		Figure 1-3
XCVU13P	FIGD2104	Figure 1-17	Figure 1-29	Table 1-8		Figure 1-4
XCVU13P	FSGA2577	Figure 1-17	Figure 1-29	Table 1-8		Figure 1-4
XCVU19P	FSVA3824	Figure 1-22	Figure 1-38	Table 1-12	Table 1-27	Figure 1-11
XCVU23P	VSVA1365	Figure 1-23	Figure 1-39	Table 1-13	Table 1-28	Figure 1-12
XCVU27P	FIGD2104	Figure 1-17	Figure 1-29	Table 1-8		Figure 1-4
XCVU27P	FSGA2577	Figure 1-17	Figure 1-29	Table 1-8		Figure 1-4
XCVU29P	FIGD2104	Figure 1-17	Figure 1-29	Table 1-8		Figure 1-4
XCVU29P	FSGA2577	Figure 1-17	Figure 1-29	Table 1-8		Figure 1-4
XCVU31P	FSVH1924	Figure 1-18	Figure 1-30		Table 1-19	Figure 1-8
XCVU33P	FSVH2104	Figure 1-18	Figure 1-31		Table 1-20	Figure 1-9
XCVU35P	FSVH2104	Figure 1-19	Figure 1-32		Table 1-21	Figure 1-9
XCVU35P	FSVH2892	Figure 1-19	Figure 1-33		Table 1-22	Figure 1-10
XCVU37P	FSVH2892	Figure 1-20	Figure 1-34		Table 1-23	Figure 1-10
XCZU25DR	FSVE1156	Figure 1-21	Figure 1-35	Table 1-9	Table 1-24	Figure 1-5
XCZU25DR	FSVG1517	Table 1-21	Figure 1-36	Table 1-10	Table 1-25	Figure 1-6
XCZU27DR	FSVE1156	Figure 1-21	Figure 1-35	Table 1-9	Table 1-24	Figure 1-5
XCZU27DR	FSVG1517	Figure 1-21	Figure 1-35	Table 1-10	Table 1-25	Figure 1-6
XCZU28DR	FSVE1156	Figure 1-21	Figure 1-35	Table 1-9	Table 1-24	Figure 1-5
XCZU28DR	FSVG1517	Figure 1-21	Figure 1-36	Table 1-10	Table 1-25	Figure 1-6
XCZU29DR	FSVF1760	Figure 1-21	Figure 1-37	Table 1-11	Table 1-26	Figure 1-7

Lidless Flip-Chip Packages

The Xilinx lidless flip-chip ball grid array (BGA) packages use the same package substrate design as traditional lidded flip-chip packages, including the same electrical board and thermal conductivity as traditional flip-chip packaging. However, removing the lid (heat spreader) and adding thermal interface material allows direct contact between the external heat sink and the die. Lidless packages reduce the thermal resistance, improve the thermal behavior, and facilitate using custom passive or active heat-sink designs that incorporate two-phase (heat pipe, vapor chamber, or even liquid) cooling methods directly adjacent to the source of the dissipated heat on the die. All these advantages produce more efficient means of removing the heat from the device. Consequently, the device can operate in higher ambient temperature environments, area-constrained surroundings, and/or higher power operations.

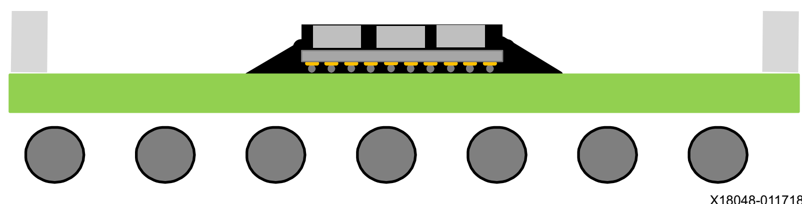

Figure 1-1: **Lidless Flip-Chip Package Diagram**

Package Mechanical Specifications

Package Mechanical Description and Drawings

Xilinx FPGAs packaged in the flip-chip BGA package are soldered directly to a PCB surface. Detailed mechanical drawings, including package dimensions and BGA ball pitch, are available for the lidless packages in the *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide* (UG575) [Ref 1] and *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075) [Ref 2], as appropriate. Refer to these user guides for the precise mechanical specification of each package.

A unique feature of the lidless Xilinx packages is the addition of a stiffener ring around the periphery of the package substrate. The stiffener ring provides additional package rigidity to improve the overall package coplanarity (flatness). It also serves as a guide for the heat sink solution applied to the device.

Mechanical Support for Testing

To support the introduction of lidless packages, Xilinx FPGAs can include an accompanying floating lid. To reduce package warpage, Xilinx lidless FPGAs can be designed with a stiffener ring that is higher than the die. When not using a heat sink or test socket with a raised island to contact the die, a floating lid may be used. The floating lid applies pressure to the die, ensuring good contact between the package and test socket or thermal solution.

Floating lids are intended for temporary use in bring-up. If a more permanent testing solution is required, please contact Xilinx support. These designs are provided as-is and are not qualified. Be aware that using a floating lid can reduce thermal performance compared to direct installation of a heat sink on the silicon.

Xilinx provides reference designs for floating lids on some of its lidless packages. These designs are intended to be used with a thermal interface material (TIM) between the die and floating lid. This TIM layer should be approximately 100 µm thick. Illustrations of the floating lids without this TIM layer are shown in the following figures. Drawings (.dwg and .pdf) are available in the Reference Design Files.

Floating lids can be ordered from JenTech Precision Industrial Co., LTD (http://www.jentech.com.tw/).

Floating Lid Designs

The floating lid for XCVU11P-FSGD2104 is available from JenTech (http://www.jentech.com.tw/) (part number not available). Drawings of the design are available in the Reference Design Files.

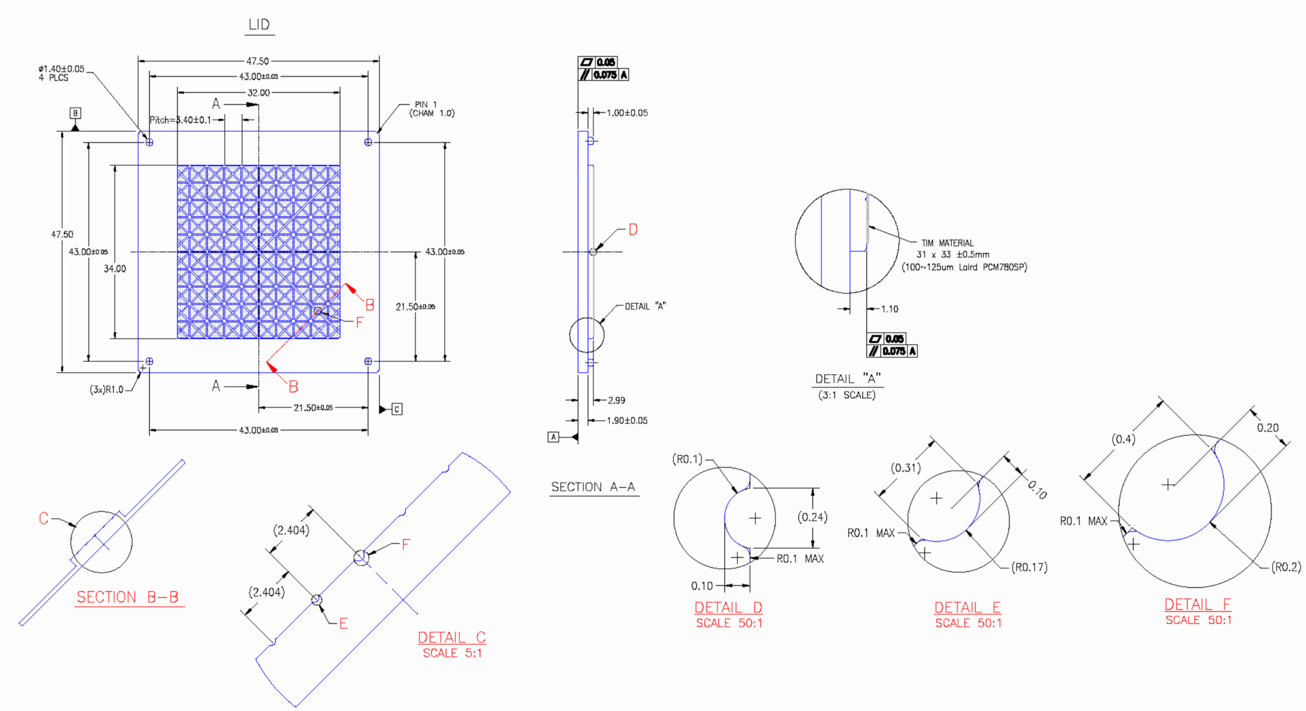

Figure 1-2: **Floating Lid for XCVU11P-FSGD2104**

The floating lid for XCVU9P-FSGD2104 is available from JenTech (http://www.jentech.com.tw/), part number 60004745. Drawings of the design are available in the Reference Design Files.

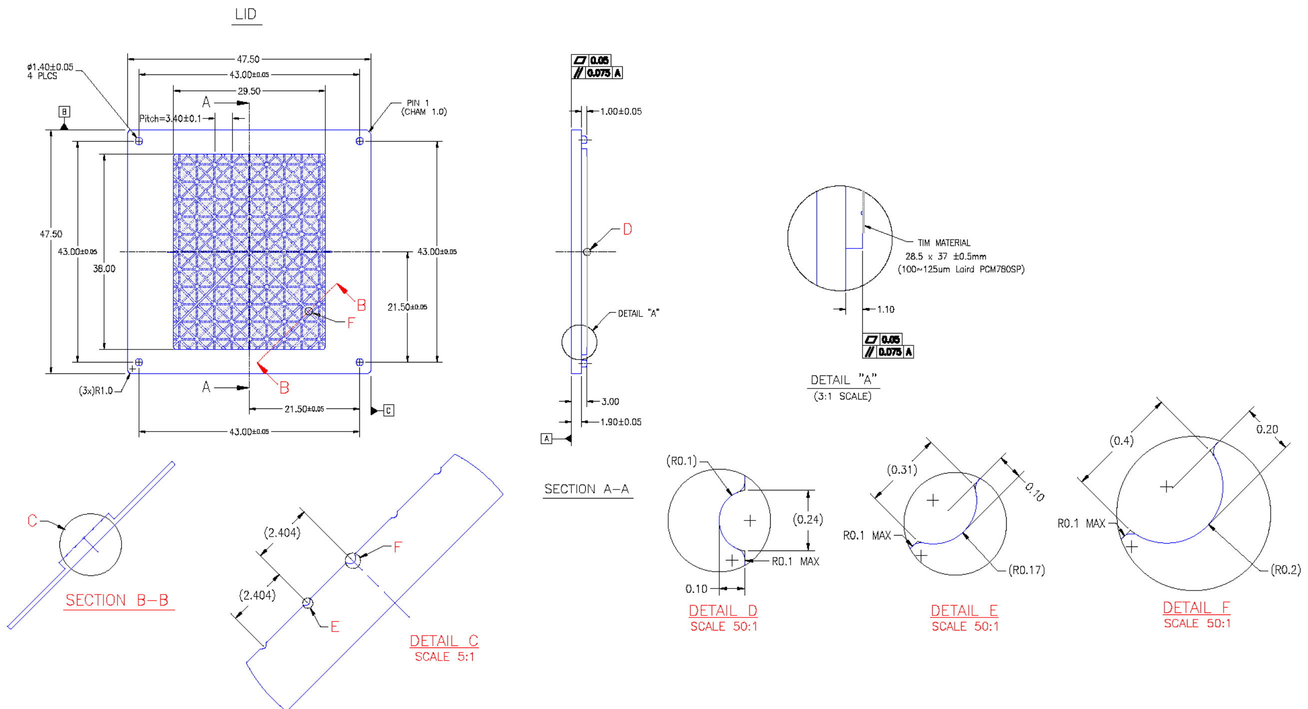

Figure 1-3: **Floating Lid for XCVU9P-FSGD2104**

The floating lids for XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577 are available from JenTech (http://www.jentech.com.tw/), part number 60004989. Drawings of the design are available in the Reference Design Files.

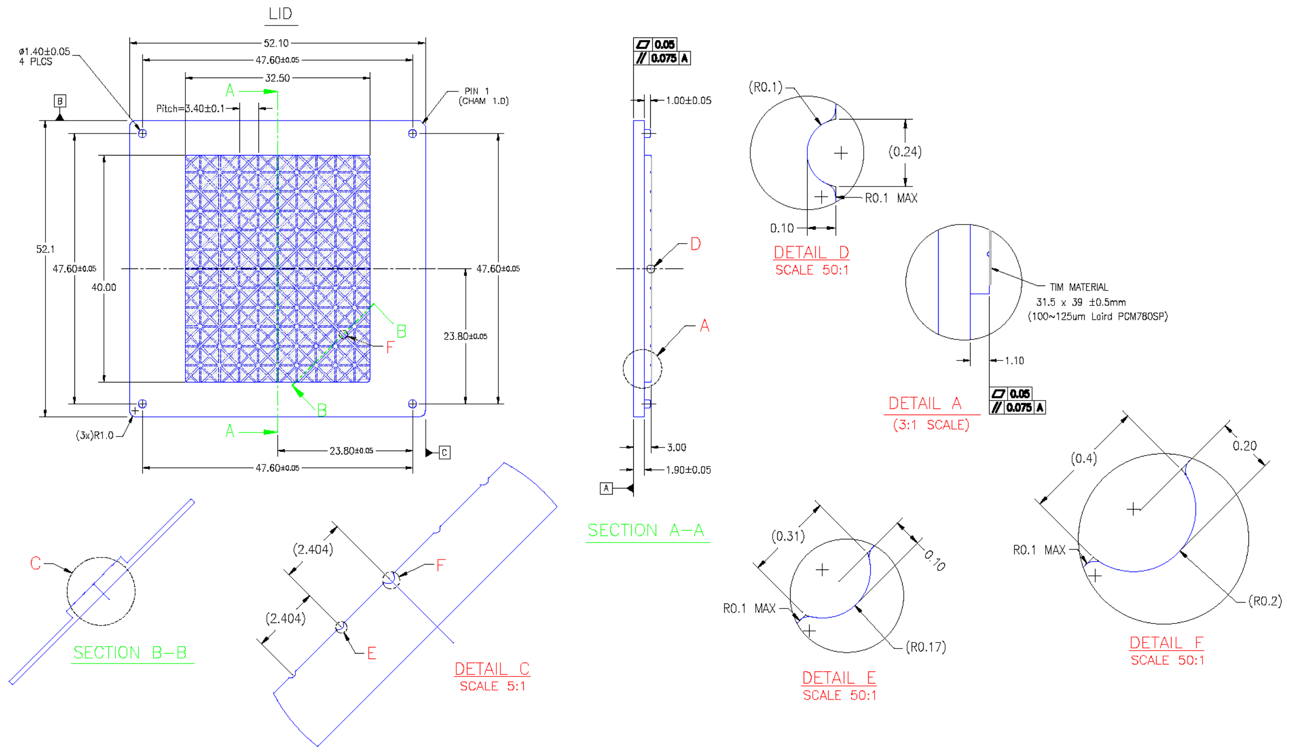

Figure 1-4: **Floating Lid for XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577**

The floating lid for XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156 is available from JenTech (http://www.jentech.com.tw/), part number 60005403. Drawings of the design are available in the Reference Design Files.

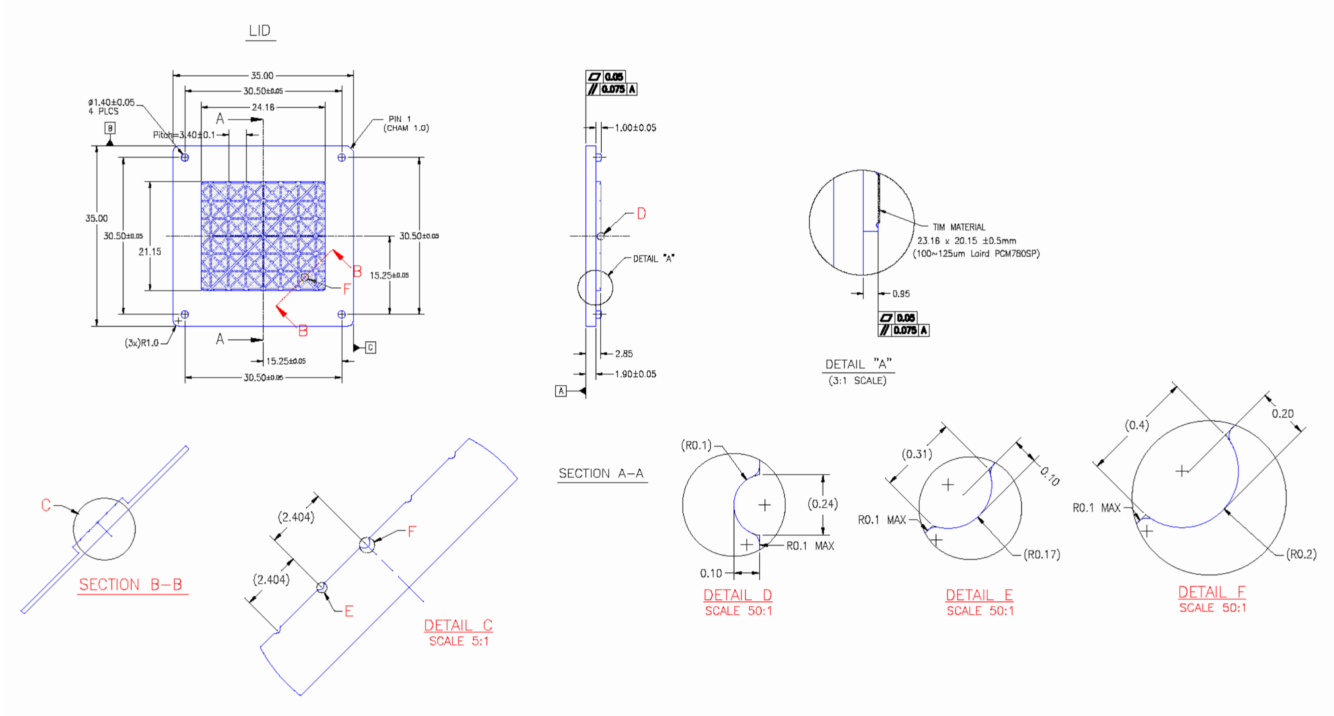

Figure 1-5: **Floating Lid for XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156**

The floating lid for XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517 is available from JenTech (http://www.jentech.com.tw/), part number 60005404. Drawings of the design are available in the Reference Design Files.

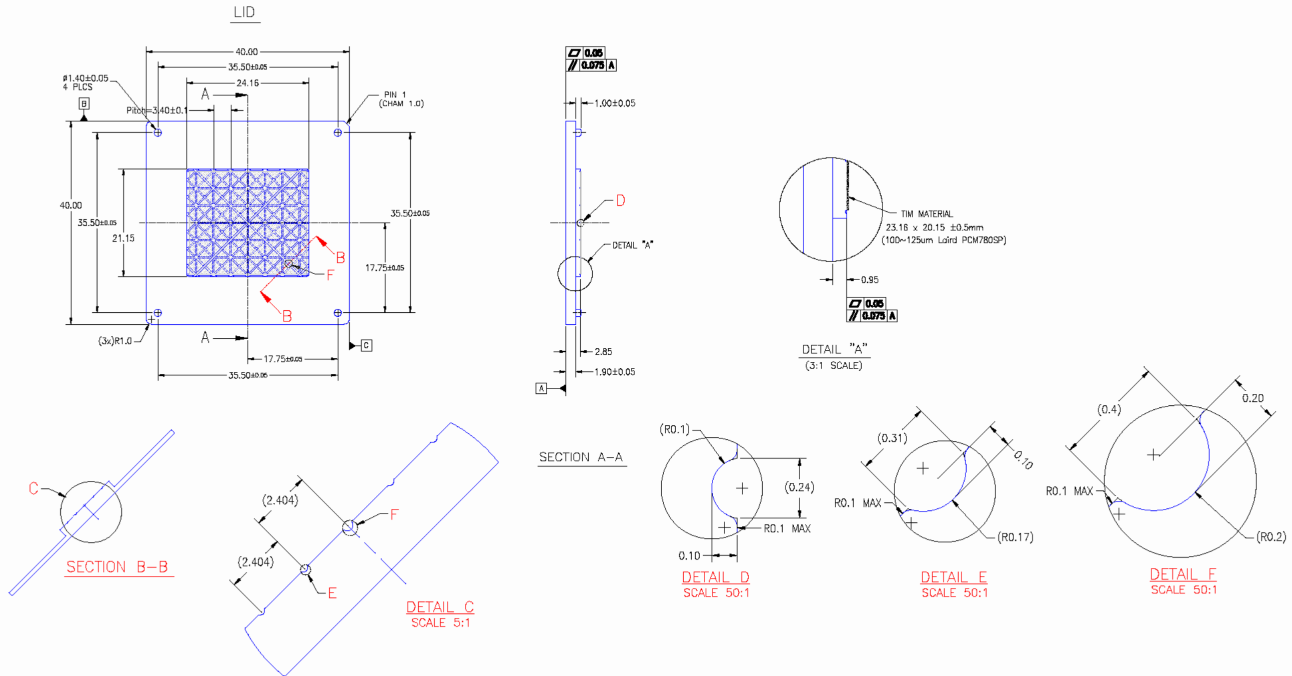

Figure 1-6: **Floating Lid for XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517**

The floating lid for XCZU29DR-FSVF1760 is available from JenTech (http://www.jentech.com.tw/), part number 60005483. Drawings of the design are available in the Reference Design Files.

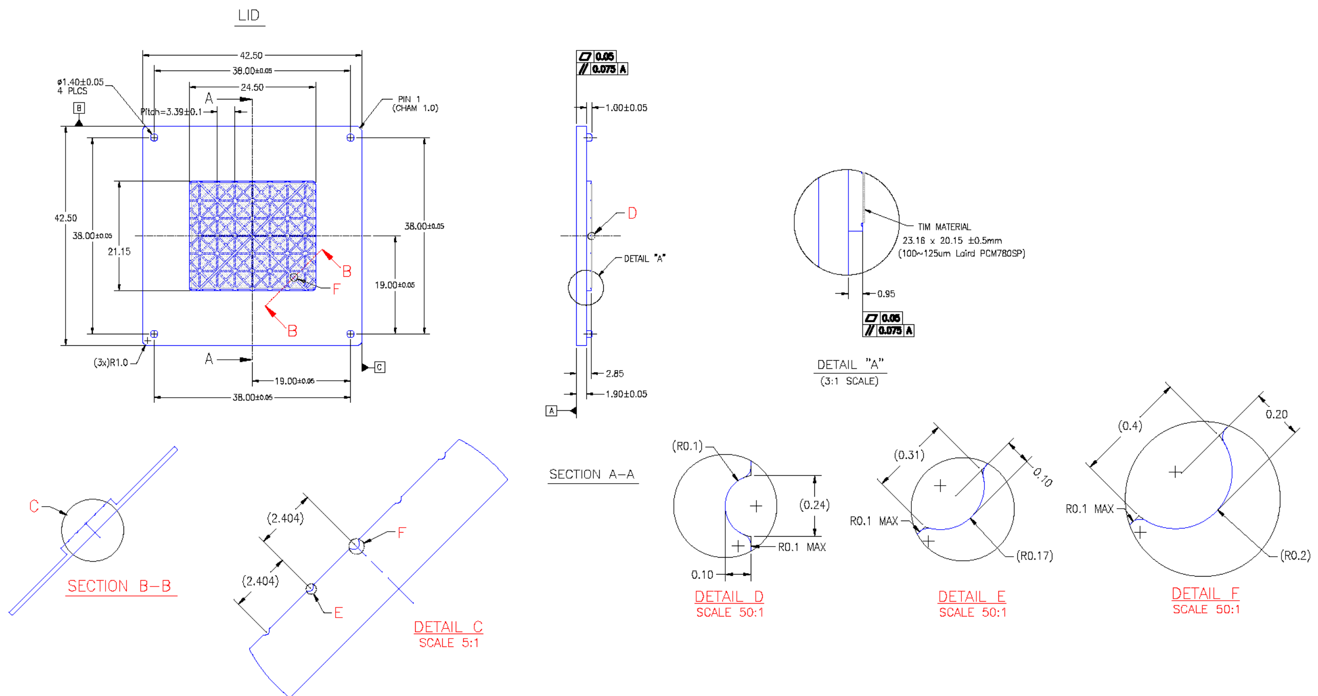

Figure 1-7: **Floating Lid for XCZU29DR-FSVF1760**

The floating lid for XCVU31P-FSVH1924 is available from JenTech (http://www.jentech.com.tw/), part number 60005649. Drawings of the design are available in the Reference Design Files.

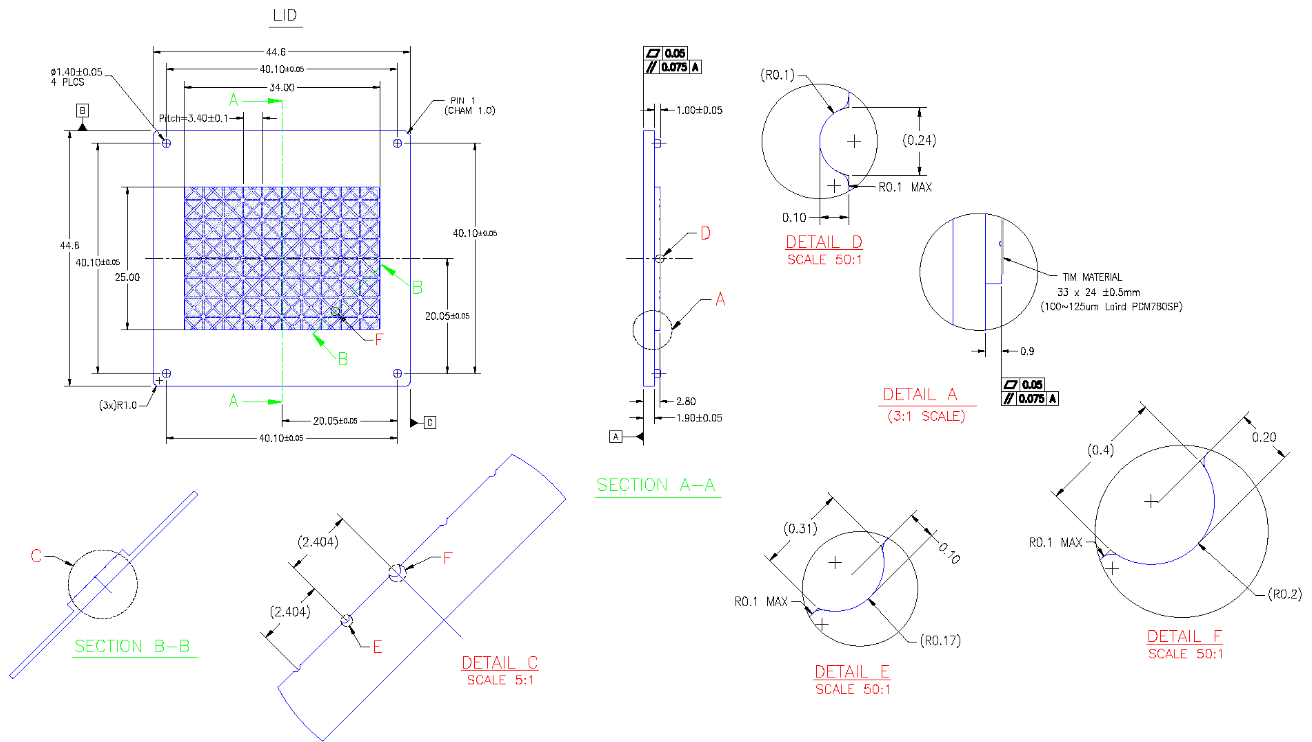

Figure 1-8: **Floating Lid for XCVU31P-FSVH1924**

The floating lids for XCVU33P-FSVH2104 and XCVU35P-FSVH2104 are available from JenTech (http://www.jentech.com.tw/), part number 60005552. Drawings of the design are available in the Reference Design Files.

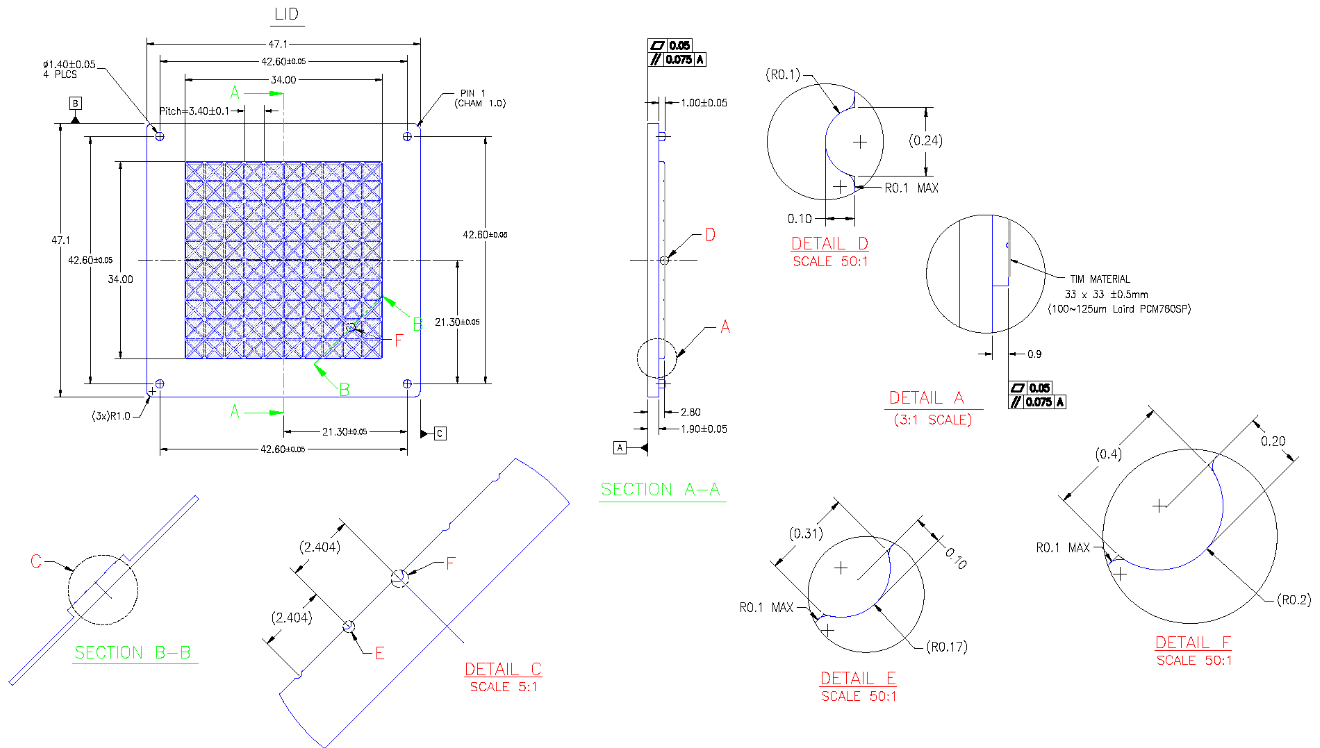

Figure 1-9: **Floating Lid for XCVU33P-FSVH2104 and XCVU35P-FSVH2104**

The floating lids for XCVU35P-FSVH2892 and XCVU37P-FSVH2892 are available from JenTech (http://www.jentech.com.tw/), part number 60005552. Drawings of the design are available in the Reference Design Files.

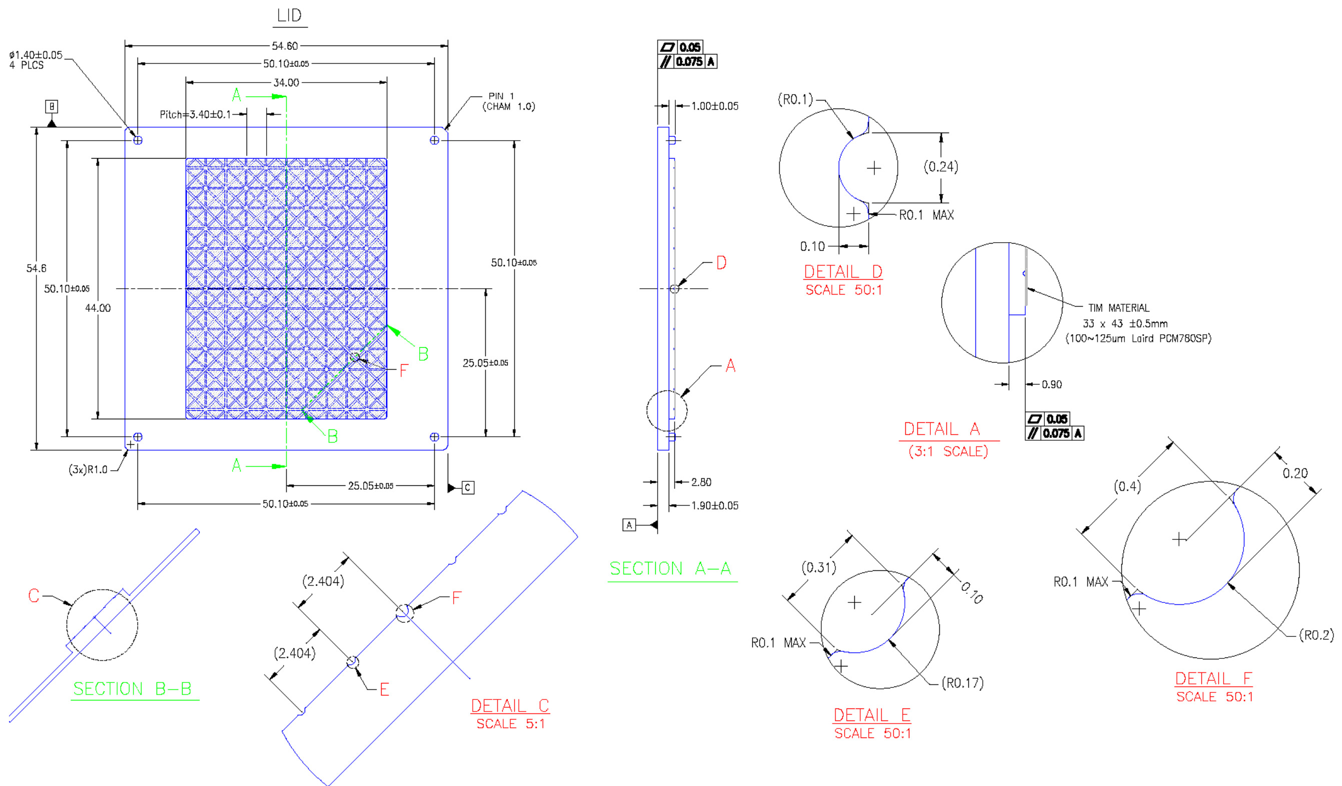

Figure 1-10: **Floating Lid for XCVU35P-FSVH2892 and XCVU37P-FSVH2892**

The floating lid for XCVU19P-FSVA3824 is available from JenTech (http://www.jentech.com.tw/), part number 60006300. Drawings of the design are available in the Reference Design Files.

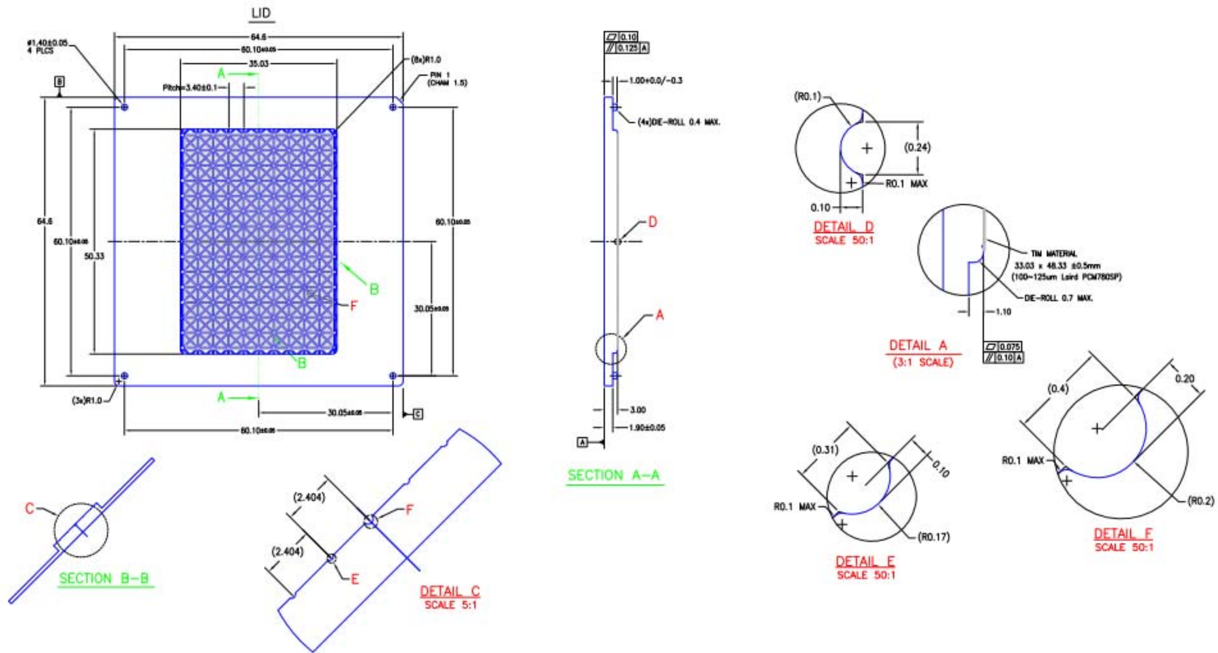

Figure 1-11: **Floating Lid for XCVU19P-FSVA3824**

The floating lids for XCVU23P-VSVA1365 is available from JenTech (http://www.jentech.com.tw/), part number 60007240. Drawings of the design are available in the Reference Design Files.

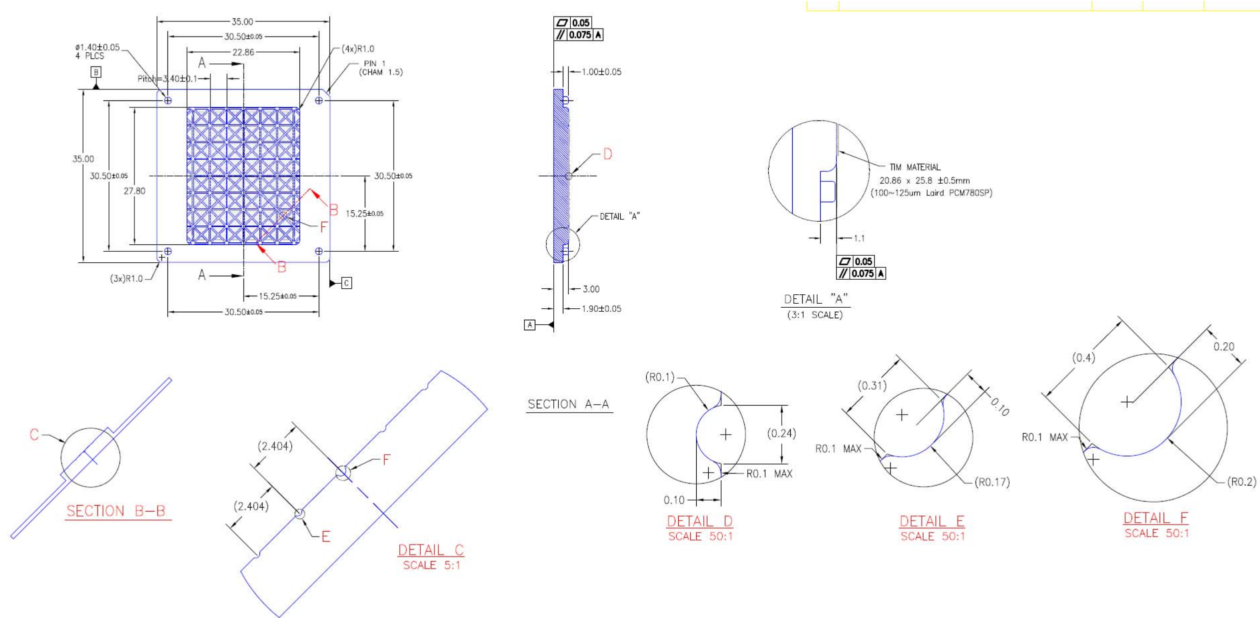

Figure 1-12: **Floating Lid for XCVU23P-VSVA1365**

Thermal Management Strategy

Exceptional thermal management starts with good package design. However, it only comes into fruition when accompanied by a well-designed heat-sink solution.

Keep-Out Zones

In BGA packages, capacitors can be placed in the area surrounding the die. These die-side capacitors are only slightly shorter than the die height. Since the capacitors could be electrically conductive, contact with electrically conductive materials must be avoided.

A thermal and mechanical solution design must not interfere with the package stiffener where it is higher than the die. Therefore, the thermal solution must have an island. The following example uses the XCVU13P-D2104.

Dimensional properties of the XCVU13P-FIGD2104 contact island:

Width = 34 mm
Length = 42 mm
Height = 1.5 mm
Flatness: < 75 μm
Surface roughness = 3~5 μm

- For more information, see the heat-sink for XCVU13P-FIGD2104 (Figure 1-17). The island requires a thermal interface material coverage of 35.5 x 44 mm. The reference design used Laird (PCM780SP) or Honeywell (PTM6500D).
- The total thermal contact of the thermal interface material is determined based on the above parameters from the thermal interface supplier's data sheet.
- The applied pressure on the package must follow the guidelines in Heat Sink Pressure. Lower pressure risks poor thermal contact and higher pressure risks damaging the device; therefore, strict control of pressure is required. See the *Applied Pressure from Heat Sink to the Package via Thermal Interface Materials* recommendation in the *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide* (UG575) [Ref 1] and *Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide* (UG1075) [Ref 2].
- Consider all uncertainties in thermal modeling, including manufacturing variations from the thermal solutions (for example, fan airflow tolerance, heat pipe or vapor chamber performance tolerance, variation of the attachment of fins to the heat sink base, and surface flatness).

The heat sink design examples include CAD files and documentation for designing heat sinks specifically for these device/package combinations. The example heat sink designs serve as a reference for the devices/packages listed in Table 1-1.

Heat Sink Solutions at the System Level

Taking into consideration the system's physical, mechanical, and environmental constraints, the overall thermal budget must be maintained so that it does not exceed the device's maximum operating temperature. The heat sink is an integral, if not the most important, part of the thermal management solution to maintain a safe operating temperature. As a result, the following are important:

- Detailed instructions on recommended Thermal Solution Installation of the Xilinx FCBGA Lidless Packages are provided in Appendix A.
- Θ_{JC} parameters from *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide* (UG575) [Ref 1] and *Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide* (UG1075) [Ref 2] must not be directly used to determine the thermal performance of the device application. These parameters are calculated according to JEDEC JESD51 standards, where system parameters differ greatly from most applications. Instead, run system thermal simulations in worst-case environmental conditions using the DELPHI thermal models, which more accurately represent the device thermal performance under all boundary conditions.
- Consider the mechanical specifications of the package, as well as selecting the best thermal interface between the die and the thermal management solution to ensure the lowest thermal contact resistance.
- Figure 1-13 shows the PCM780SP coverage after 1000 Thermal BLR Cycles for 0°C to 100°C. The package passed 5000 Thermal cycles without any failure.

Figure 1-13: **Example of Heat Sink for VU13P-FIGD2104 with PCM780SP**

Heat Sink Designs

The reference design file includes heat sink design examples with CAD files, to assist in designing heat sinks for these packages. Figure 1-15 through Figure 1-21 are examples of heat sink designs.

Note: All reference designs have been developed based on PCB thickness of 2.3 mm. If your PCB thickness is different, the screw/spring dimensions must be adjusted accordingly to ensure that the same compression is achieved.

The following figure illustrates the heat sink mounting to the PCB with a mounting hole size of 3.2 mm in diameter and an 8.0 mm keep out area surrounding each hole.

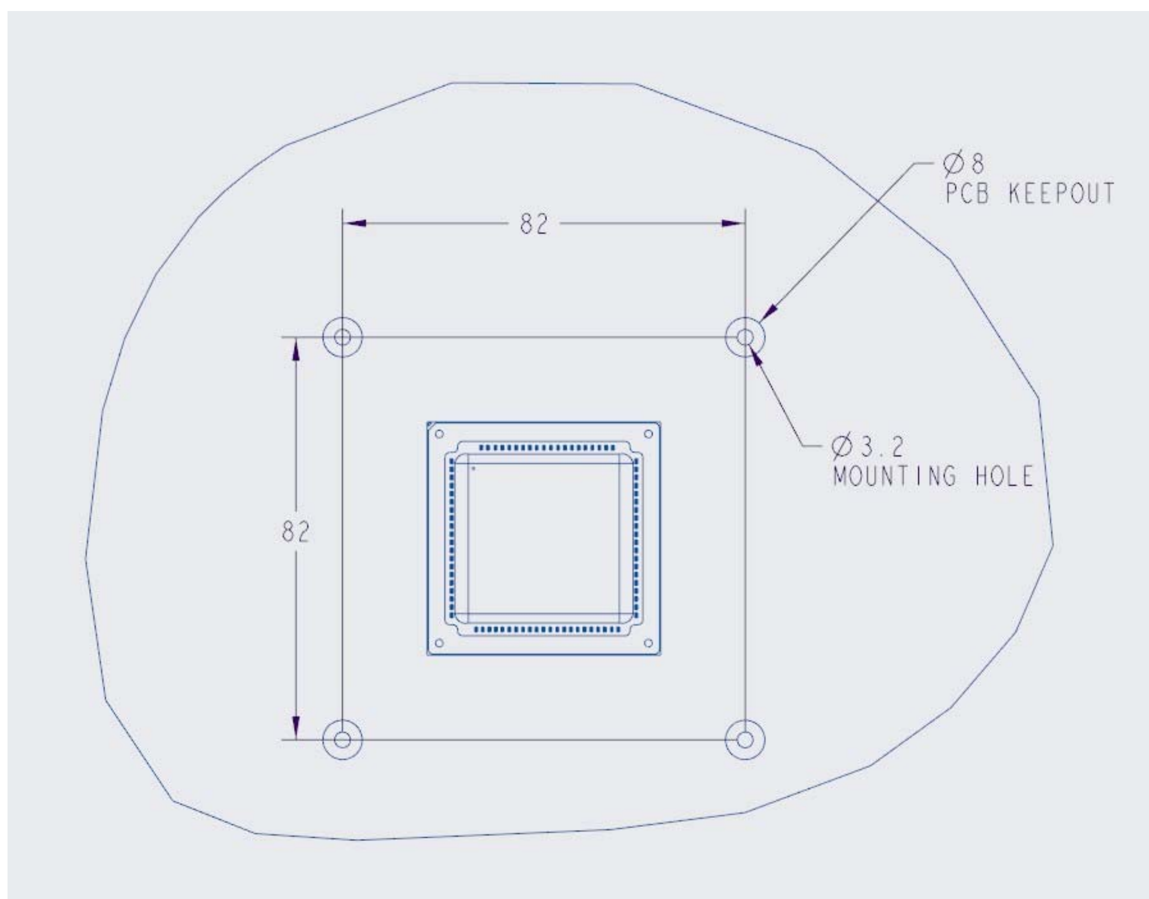

Figure 1-14: **Heat Sink Mounting to the PCB**

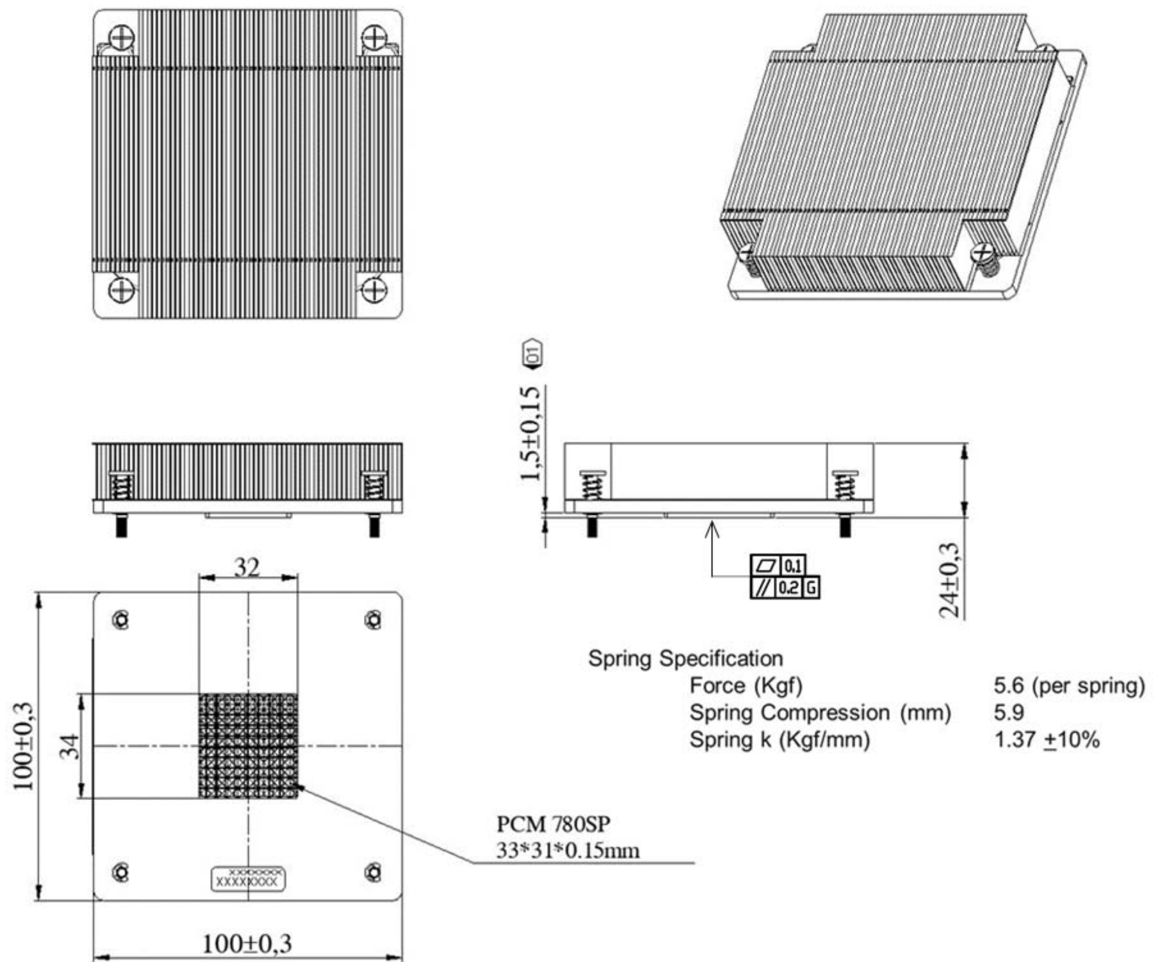

Figure 1-15: **Heat Sink (Heat-pipe with Etching Design) for XCVU11P-FSGD2104**

The heat-pipe with etching design for XCVU11P-FSGD2104 is available from supplier NTK (HK) LIMITED using part number 19020000009 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design Files.

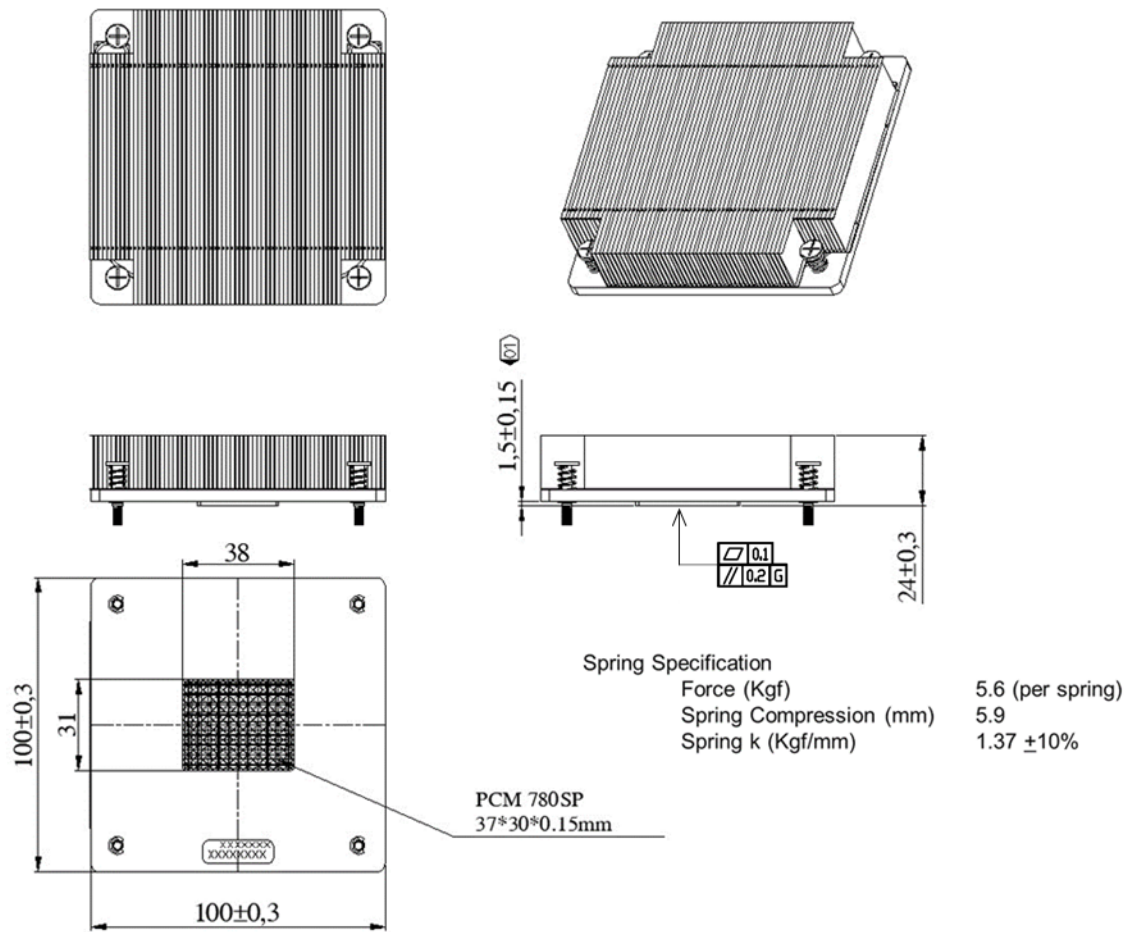

Figure 1-16: **Heat Sink (Heat-pipe with Etching Design) for XCVU9P-FSGD2104**

The heat-pipe with etching design for XCVU9P-FSGD2104 is available from supplier NTK (HK) LIMITED using part number 19020000010 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design Files.

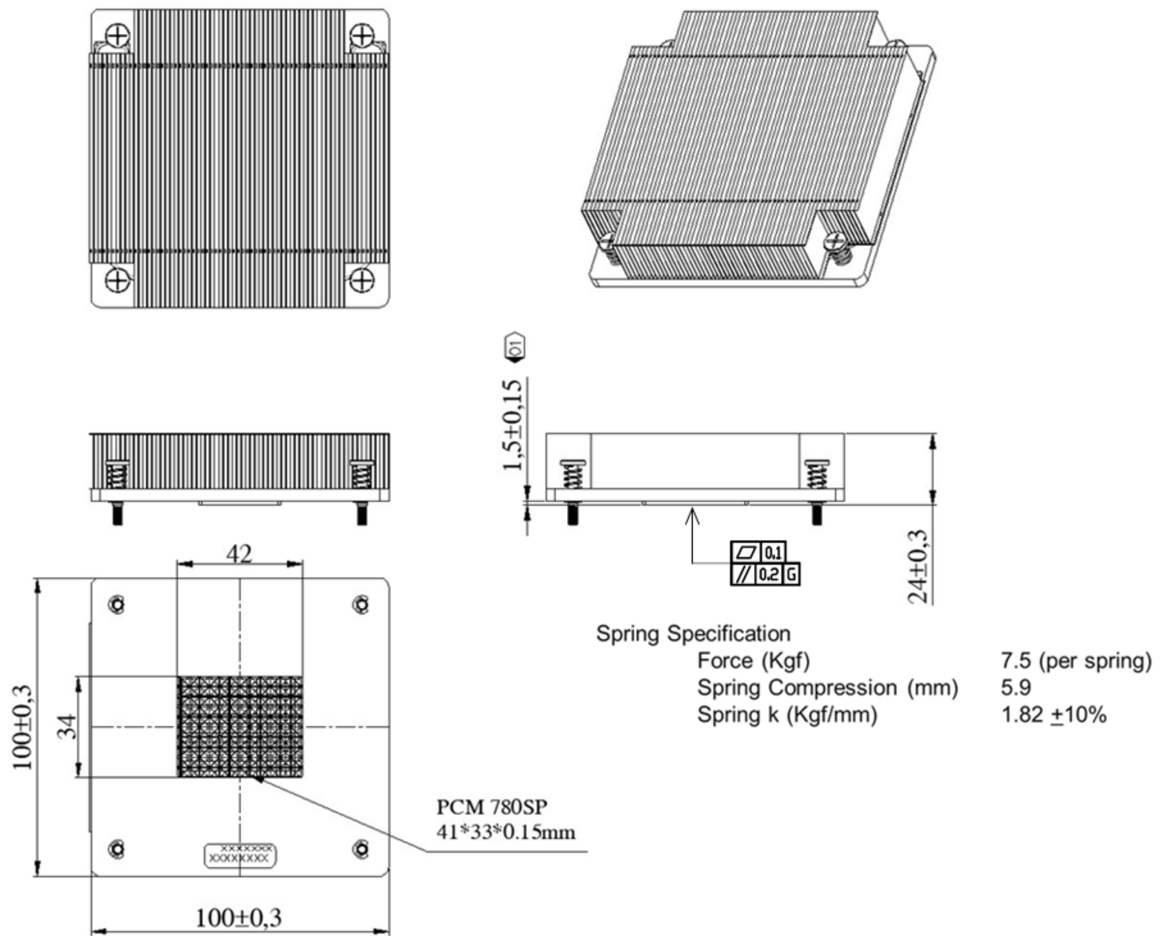

Figure 1-17: **Heat Sink (Heat-pipe with Etching Design) for XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577**

The heat-pipe with etching design for the XCVU13P- FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577 is available from supplier NTK (HK) LIMITED using part number 19020000011 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design Files.

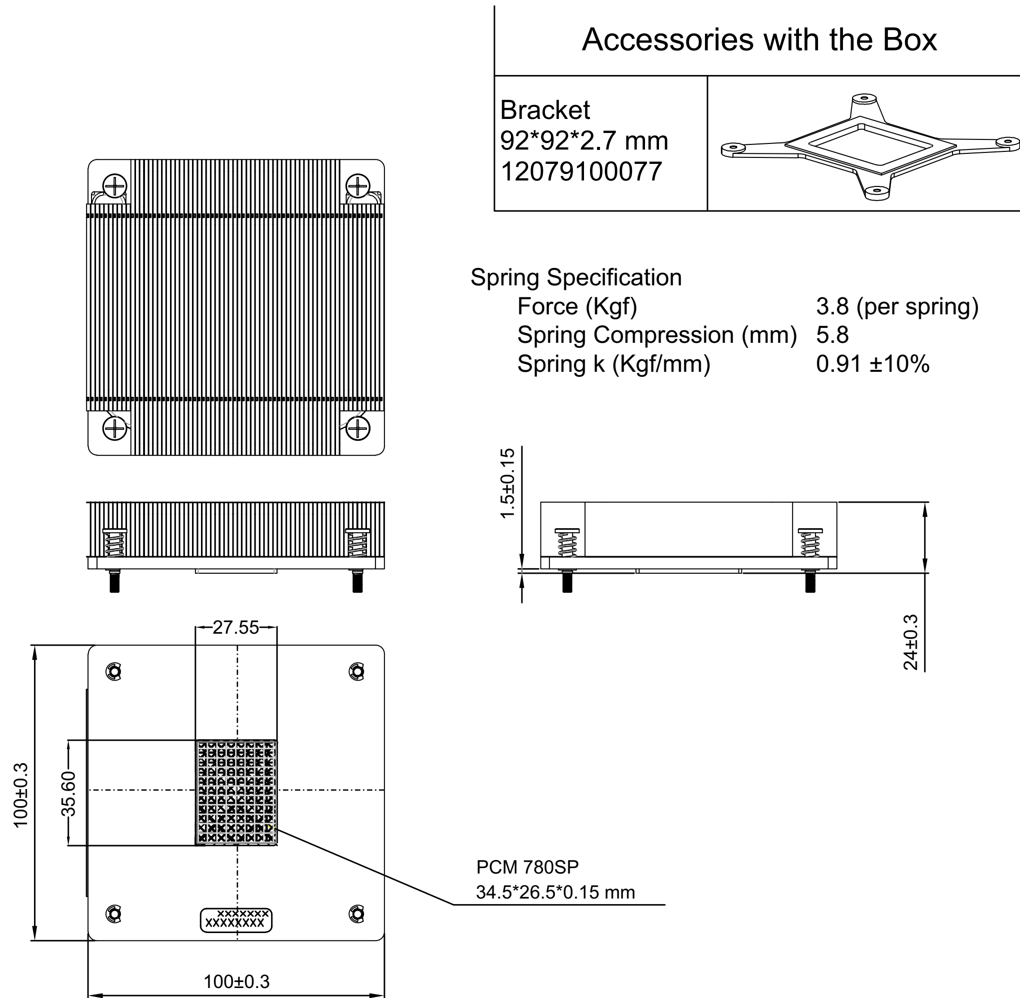

Figure 1-18: **Heat Sink (Heat-pipe Design) for XCVU31P-FSVH1924 and XCVU33P-FSVH2104**

The heat-pipe heat sink design for the XCVU31P-FSVH1924 and XCVU33P-FSVH2104 is available from the supplier NTK (HK) LIMITED using part number 19020000006 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design Files.

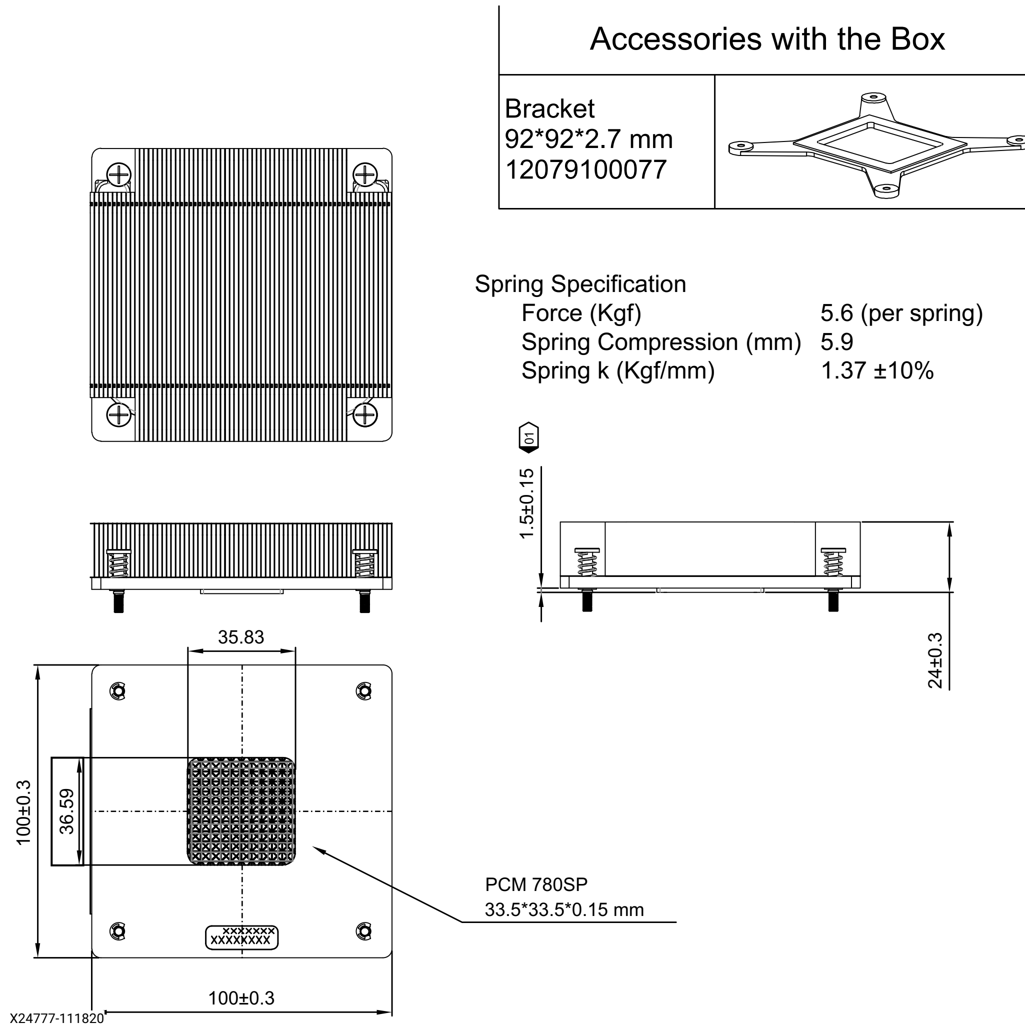

Figure 1-19: **Heat Sink (Heat-pipe Design) for XCVU35P-FSVH2104 and XCVU35P-FSVH2892**

The heat-pipe heat sink design for the XCVU35P-FSVH2104 and XCVU35P-FSVH2892 is available from the supplier NTK (HK) LIMITED using part number 19020000007 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design Files.

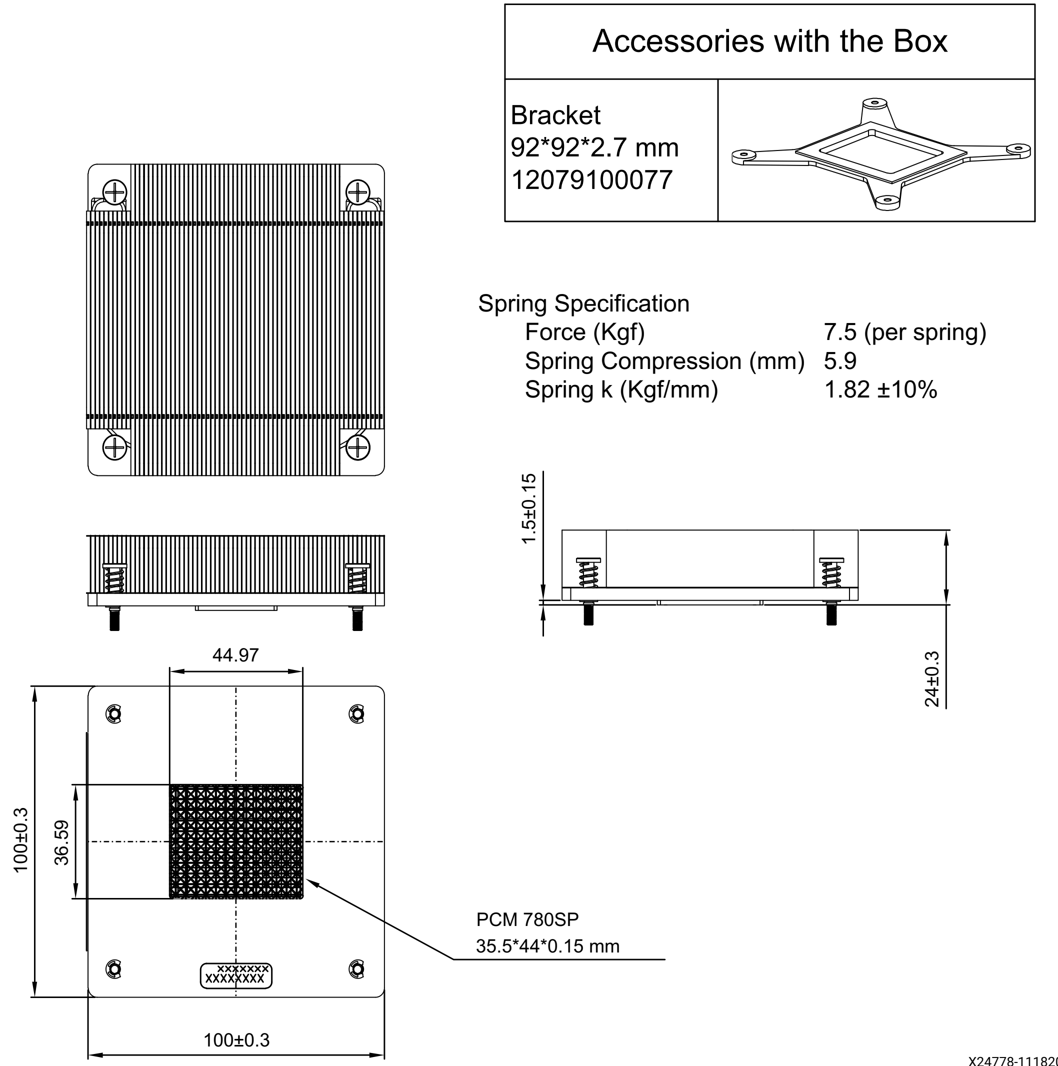

Figure 1-20: **Heat Sink (Heat-pipe Design) for XCVU37P-FSVH2892**

The heat-pipe heat sink design for the XCVU37P-FSVH2892 is available from the supplier NTK (HK) LIMITED using part number 19020000008 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design Files.

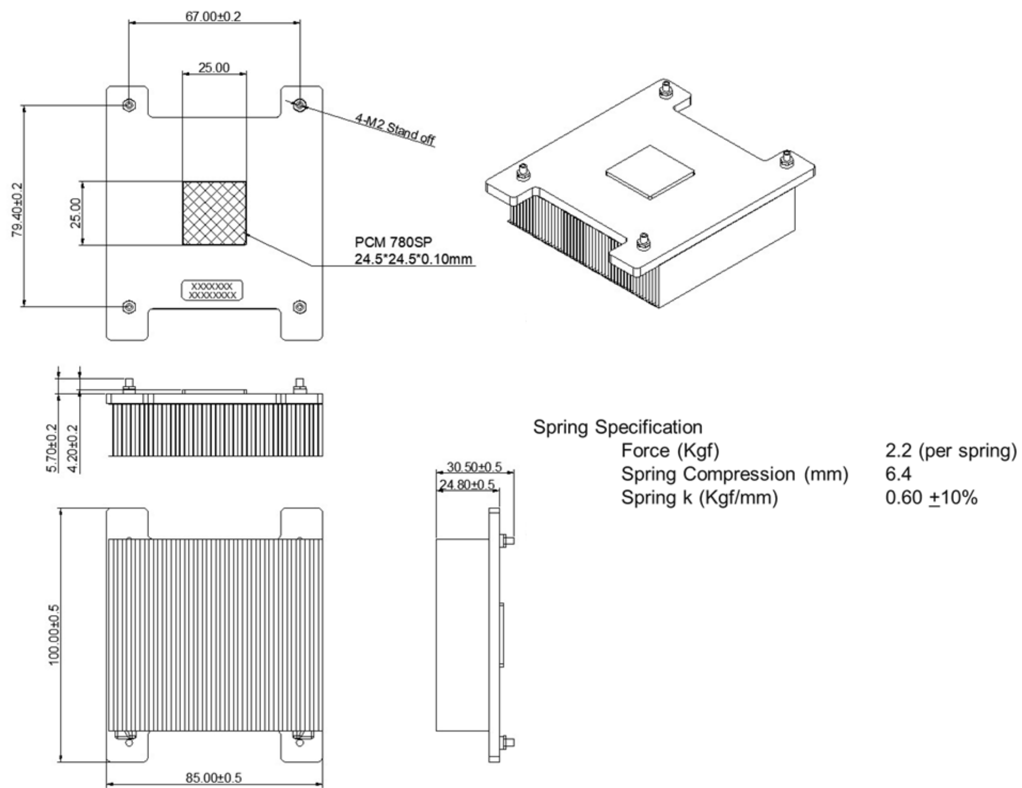

Figure 1-21: **Heat Sink (Heat-pipe Design) for XCZU25DR-FSVE1156, XCZU25DR-FSVG15h17, XCZU27DR-FSVE1156, XCZU27DR-FSVG1517, XCZU28DR-FSVE1156, XCZU28DR-FSVG1517, and XCZU29DR-FSVF1760**

The heat-pipe heat sink design for the XCZU25DR-FSVE1156, XCZU25DR-FSVG1517, XCZU27DR-FSVE1156, XCZU27DR-FSVG1517, XCZU28DR-FSVE1156, XCZU28DR-FSVG1517, and XCZU29DR-FSVF1760 is available from the supplier NTK (HK) LIMITED using part number 15029000217 (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design Files.

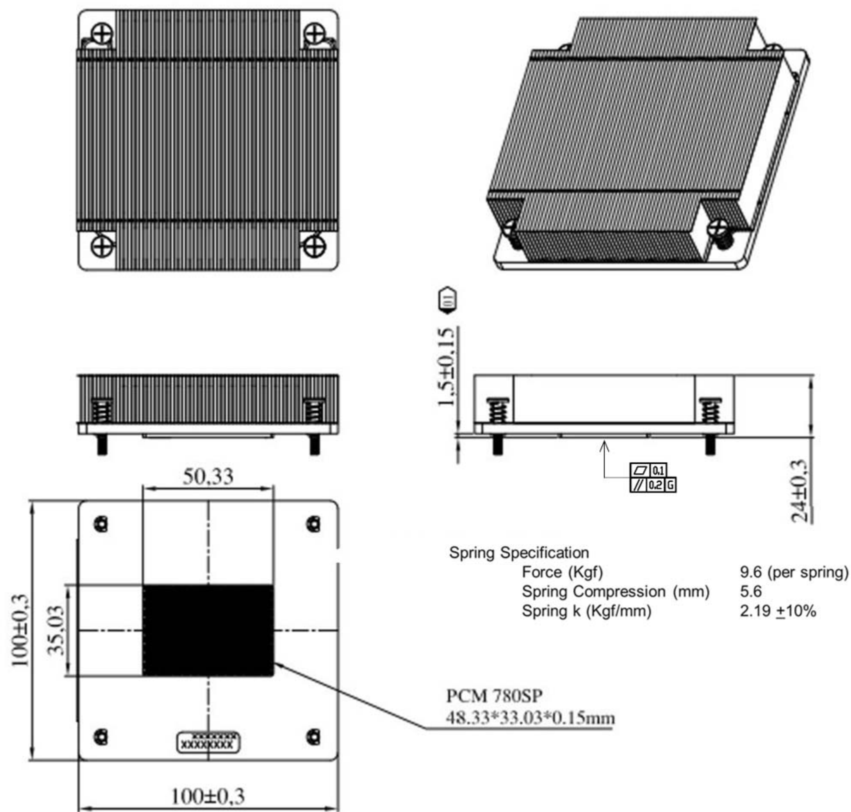

Figure 1-22: **Heat Sink (Heat-pipe Design) for XCVU19P-FSVA3824**

The heat-pipe heat sink design for the XCZU19P-FSVA3824 is available from the supplier NTK (HK) LIMITED using part number 1.02.01.0197H (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design Files.

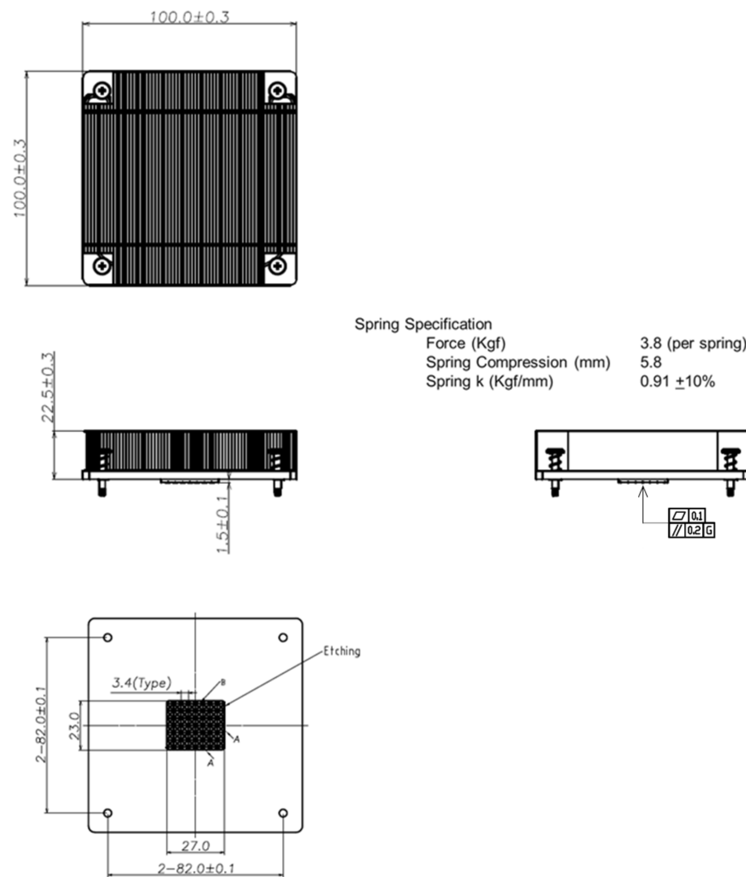

Figure 1-23: **Heat Sink (Heat-pipe Design) for XCVU23P-VSVA1365**

The heat-pipe heat sink design for the XCVU23P-VSVA1365 is available from the supplier NTK (HK) LIMITED using part number 5.02.09.0621H (www.ntkltd.com). A 3D model of this design is available in STEP format in the Reference Design Files.

Heat Sink Pressure

The typical engineering practice is to use 20 to 50 psi pressure, based on die size, pin count, and other factors. This optimizes thermal performance contact between the silicon and the thermal solution via the thermal interface material (TIM).

Note: In the past, Xilinx has recommended 20 to 40 psi in some places and 5 to 10 g force per pin in other places. These recommendations were based on individual product cases, which were verified to work. Typical industry recommendations are 20-60 psi or 5-15 g force per pin (varies by die and package size).

The amount of force the screws apply on the heat sink should be approximately equal to the amount of force the heat sink applies on the die, transferred through the TIM. When designing the heat sink, the amount of force the screws will apply on the heat sink can be approximated by:

$$F = n \times k \times \delta$$ *Equation 1-1*

Where n is the number of springs, k is the spring constant and δ is the compression length of the spring. In the reference designs provided here, n is 4. The spring constant can be obtained from the vendor or measured. The compression length is:

$$\delta = l_c - l_0$$ *Equation 1-2*

Where l_c is the compressed spring length and l_0 is the uncompressed or initial spring length. These spring lengths can be determined by performing a stack-up analysis of the components as shown in Figure 1-24. For example, l_c is [1] in Figure 1-24. An example of stack-up analysis, in which the screw stop is on the top of the motherboard, is:

$$l_c = h_s - h_c - h_{TIM} - h_{HS} - h_{PCB}$$ *Equation 1-3*

Where h_s is the dimension of the spring between the stopper and screw-head (e.g. [1] + [2] in Figure 1-24, h_c is the dimension of the assembled package (BGA to die surface), h_{TIM} is the thickness of the TIM1.5, h_{HS} is the dimension of the heat sink from the heat sink island to the plane the spring sits on, and h_{PCB} is the PCB thickness.

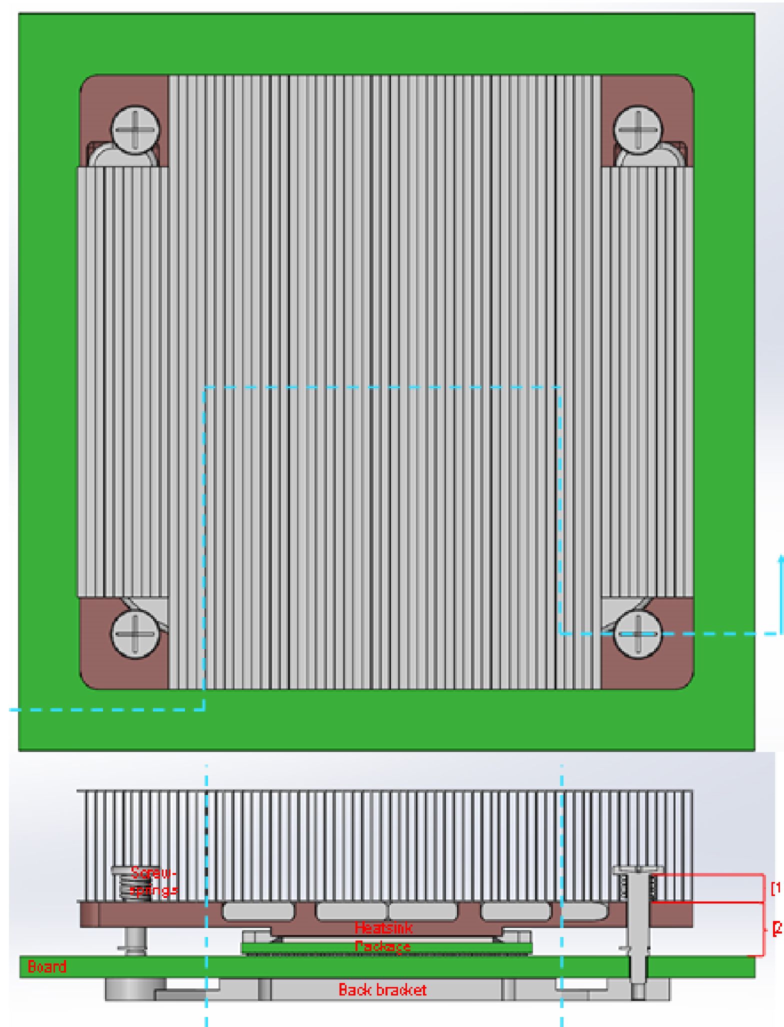

Figure 1-24: **Overhead Heat Sink Schematic for Screw-Spring Design (Top) and Cross-Section of Heat Sink Schematic for Screw-Spring Design (Bottom)**

In the reference designs of heat sink, the springs compression is defined based on the stack-up analysis shown in the following figure.

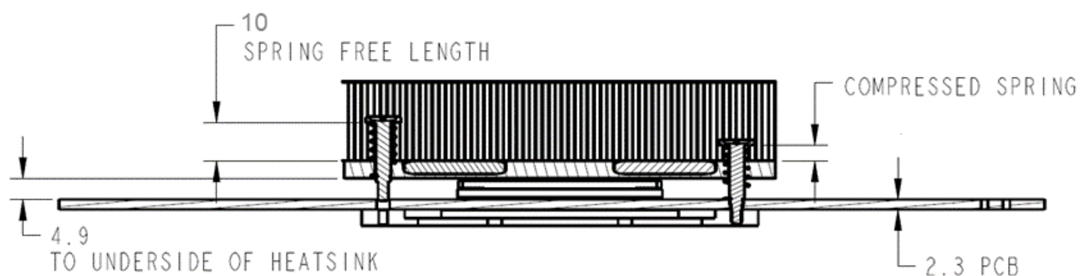

Figure 1-25: **Stack Up for Reference Heat Sink Design Spring Specification in mm**

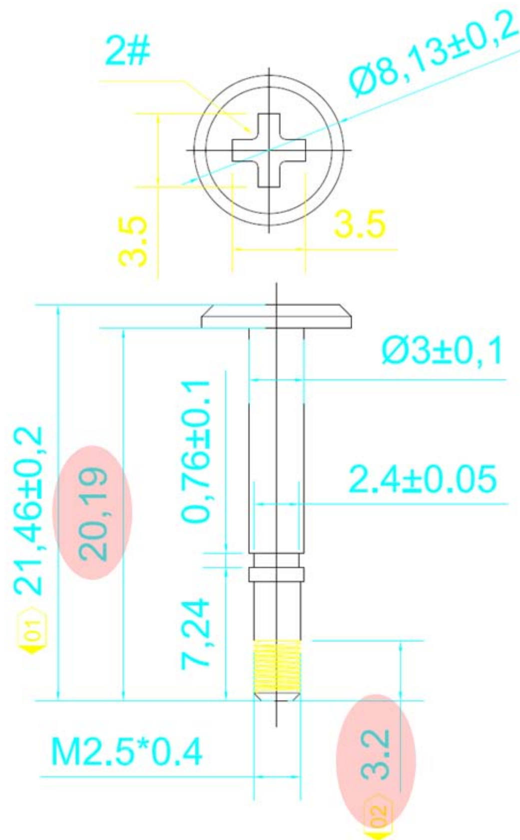

Figure 1-26: **Screw and E-Ring Stopper Clip Dimension**

For XCSZU25DR reference heat sink, the compressed string is:

$$\delta = l_c - l_0 \quad \text{Equation 1-4}$$

where:

$$l_c = h_s - h_c - h_{TIM} - h_{HS} - h_{PCB} \quad \text{Equation 1-5}$$

With the following values:

Table 1-2: **Compressed Spring Length Calculation for Reference Heat Sinks**

Value	Description	XCSZU25DR FFSVE1156	XCSZU25DR FSVA3824
h_s	Dimension of the spring between the stopper and screw-head	20.19-3.2 (from Figure 1-26) = 16.99 mm	20.19-3.2 (from Figure 1-26) = 16.99 mm
h_c	Dimension of the assembled package (BGA to die surface)	3.23 mm	3.48 mm
h_{TIM}	Thickness of the TIM	0.07 mm	0.07 mm
h_{HS}	Dimension of the heat sink from the heat sink island to the plane the spring sits on	5.5 mm	5.5 mm

Table 1-2: **Compressed Spring Length Calculation for Reference Heat Sinks *(Cont'd)***

Value	Description	XCSZU25DR FFSVE1156	XCSZU25DR FSVA3824
h_{PCB}	PCB thickness	2.3 mm	2.3 mm
l_c	h_s-h_c-h_{TIM}-h_{HS}-h_{PCB}	5.89 mm	5.64 mm
l_0	Uncompressed/initial spring length	10.0 mm	10.0 mm
δ	Compression length of the spring	4.11 mm	4.36 mm

Based on the force the heat sink applies on the die, the pressure can be calculated as:

$$P = \frac{F}{A_{die}}$$ *Equation 1-6*

Where A_{die} is the die area, which can be obtained from *Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide* (UG1075) [Ref 1] or *Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide* (UG1075) [Ref 2].

For lidless package:

The applied force f (kgf)==0.031*(A^1.25)/(N)^0.25

The applied pressure (PSI)=44*(A/N)^0.25

Where:

- N is the number of BGA
- A is the contact area of the package with heatsink in mm^2.

From the force defined by the recommended spring compression and spring k constant, the pressure for the reference heat sink is shown in the following table.

Table 1-3: **Reference Heat Sink Pressure**

Pkg	Device	Force (Kgf)	PSI	Spring compress, δ (mm)	spring k (kgf/mm)
2104	XCVU9P	22.47	32.74	4.11	1.37
2104	XCVU11P	22.47	35.77	4.11	1.37
2104	XCVU13P	29.86	36.17	4.11	1.82
2104	XCVU27P/29P	29.86	36.12	4.11	1.82
2577	XCVU13P	29.27	35.47	4.03	1.82
2577	XCVU27P/29P	29.27	35.42	4.03	1.82
1924	XCVU31P	15.22	33.52	4.20	0.91
2104	XCVU33P	15.22	32.84	4.20	0.91
2104	XCVU35P	22.97	34.74	4.20	1.37
2892	XCVU35P	22.97	34.74	4.20	1.37

Table 1-3: **Reference Heat Sink Pressure**

Pkg	Device	Force (Kgf)	PSI	Spring compress, δ (mm)	spring k (kgf/mm)
2892	XCVU37P	30.51	35.53	4.20	1.82
1156	XCZU25DR/27DR/28DR	8.70	32.23	3.65	0.60
1517	XCZU25DR/27DR/28DR	8.70	32.23	3.65	0.60
1760	XCZU29DR	8.70	32.23	3.65	0.60
3824	XCVU19P	38.19	35.78	4.36	2.19
1365	XCVU23P	15.37	44.37	4.20	0.91

Xilinx recommends using heat sink dynamic mounting, which refers to using screw-springs to attach the heat sink. As the board warps during thermal excursion or other deflection occurs due to mechanical force, the springs will adjust to apply greater force at smaller deflections, dynamically adjusting to any changes. Through screw-spring design, as detailed above, the compressed length of the spring should be fixed, creating a product with consistent heat sink force. For a given product, the die size is fixed, leading to a constant heat sink pressure on the die. Xilinx also recommends using a back bracket or back plate to provide mechanical support.

During installation, the amount of screw torque necessary to obtain that pressure is best determined through measurement, as detailed in Appendix A. Xilinx has found that a torque of 2.5 in-lbf on each screw usually produces a pressure within the desired range. Any screw torque should be verified for pressure on the die.

During pressure measurement (or normal operation), thermocouples should not be present between the package and the heat sink, as their presence will degrade the thermal contact and result in incorrect thermal measurements. The best practice is to select the appropriate pressure for the optimum thermal contact performance between the package and the thermal system solution, and the mechanical integrity of the package, with the thermal solution to pass all mechanical stress and vibration qualification tests.

Thermal Simulation and the Use of Thermal Models

Xilinx offers and supports a suite of integrated device power analysis tools to help quickly and accurately estimate the power requirements of your design. Download and fill out the latest version of the Xilinx Power Estimator (XPE) at https://www.xilinx.com/power. The variability of design power requirements makes it difficult to apply predetermined thermal solutions. The estimated power of the device using XPE, coupled with system operating conditions and constraints dictate the appropriate solution.

Xilinx recommends using the simplified thermal model or DELPHI thermal model during thermal modeling of the system. Xilinx does not recommend using a 2-resistor model for thermal simulation and design due to lack of precision and accuracy. A detailed model representation of the package might consume more simulation memory and runtime during use. The user of the thermal model needs to consider thermal sensor accuracy, thermal interface material parameters, and manufacturing variations on the thermal solution. Examples of manufacturing variations include airflow tolerance from a fan, performance tolerance of the heat pipe and vapor chamber, and the manufacturing variation of attaching fins to the heat-sink base and the flatness of the surface.

Simplified Model

A simplified model seeks to capture the thermal behavior of the package more accurately to predict the junction temperature with reduced package modeling complexity. Unlike a full detailed model, simplified models are computationally efficient and work well in an integrated system simulation environment. Simplified models are appropriate in the early stages of a design to have an estimated value of the thermal solution. However, a Detailed Model should be completed before finalizing a design.

A simplified model is available on the Xilinx support download center under UltraScale+ FPGAs - Package Thermal Models. Simplified models are available in both Ansys IcePak and Mentor FloTHERM formats.

The constructed model must accurately represent the package, especially if your simulation tool is not FloTHERM or Icepack. The definition of the TIM1.5 or contact surface for the top of the simplified model must be correctly defined for the package to produce the correct results. This simplified model has a defined top-contact surface of the die, which may not be the full package size.

When using the detailed model, account for the following:

1. Use the correct top surface contact for the package when modeling TIM on top of the detailed model, as the top surface contact may not be the actual full package size.
2. The temperature junction monitor point is at the die center. The junction monitor point needs to be positioned or added to the relevant location for your design.
3. You must replace the default power with your specific power requirement, especially if the power density varies throughout the die.

Two-Resistor Model

A two-resistor thermal model is not recommended because with different thermal solutions, the heat spreading inside the package varies. The same variation of (Θ_{JB}) also occurs when the package is mounted in a PCB with different layers and the PCB can dissipate its heat to the surrounding ambient environment. The thermal resistance from

junction to case (Θ_{JC}) and the thermal resistance of junction to board (Θ_{JB}) as functions of the surrounding conditions are available.

Do not to place a thermocouple between the die and any surface in contact with it because it could create a poor thermal contact and lead to the package overheating. Junction temperature values should be taken using the System Monitor.

Table 1-4 shows the variation of Θ_{JC} functions of the surrounding conditions and Table 1-5 shows the thermal resistance from junction to board, Θ_{JB}, for the selected device/package combinations. The reported Θ_{JC} and Θ_{JB} enable comparison of different packages under the same condition.

Table 1-4: **Variation of Θ_{JC} with Different External Thermal Solution by Customer**

Device	h (W/m^2 K)	100	1000	5000	10000	JEDEC
XCVU11P-FSGD2104	Θ_{JC}	0.004	0.004	0.004	0.004	0.004
XCVU9P-FSGD2104	Θ_{JC}	0.003	0.003	0.003	0.003	0.003
XCVU13P-FIGD2104, XCVU13P-FSGA2577	Θ_{JC}	0.003	0.003	0.003	0.003	0.003
XCVU31P-FSVH1924	Θ_{JC}	0.367	0.324	0.247	0.213	0.055
XCVU33P-FSVH2104	Θ_{JC}	0.306	0.270	0.208	0.180	0.034
XCVU35P-FSVH2104	Θ_{JC}	0.145	0.127	0.100	0.088	0.017
XCVU35P-FSVH2892	Θ_{JC}	0.142	0.126	0.099	0.087	0.017
XCVU37P-FSVH2892	Θ_{JC}	0.086	0.078	0.065	0.059	0.013
XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, XCZU28DR-FSVE1156	Θ_{JC}	0.0189	0.0188	0.0186	0.0183	0.0164
XCZU25DR-FSVG1517 XCZU27DR-FSVG1517 XCZU28DR-FSVG1517	Θ_{JC}	0.0190	0.0188	0.0185	0.0170	0.0164
XCZU29DR-FSVF1760	Θ_{JC}	0.0190	0.0188	0.0185	0.0183	0.0164
XCVU27P-FIGD2104 XCVU27P-FSGA2577 XCVU29P-FIGD2104 XCVU29P-FSGA2577	Θ_{JC}	0.003	0.003	0.003	0.003	0.003
XCVU19P-FSVA3824	Θ_{JC}	0.002	0.002	0.002	0.002	0.002
XCVU23P-VSVA1365	Θ_{JC}	0.01	0.01	0.01	0.01	0.01

Table 1-5: **Variation of Θ_{JB} with the Different External Thermal Solutions**

Devices	h (W/m² K)	$K_{x,y}$=25, K_z=0.4 K_e=0.78	$K_{x,y}$=50, K_z=0.75 K_e=1.48	$K_{x,y}$=90, K_z=1.5 K_e=2.45	$K_{x,y}$=110, K_z=5 K_e=9.6
XCVU11P-FSGD2104	100	0.324 (modified JEDEC)	0.292	0.253	0.219
XCVU9P-FSGD2104	100	0.340 (modified JEDEC)	0.300	0.257	0.220
XCVU13P-FIGD2104X CVU13P-FSGA2577	100	0.272 (modified JEDEC)	0.244	0.212	0.185
XCVU31P-FSVH1924	100	0.70 (modified JEDEC)	0.63	0.54	0.47
XCVU33P-FSVH2104	100	0.74 (modified JEDEC)	0.66	0.56	0.47
XCVU35P-FSVH2104	100	0.45 (modified JEDEC)	0.40	0.33	0.28
XCVU35P-FSVH2892	100	0.55 (modified JEDEC)	0.48	0.40	0.33
XCVU37P-FSVH2892	100	0.39 (modified JEDEC)	0.34	0.28	0.24
XCZU25DR-FSVE1156 XCZU27DR-FSVE1156 XCZU28DR-FSVE1156		1.13	0.99	0.86	0.76
XCZU25DR-FSVG1517 XCZU27DR-FSVG1517 XCZU28DR-FSVG1517		1.18	1.02	0.86	0.74
XCZU29DR-FSVF1760		1.25	1.05	0.88	0.75
XCVU27P-FIGD2104 XCVU27P-FSGA2577 XCVU29P-FIGD2104 XCVU29P-FSGA2577	100	0.272 (modified JEDEC)	0.244	0.212	0.185
XCVU19P-FSVA3824	100	0.292 (modified JEDEC)	0.271	0.252	0.238
XCVU23P-VSVA1365	100	1.03 (modified JEDEC)	0.950	0.830	0.880

The effective thermal conductivity of the PCB, k_e, as referenced in Lemczyk et al. (1992)

$$k_e = \frac{2(k_x k_z)}{k_x + k_z} \quad \text{Equation 1-7}$$

The relation of Θ_{JB} as a function of k_e can be correlated as shown in Figure 1-27 through Figure 1-37:

For XCVU11P-FSGD2104: $\Theta_{JB} = 0.3063k_e^{-0.157}$

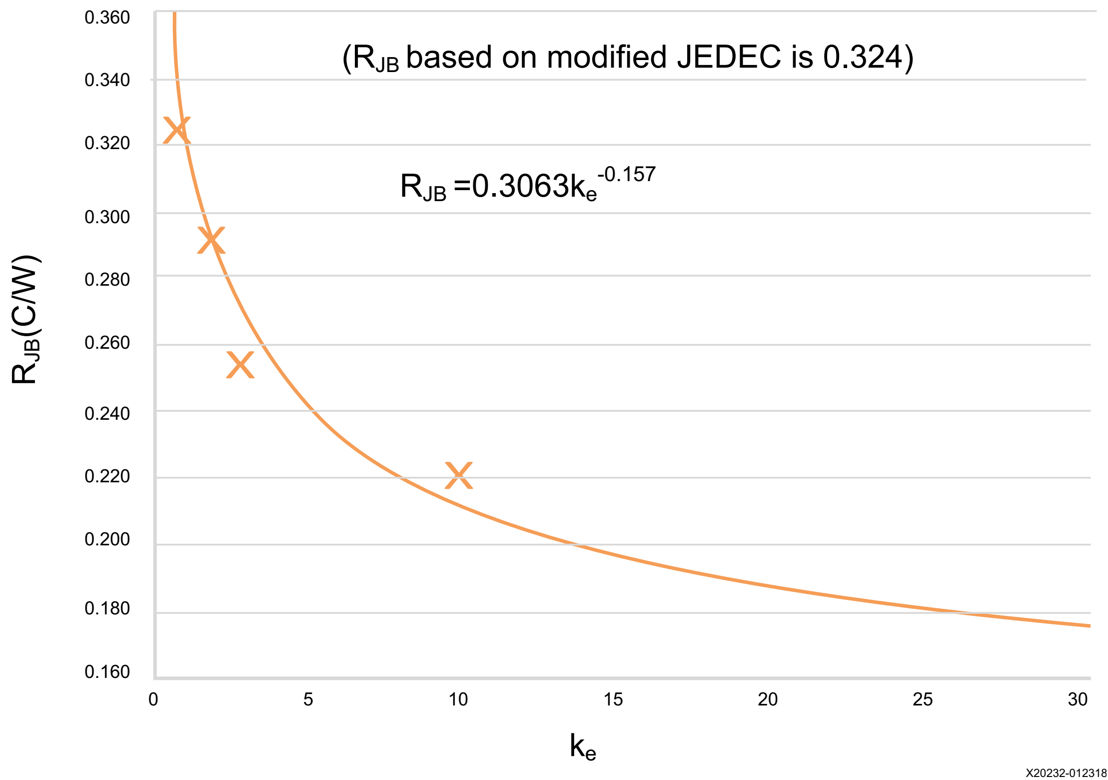

Figure 1-27: **XCVU11P-FSGD2104: The Relationship Between Θ_{JB} and k_e**

For XCVU9P-FSGD2104: $\Theta_{JB} = 0.318k_e^{-0.173}$

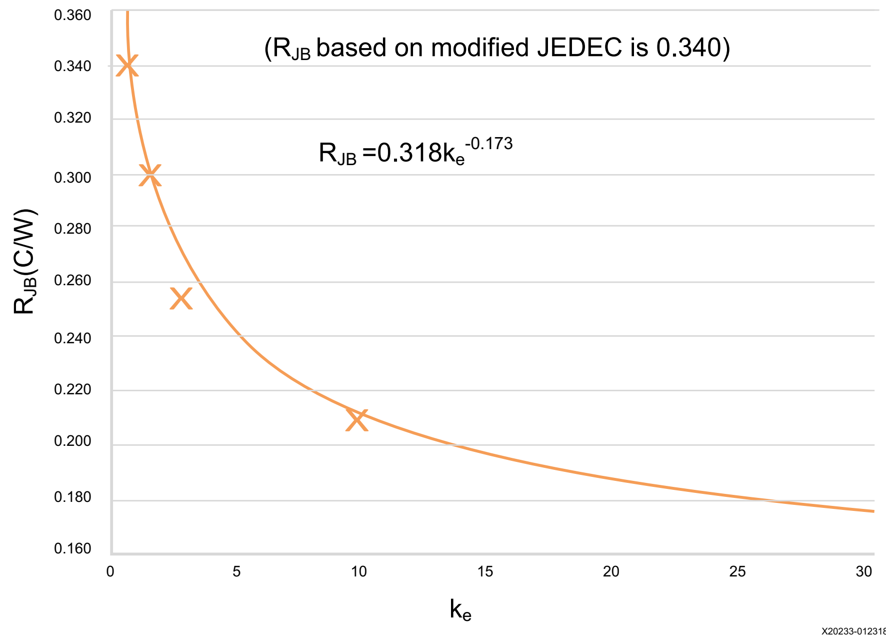

Figure 1-28: **XCVU9P-FSGD2104: The Relationship Between Θ_{JB} and k_e**

For XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577: $\Theta_{JB} = 0.2564k_e^{-0.154}$

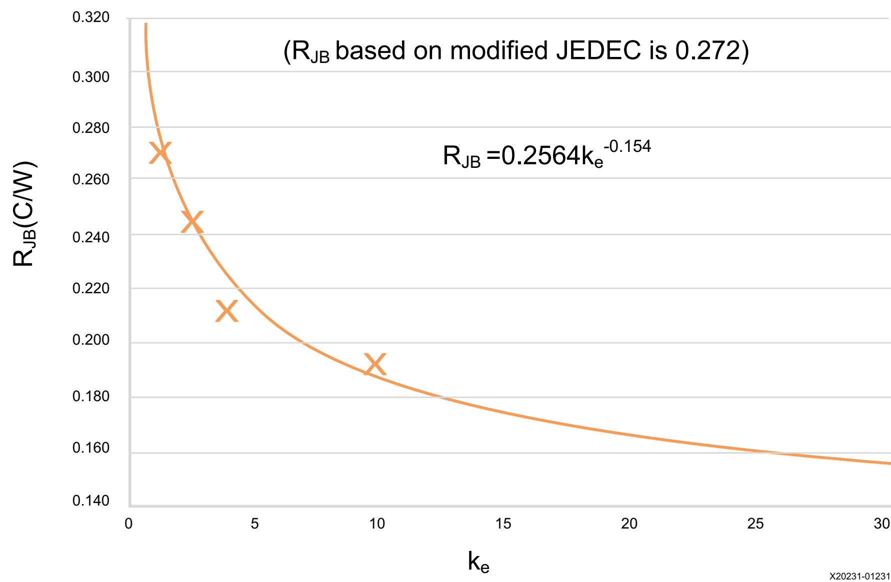

Figure 1-29: **XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577: The Relationship Between Θ_{JB} and k_e**

For XCVU31P-FSVH1924: $\Theta_{JB} = 0.66k_e^{-0.16}$

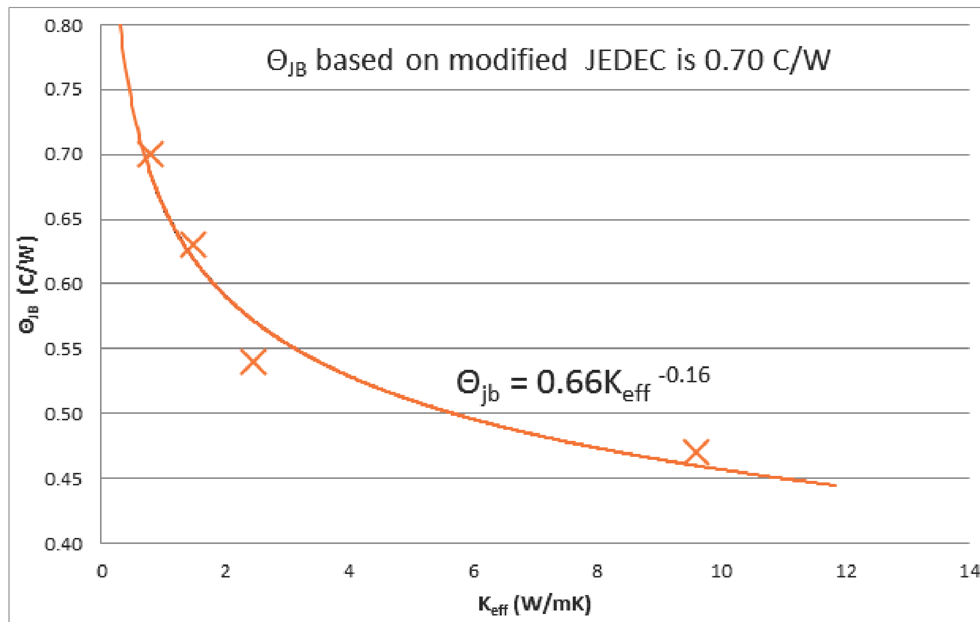

Figure 1-30: **XCVU31P-FSVH1924: The Relationship Between Θ_{JB} and k_e**

For XCVU33P-FSVH2104 $\Theta_{JB} = 0.6961k_e^{-0.182}$

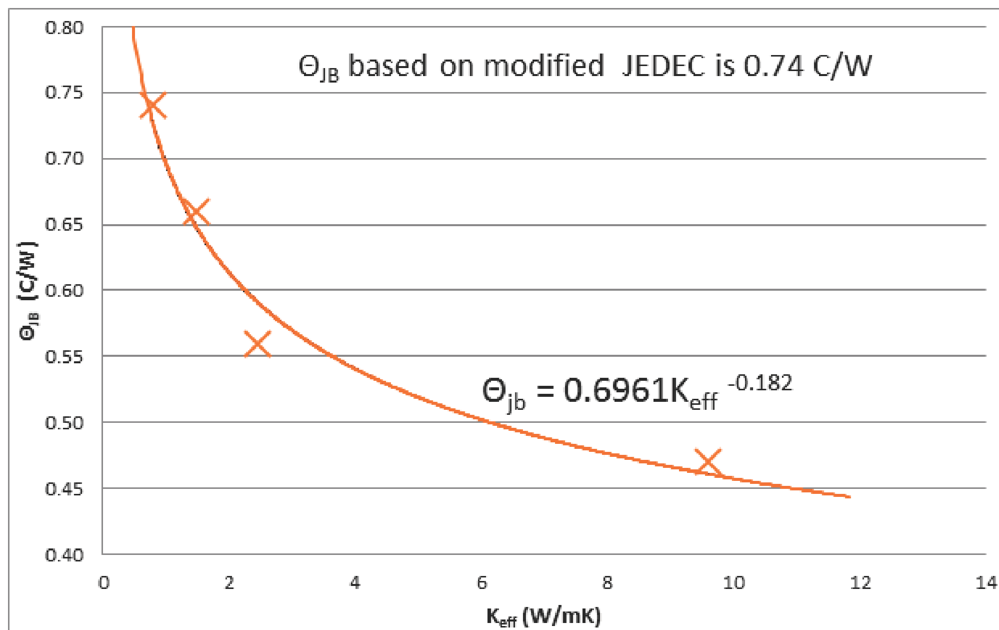

Figure 1-31: **XCVU33P-FSVH2104: The Relationship Between Θ_{JB} and k_e**

For XCVU35P-FSVH2104 $\Theta_{JB} = 0.4206k_e^{-0.191}$

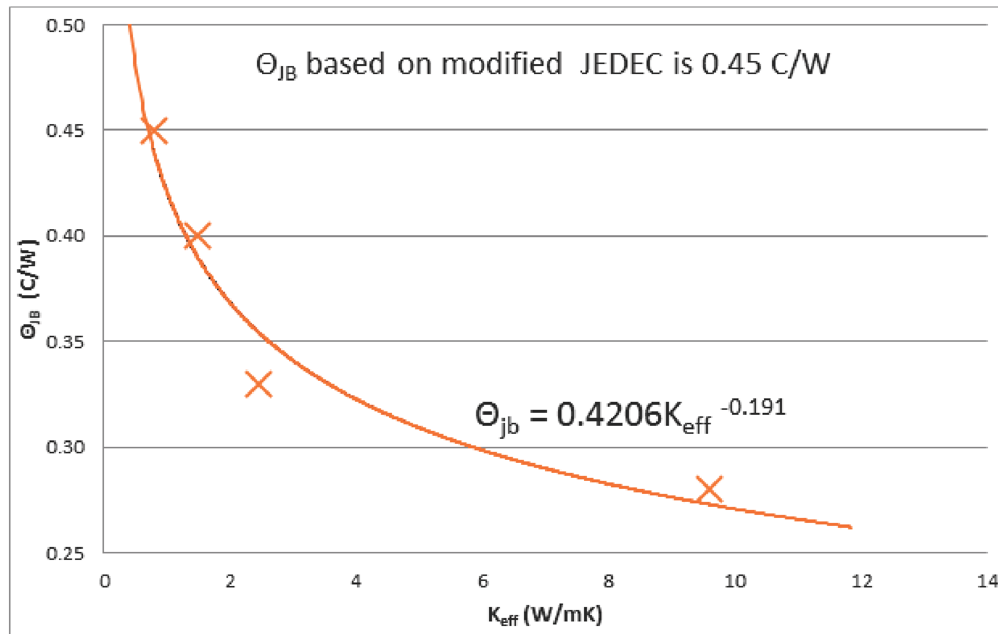

Figure 1-32: **XCVU35P-FSVH2104: The Relationship Between Θ_{JB} and k_e**

For XCVU35P-FSVH2892 $\Theta_{JB} = 0.5115k_e^{-0.205}$

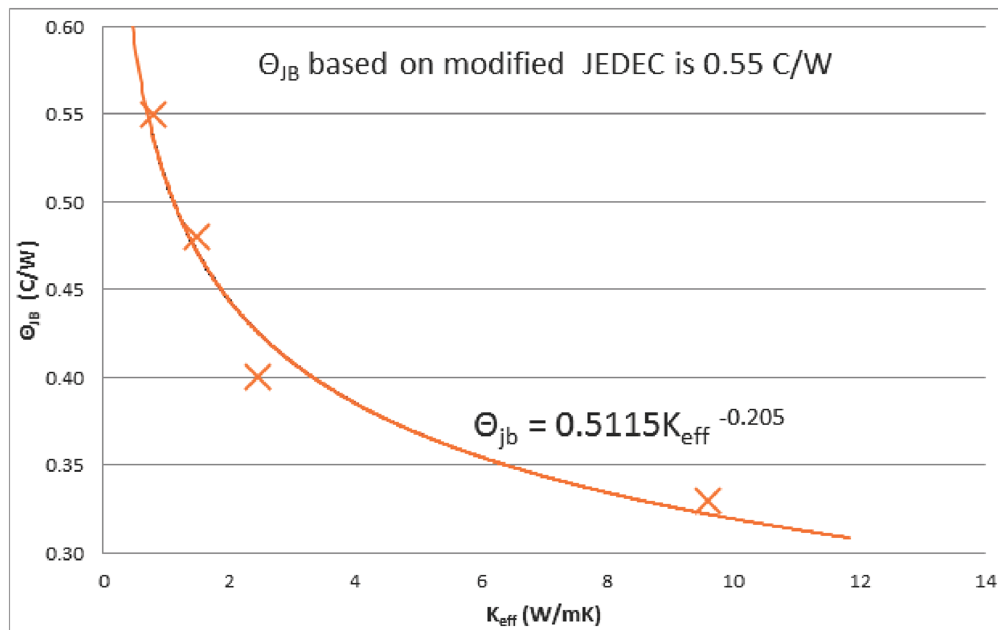

Figure 1-33: **XCVU35P-FSVH2892: The Relationship Between Θ_{JB} and k_e**

For XCVU37P-FSVH2892 $\Theta_{JB} = 0.3606k_e^{-0.194}$

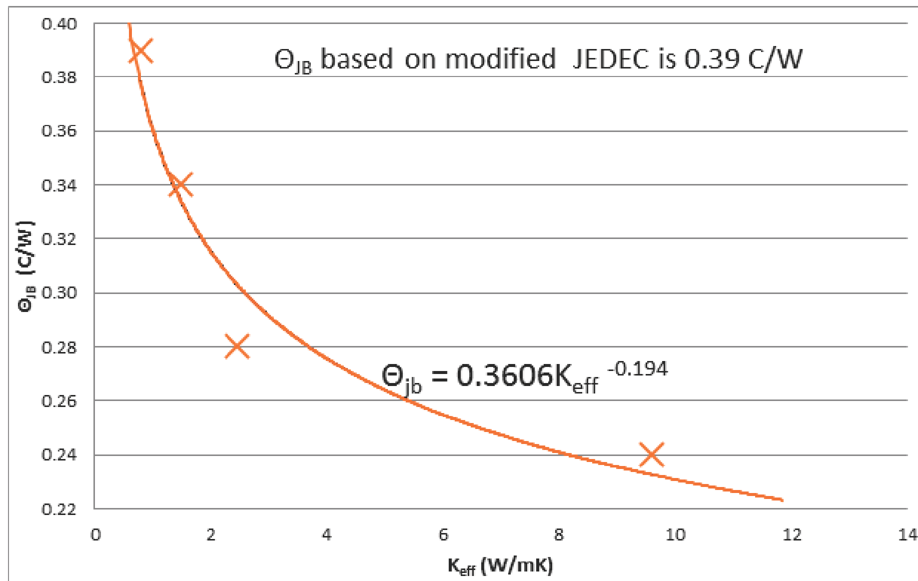

Figure 1-34: **XCVU37P-FSVH2892: The Relationship Between Θ_{JB} and k_e**

For XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156: $\Theta_{JB} = 1.0518k_e^{-0.156}$

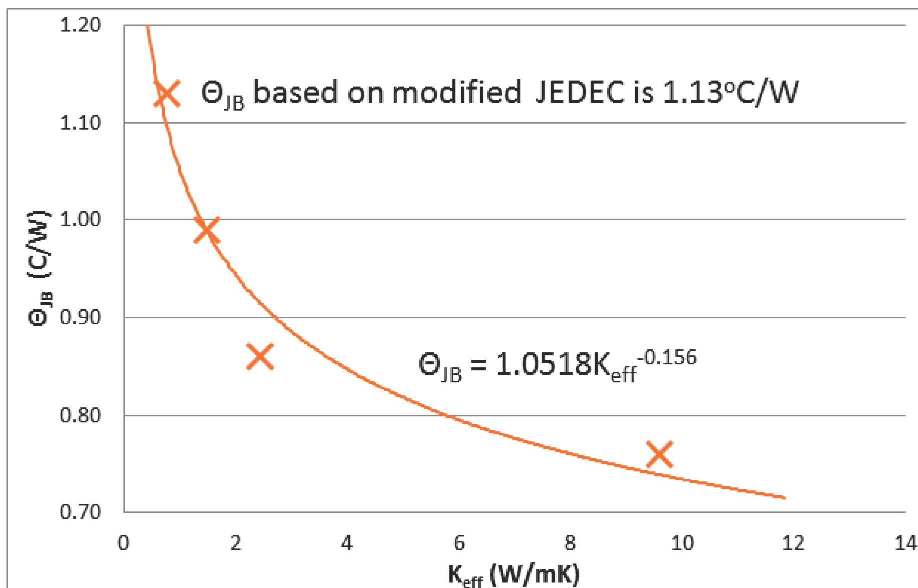

Figure 1-35: **XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, andXCZU28DR-FSVE1156: The Relationship Between Θ_{JB} and k_e**

For XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517: $\Theta_{JB} = 1.0895k_e^{-0.185}$

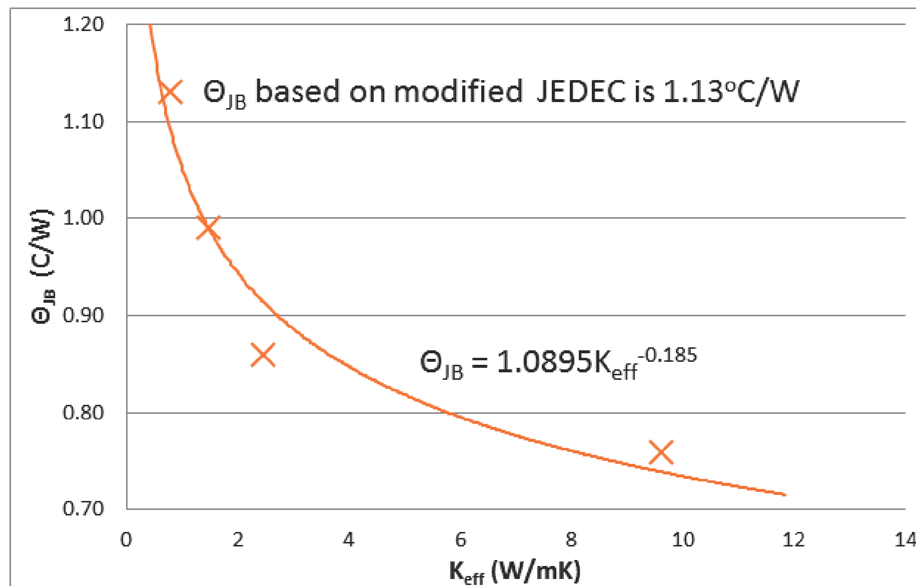

Figure 1-36: **XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517: The Relationship Between Θ_{JB} and k_e**

For XCZU29DR-FSVF1760: $\Theta_{JB} = 1.1382k_e^{-0.2}$

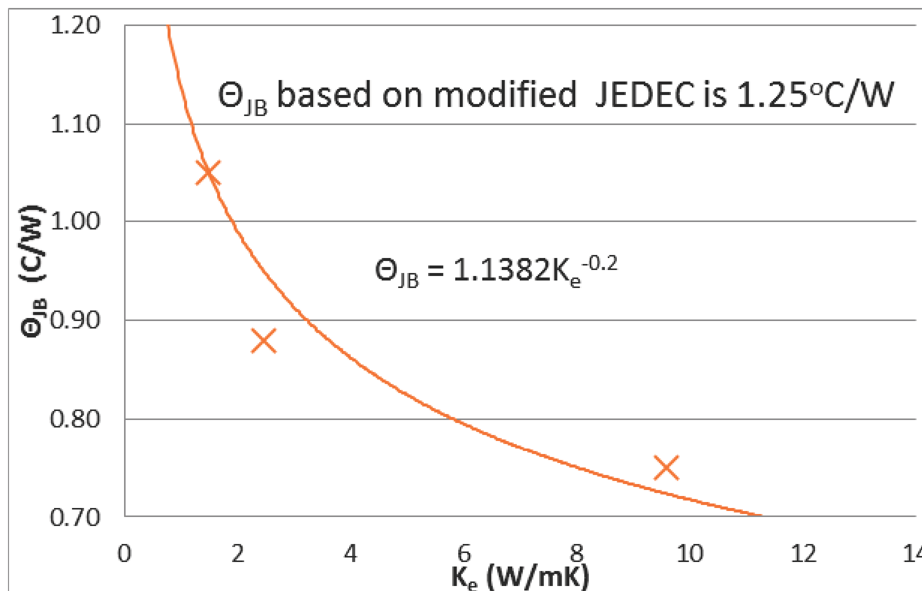

Figure 1-37: **XCZU29DR-FSVF1760: The Relationship Between Θ_{JB} and k_e**

For XCVU19P-FSVA3824: $\Theta_{JB} = 0.2807k_e^{-0.08}$

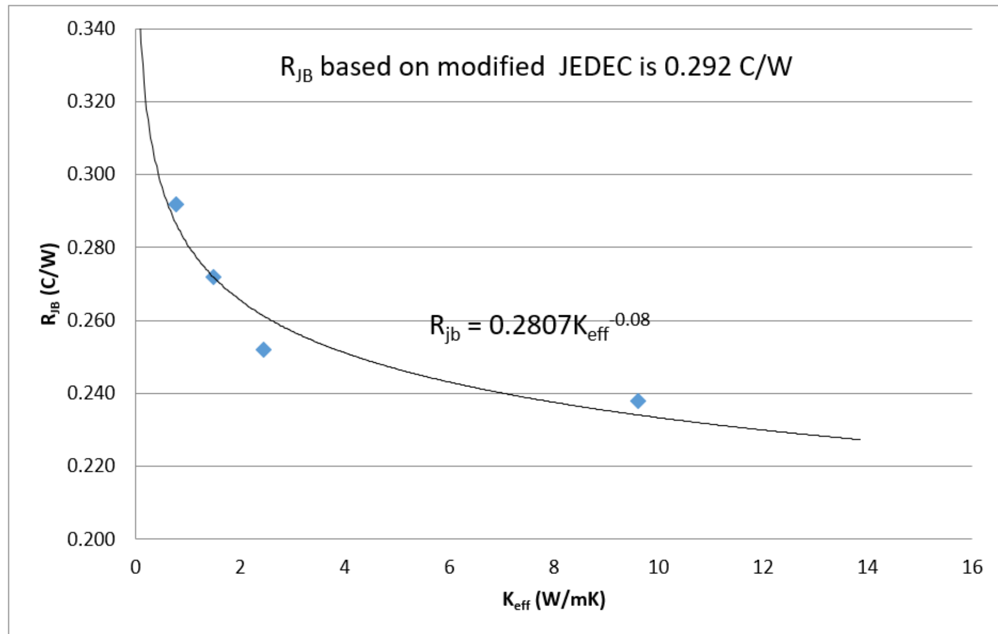

Figure 1-38: **XCVU19P-FSVA3824: The Relationship Between Θ_{JB} and k_e**

For XCVU23P-VSVA1365: $\Theta_{JB} = 0.9657k_e^{-0.063}$

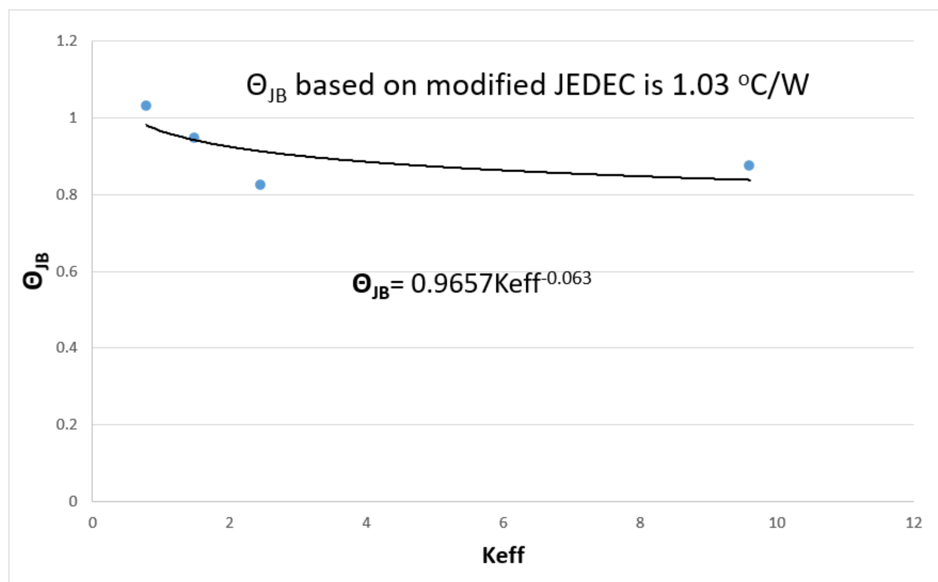

Figure 1-39: **XCVU23P-VSVA1365: The Relationship Between Θ_{JB} and k_e**

Detailed Model

A detailed thermal model is a direct representation of the device and package. This model provides geometric details describing the packaging, specifically in regards to the die, under fill, substrate, and solder balls or leads. Each specific component in the detailed model has associated material properties.

Due to the computationally intensive nature of this model, do not use it early in thermal management development when several iterations might be needed to find the solution. Instead, use the Simplified Model of the package, saving the detailed model for the end of the development cycle to more precisely verify the system's thermal margin.

For accurate results, a constructed model must accurately represent the package, especially if your simulation tool is not FloTHERM or IcePak. Because the detailed model is more accurate when compared to a DEPLHI or two-resistor model, your simulations must account for any accuracy differences.

DELPHI Model

The DELPHI model seeks to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes. Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. The DELPHI model is more appropriate for estimating the value of the thermal solution in the early stages of a design.

The DELPHI model is available on the Xilinx support download center (under *Model Type*, see Package Thermal Models).

Table 1-6 through Table 1-13 show the thermal resistances for Xilinx's lidless flip-chip packages.

Table 1-6: **XCVU11P-FSGD2104 DELPHI Thermal Resistance Value (°C/watt)**

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Junction	0.004	0.39	∞	5.38	225.00
Top Inner		∞	∞	135.18	∞
Bottom Inner			∞	17.79	∞
Top Outer				∞	∞
Bottom Outer					1.44

Table 1-7: **XCVU9P-FSGD2104 DELPHI Thermal Resistance Value (°C/watt)**

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Junction	0.003	0.40	∞	4.78	75.00
Top Inner		∞	∞	661.15	∞
Bottom Inner			∞	35.21	∞
Top Outer				∞	∞
Bottom Outer					1.43

Table 1-8: **XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577 DELPHI Thermal Resistance Values (°C/watt)**

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Junction	0.003	0.38	∞	1.68	100.00
Top Inner		∞	∞	∞	∞
Bottom Inner			∞	4.29	3.6
Top Outer				∞	∞
Bottom Outer					∞

Table 1-9: **XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156 DELPHI Thermal Resistance Values (°C/watt)**

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Junction	0.02	0.62	6.98	7.25	41.90
Top Inner		∞	∞	∞	∞
Bottom Inner			143.39	37.6	75.73
Top Outer				6.19	6.12
Bottom Outer					66.71

Table 1-10: **XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517 DELPHI Thermal Resistance Values (°C/watt)**

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Junction	0.02	0.43	7.45	7.99	458.49
Top Inner		∞	∞	∞	∞
Bottom Inner			25.01	30.73	∞
Top Outer				6.16	5.12
Bottom Outer					27.44

Table 1-11: **XCZU29DR-FSVF1760 DELPHI Thermal Resistance Values (°C/watt)**

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Junction	0.02	0.51	7.43	7.73	31.69
Top Inner		∞	∞	∞	∞

Table 1-11: **XCZU29DR-FSVF1760 DELPHI Thermal Resistance Values (°C/watt)**

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Bottom Inner			59.99	63.63	230.15
Top Outer				6.16	4.60
Bottom Outer					18.79

Table 1-12: **XCVU19P-FSVA3824 DELPHI Thermal Resistance Values (°C/watt)**

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Junction	0.004	0.22		2.36	70.24
Top Inner		∞	∞	∞	∞
Bottom Inner			16.73	∞	10.52
Top Outer				∞	∞
Bottom Outer					∞

Table 1-13: **XCVU23P-VSVA1365 DELPHI Thermal Resistance Values (°C/watt)**

	Top Inner	Bottom Inner	Top Outer	Bottom Outer	Side
Junction	0.02	0.62	6.03	6.4	29.79
Top Inner		∞	∞	∞	∞
Bottom Inner			53.02	45.01	605.37
Top Outer				∞	5.06
Bottom Outer					7.62

The DELPHI model is available pre-compiled in both Ansys IcePak and Mentor FloTHERM. If using a different thermal modeling tool, the DELPHI model can be constructed using the above thermal resistances. These thermal resistances must be in a block with the structure shown in Figure 1-40 and the dimensions specified in Table 1-14.

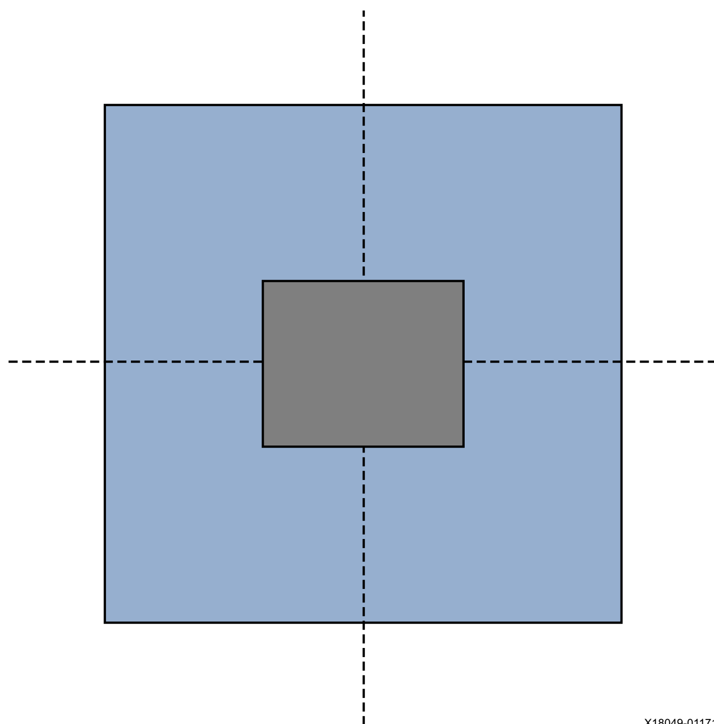

Figure 1-40: **The Top Inner Area Location in the Top Outer Area**

Table 1-14: **Top Inner and Top Outer Dimensions (mm)**

Device	Top Inner		Top Outer		Side
	X	Y	X	Y	Z
XCVU11P-FSGD2104	28.72	27.78	47.5	47.5	2.724
XCVU9P-FSGD2104	25.55	34.44	47.5	47.5	2.724
XCVU13P-FSGD2104 XCVU13P-FSGA2577	28.72	37.08	52.5	52.5	2.724
XCZU28DR-FSVE1156 XCZU25DR-FSVE1156 XCZU27DR-FSVE1156	21.13	18.144	35	35	2.272
XCZU28DR-FSVG1517 XCZU25DR-FSVG1517 XCZU27DR-FSVG1517	21.13	18.144	40	40	2.272
XCZU29DR-FSVF1760	21.13	18.144	42.5	42.5	2.272
XCVU27P-FIGD2104 XCVU27P-FSGA2577 XCVU29P-FIGD2104 XCVU29P-FSGA2577	28.72	37.08	52.5	52.5	2.724
XCVU19P-FSVA3824	46.50	30.14	65	65	2.72
XCVU23P-VSVA1365	26.24	17.91	40	40	3.16

The bottom inner area is shown in Figure 1-41 and the dimensions are specified in Table 1-15.

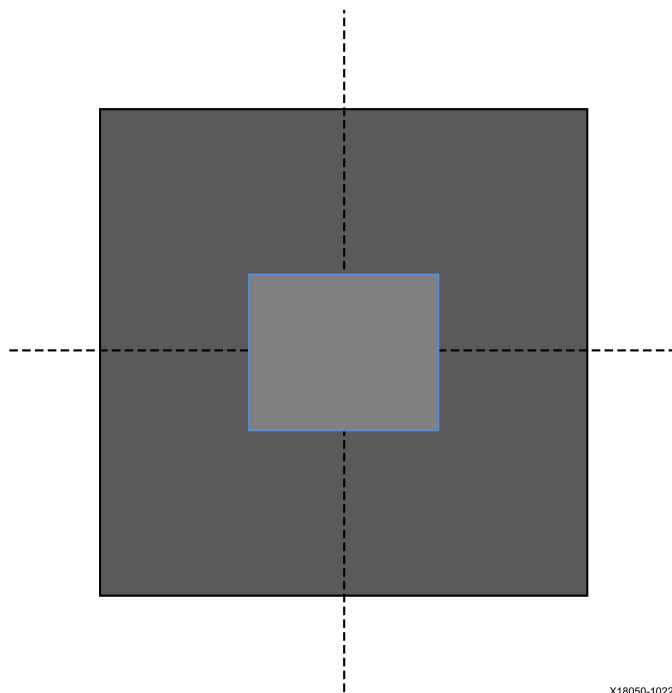

Figure 1-41: **The Bottom Inner Area Location in the Bottom Outer Area**

Table 1-15: **Bottom Inner and Bottom Outer Dimensions (mm)**

Device	Bottom Inner		Bottom Outer	
	X	Y	X	Y
XCVU11P-FSGD2104	28.72	27.78	47.5	47.5
XCVU9P-FSGD2104	25.56	34.46	47.5	47.5
XCVU13P-FIGD2104 XCVU13P-FSGA2577	30.07	38.82	52.5	52.5
XCZU25DR-FSVE1156 XCZU27DR-FSVE1156 XCZU28DR-FSVE1156	21.22	18.22	35	35
XCZU25DR-FSVG1517 XCZU27DR-FSVG1517 XCZU28DR-FSVG1517	21.27	18.27	40	40
XCZU29DR-FSVF1760	21.27	18.27	42.5	42.5
XCVU27P-FIGD2104 XCVU27P-FSGA2577 XCVU29P-FIGD2104 XCVU29P-FSGA2577	30.07	38.82	52.5	52.5
XCVU19P-FSVA3824	44.23	29.32	65	65
XCVU23P-VSVA1365	26.75	18.26	40	40

For accurate results, ensure that the constructed model accurately represents the package, especially if the simulation tool is not FloTHERM or IcePak. The reported DELPHI model has better accuracy compared to the detail model versus solely the two-resistor model.

Model Comparisons

This section shows model comparisons between simplified models, DELPHI models, and detailed models, as available. Temperature comparisons are made using degrees Celsius. These comparisons are based on Icepak simulations.

Table 1-16: **Comparison between the Detailed Model and Different DELPHI Model for XCVU11P-FSGD2104**

Boundary	h (W/m^2 K)	Detailed Model	DELPHI Model
Top Boundary	100	X	0.999X
	10000	X	1.000X
Bottom Boundary	100 (k_e = 0.78)	X	0.991X
	100 (k_e = 9.6)	X	1.009X

Table 1-17: **Comparison between the Detailed Model and Different DELPHI Model for XCVU9P-FSGD2104**

Boundary	h (W/m^2 K)	Detailed Model	DELPHI Model
Top Boundary	100	X	1.000X
	10000	X	1.000X
Bottom Boundary	100 (k_e = 0.78)	X	0.995X
	100 (k_e = 9.6)	X	1.009X

Table 1-18: **Comparison between the Detailed Model and Different DELPHI Model for XCVU13P-FIGD2104, XCVU13P-FSGA2577, XCVU27P-FIGD2104, XCVU27P-FSGA2577, XCVU29P-FIGD2104, and XCVU29P-FSGA2577**

Boundary	h (W/m^2 K)	Detailed Model	DELPHI Model
Top Boundary	100	X	1.000X
	10000	X	0.929X
Bottom Boundary	100 (k_e = 0.78)	X	1.040X
	100 (k_e = 9.6)	X	1.054X

Table 1-19: **Comparison between the Simplified Model and Detailed Model for XCVU31P-FSVH1924**

Boundary	h (W/m^2 K)	Detailed Model T_J	Simplified Model T_J
Top Boundary	100	X	1.0178X
	10000	X	0.9860X
Bottom Boundary	100 (k_e = 0.78)	X	1.0144X
	100 (k_e = 9.6)	X	1.0310X

Table 1-20: **Comparison between the Simplified Model and Detailed Model for XCVU33P-FSVH2104**

Boundary	h (W/m^2 K)	Detailed Model T_J	Simplified Model T_J
Top Boundary	100	X	1.0126X
	10000	X	0.9600X
Bottom Boundary	100 (k_e = 0.78)	X	1.0106X
	100 (k_e = 9.6)	X	1.0297X

Table 1-21: **Comparison between the Simplified Model and Detailed Model for XCVU35P-FSVH2104**

Boundary	h (W/m^2 K)	Detailed Model T_J	Simplified Model T_J
Top Boundary	100	X	1.0114X
	10000	X	0.9890X
Bottom Boundary	100 (k_e = 0.78)	X	1.0083X
	100 (k_e = 9.6)	X	1.0245X

Table 1-22: **Comparison between the Simplified Model and Detailed Model for XCVU35P-FSVH2892**

Boundary	h (W/m^2 K)	Detailed Model T_J	Simplified Model T_J
Top Boundary	100	X	1.0103X
	10000	X	0.9860X
Bottom Boundary	100 (k_e = 0.78)	X	1.0126X
	100 (k_e = 9.6)	X	1.0314X

Table 1-23: **Comparison between the Simplified Model and Detailed Model for XCVU37P-FSVH2892**

Boundary	h (W/m^2 K)	Detailed Model T_J	Simplified Model T_J
Top Boundary	100	X	1.0100X
	10000	X	0.9820X
Bottom Boundary	100 (k_e = 0.78)	X	1.0086X
	100 (k_e = 9.6)	X	1.0242X

Table 1-24: **Comparison between the Detailed Model and DELPHI Model for XCZU25DR-FSVE1156, XCZU27DR-FSVE1156, and XCZU28DR-FSVE1156**

Boundary	h (W/m² K)	Detailed Model T_J	Detailed Model T_J
Top Boundary	100	X	1.0002X
	10000	X	0.9948X
Bottom Boundary	100 (k_e = 0.78)	X	0.9938X
	100 (k_e = 9.6)	X	0.9944X

Table 1-25: **Comparison between the Detailed Model and DELPHI Model for XCZU25DR-FSVG1517, XCZU27DR-FSVG1517, and XCZU28DR-FSVG1517**

Boundary	h (W/m² K)	Detailed Model T_J	Detailed Model T_J
Top Boundary	100	X	0.9998X
	10000	X	0.9974X
Bottom Boundary	100 (k_e = 0.78)	X	0.9867X
	100 (k_e = 9.6)	X	0.9846X

Table 1-26: **Comparison between the Detailed Model and DELPHI Model for XCZU29DR-FSVF1760**

Boundary	h (W/m² K)	Detailed Model T_J	Detailed Model T_J
Top Boundary	100	X	1.0003X
	10000	X	0.9948X
Bottom Boundary	100 (k_e = 0.78)	X	0.9762X
	100 (k_e = 9.6)	X	0.9881X

Table 1-27: **Comparison between the Detailed Model and DELPHI Model for XCVU19P-FSVA3824**

Boundary	h (W/m² K)	Detailed Model T_J	Detailed Model T_J
Top Boundary	100	X	1.1480X
	10000	X	1.0868X
Bottom Boundary	100 (k_e = 0.78)	X	1.0393X
	100 (k_e = 9.6)	X	1.0044X

Table 1-28: **Comparison between the Detailed Model and DELPHI Model for XCVU23P-VSVA1365**

Boundary	h (W/m² K)	Detailed Model T_J	Detailed Model T_J
Top Boundary	100	X	1.0034X
	10000	X	1.0136X
Bottom Boundary	100 (k_e = 0.78)	X	0.9295X
	100 (k_e = 9.6)	X	0.9433X

Example Heat Sink Thermal Performance

Figure 1-42 through Figure 1-44 present graphical data extracted from experiments done using the detailed thermal model with the VU13P-FIGD2104.

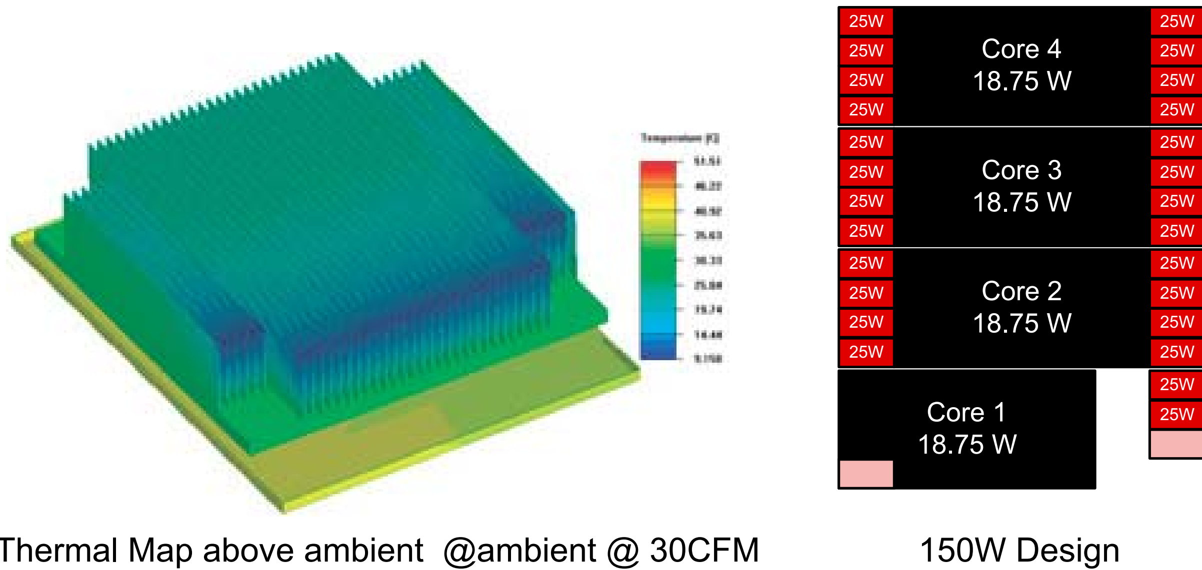

Figure 1-42: **Thermal Map Above Ambient at 30 CFM**

The graph data in Figure 1-43 and Figure 1-44 was extracted from thermal simulations using the VU13P-FIGD2104 package models with the heat sink solution shown above for a 150 Watt FPGA design. Using the first graph on the left in Figure 1-43, with an air flow rate of 30 CFM, you can calculate an effective thermal resistance of ~0.23°C/Watt. Using the second graph (Figure 1-43, on the right), the thermal solution operating at that airflow measures (at SYSMON) approximately 35°C above ambient, implying that the maximum ambient under these conditions can be as high as 65°C. Using an equivalent lidded package like the B2104 would yield a maximum ambient temperature of 58°C (7°C lower), as shown in the experiment data in Figure 1-44.

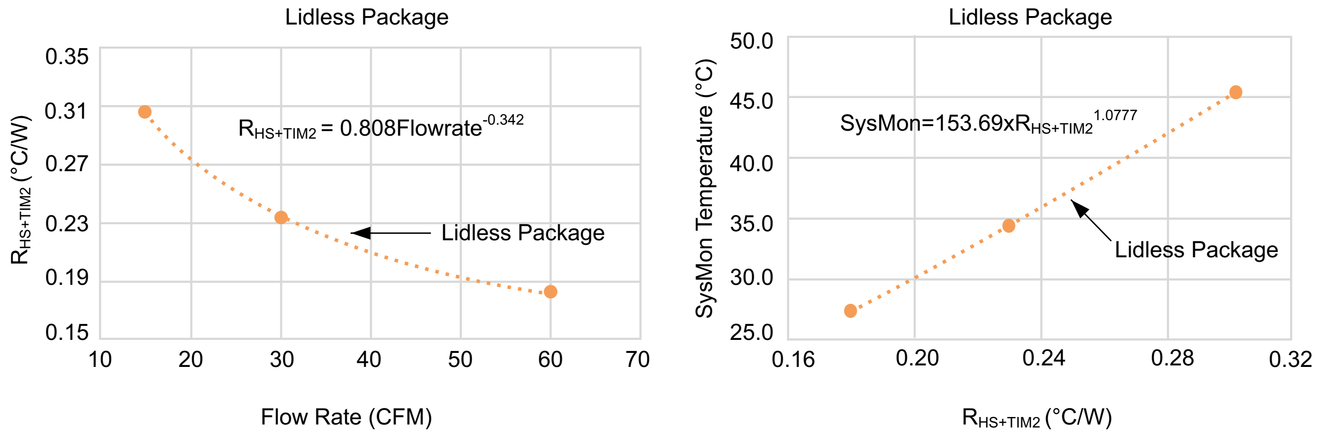

Figure 1-43: **150W Design**

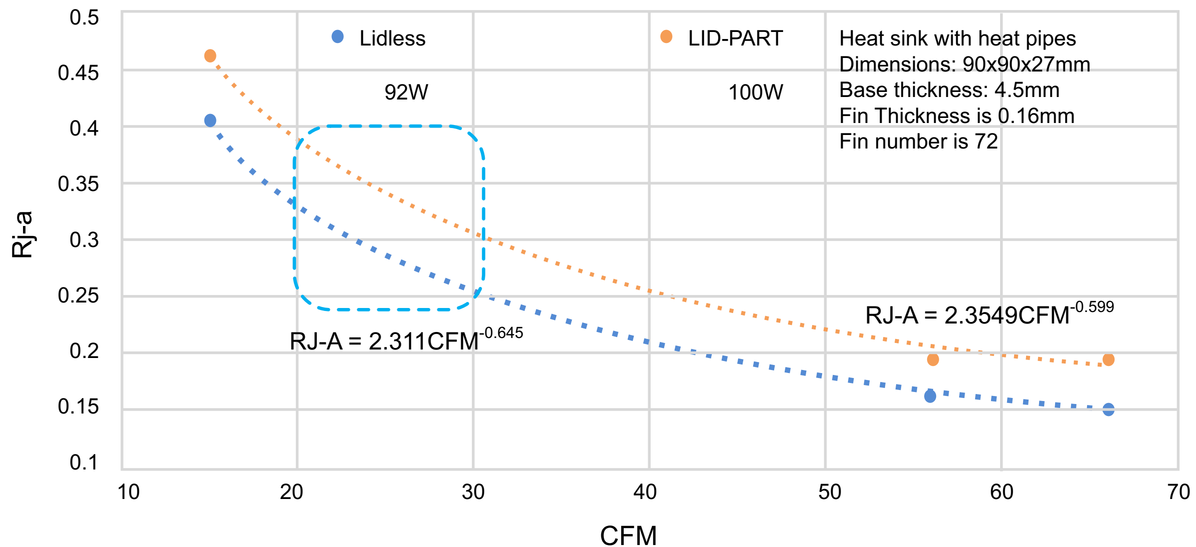

Figure 1-44: **Experimental Comparison between Lid and Lidless Devices**

The following pad recommendations are listed in the *Recommended PCB Design Rules for BGA Packages* chapter of *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide* (UG575) [Ref 1] and *Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide* (UG1075) [Ref 2], as appropriate.

- PCB Pad Recommendations
- Pad Type Recommendations
- Solder Pad Recommendation

Removing Heat Sink Phase Change Material

If heat sinks are removed or reworked, the phase change material residue must be removed from the die surface. Laird Technologies, Inc. has provided the following guidance for complete removal of the phase change material from the component.

Instructions:

1. Separate the Components
2. Clean Remaining Residue with Solvent

Also see Working with Laird Material for more information.

Separate the Components

At room temperature, use a back and forth twisting motion to break the bond between the phase change TIM and mated components (i.e., heat sink and CPU). See Figure 1-45.

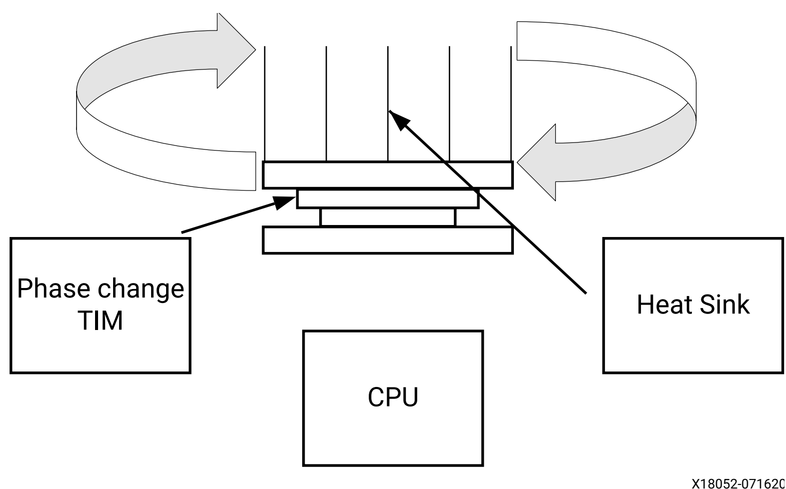

Figure 1-45: **Breaking the Bond between TIM and Mated Components**

For smaller components (typically 15 mm x 15 mm or less), the bond usually breaks free easily at room temperature. For larger components, situations where minimal movement is available, or if using fragile components, heat the component (preferable) or heat sink to between 40°C and 60°C before removal.

While the guideline is between 40°C and 60°C, you might find that heating to 35°C is adequate. Others might prefer to heat to 70°C so that the phase change TIM is very soft and the components are easy to separate.

Clean Remaining Residue with Solvent

Using a clean cloth/wipe, wet it with one of the solvents below and wipe away any remaining residue.

- Toluene (best)
- Acetone (very good)
- Isoparaffinic hydrocarbon (trade names Isopar and Soltrol) (very good)
- Isopropyl alcohol (OK)

Working with Laird Material

Safe handling, disposal, and first-aid measures for working with phase-change material are included in the Laird Technologies material safety data sheet (MSDS). Read the MSDS before using or handling. See the Laird Technologies, Inc. website, www.lairdtech.com.

Measurement Debug

When performing in-system thermal testing, to ensure accurate data and not incur damage to the device, do not place a thermocouple in between the die and the heat sink. On the extreme side, it might cause additional mechanical and/or thermal stress to the die, leading to damage. Even if damage does not occur, it often leads to thicker and or uneven TIM thickness, leading to different thermal performance from a system without the thermocouple. To obtain the device temperature, use System Monitor (SYSMON) because it is a non-invasive means to get accurate die measurements while debugging the system.

Reference Design Files

Download the reference design files for this application note from the Xilinx website.

Conclusion

This application note addresses the specific mechanical and thermal design requirements of the device and package combinations listed in Table 1-1. Further information on removing a heat sink, including removal of phase change material, is available in the *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide* (UG575) [Ref 1] and *Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide* (UG1075) [Ref 2], as appropriate.

XILINX

Appendix A

Recommended Thermal Solution Installation of Xilinx FCBGA Lidless Packages

Overview

This appendix presents the recommended installation procedure for the Xilinx FCBGA lidless packages. These devices are capable of generating high power and thus large amounts of heat, so a thermal solution (cooler) is required to dissipate the energy to keep the device working within the specific operating temperature limits. Attaching the cooler to the device with fasteners can be a challenge while not damaging the silicon.

Challenges

To achieve the best thermal conductivity, the interface between the silicon and cooler must have very good contact. Due to inevitable mechanical limitations, the two surfaces are not perfectly flat or smooth and a Thermal Interface Material (TIM) is typically applied to fill any imperfections.

The TIM grain size must be smaller than the gaps so it is only filling the voids and not creating a thick bond line between the two devices. A certain pressure is required to hold the two devices together, maintaining minimum bond line and not damaging the silicon. This pressure is usually provided by the device manufacturer.

The device should be attached to the thermal solution by mechanical fasteners. The installation process has to be well designed so that the pressure is evenly distributed over the silicon surface and the two surfaces are parallel with a specific pressure. The TIM is evenly spread filling the voids and maintaining the minimum bond line.

Installation Control

The assembly floor should have similar tools as listed here to ensure that the thermal solution is appropriately assembled on the top of the FCBGA.

IMPORTANT: *During heatsink installation, you must control the torque pressure so that it does not exceed 50 psi. It is recommended that you use a smart torque screwdriver that is calibrated for the correct fastening speed so that it does not exceed this pressure level. See Using Smart Torque Screwdriver for Assembly, page 62.*

Equipment and Calibration

The equipment used for the mechanical installation process are:

- Adjustable torque screwdriver or smart torque screwdriver (Figure A-1). See Using Smart Torque Screwdriver for Assembly, page 62 for more information about the advantages of using a smart torque screwdriver.
- Calibrator (Figure A-2)
- Tekscan FlexiForce A201 pressure gauge with multiple handle ELF system (Figure A-3)
- Tactilus free form square pressure sensors (Figure A-4)

Figure A-1: **Digital Torque Screwdriver (Top), Hios CL 2000 (Middle), and Hios CL 2000 (Bottom)**

X20659-041318

Figure A-2: **Screw Torque Calibrator – Hios HP-10**

FlexiForce

Physical Properties

Thickness	0.203 mm (0.008 in.)
Length	191 mm (7.5 in.)** (optional trimmed lengths: 152 mm (6 in.), 102 mm (4 in.), 51 mm (2 in.))
Width	14 mm (0.55 in.)
Sensing Area	9.53 mm (0.375 in.) diameter
Connector	3-pin Male Square Pin (center pin is inactive)
Substrate	Polyester
Pin Spacing	2.54 mm (0.1 in.)

X22241-011619

Figure A-3: **Pressure Gauge – Tekscan FlexiForce A201 Multiple Handle ELF System**

Figure A-4: **Pressure Sensor – Tactilus Free Form Square Sensors**

Figure A-5: **Tekscan Pressure Sensor – Zoomed In**

Using Smart Torque Screwdriver for Assembly

Xilinx recommends transient pressure to die of 50 psi or less. You must control the max torque by fastening screws slowly during heatsink assembly.

The recommended tool for assembly is the Atlas Copco MicroTorque handheld screwdriver with the following specifications:

- Model: ETD M 50 ABL V2
- Torque setting: MTF6000
- Software version: ToolsTalk MT 7.10.1.0

Figure A-6: **Atlas Copco MicroTorque Information**

Stress Comparison

The following figures show the stress fluctuations when using a smart torque screwdriver versus normal torque without speed control.

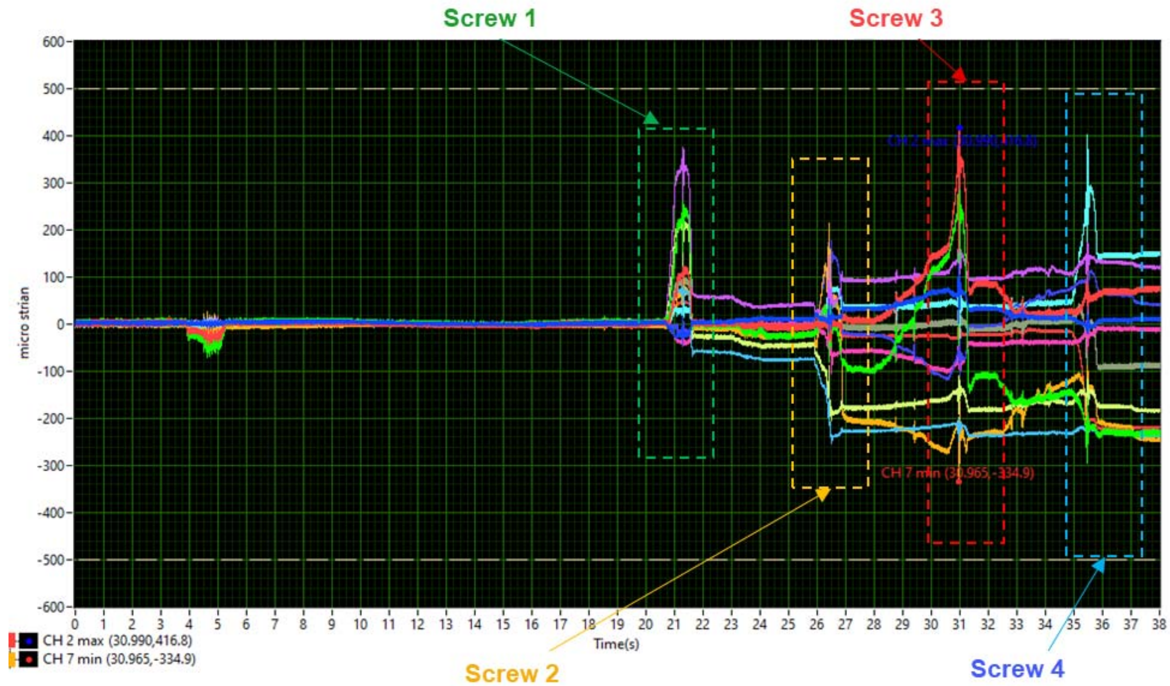

Figure A-7: **Stress with Normal Torque and No Speed Control (Not Recommended)**

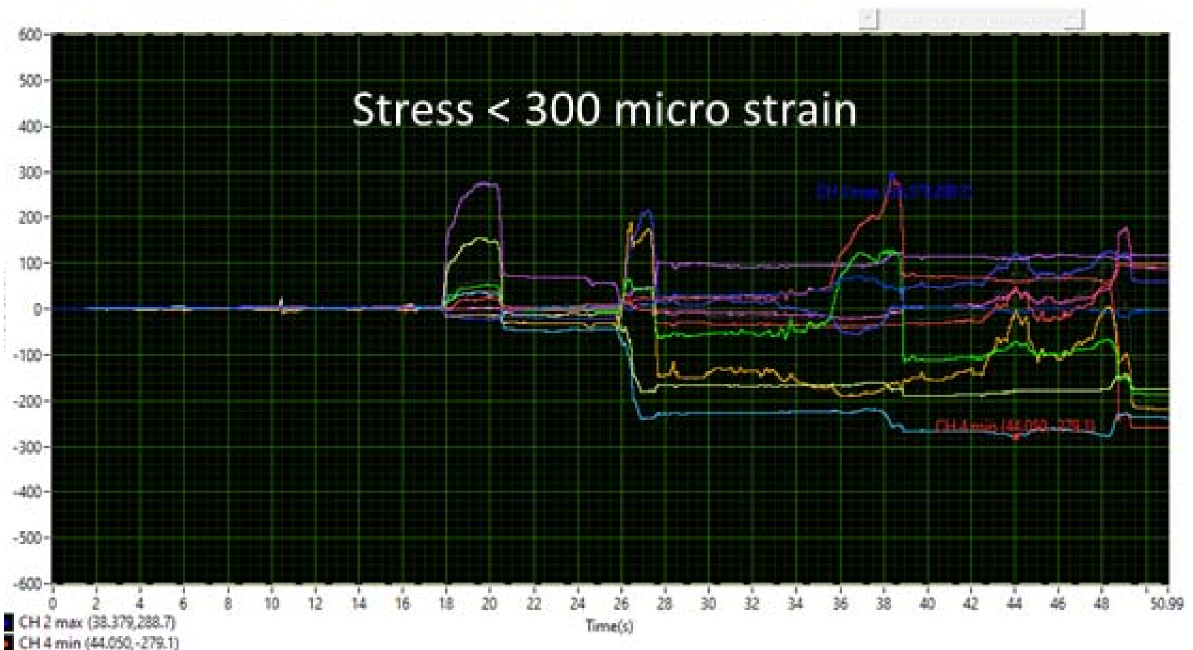

Figure A-8: **Stress with Smart Torque Screwdriver and Pressure Regulation (Recommended)**

Smart Torque Advantages

Using a smart torque screwdriver for assembly has the following advantages:

- You can optimize your quality and productivity by creating customized tightening programs.
- You can define the angle, speed, and torque, and easily change the settings whenever needed.
- You can set a workflow sequence with a batch sequence. The system will automatically apply the requested torque or instruct the operator, to ensure an error-proof and productive assembly.
- The torque screwdriver is integrated with the assembly jig.
- A user password controls access to the assembly program.
- The system provides real-time data monitoring and recording.

Figure A-9 shows the Smart Torque assembly workstation.

Figure A-9: **Smart Torque Assembly Workstation**

Best Engineering Practices to Control Stress on Package

To control stress on the package, follow the following best practices during assembly and manufacturing.

- Introduce backplate and edge bond to minimize the impact of the associated stress during assembly and the design.

  A backplate adds more support to the PCB and edge bond will provide more strength to the package to be hold to the PCB for better support.

- Validate your heatsink performance using the following measures:
    - Conduct pressure measurements using a gauge sensor.

      Note: Pressure measurement using a gauge sensor alone provides initial feedback on the heatsink contact, but it should not be the only measurement used to validate the heatsink performance.

    - Use a thermal test to validate the actual performance impact of the heatsink.
    - Use the strain gauge for mechanical design representation and validation.

      Note: Xilinx engineering practice is to validate that strain gauge is less than 500 µstrain diagonal. This strain gauge value should not impact the package mechanical structure integrity.

Set Up and Calibration

The torque of the screwdriver is calibrated by the calibrator and set to the torque (calculated based on the required pressure, die surface area) using the digital torque meter. For guidelines on pressure recommendations, see Heat Sink Pressure.

Note: Calibration of the digital torque calibrator/meter is done annually.

Process Qualification

Pressure and Force Verification

The screw-spring has to be designed with the required force that can achieve the target pressure at the interface between the die surface and the cooler. For example:

Chosen target pressure = 32 psi (between 20 and 50 psi)

Die size = 0.5 inch by 0.5 inch

Target force = 32 psi × 0.5 inch × 0.5 inch = 8 lbf

Installation Verification

Use the exact FCBGA, PCB, and thermal solution with the screws verified in the previous section. Install and verify if the target is achieved. The following figure shows the FCBGA board layouts.

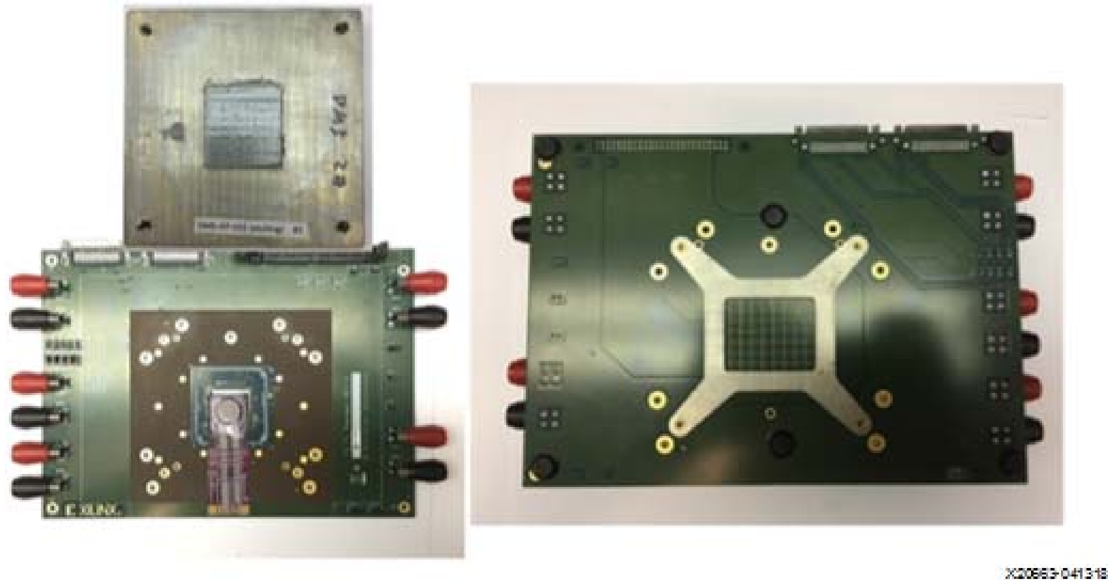

Figure A-10: **FCBGA Board Layouts**

The target force can be reproduced and the force exerted on the die surface is close to the target of 32 psi.

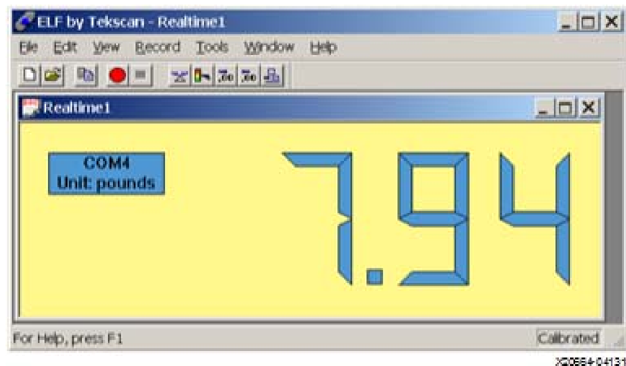

Figure A-11: **Target Force**

IMPORTANT: *During heatsink installation, you must control the torque pressure so that it does not exceed 50 psi. It is recommended that you program the smart torque screwdriver so that it does not exceed this pressure level. If you are not using a smart torque screwdriver, be sure to fasten the screws slowly during installation to control the torque.*

Installation Process

There are different approaches to assemble the thermal solution on the FCBGA. This depends on the type of mechanical attachment. The following examples illustrate how the screws affect the thermal solution from either the back side of the board or the front side of the board.

Heat Sink Assembly for Dynamic Back Side Mounting

This example is given based on the PCIe card, which has the following items:

- Heatsink bottom plate (Figure A-12)
- PCIe component (Figure A-13)
- Active top plate, core heat sink, and shroud assembly (Figure A-14)
- Smart Torque assembly workstation (Figure A-9)

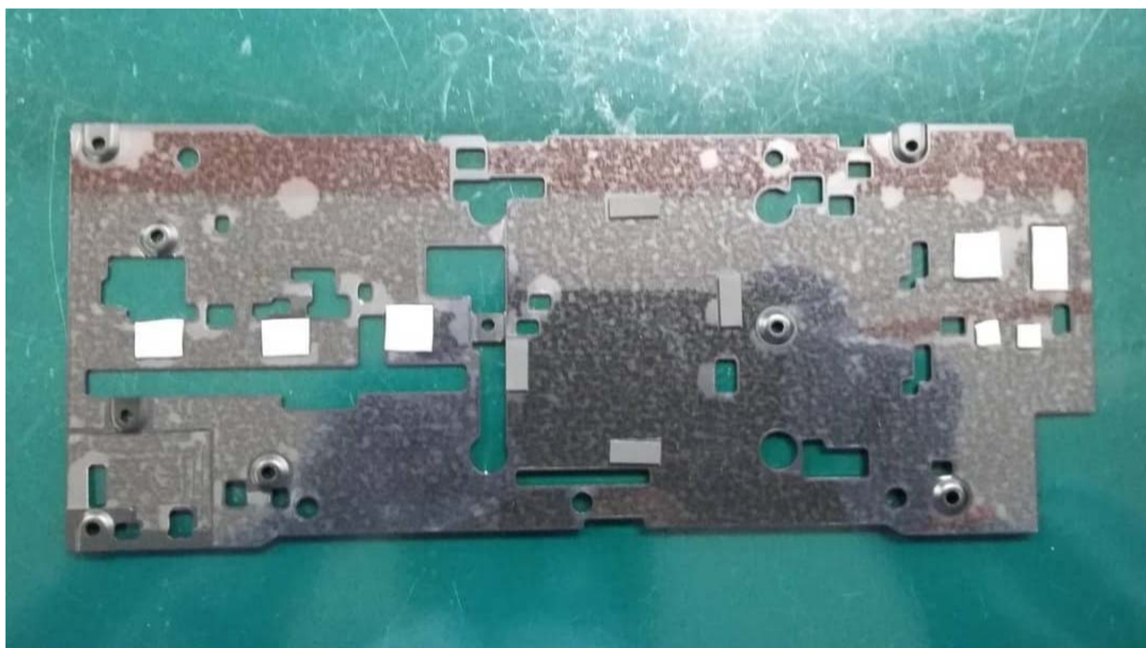

Figure A-12: **Heatsink Bottom Plate**

Figure A-13: **PCIe Card**

Figure A-14: **Active Top Plate, Core Heat Sink, and Shroud Assembly**

The following details the assembly procedure for the heat sink. Before you begin, Figure A-15 shows a jig set up, which is critical for smooth and faster alignment during assembly.

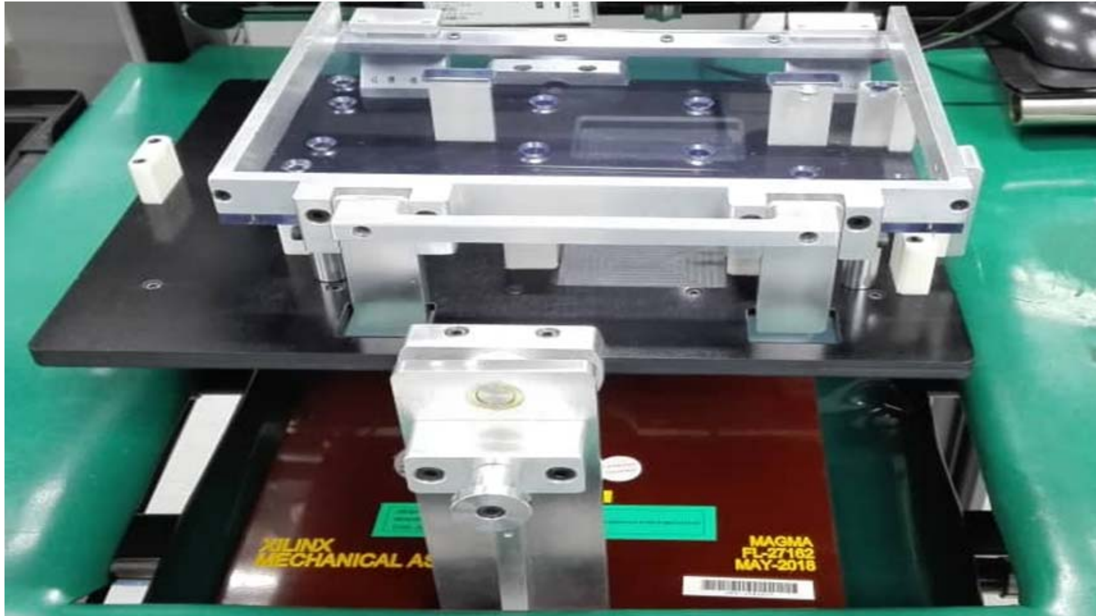

Figure A-15: **Jig Set Up**

Assembly

To assemble the heat sink:

1. Put the heat sink in the mechanical assembly jig.

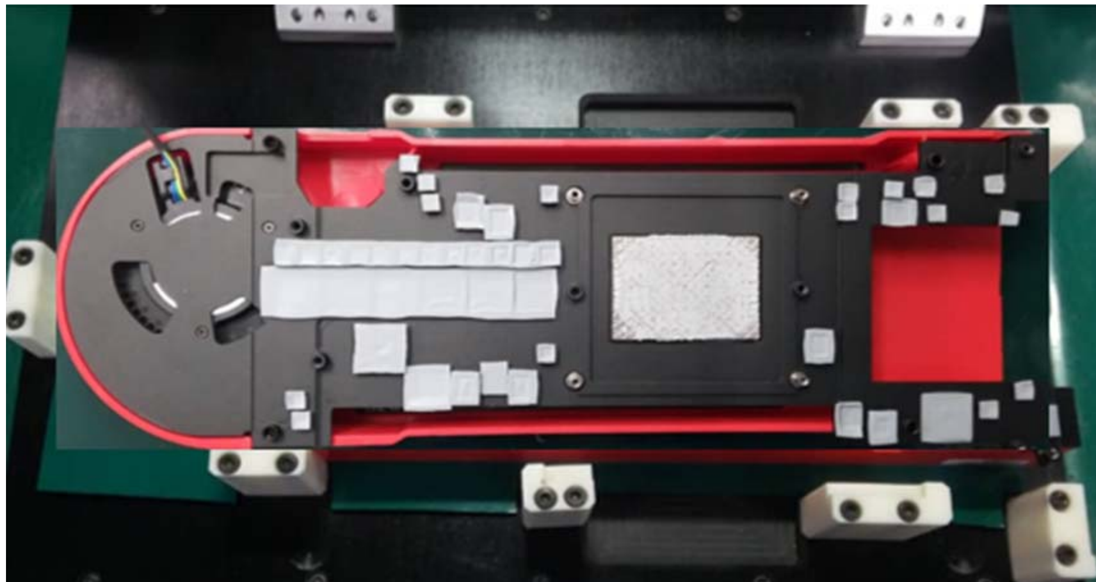

Figure A-16: **Active Heat Sink in Jig**

2. Put the PCBA on top of the heat sink.

Figure A-17: **Heat Sink with PCBA on top**

3. Put the bottom plate on top of the PCBA.

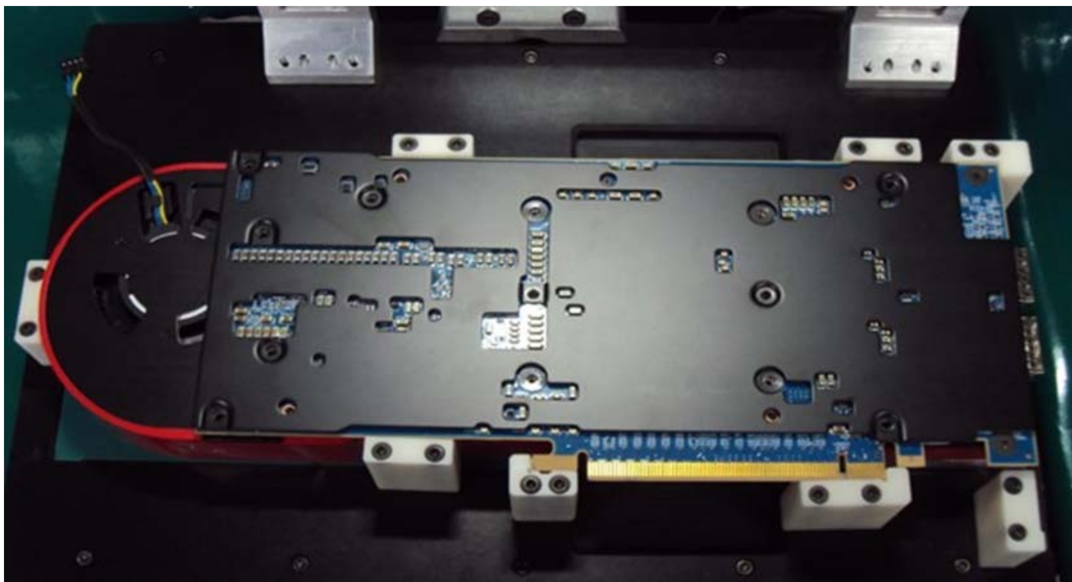

Figure A-18: **Bottom Plate**

4. Put the IO bracket in place.

Figure A-19: **IO Bracket**

5. Clamp down the assembly jig cover.

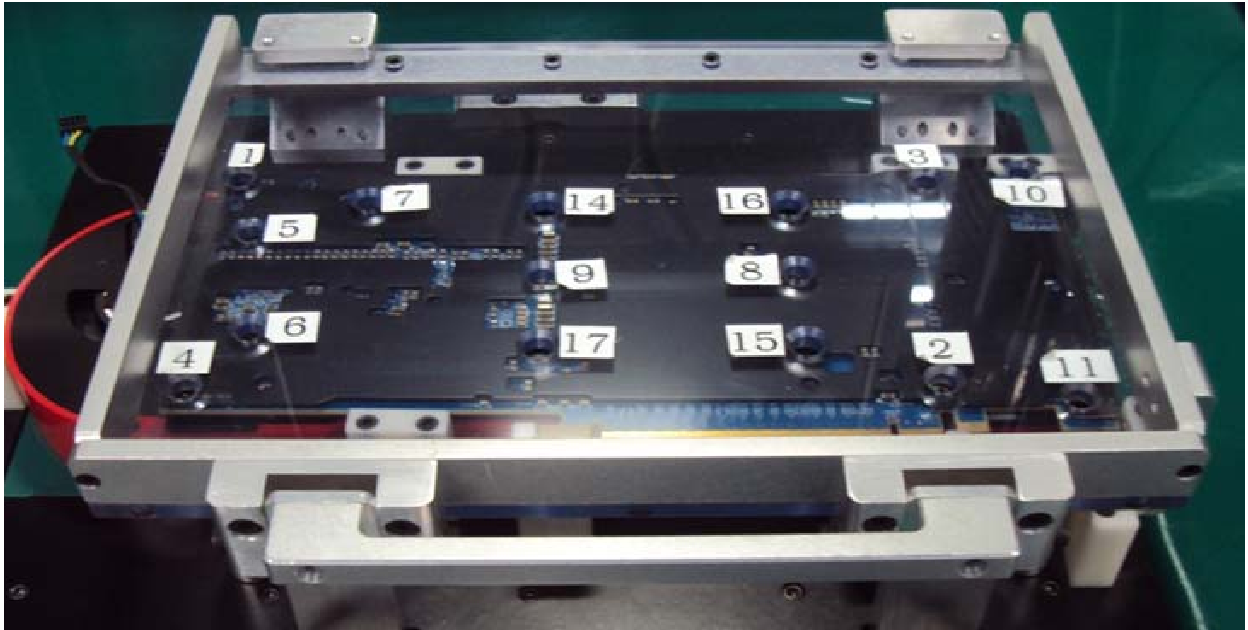

Figure A-20: **Assembly Jig Cover**

6. Tighten the screws using the smart torque (shown below) or using a digital torque screwdriver.

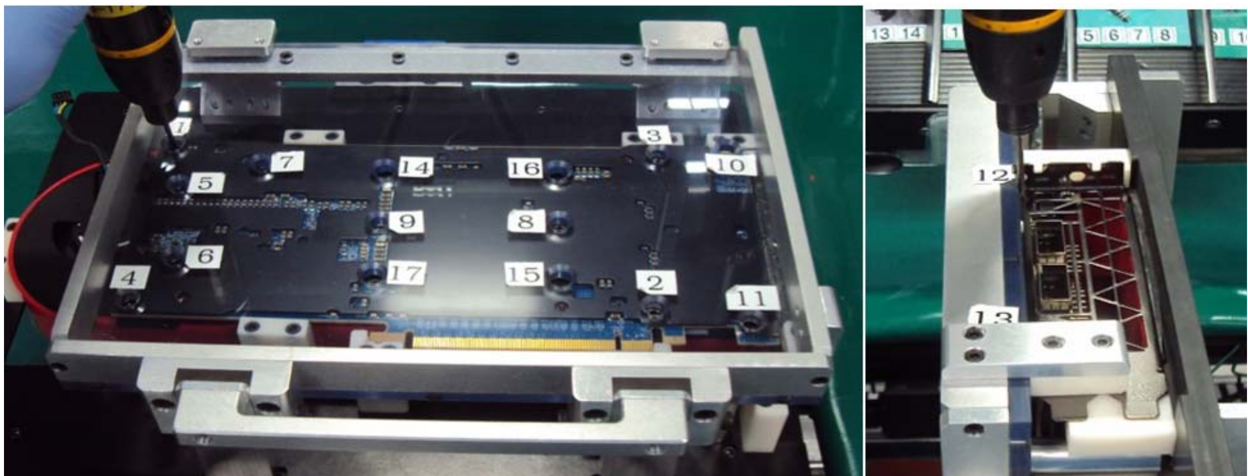

Figure A-21: **Screw Assembly**

Heat Sink Assembly for Dynamic Top Side Mounting of Lidless Unit

Components

The following components are used for this heat sink assembly:

- Heat sink and back clip (Figure A-22)
- PCB board (Figure A-23)

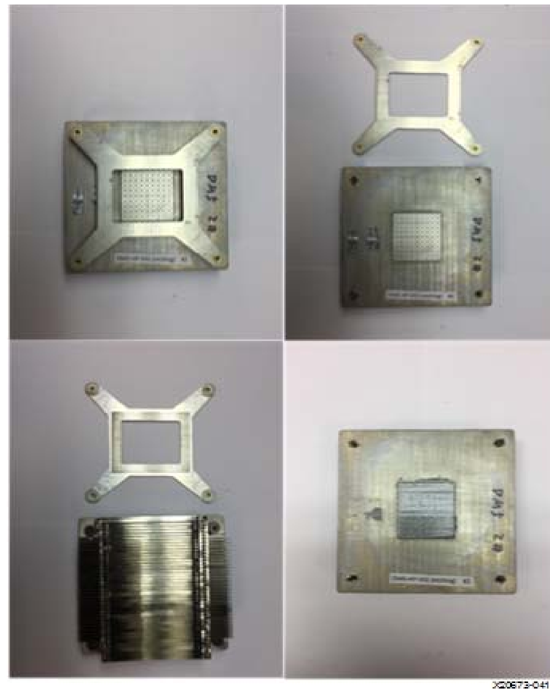

Figure A-22: **Heat Sink and Back Clip**

Figure A-23: **PCB Board**

Assembly

Figure A-24 shows a flowchart of the heat sink assembly for a lidless unit.

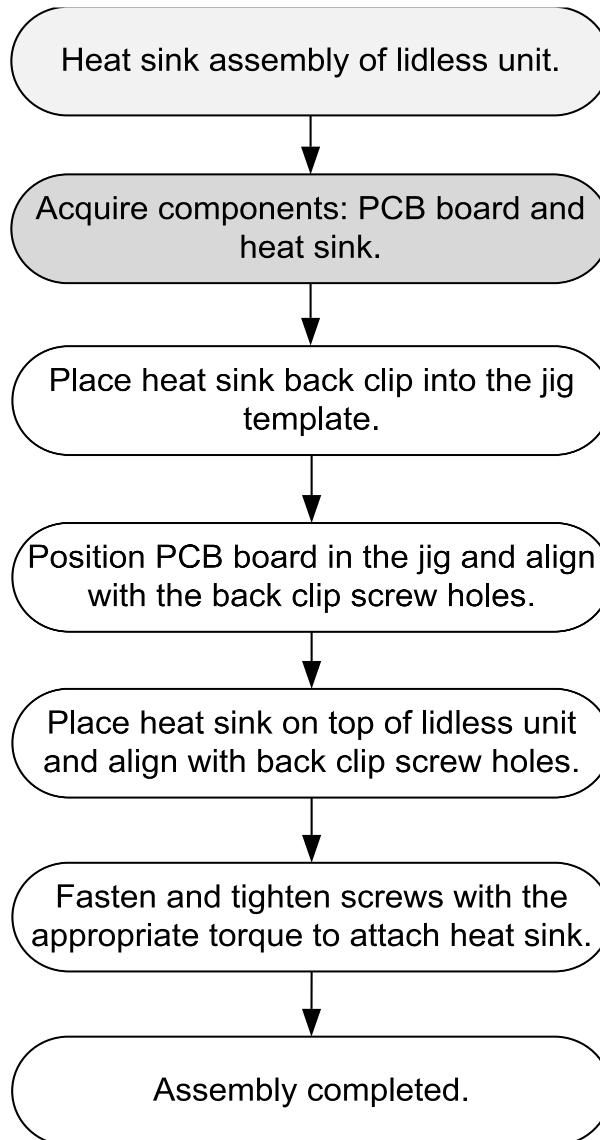

Figure A-24: **Flowchart of the Heat Sink Assembly**

The following details the assembly procedure for the heat sink. Before you begin, Figure A-25 shows a jig template which can be used during assembly.

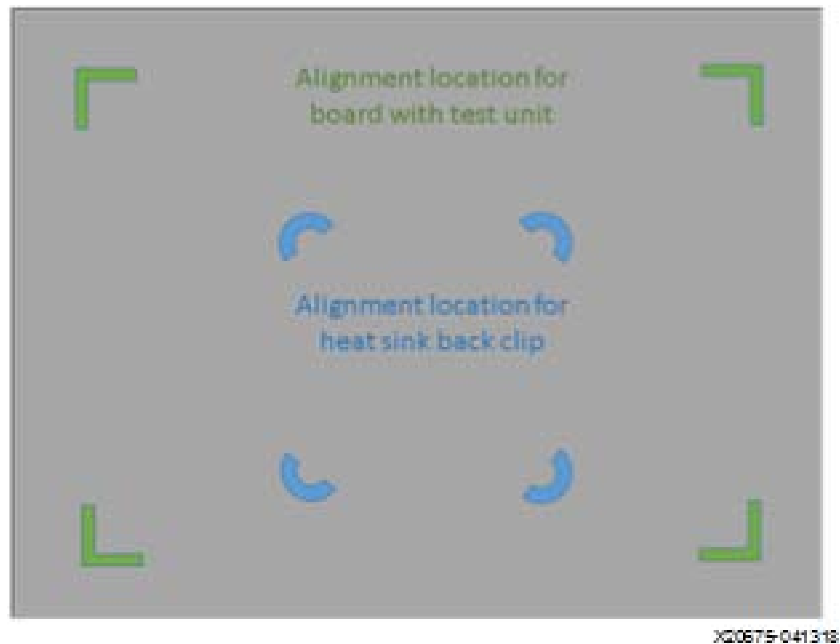

Figure A-25: **Jig Template**

To assemble the heat sink:

1. Place the heat sink back clip into the defined position of the jig template.

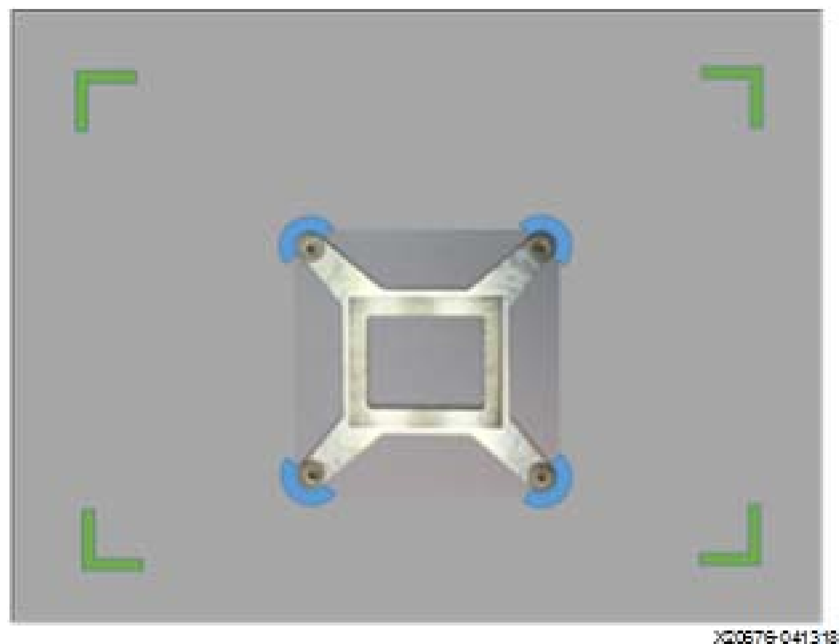

Figure A-26: **Heat Sink in Jig**

2. Position the test board with the lidless unit on top of the heat sink back clip into the defined position of the jig template.

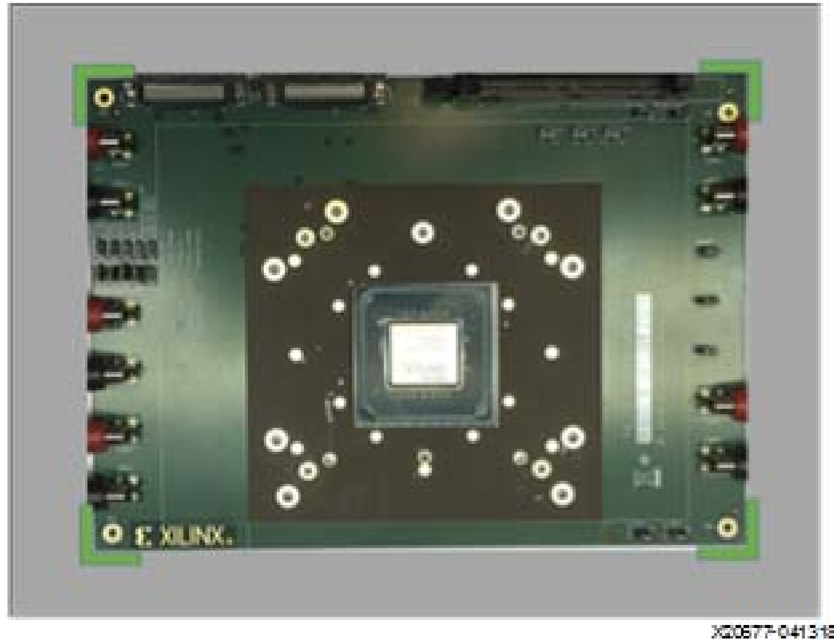

Figure A-27: **Test Board and Lidless Unit in Jig**

3. Place the heat sink on top of the lidless unit on the board. Align to the screw holes (highlighted in red) of the back clip.

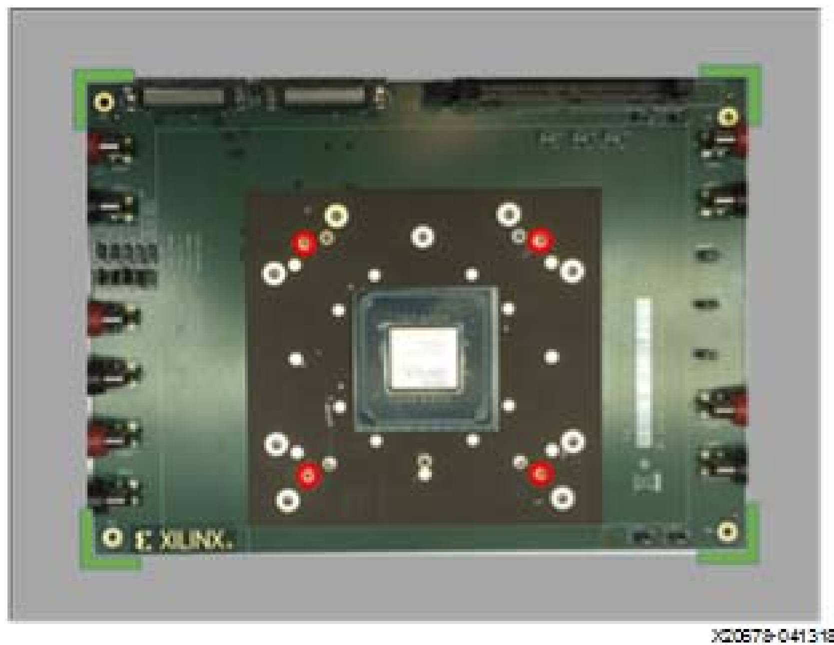

Figure A-28: **Screw Locations for Heat Sink and Lidless Unit in Jig**

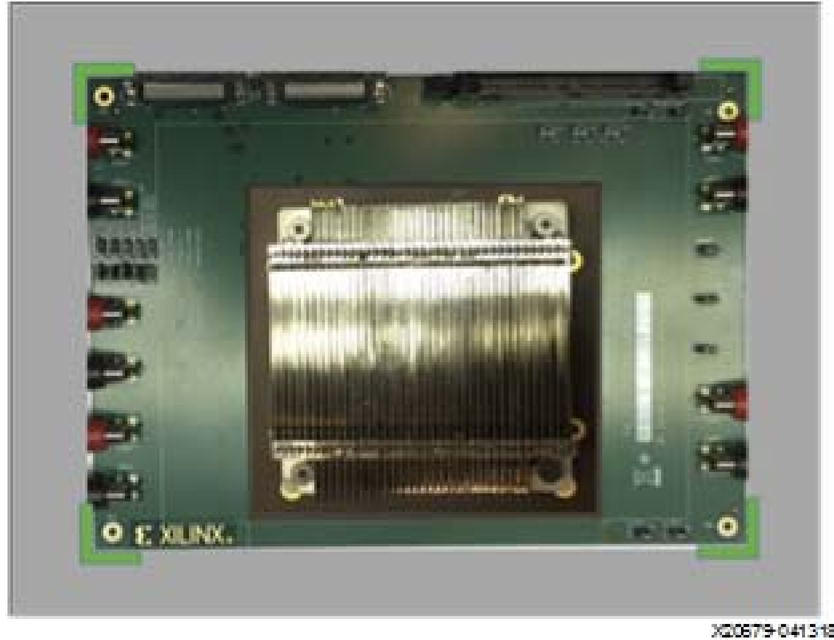

Figure A-29: **Heat Sink and Lidless Unit in Jig**

4. Lightly fasten the screws to hold the clip. Use the preset screwdriver to tighten the four screws of the heat sink in the following sequence to finish assembly.

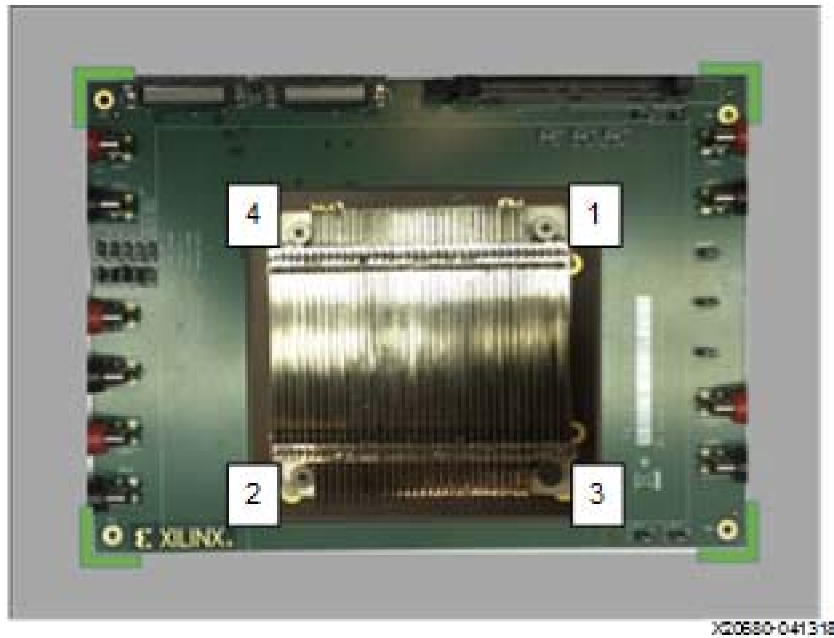

Figure A-30: **Screw Sequence for Final Assembly**

Heat Sink Assembly for Dynamic Bottom Side Mounting of Wireless Heat Sink

Components

The following components are used for this heat sink assembly:

- Lidless unit on board (Figure A-31)
- Cu block with pedestal (Figure A-32)
- Heat sink for wireless application (Figure A-33)

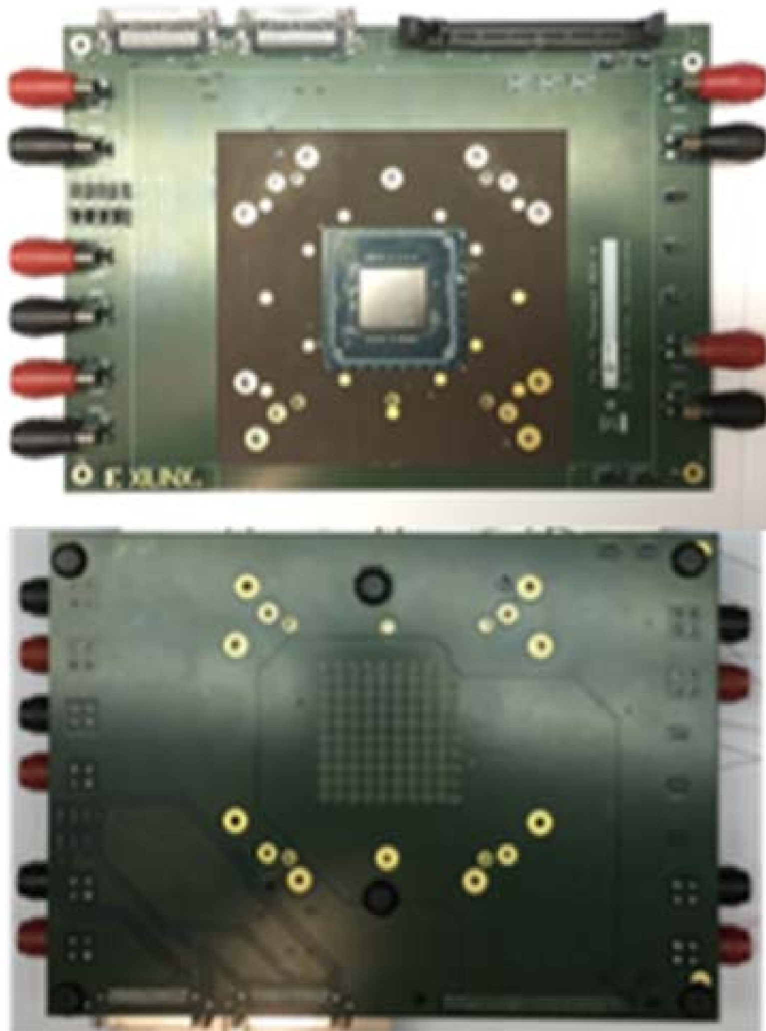

Figure A-31: **Lidless Unit on Board**

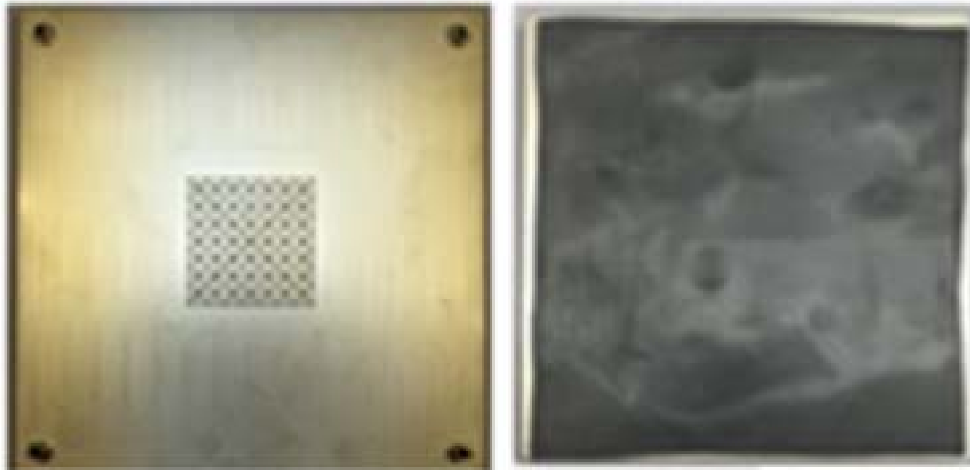

Figure A-32: **Cu Block with Pedestal – Bottom Side and Top Side**

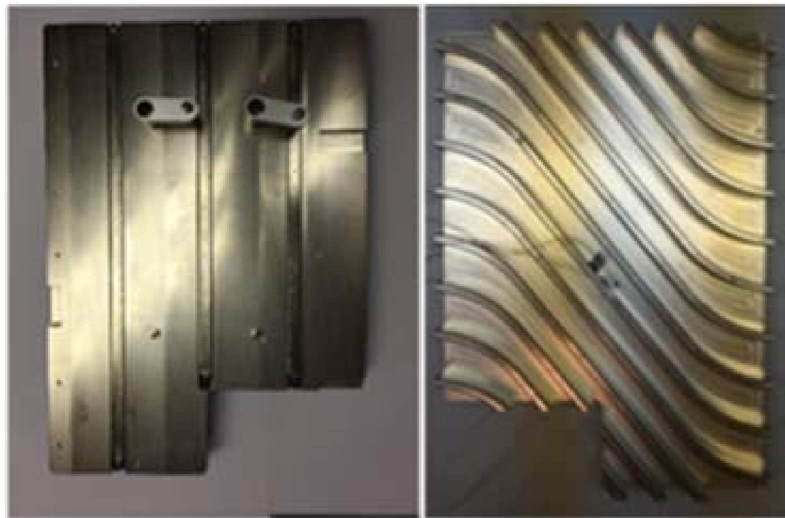

Figure A-33: **Heat Sink for Wireless Application**

Assembly

Figure A-34 shows a flowchart of the heat sink assembly for a wireless application.

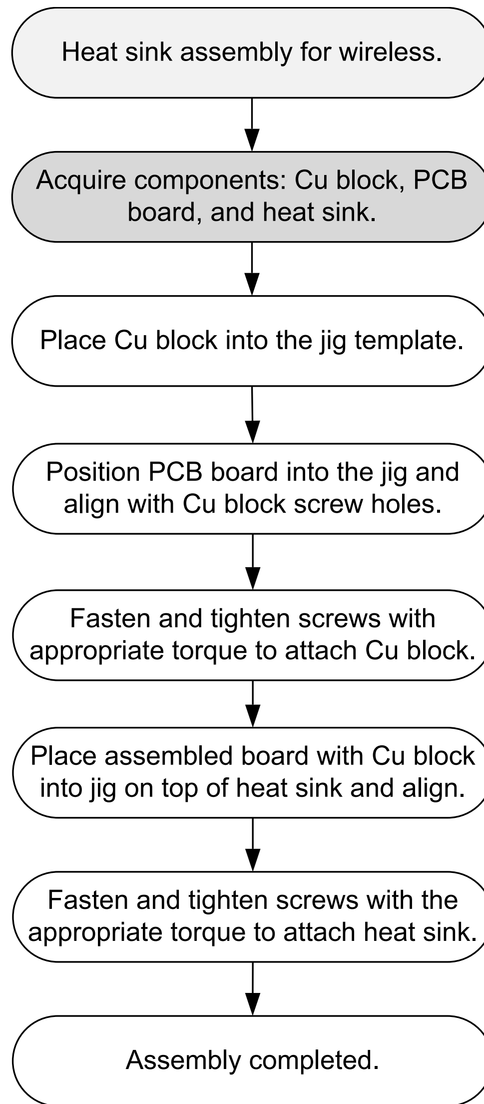

Figure A-34: **Flowchart of the Heat Sink Assembly**

The following details the assembly procedure for the heat sink. Before you begin, Figure A-35 and Figure A-36 show the jig templates that can be used during assembly.

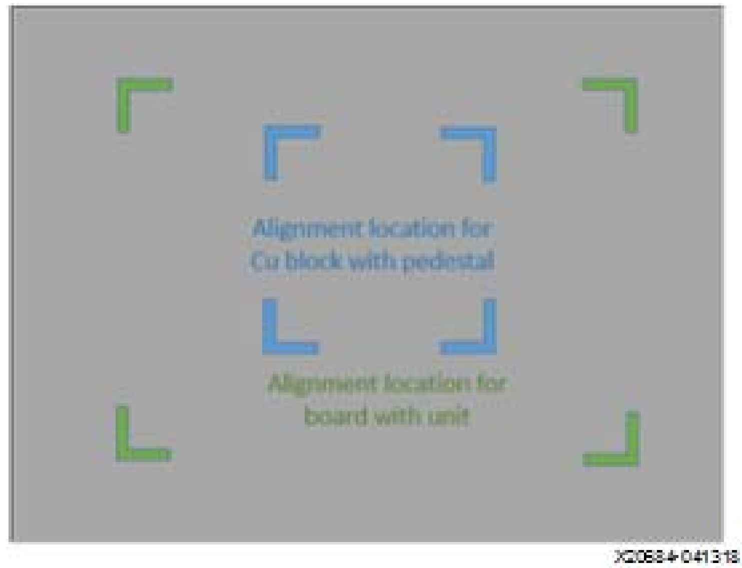

Figure A-35: **Jig Template for Cu Block with Pedestal**

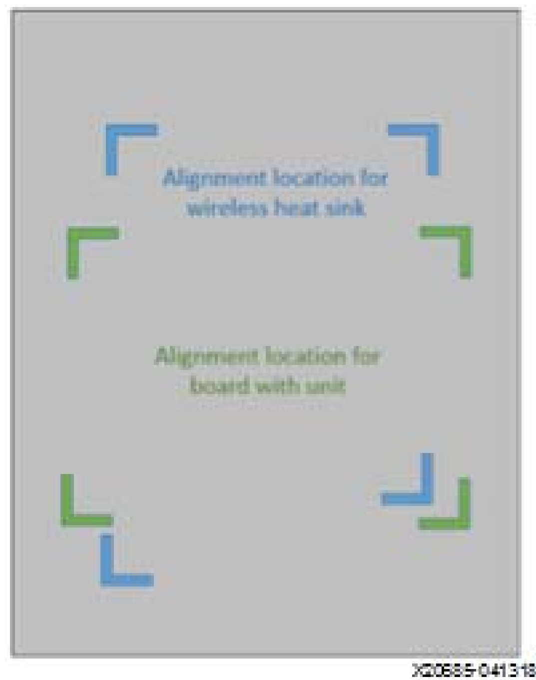

Figure A-36: **Jig Template for Wireless Heat Sink and Board**

To assemble the heat sink:

1. Apply thermal interface material to the Cu block pedestal.

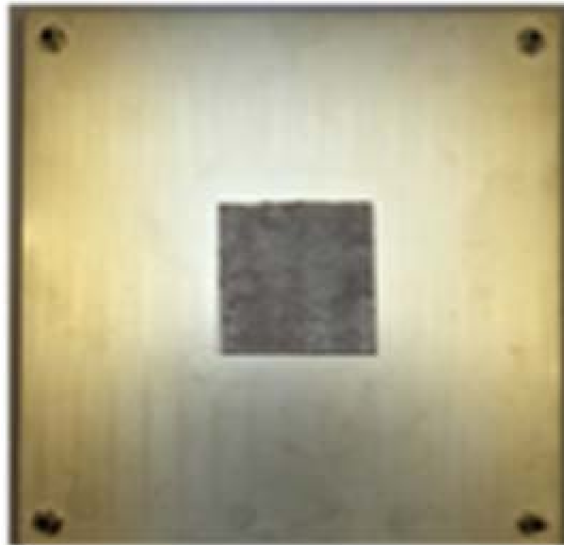

Figure A-37: **Thermal Interface Material to Cu Block Pedestal**

2. Place Cu block into the defined location of the jig template.

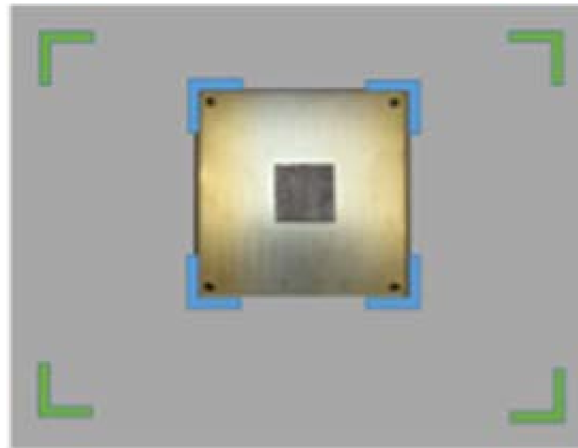

Figure A-38: **Cu Block in Jig**

3. Flip over and position board on top of the Cu block in the jig and align to screw holes (highlighted in red) of Cu block.

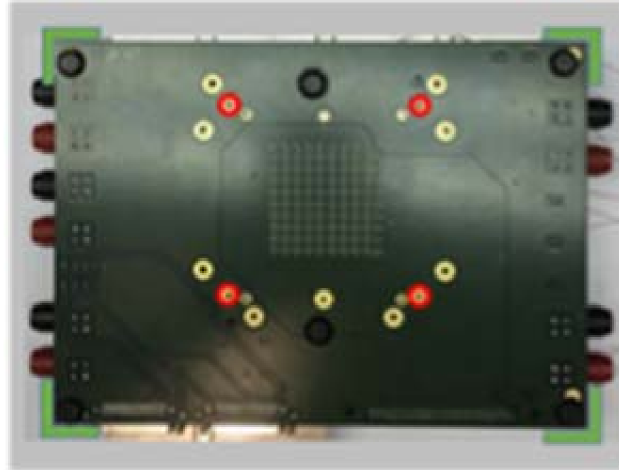

Figure A-39: **Screw Locations for Cu Block on Board**

4. Rotate the screws for a couple turns to hold the board in place. Use the preset screwdriver to tighten the four screws of the heat sink in the sequence as shown.

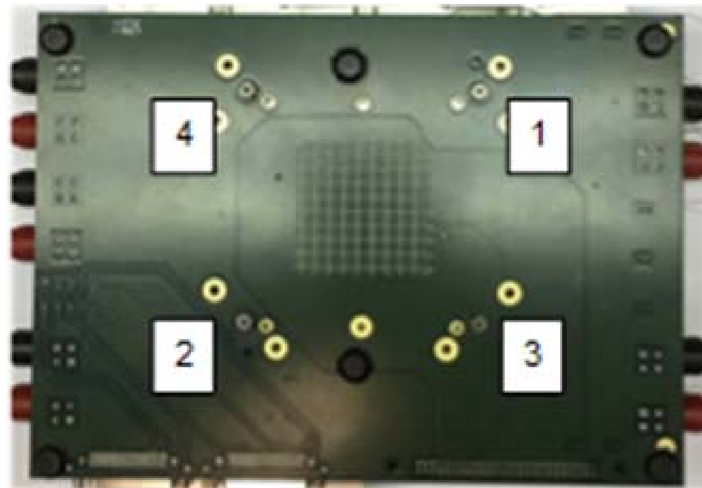

Figure A-40: **Screw Sequence for Board**

5. Finish assembled board with the Cu block.

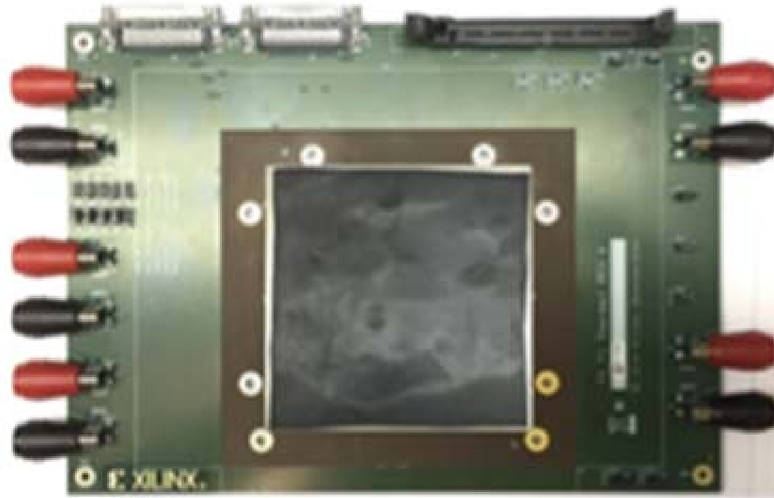

Figure A-41: **Assembled Board with Cu Block**

6. Place heat sink into the defined location of the jig.

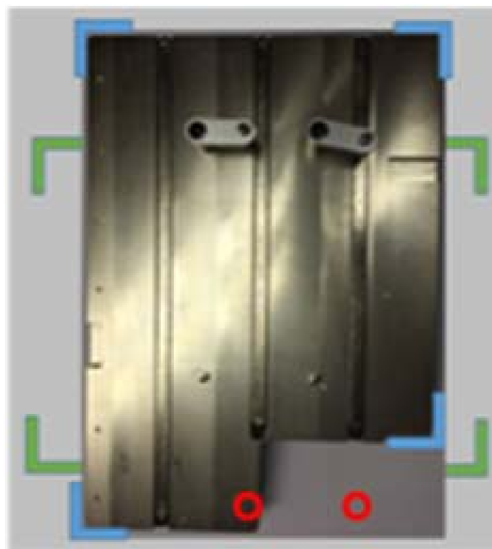

Figure A-42: **Heat Sink in Jig**

7. Assemble board with the Cu block on top of the heat sink. Align to screw holes (highlighted in red) of the heat sink.

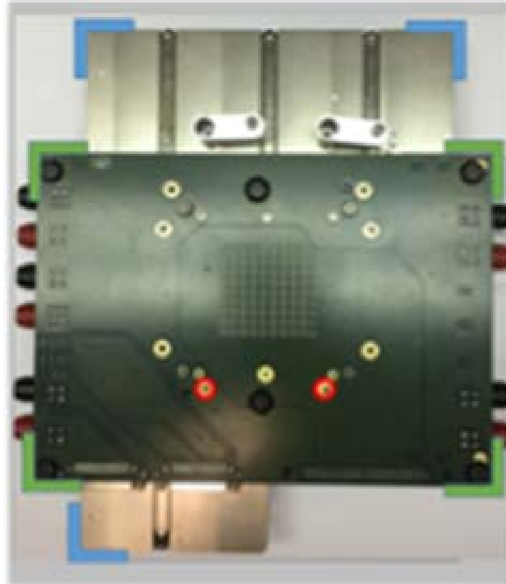

Figure A-43: **Screw Locations for Cu Block on Heat Sink**

8. Fasten screws in the appropriate sequence to finish assembly

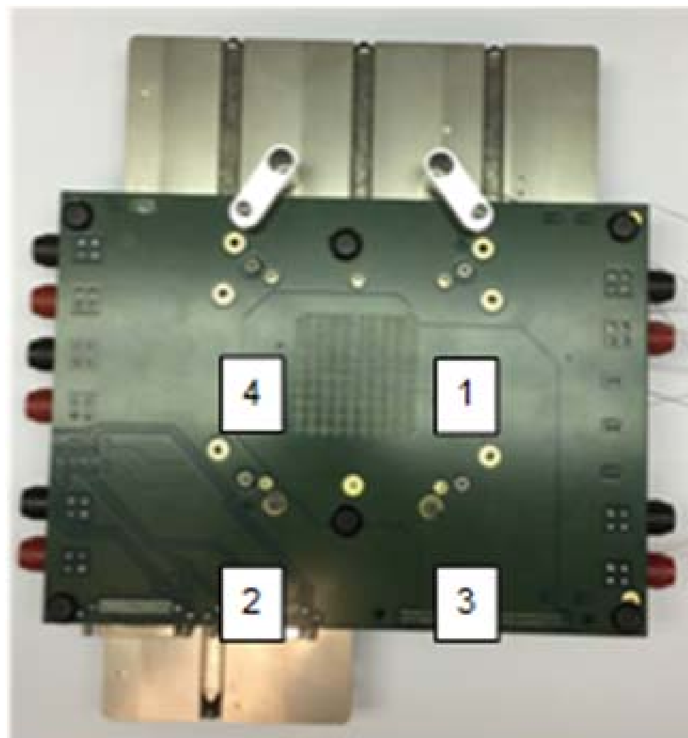

Figure A-44: **Screw Sequence for Final Assembly**

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

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Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

For additional information on heat management and contact information:

1. *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification User Guide* (UG575)
2. *Zynq UltraScale+ MPSoC Packaging and Pinouts Product Specification User Guide* (UG1075)
3. Virtex UltraScale+ FPGA Package Thermal Models (Xilinx support)

Refer to the following websites for CFD tools supported by Xilinx with thermal models:

1. Mentor (FloTHERM)
2. ANSYS (IcePak)

Refer to the following papers on thermal modeling:

1. Lemczyk, T.F., Mack, B., Culham, J.R. and Yovanovich, M.M., 1992, "Printed Circuit Board Trace Thermal Analysis and Effective Conductivity," ASME J. Electronic Packaging, Vol. 114, pp. 413 - 419.
2. Refai-Ahmed, G. and Karimanal, K., 2003, "Validation of Compact Conduction Models of BGA Under Realistic Boundary," J. of Components and Packaging Technology, Vol. 26, No. 3, pp. 610-615.
3. Sansoucy, E, Refai-Ahmed, G., and Karimanal, K., 2002, "Thermal Characterization of TBGA Package for an integration in Board Level Analysis," Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego., USA.
4. Karimanal, K. and Refai-Ahmed, G., 2002, "Validation of Compact Conduction Models of BGA Under Realistic Boundary Conditions," Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego, USA.
5. Karimanal, K. and Refai-Ahmed, G., 2001, "Compact conduction Model (CCM) of Microelectronic Packages—a BGA Validation Study," APACK Conference on Advance in Packaging, Singapore.

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