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Xilinx Multi-node Technology Leadership Continues with UltraScale+ Portfolio "3D on 3D" Solutions

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After clear quality and execution leadership at the 28nm and 20nm nodes, Xilinx continues its tradition of excellence and technology innovation at the 16nm node by delivering 3D FinFET transistors on 3D IC stacked-silicon interconnect (SSI) technology.

ABSTRACT

With the UltraScale+™ family of All Programmable FPGAs and MPSoCs, Xilinx and foundry partner TSMC are delivering the next generation of devices enabled by "3D on 3D" technology: 3D FinFET transistors on a 3rd-generation 3D IC process. TSMC's 16nm FinFET+ process delivers new levels of performance and power efficiency to the proven Xilinx® UltraScale™ architecture established at 20nm. Accordingly, Xilinx's stacked-silicon interconnect (SSI) technology implemented with TSMC's Chip-on-Wafer-on-Substrate (CoWoS) process enables Xilinx's third-generation devices to break through the limitations of Moore's law, delivering the highest levels of product capability and systems integration.

"3D on 3D" technology continues the Xilinx and TSMC track record of industry firsts, putting the most advanced solutions in customers' hands sooner. As the world's number one foundry, TSMC provides access to the most comprehensive technology portfolio, and also delivers on all aspects of design enablement, foundry services, and supply-chain support, from introduction to volume production. This partnership—coupled with Xilinx's proven ASIC-class UltraScale architecture, ASIC-strength Vivado® design tools, and robust new product introduction methodologies—sets the stage for another generation of All Programmable FPGAs and SoCs that deliver the best technology to customers with the lowest risk.

Introduction

For nearly half a century, CMOS technologies have more or less followed the central tenet of Moore's law, predicting a doubling of transistor density for semiconductor devices every two years. At the same time, much has been written about the predicted demise of this historical trend that has guided the roadmap and research efforts of the industry, serving as a benchmark against which to measure the rate of progress. There is no doubt that the continued progression down the process node curve has become more challenging. The fundamental limits of physics have turned issues like leakage and area scaling into industry-wide concerns that must be overcome to continue delivering on the promises of process migration.

While the rate of Moore's law has arguably slowed over the past decade, the demand for the benefits traditionally associated with the move to more advanced process nodes has not. The semiconductor industry and its customers continue to demand higher performance, better power efficiency, and increased integration to meet end market demands for increased bandwidth, greater processing capabilities, smaller form factors, and reduced operating costs. Through the collective innovation of the industry over the past ten-plus years, technologies such as copper interconnect, strained silicon, and high-K metal gate transistors have enabled continued migration down the process technology curve to satisfy these ever increasing demands.

However, the advanced technologies required to keep Moore's law on track have led to process development and fab construction costs that together exceed $10 billion for a new node. Correspondingly, chip development costs have also increased substantially, a fact that explains the ongoing decline in ASIC and ASSP design starts. The non-recurring engineering (NRE) charges associated with developing a chip for a specific market or application have increased to a level where very large unit volumes are required to justify the upfront development costs. This trend is a driving force in the continued displacement of ASICs and ASSPs by Xilinx's All Programmable FPGAs and SoCs, which now typically have a lower total cost for volumes well into the hundreds of thousands of units.

As ASICs and ASSPs become harder to justify due to the economics and risk associated with targeting specific and often rapidly changing markets, programmable solutions must rise to the challenge of providing ASIC-class capabilities to service the needs of future systems. Two key technologies are required to meet this challenge: 3D FinFET transistors and 3D IC integration. With the UltraScale+ family of All Programmable devices, Xilinx and foundry partner TSMC are delivering industry-leading "3D on 3D" solutions based on TSMC's 16nm FinFET+ process and Xilinx's 3rd-generation stacked silicon interconnect (SSI) technology.

These new programmable solutions use an enhanced ASIC-class UltraScale™ architecture with support from the ASIC-strength Vivado® design tools to deliver the underlying promise of "3D on 3D" silicon technologies, including:

- **Performance-per-watt leadership,** leveraging the full capability of FinFET technology to allow users to choose the performance and power efficiency characteristics that best suit their application requirements.
- **Maximum systems integration,** based on production-proven, 3rd-generation SSI technology, which delivers greater device capacity with earlier volume ramps and optimal power efficiency.

- **Lowest risk path** to realizing the benefits of FinFET technology in next-generation systems by leveraging a proven architecture and design tool suite designed to scale to 16nm and beyond, along with the proven quality and execution track record of the Xilinx/TSMC partnership.

3D FinFET Transistor Technology History and Benefits

While the traditional planar CMOS transistor has served the industry well for decades, continued shrinking of this structure beyond the 20nm node is limited by physical and electrical characteristics, mandating the development of an alternative. While various options have been researched over the years, the 3D FinFET transistor is now recognized as the primary solution to continued transistor scaling for at least the next few process nodes due to its superior electrical characteristics and large-scale manufacturability.

3D transistors were proposed as early as 1990, but it was not until 1997, when the Defense Advanced Research Projects Agency (DARPA) began funding a team of researchers led by Dr. Chenming Hu at the University of California, Berkeley, that the promise of FinFET technology started to take shape. The charter was to explore technologies for CMOS transistor fabrication down at the 25nm level, an area beyond the end of any transistor roadmap at the time. In 1998, Dr. Hu's team documented the first N-channel FinFETs, showing successful fabrication of transistors with gate lengths as small as 17nm. [Ref 1] They quickly followed this success with fabrication of the first P-channel FinFETs in 1999. [Ref 2] A key contribution of these research efforts was demonstration of FinFET fabrication using traditional CMOS process flows, setting the stage for mass-scale manufacturing of 3D transistor technology in the future.

Dr. Hu became Chief Technology Officer of TSMC in 2001, bringing his extensive knowledge of FinFET transistor fabrication to the world's number one foundry, where he continued to drive industry-leading research and lay the foundation for TSMC's advancements into deep submicron process technologies, including 16nm FinFET+. Dr. Hu has been called "the Father of the FinFET" for the contributions he and his team have made to developing and advancing 3D transistor technology; he has received numerous awards from national and international societies and standards bodies for his work.

The basic physical distinction between standard planar CMOS technology and 3D FinFET technology is shown in Figure 1. This difference is in the physical geometry and transistor construction, which directly contributes to the superior density and electrical characteristics of FinFET transistors, making them the primary solution for semiconductor device fabrication below the 20nm node. As shown in Figure 1, conventional planar transistors are constructed by layering a gate electrode over a flat, two-dimensional silicon region to form the channel of the transistor between the source and drain nodes. For very short channel transistors (gate length (L_G) < 20nm), this structure leads to the following challenges:

- **High leakage current:** The transistor exhibits excessive sub-threshold leakage current between the source and drain in the OFF state because the gate electrode cannot exercise adequate electrostatic control of the channel region from just one side. This means higher static power consumption and variability for the device.

- **Performance limitations:** As a result of the gate control issue, small-geometry planar transistors have difficulty achieving the desired improvements in drive strength without leading to excessive leakage current. As a result, a good balance between performance and power is difficult to achieve.
- **Area scaling limitations:** More die area is required to create a planar transistor of a given drive strength, because the width (W) and length (L) are constrained to two dimensions, which directly determine the transistor's footprint.

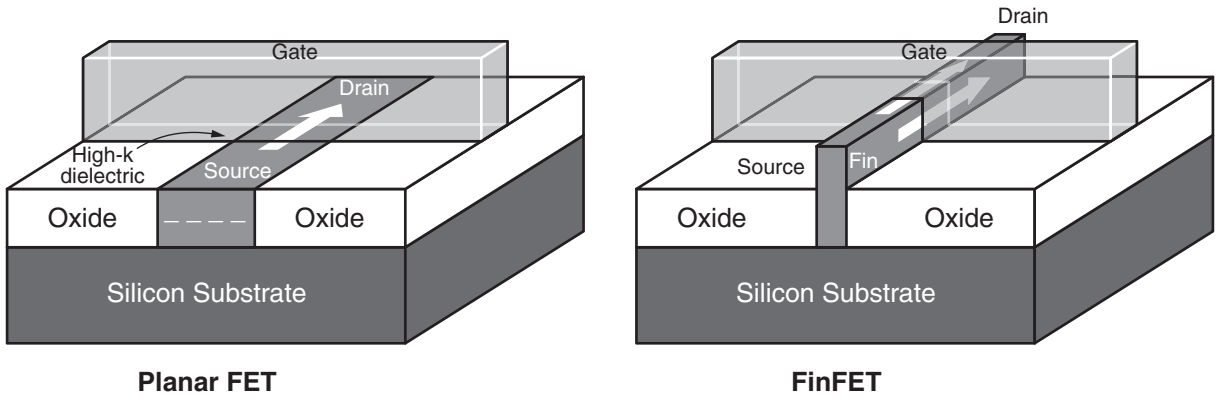

Figure 1: **Planar vs. FinFET Transistor Construction**

With FinFET transistors, the gate electrode wraps around one or more three-dimensional silicon "fins" to form the channel region between source and drain nodes. This structure has several advantages over a conventional planar transistor:

- **Lower leakage (static power).** With the gate electrode wrapped around three sides, the electrostatic control of the channel is much better, resulting in substantially lower sub-threshold leakage current in the OFF state. This means much lower and more consistent static power for the device.
- **Lower dynamic power.** Superior leakage control also allows for reduction in transistor threshold voltage (V_t), which enables lower operating voltages, directly resulting in lower dynamic power.
- **Higher performance.** Better electrostatic control of the channel region from three sides enables faster on/off transistor switching speeds, leading to substantially faster overall device performance.
- **Area reduction.** FinFET transistors have an effective channel width that is roughly two times the height plus the width of the fin. Channel width is directly proportional to the drive strength and performance of a transistor. By extending the width into the third dimension, a FinFET transistor of equivalent drive strength can be created in a smaller area than a planar transistor.

Taken collectively, the advantages of 3D FinFET transistor technology enable semiconductor devices to achieve *significantly higher performance at similar power levels* than prior generation devices—or, alternatively, *much lower power consumption at similar performance levels*. As demonstrated in Xilinx's UltraScale+ devices, achieving both performance improvement and better power efficiency is also possible with the right FinFET process and design targets. Also, improved

area efficiency at the transistor level enables a major improvement in the integration of ASIC-class features and capabilities.

While improvements in performance, power efficiency, and area are the primary benefits of FinFET transistors, their unique vertical "fin" construction contributes to a significant reduction in single event upsets (SEUs). The substantial reduction in cross-sectional area where the source/drain regions meet the substrate results in a smaller region for charge accumulation resulting from ionized particles, the cause of SEUs.

Advantages of "3D on 3D" Technology for UltraScale+ All Programmable FPGAs and MPSoCs

In the UltraScale+ family, Xilinx and TSMC are continuing a successful collaboration of bringing industry-first technologies to market, delivering new ASIC-class capabilities in an All Programmable architecture. TSMC's 16nm FinFET+ 3D transistor technology provides the foundation for manufacturing both monolithic and 3D IC devices constructed with an enhanced Xilinx UltraScale architecture that scales from 20nm to 16nm and beyond.

The 3D IC-based products utilize Xilinx's proven SSI technology implemented with TSMC's CoWoS (Chip-on-Wafer-on-Substrate) process, which was production qualified in the 28nm node. Based on this collaboration of technologies, Xilinx and TSMC continue to deliver the highest performance, most power efficient, most highly integrated FPGAs and SoCs available, providing superior overall device reliability.

Best Performance-per-Watt with 3D Transistors

Increasingly, customers of semiconductor-based products are focused on smaller form factors, reduced operating costs, and more environmentally friendly technologies. While performance capabilities are still a crucial requirement for new systems, performance at any price is rarely an acceptable design criteria for next-generation systems; in many applications, power efficiency has become an issue of at least equal, if not greater, concern. As a result, Xilinx is focused on delivering programmable solutions with the best performance-per-watt characteristics across a multi-node portfolio of devices.

Beginning at 28nm, Xilinx and TSMC established a deep partnership to optimize process technology for both performance and power efficiency. This collaboration led to the development of the HPL process, which set a new standard in optimizing programmable devices for performance per watt. Xilinx achieved performance levels similar to or better than competing solutions that took a "performance at any cost" approach—while also achieving substantially lower power consumption. Figure 2 shows how Xilinx and TSMC are continuing to raise the performance-per-watt targets at 20nm and 16nm. At 20nm, Xilinx designed for an operating point within TSMC's 20SOC process technology window, which enabled a 70% performance-per-watt improvement relative to 28nm.

At 16nm, Xilinx and TSMC raise the bar again by delivering the highest performance-per-watt FinFET-based programmable devices in the industry. FinFET transistors can support a broader range of voltage operation while still delivering superior performance and leakage. UltraScale+ devices leverage these characteristics to deliver products with dual operating voltage capability:

nominal voltage (V_{NOM}) and a lower supply voltage (V_{LOW}). The voltage option allows the designer to select the operating range that delivers the optimal performance and power for a specific application. At the V_{NOM} supply voltage (0.85V), UltraScale devices deliver 60% more performance and 20% lower power than 28nm solutions, resulting in a 2X improvement in performance per watt. For applications requiring the maximum power efficiency, the V_{LOW} supply voltage (0.72V) delivers more than a speed grade performance improvement with up to 50% power savings relative to 28nm devices, for an impressive 2.4X improvement in performance per watt.

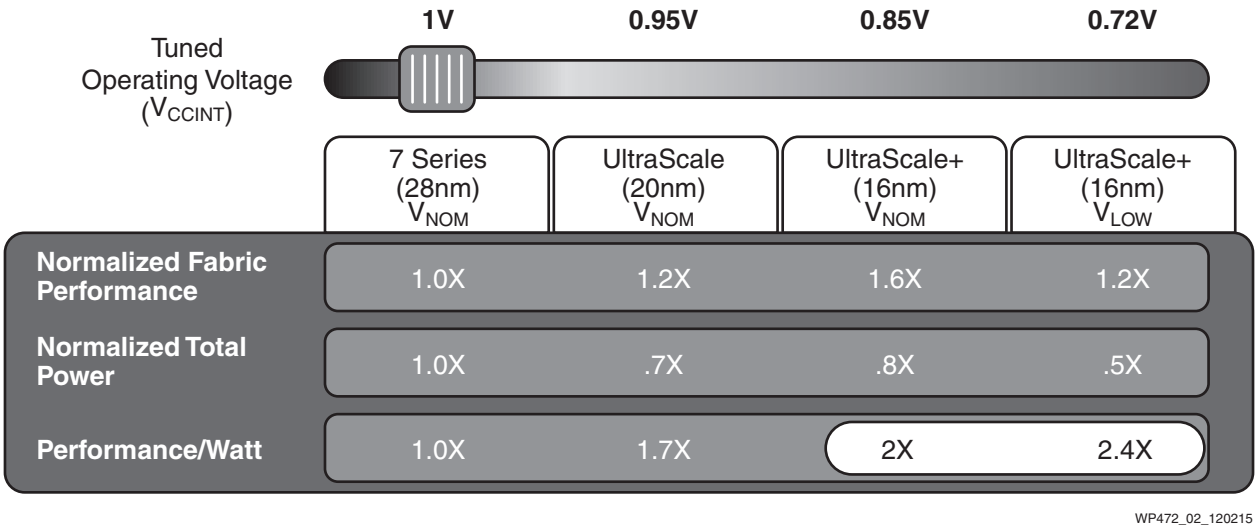

Figure 2: **Xilinx Leadership in Performance-per-Watt**

Highest Integration with 3D IC Packaging

SSI technology is another area where Xilinx and TSMC have a deep collaboration and proven track record of success in expanding the benefits of programmable devices, delivering ASIC-class integration and capabilities. At 28nm, Xilinx's SSI technology demonstrated the integration, power management, and time-to-market benefits of 3D IC programmable devices, delivering the industry's first homogeneous and heterogeneous 3D IC solutions. Using TSMC's proven CoWoS 3D IC process, Xilinx produced devices with over twice the capacity of competing FPGA products, and did so near the beginning of the 28nm process cycle when attempts at yielding the largest monolithic devices are normally futile due to the higher defect densities characteristic of a process in the early stage. A short time later, Xilinx demonstrated the much-discussed promise of 3D IC technology by combining programmable logic and 28Gb/s transceiver technologies manufactured on two different nodes. This represented the first heterogeneous 3D IC product in the industry.

At 20nm, Xilinx and TSMC again leveraged 3D IC technology to deliver devices with four times the capacity of competing solutions, as shown in Figure 3. This technological collaboration enabled high-density applications (such as ASIC prototyping and emulation) a full process node and generation ahead of planned monolithic solutions. Devices of this logic capacity are physically impossible to achieve in a 20nm monolithic solution, as they would exhibit unacceptable variation in performance and static power consumption—if they could be constructed at all. SSI technology allows performance- and power-matched devices to be integrated together for optimal, more consistent results.

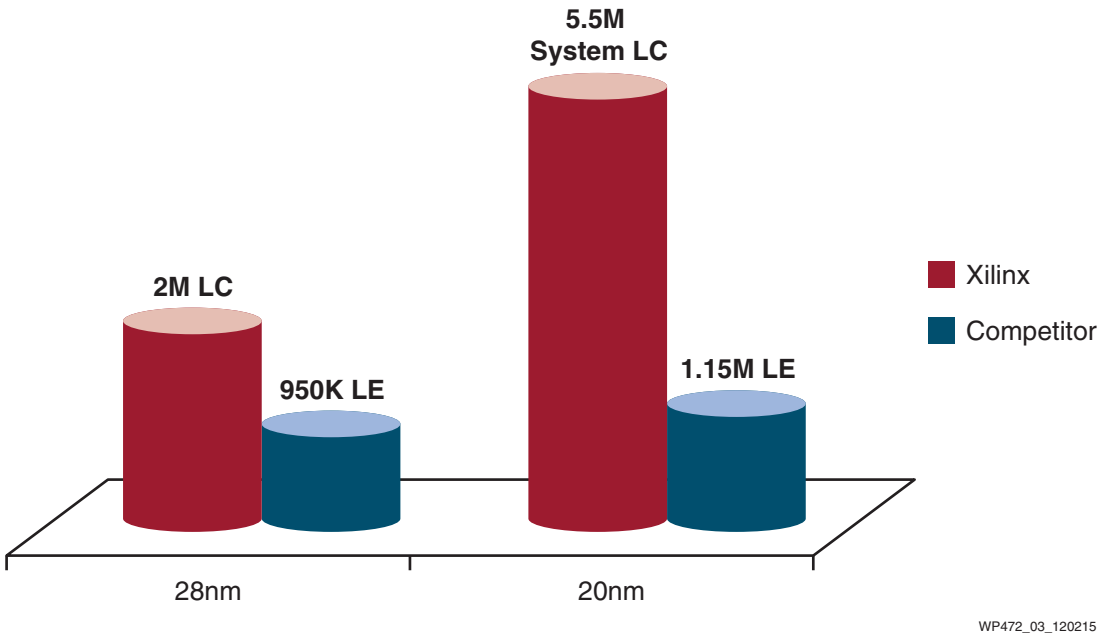

Figure 3: **Xilinx 3D IC History vs. Competing Monolithic Solutions**

For the UltraScale+ family, Xilinx and TSMC are once again implementing 3D IC solutions, this time on 3D FinFET transistor technology. This 3rd generation of 3D IC products based on TSMC's proven CoWoS process represent another industry first in the application of the most advanced technologies to deliver the highest levels of system performance, power efficiency, and integration. These solutions offer ASIC and ASSP users—previously constrained to hard-wired solutions by performance and power requirements—the opportunity to leverage the flexibility and time to market advantages of All Programmable FPGA and MPSoC solutions.

While Xilinx leads the way in productizing interposer-based 3D IC solutions for maximum systems integration, the rest of the semiconductor industry is following suit. Today, this 3D IC technology is becoming the industry standard for multi-die integration in a package. In 2016, for example, leading GPU vendors are expected to release products with integrated High Bandwidth Memory (HBM) based on this 3D IC technology, a testament to the production-proven solutions pioneered by Xilinx.

Lowest Risk Path to Next-Generation Solutions

Innovation to provide customers with the most advanced technology is the foundation of Xilinx product definition and development, but innovation without execution is a largely academic endeavor. As such, Xilinx is committed to delivering products when and as promised, with the absolute highest quality, providing customers the lowest risk path to accessing the best available technology. Through a carefully planned strategy of partnerships, product development, and new product introduction methodologies, Xilinx has a proven track record of delivering solutions that meet design specifications and schedules with the highest initial and production quality. This proven formula established at 28nm and repeated at 20nm has created a solid foundation for the move to "3D on 3D" solutions at the 16nm node.

Proven Partnership

As the number one foundry in the world, TSMC has a clear track record of delivering the best technology to customers in the fabless semiconductor industry. For Xilinx, TSMC's leadership in two critical technologies, Cortex™-class ARM® core integration and 3D IC solutions, made them the clear technology partner of choice. TSMC's early and deep engagement with ARM at each node provides a proven approach to validating the functionality, performance, and design/process interactions of ARM's processor IP on a targeted silicon technology. This foundation paved the way for rapid fabrication and bring-up of the Xilinx Zynq® UltraScale+ MPSoC device on TSMC's 16nm FinFET+ technology. Zynq UltraScale+ MPSoCs include a Quad-core ARM Cortex-A53 MPCore operating at up to 1.5GHz, along with many other heterogeneous processing engines. All major blocks of this device were verified within days of first silicon, enabling initial shipments to begin ahead of schedule in October 2015.

For 3D IC devices, Xilinx and TSMC are putting their third generation of production quality solutions into the market at 16nm. Like FinFET, 3D IC technology is recognized as a major event in the semiconductor industry roadmap, allowing continued improvements in integration, power efficiency, and system performance that are impossible to achieve through conventional monolithic devices. Having two prior generations of production experience with 3D IC technologies enables Xilinx and TSMC to implement these solutions with a high degree of confidence on FinFET-based devices. Meanwhile, competing solutions are targeting unproven 3D IC technologies in a first attempt at multi-die integration.

While access to advanced technology is a key aspect of Xilinx's partnership with TSMC, it is only one of several critical elements that make this the right relationship for providing customers with the most advanced, highest quality FPGAs and MPSoCs. As shown in Figure 4, with nearly three decades of experience focusing solely on the needs of the fabless semiconductor industry, TSMC is uniquely positioned to provide the complete range of support for all aspects of new product development, introduction, and volume ramp.

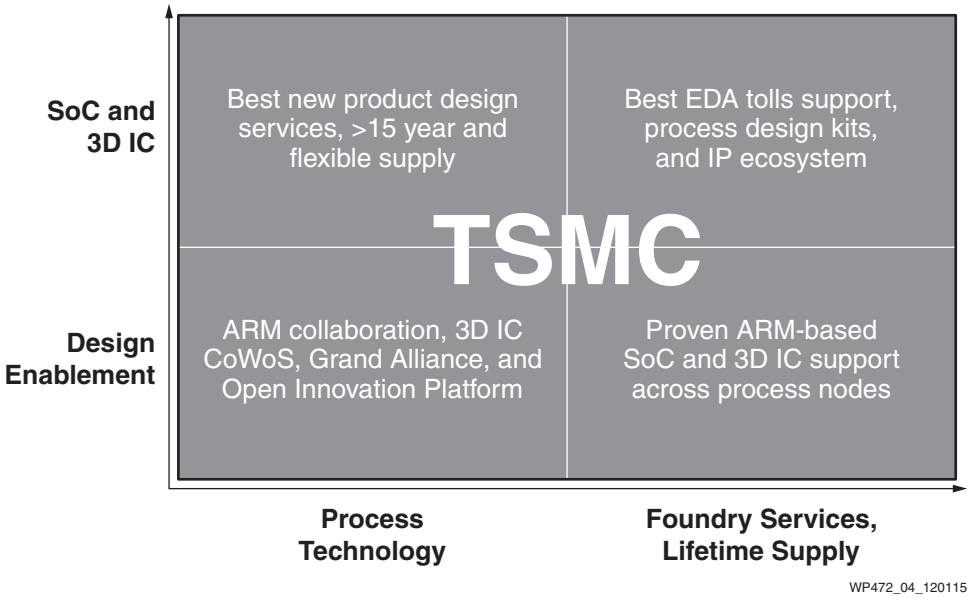

Figure 4: **TSMC's Comprehensive Technology and Foundry Services**

TSMC's design-enablement capabilities provide access to robust, industry-standard EDA tools, along with the broadest IP ecosystem in the semiconductor industry. Their foundry services provide the best support for new product design with a flexible, robust device supply of 15 years or longer from initial product introduction. All of these factors provide the supporting infrastructure for accessing and leveraging TSMC's world-class technologies and the strength of their "Grand Alliance" of EDA, IP, manufacturing equipment, and design ecosystem partners.

Proven Tools and Architecture

Over the past several years, Xilinx has made a series of carefully timed product development and introduction decisions to enable customers with both ASIC-class design tools and silicon architectures while mitigating the risks of new product adoption. After four years of development, Xilinx publicly launched the Vivado ASIC-class design environment in July 2012. Now, more than three years later, Xilinx customers continue to experience the proven benefits of the Vivado design tools, including substantial run-time improvement, better-quality results, higher device utilization, and significantly faster development time through the UltraFast™ design methodology.

In late 2013, Xilinx began shipping 20nm devices based on the new UltraScale architecture, the first ASIC-class programmable architecture. UltraScale devices deliver unprecedented levels of integration and system-level performance for the most demanding applications requiring massive I/O and memory bandwidth, massive data flow, and superior DSP and packet-processing performance. The UltraScale architecture has been proven in 20nm and was designed to scale to 16nm to address the requirements of next-generation applications requiring additional levels of performance, power efficiency, and integration. UltraScale+ devices deliver an enhanced version of this architecture fabricated on TSMC's 16nm FinFET+ technology.

By strategically introducing and proving out new design tools and architectures over a period of time, Xilinx has dramatically reduced the risk of making the move to FinFET process technology. All the development, learning, and optimization applied to the tools and architecture enable a very fast adoption ramp and realization of benefits for customers utilizing Xilinx 16nm devices. Competing solutions are changing design tools, architectures, manufacturing partners, and process technologies all at the same time for the FinFET generation of products, introducing many variables that can be expected to affect the quality, execution, and time required to result in a stable solution.

Absolute Quality and Total Execution

At the 28nm node, Xilinx devices have maintained a less than 2 part per million (ppm) quality standard throughout the shipment of millions of FPGA and SoC devices. Xilinx 7 series FPGAs and Zynq-7000 SoCs have been delivered on time and to specification, with no production mask set changes or errata items associated with device blocks developed by Xilinx. This level of quality and execution is unmatched by competing solutions and is a testament to Xilinx's robust new product introduction methodologies that have evolved over the past several generations into a comprehensive process that scales with the demands of each new family. Xilinx has a proven approach to process modeling and design validation that begins well before the first product tapeout with silicon test vehicles. These platforms are used for insights on design and process characteristics to create a foundation for building best-in-class products. When first product silicon

arrives, a four-stage verification and characterization program begins to identify any critical issues early, leading to quick resolution and better quality in both ES and Production silicon.

This proven formula was repeated at 20nm with the rapid introduction and widespread sampling of Kintex® UltraScale devices based on the first mask set. These devices had very high initial quality and demonstrated full operation of all major blocks, including 16Gb/s transceivers, within days of receiving first silicon. This level of quality and execution allowed for the pull-in of production qualification and paved the way for rapid, on-time rollout of the remaining Kintex and Virtex® UltraScale devices. At 20nm, Xilinx's approach to quality and execution resulted in a time-to-market advantage of more than a year ahead of competing solutions, enabling customers to bring new systems to market sooner and with lower risk.

With the successful rollout of two recent nodes, Xilinx is extending this formula to 16nm FinFET+ devices to deliver the UltraScale+ family of FPGAs and MPSoCs with absolute quality and total execution. All the verification, characterization, and learning from prior nodes are providing a solid foundation for continued success. The first silicon of Zynq UltraScale+ MPSoC devices experienced rapid bring-up and verification of all major blocks that surpassed the high standard established in the prior generation. By using proven new product introduction methodologies in collaboration with TSMC and leveraging a proven UltraScale architecture fully supported and co-optimized with Vivado design tools, Xilinx enables customers with the lowest risk path to realizing the benefits of FinFET technology.

Conclusion

At 16nm, Xilinx and TSMC are bringing the era of "3D on 3D" solutions to UltraScale+ All Programmable devices, providing the highest levels of performance, power efficiency, and integration for next-generation systems. Based on an ASIC-class architecture and supported by ASIC-strength design tools, these devices enable further displacement of fixed-function products and enable customers with the traditional flexibility and time-to-market advantages of programmable solutions. With two recent nodes of clear quality and execution leadership, Xilinx All Programmable devices and development tools are becoming the de facto industry standard. Xilinx UltraScale+ devices are extending this formula to deliver a third generation of the best technology with the lowest risk to customers.

For more information about the Xilinx UltraScale+ portfolio and to start designing with the products today, visit the UltraScale Architecture Technology page on the Xilinx website, and review DS890, *UltraScale Architecture and Product Overview*.

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Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/15/2015	1.0	Initial Xilinx release.

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