WP432 (v1.1) September 13, 2013

Balancing Performance, Power, and Cost with Kintex-7 FPGAs

By: Ehab Mohsen

In the past, FPGA vendors commonly segmented their portfolios between "high-end" and "low-cost" devices. However, as developers have refined the way they leverage FPGA technologies, they have voiced the need for a "mid-range" solution, featuring high-end functionality and performance in a cost-effective package. The Xilinx® Kintex™-7 family of FPGAs was developed for these applications, delivering the most balanced power and performance in the industry while providing high-end features, such as cutting-edge transceivers, integrated IP, and extensive DSP resources.

This white paper describes the importance of building the Kintex-7 FPGA on the 28 nm high-performance, low-power (HPL) silicon process; reviews some of the mid-range family's key features; and provides examples demonstrating how the Kintex-7 FPGA is an ideal fit for a variety of applications.

Selecting the 28 HPL Process for Optimal per-Watt Performance

While Moore's law continues to hold true, the benefits of moving to the latest silicon process are diminishing with shrinking geometries. Power reduction, for example, has become a major concern. Because higher circuit speeds increase dynamic power consumption, developers find it challenging to improve performance — not because of technology limitations, but rather because of power budget. Greater static power consumption leaves less room for *usable performance*, defined as available data processing throughput within a given power budget. To develop a 28 nm solution, Xilinx realized that a considerable shift in approach would be needed, or system power consumption would become untenable for many FPGA applications.

The root of the challenge is the polysilicon gate and silicon oxynitride gate (Poly/SiON) dielectric stack that has been used for decades to build transistors in ICs. As the gate dielectric layer becomes progressively thinner to improve transistor speed, leakage current increases. To mitigate this problem at 28 nm, Xilinx worked with Taiwan Semiconductor Manufacturing Company (TSMC) to adopt a new gate dielectric material, hafnium oxide. As a key enabler of the 28 nm high-performance, low-power (HPL) process jointly developed by Xilinx and TSMC, this dielectric material allows for higher gate thickness, thereby reducing leakage current while still supporting high transistor performance. Coupled with key architectural innovations at the device level, the HPL process is optimized to deliver a balance of performance and power efficiency in the Xilinx 28 nm 7 series FPGAs.

Other TSMC processes exist at 28 nm, namely the high performance (HP) and low power (LP) variants, neither of which is ideal for FPGAs. The HP process, while offering more performance than is required in an FPGA, dramatically increases power consumption to levels that are unacceptable in many applications. The LP variant reduces risk by using a simple evolution of the Poly/SiON 40 nm approach, but its lower transistor switching speed and performance is unsuitable for reasonable FPGA performance ranges in most market segment.

The 28 HPL process, by contrast, offers a better performance/power metric than both 28 LP and 28 HP processes when taking FPGA switching speeds into account. See Figure 1. To date, although the 28 nm HPL process is now used by many silicon vendors, Xilinx is the only FPGA manufacturer using it. For more information on the benefits of the 28 nm HPL process, refer to WP312, *Xilinx Next Generation 28 nm FPGA Technology Overview.*

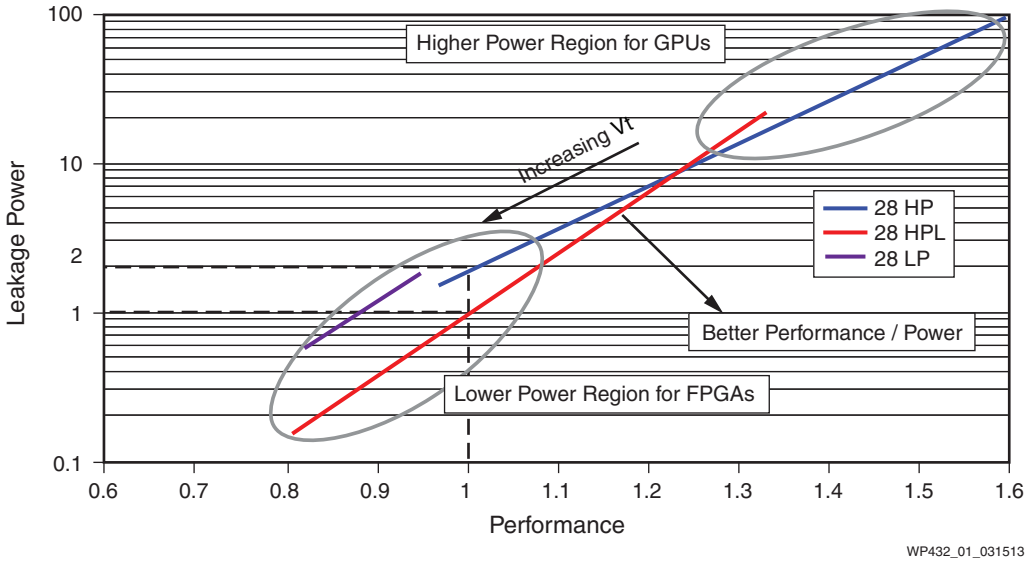

Figure 1: **Performance vs. Leakage in 28 HPL, 28 HP, and 28 LP Processes**

Scalable Optimized Architecture

In addition to choosing a silicon manufacturing process ideally suited for FPGAs, Xilinx refined its device architecture to further cut power consumption and produce a series of device families with the best performance per watt. The Artix™-7 family is ideal for low-power and low-cost applications, while the Virtex®-7 family is suitable for systems requiring the highest performance and capacity. The Kintex-7 family serves as the ideal mid-range solution, delivering the industry's best price/performance-per-watt FPGA.

For flexibility, all 7 series families use the same architectural building blocks, providing easy design migration across families and eliminating time-consuming design modification and re-optimization. Common architectural blocks include logic fabric, block RAM, DSP, clocking, and analog mixed signal (AMS).

Targeting a Kintex-7 device for a new product ensures upward scalability to a Virtex-7 FPGA for greater performance, or downward scalability to an Artix-7 FPGA for further reductions in cost and power. For example, a portable ultrasound system implemented with a Kintex-7 FPGA can be re-targeted for a high-end cart application using a Virtex-7 FPGA, or for a lower-end portable system using an Artix-7 FPGA to support a smaller form factor and smaller feature set.

By using a scalable optimized architecture, developers can easily retarget their designs and save many months of development effort. Re-using design elements also permits designers to dramatically lower their code verification and maintenance costs. For more information, refer to WP373, *Xilinx Redefines Power, Performance, and Design Productivity with Three Innovative 28 nm FPGA Families:* Virtex-7, Kintex-7, *and* Artix-7.

Industry's Leading Performance-per-Watt Solution

To achieve superior performance per watt, Xilinx leveraged a number of architectural innovations. The Xilinx fourth-generation column-based Advanced Silicon Modular Block (ASMBL™) architecture made it possible to design Kintex-7 devices with an ideal feature mix at the lowest price point. This columnar layout eliminates constraints, such as dependencies between I/O count and fabric array size; it allows power and ground to be placed anywhere on the device, and allows disparate hard IP blocks to be scaled, independent of each other and of surrounding resources. Because of this columnar layout, the Kintex-7 family flexibly balances different types of resources — including logic fabric, block RAMs, and DSP resources to target mid-range applications.

Critical to the resource mix are the types of inputs/outputs (I/Os) and the transceiver count needed for specific applications. As shown in Table 1, The XC7K70T, XC7K160T, XC7K325T, XC7K410T devices feature a moderate number of transceivers and high-range (HR) I/Os — ideal for applications requiring price-performance balance, such as wireless, audio, video, broadcast, aerospace, and defense. In addition, due to the flexibility of the architecture, the family also includes the XC7K355T, XC7K420T, and XC7K480T FPGAs. These devices provide higher transceiver-to-I/O ratios, ideal for higher-performance wired applications.

Table 1: **Kintex-7 Device Table and Resource Mix**

Device	XC7K70T	XC7K160T	XC7K325T	XC7K410T	XC7K355T	XC7K420T	XC7K480T
Market	**Ideal Price-Performance Balance**				**Higher Transceiver-to-I/O Ratios**		
Sample Applications	**Wireless, Audio, Video, Broadcast, and Aerospace and Defense**				**Higher Performance Wired Applications**		
Logic Cells (k)	65,600	162,240	326,080	406,720	356,160	416,960	477,760
Block Memory (Kb)	4,860	11,700	16,020	28,620	25,740	30,060	34,380
I/O	300	400	500	500	300	400	400
DSP48E1 Slices	340	600	840	1,540	1,440	1,680	1,920
PCIe Gen2 Hard Block(1)	1	1	1	1	1	1	1
Analog Mixed Signal Block	1	1	1	1	1	1	1
Transceivers (12.5 Gb/s)	8	8	16	16	24	32	32
Memory Interface Performance (Mb/s)(2)	1,866	1,866	1,866	1,866	1,066	1,066	1,066

Notes:

1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
2. Supported in a mid-speed grade devices.

Cost-effective packaging options contribute to the Kintex-7 FPGAs' price-performance leadership. For example, lidless flip-chip packages are available for much of the family to meet performance requirements while dramatically reducing device cost. The Kintex-7 FPGA packaging technology also contributes to transceiver quality, as explained in the High-Speed Transceivers section.

Kintex-7 devices are half the cost of the Virtex-6 HXT device *and* offer essentially equivalent performance. With similar fabric architecture, the Kintex-7 family is an attractive option for Virtex-6 device users seeking to reduce system power and cost. Compared to the Spartan®-6 family, Kintex-7 FPGAs offer major performance advantages and 3X the capacity at the same cost, all while consuming half the power. The result is the industry's best price/performance-per- watt solution.

Key Features

There are a number of key architectural blocks that differentiate the Kintex-7 FPGA as the industry's leading mid-range device. Among those include the main logic fabric, embedded memory, DSP resources, high-speed transceivers and memory interface, and integrated block for PCI Express.

Logic Fabric

As part of their scalability, all 7 series FPGAs use the same logic architecture. Configurable logic blocks (CLBs) consist of two slices, each comprised of four 6-input look-up tables (LUTs), four flip-flops, carry-chain logic, and four additional flip-flops that can be configured as latches, as shown in Figure 2. There are also dedicated multiplexers that can be used to build larger high-speed multiplexers without having to use LUTs, resulting in more efficient use of the fabric.

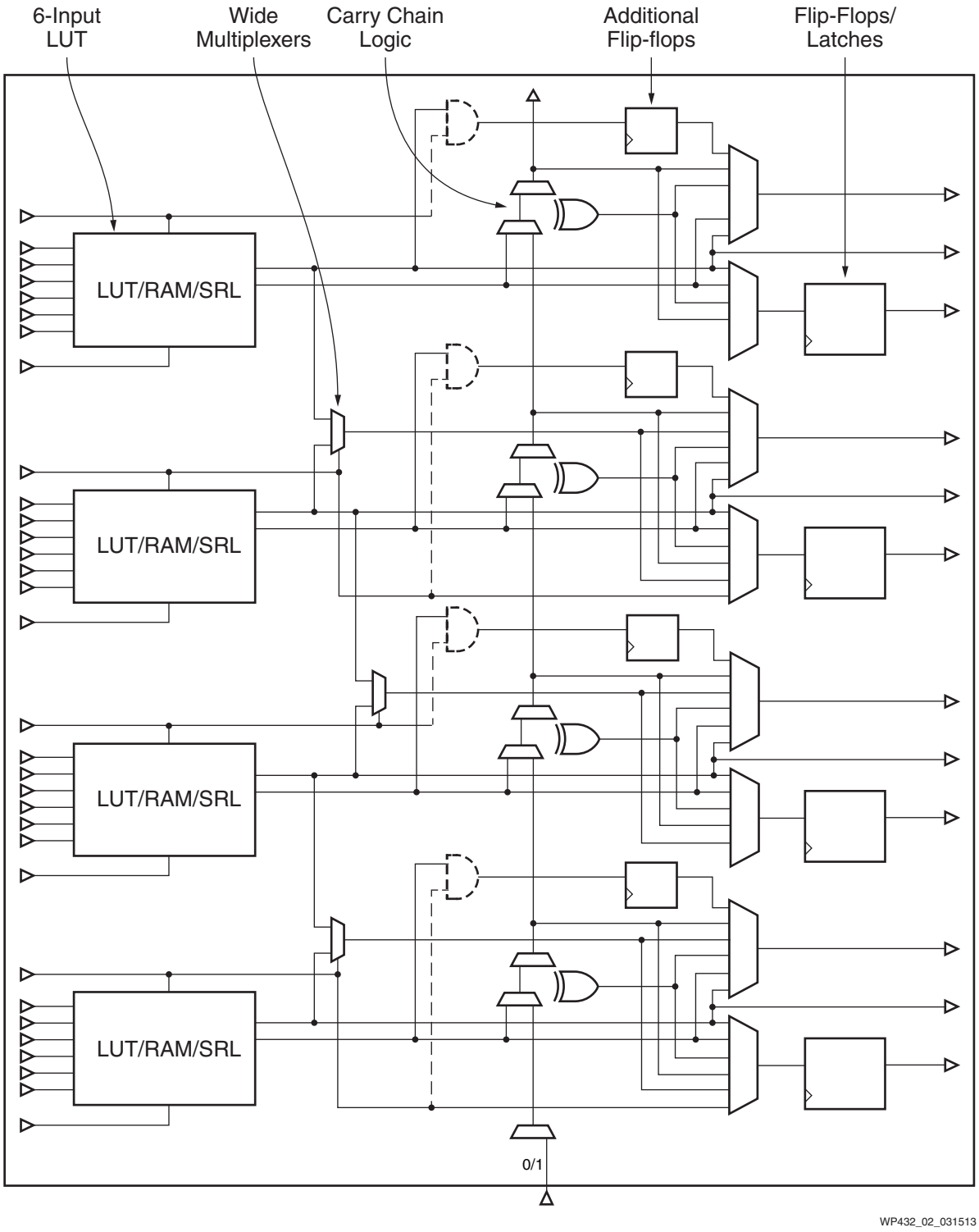

Figure 2: **Configurable Logic Block**

The slice architecture is a further development of the Virtex-6 family, using the same LUT structure, control logic, enables, and outputs. Hence, the similarity with Kintex-7 FPGAs enables an easy migration path from Virtex-6 FPGA applications. For more information on the CLB architecture, refer to WP405, *Xilinx 7 Series FPGAs: The Logical Advantage*.

Embedded Memory

With the highest block RAM-to-logic ratio in a mid-range device, the Kintex-7 family provides up to 34 Mb within 477K logic cells. Each dual-port block RAM stores 36 Kb, with 32 Kb allocated for data storage and 4 Kb used as parity bits. A block RAM can be divided into two completely independent 18 Kb block RAMs that can each be configured to any aspect ratio from 16Kx1 to 512x36. Conversely, two adjacent 36 Kb block RAMs can be cascaded without any additional logic to implement a 64Kx1 dual-port RAM.

Along with the flexibility of the block RAM itself, users can use 6-input LUTs in the FPGA logic as small memory arrays and combine them with block RAMs to create memories in a variety of sizes. Designers benefit from the granularity of LUTs and the configurability of embedded block RAMs to implement any size of storage or buffering function. For more information on this subject, refer to WP377, *Xilinx 7 Series FPGAs Embedded Memory Advantages*.

Other features of embedded memory include integrated error correction (ECC), byte-wide write enable, and power-down mode. Each 64-bit-wide block RAM can leverage eight additional Hamming-code bits to perform single-bit or double-bit ECC during the read process. Byte-wide write enable gives the ability to write 8-bit portions of incoming data, useful when interfacing to microprocessors. As for power-down mode, the Xilinx ISE® and Vivado™ configuration software can automatically recognize when block RAMs are unused and disable them as appropriate, conserving overall system power.

DSP Resources

With up to 1,920 DSP slices and 2,845 GMACs of performance, the Kintex-7 family more than doubles the DSP bandwidth of competing devices in its class. Each multiplier supports 18x25 bits to implement up to 35x25 multiply operations using a pre-add block running at up to 741 MHz. These devices share the same high-performance silicon process and DSP architecture as Virtex-7 FPGAs, but the logic-to-DSP ratio has been optimized to lower costs for higher-volume, performance driven markets. These applications include wireless and wired communications, broadcast, medical imaging, and military radar.

High DSP performance is achieved through the capabilities of the fourth generation DSP48E1 slice. As shown in Figure 3, five high-speed interconnects are used to combine two DSP48E1 slices into a single DSP48E1 tile to implement a variety of arithmetic operations of variable precision while maintaining F_{MAX} performance.

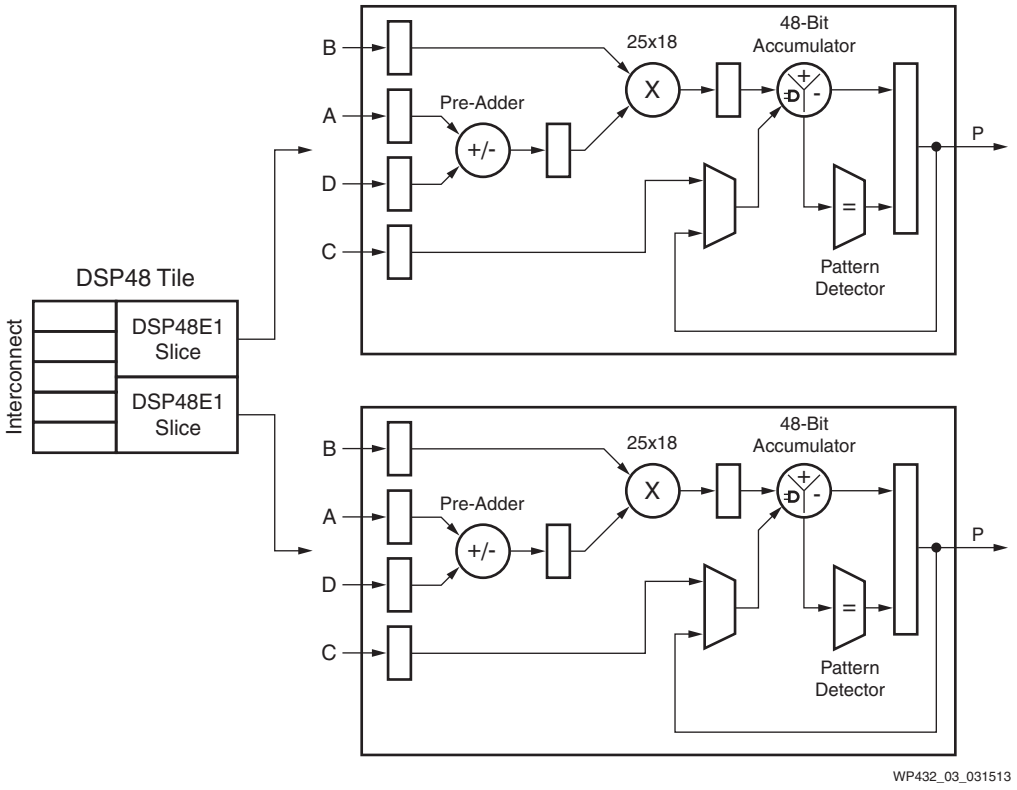

Figure 3: **DSP48E1 Slice Architecture**

High-Speed Transceivers

The Kintex-7 family features high-speed serial transceivers (GTX) capable of data rates of up to 12.5 Gb/s — the highest line rate available in a mid-range FPGA. Up to 32 transceivers in a single device deliver 800 Gb/s of peak serial bandwidth (full duplex), ideal for wired, wireless, storage, military, and broadcast applications. Because GTX transceivers cover a wide variety of connectivity and applications — some of which require high performance, while others can sacrifice performance for power efficiency and flexibility — the transceivers are based on a rich mix of both ring and LC tank oscillator-based PLLs to enable the lowest jitter performance and highest signal quality in their class.

Among the protocols these GTX line rates support are 11G SONET and OTU2 for networking, 9.8G CPRI for wireless, and PCI Express Gen 3. In the case of wired communications infrastructure, these transceivers are suitable for low-cost *N*x10G systems — particularly 10G backplane applications, where industry-leading continuous time linear equalization (CTLE) and auto-adaptive decision feedback equalization (DFE) features make the Kintex-7 family a robust solution. These equalization capabilities compensate for signal distortion across transmission channels with minimal user intervention (a key concern in backplane applications), eliminating the need for manual tuning of each backplane channel. In the case of wireless applications, the combination of transceivers, DSP resources, and specialized IP enable the smallest antennas for remote radio head, LTE, and 4G applications.

The Kintex-7 family includes a unique combination of transceiver technology and packaging to deliver the highest signal integrity at the lowest price point. While high-performance transceiver technology is paired with higher performance packaging, moderate transceiver performance is paired with less expensive

packaging. To deliver its mid-range leadership, Kintex-7 devices offer "market-tuned" serial bandwidth coupled with cost-optimized packaging. See DS180, *7 Series FPGAs Overview* for more details.

Memory Interface

Memory read/write bandwidth can often dictate overall system performance. To dramatically improve interface speeds at 28 nm, Xilinx made significant advances in clocking technology and chose to harden critical datapath components. As a result, the Kintex-7 device offers up to 1,866 Mb/s DDR3 data rates in a mid speed grade.

The memory solution consists of a flexible controller and physical layer (PHY) for interfacing designs to DDR3 and DDR2 SDRAM devices. The memory controller supports an array of external memory types for flexible system design such as for streamlined access to video and data storage.

PCI Express

The family features both soft IP for PCI Express (PCIe) Gen 3 and integrated hard IP for PCIe Gen 2, with full support for endpoint and root port configurations. The integrated hard block supports up to eight Gen 1 and Gen 2 channels, while the soft IP supports up to eight Gen 3 channels with 8 Gb/s performance. This approach permits systems to be implemented with PCIe Gen 1 or Gen 2 initially, and then benefit from upgrades to PCIe Gen 3 later. IP solutions for PCIe Gen 3 can be shown to offer performance similar to hard block solutions.

All PCIe solutions for 7 series FPGAs are designed to the AMBA4 AXI4 specification. This provides a plug-and-play use model when integrating the PCI-Express block with the rest of the FPGA design.

Applications

The versatility of the Kintex-7 FPGA makes it ideal for a variety of applications. The following examples demonstrate how its features, along with the device's overall performance-per-watt, make it an excellent fit in many end markets.

Remote Radio Head for Wireless Infrastructure

Smartphones and tablets are driving ubiquitous connectivity, and the surging demand for data and video over cellular networks requires careful network planning to future-proof networks as much as possible while optimizing growing investment needs. While the demand for data is swamping networks, voice traffic continues to leverage earlier-generation standards such as GSM and WCDMA. As operators build out network capacity to serve the ever-growing demand for data, wireless infrastructure must support numerous standards such as GSM, WCDMA, and LTE in a multi-mode, or *heterogeneous*, network.

Radio heads are critical components in a wireless infrastructure that brings the network to users as one of its closest touch-points. To improve performance and reach, radio heads are no longer sitting in the base station chassis, but are instead reaching out as remote components in wireless networks to gain greater proximity with users. Closer user proximity improves spectrum utilization, network capacity, and a better user experience at lower cost. Radio heads in the network, though agnostic of air interface technology to a great extent, are required to support multiple air interfaces, several carriers over contiguous or non-contiguous bands, and multiple antennas. To

adapt to a continuously evolving technology and demand profile, these radio heads are designed to be field-upgradable with capabilities to allow remote control, configuration, and monitoring.

Among the key requirements in remote radio head design is DSP and transceiver performance, enabling support for more complex waveforms, wider bandwidths, and the latest interface standards. Transceiver performance is closely coupled with the need for higher signal processing capability to transfer data to and from the base station chassis and provide efficient connectivity to high-speed data converters. Because remote radio heads are commonly installed at the top of cell towers, buildings, or other infrastructure, their size and weight are critical to installation, reliability, maintenance, and operational expenses. In addition to these constraints, pricing pressures in the remote radio head market rivals that of consumer markets; therefore, system cost is also key.

With an optimal balance of performance, power, and cost, the Kintex-7 FPGA is an ideal fit for remote radio head design. With up to 1,920 DSP slices, these devices deliver the highest GMAC processing capacity in their class — important for implementing critical digital algorithms in these systems. As illustrated by the block diagram in the Figure 4, Xilinx offers a comprehensive portfolio of IP building blocks for multi-mode radio design, providing functionality for digital up-conversion (DUC), digital down-conversion (DDC), crest factor reduction (CFR), and pre-distortion (DPD).

Additionally, transceivers are capable of supporting CPRI 9.8 Gb/s for connectivity between the remote radio head and the base station chassis as well as 12.5 Gb/s JESD204A/B for data converter connectivity on the radio. Because of the constraints posed by outdoor operation, the low-power architecture of the Kintex-7 FPGA provides critical value in a distributed base-station architecture, where operating costs must be minimized and cooling resources are limited. The HPL process and architectural innovations of the 7 series enable this device family to deliver the highest performance per watt. See Figure 3.

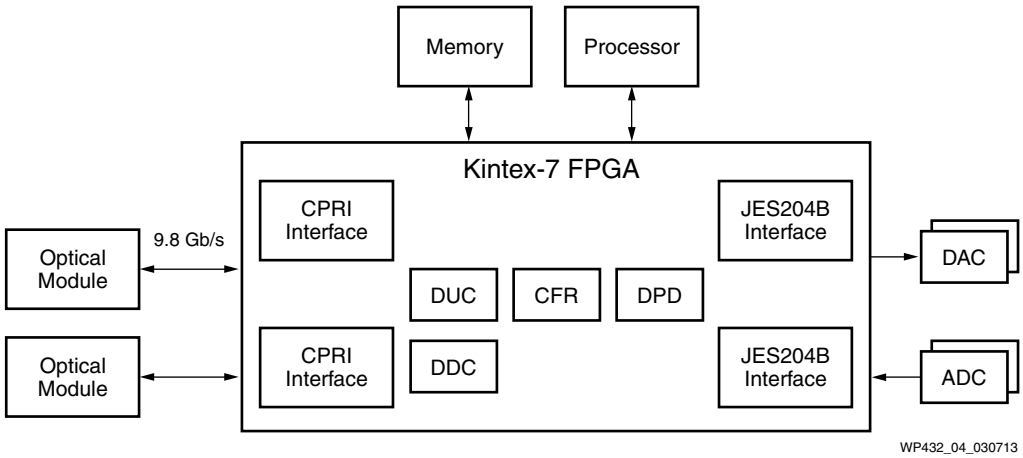

Figure 4: **Remote Radio Head Design with the Kintex-7 FPGA**

Airborne and Vehicular Military Radio

Another application for the Kintex-7 FPGA is software-defined radio (SDR), now a common method of military communication. Radios are carried by foot soldiers, installed in air and ground vehicles, and located at base stations. Distinguishing signals, identifying the number of discrete signals that can be supported, selectivity, noise blanking, and signal demodulation all depend heavily on the DSP processing capacity of the receiver circuit.

A Kintex-7 FPGA is a natural fit for mid-range and high-end SDR systems requiring more bandwidth support than handheld radios but still needing power efficiency. The device delivers the necessary DSP bandwidth to support a continually growing number of channels and modulation schemes while delivering optimal performance per watt. Vehicular and airborne SDR systems, in particular, are typically installed in standard-sized compartments with very limited area, ventilation, and cooling resources. This in turn creates design challenges for heat dissipation. Because the Kintex-7 device is based on the HPL process, power efficiency and performance compared to competing solutions make the Kintex-7 FPGA family highly optimal for vehicular and airborne SDR systems.

Data security is usually a priority in military communication systems. A common requirement is the separation of encrypted and unencrypted data in the hardware. One way to accomplish this is using two different devices to achieve separation. The need for multiple devices can be avoided, however, when leveraging the Xilinx Isolation Design Flow (IDF), which enables multiple physically isolated functions to be implemented within a single FPGA. IDF utilizes a "fence" of unused device components between each function, preventing information leaks of classified or sensitive information out of the system. By implementing IDF, designers can achieve optimal system integration within a single Kintex-7 FPGA.

Figure 5 illustrates a typical approach to an SDR design concept using the Kintex-7 FPGA SDR architecture.

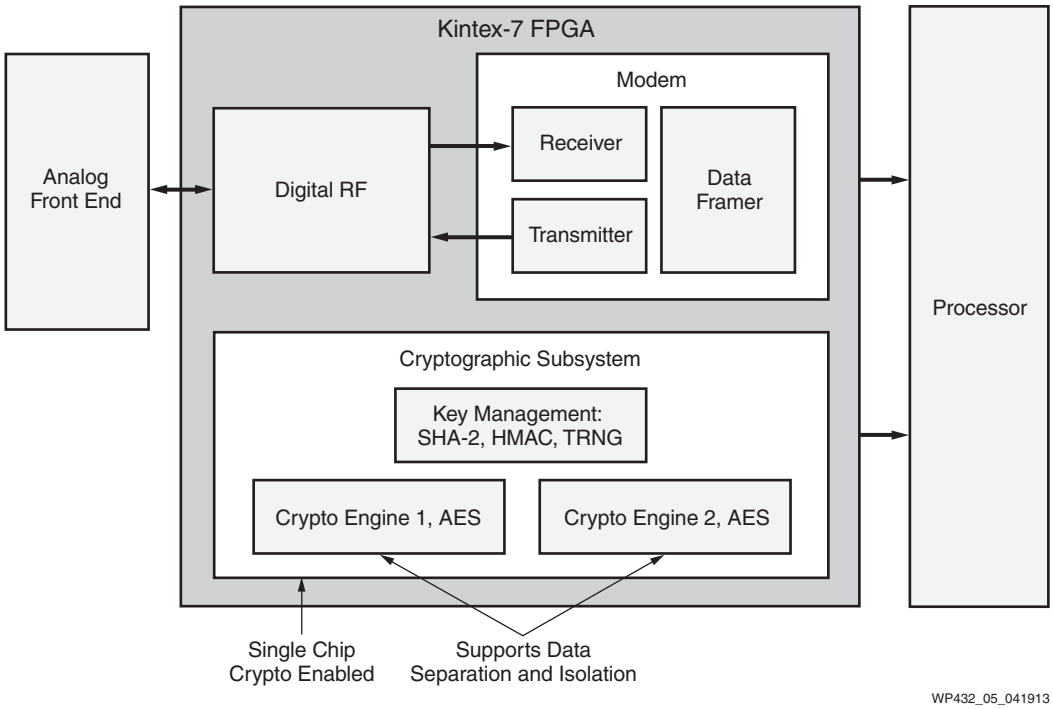

Figure 5: **Software Defined Radio Design with a Kintex-7 FPGA**

Conclusion: A Balanced Approach to Performance, Power, and Cost

Wireless communications infrastructure and software defined radio are just a few of the market segments served by the Kintex-7 family. Its DSP resources, serial connectivity, memory, and logic performance — all combined with power efficiency and ideal price point —make it suitable for applications such as high-volume 10G PON OLT line cards, cockpit displays in avionics, and 128-channel high-resolution portable ultrasound, among others. Table 2 shows a sample set of applications where the Kintex-7 FPGA is an ideal fit.

Table 2: **Application Examples for Kintex-7 FPGAs**

Industry	Application Example
Wireless	Remote radio head, base stations, channel cards, microcells, mobile backhaul
Wired	GPON, 40G and 100G bridging and switching, packet processing, muxponders, datacenter applications
Medical	Portable ultrasound, medical imaging
Aerospace and Defense	Military radio, software defined radio, synthetic aperture radar, avionics, munitions
Audio, Video, and Broadcast	Routers, switches, 4K2K camera, edge QAM, projectors
Consumer	4K2K displays
Industrial	Smart surveillance, cameras, machine vision, automotive vision, industrial printers

The need for a mid-range solution represents the evolving requirements of the programmable device market. While FPGA use models have historically ranged from simple glue logic to ultra-high bandwidth processing, many designs now need sophisticated functionality that lies between these two extremes. The versatility of the 7 series FPGAs allows designers to meet such a wide range of requirements, and the Kintex-7 family, by way of its optimal mix of resources, strikes an ideal balance of price, performance, and power efficiency.

To learn more, visit www.xilinx.com/kintex7, or to get started designing with a Kintex-7 device, visit www.xilinx.com/products/boards_kits/7series.htm.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/24/13	1.0	Initial Xilinx release.
09/13/13	1.1	Updated Table 1.

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