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# Artix-7 FPGAs: Performance and Bandwidth in a Cost-Optimized Device

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In FPGA and SoC-based applications, aggressive cost constraints are often coupled with low power requirements, typically due to the small form factor and high-volume nature of these end-applications and respective markets. The challenge is balancing performance and capability within these constraints. In military radio, for example, battery life is important, but so is high-speed transmission of video, voice and data. The same can be said for wireless infrastructure equipment: small cell base stations must maximize bandwidth in a small form factor with limited cooling resources.

Xilinx introduced the Artix®-7 FPGA family with these types of applications in mind, delivering high-end performance at the lowest achievable power and cost. This white paper provides an overview of this FPGA family and how it achieves high-end functionality in a low-cost part. The white paper concludes with multiple application examples, highlighting the Artix-7 FPGA's diverse capabilities.

# The Compounding Effects of Power Consumption

Designers seeking power efficiency are not concerned solely with, say, extending operational time. They also consider the impact power has on cost, performance, and form factor.

As power consumption increases, so do cooling costs and the real estate needed for power management. More regulators, heat sinks, and cooling fans require more power to operate, aggravating the energy consumption problem. More components translate into more PCB area and complexity, adding to board cost and lengthening development time. As a result, high power consumption has secondary effects on system cost.

The other indirect effect is on performance; more switching across the logic fabric and I/Os increases dynamic power. Make-or-break performance requirements can force a system to exceed a desired power budget, or stringent power requirements might not give adequate headroom for performance.

Because of these secondary effects, selecting the right device can be non-trivial. Some FPGA vendors attempt to focus on either performance or power, while in the process neglecting those applications that need to cost-effectively balance both.

# High Performance with Reduced System Power and Cost

When performance is a priority, many designers are forced to move to more expensive mid-range devices — sacrificing power and cost — or settle for low-end solutions that sacrifice performance and feature set. The Artix-7 FPGA attempts to resolve this dilemma, focusing much of its innovation on high-end functionality for cost-conscious markets. Table 1 shows a high-level view of some of the applications covered by Artix-7 FPGAs.

*Table 1:* **Applications for Artix-7 FPGAs**

| Industry | Application Example |
|---|---|
| Wireless | Picocells, Backhaul Units |
| Wired | Access Devices |
| Medical | Portable Ultrasound, Endoscopes |
| Aerospace and Defense | Military Radio, Munitions |
| Audio, Video, and Broadcast | Routers and Switches, Monitors, Projectors |
| Consumer | DSLR Cameras, Digital Displays, Set-Top Boxes |
| Automotive | Infotainment |
| Industrial | Machine Vision, Programmable Logic Controllers |

Table 2 shows the breadth of devices of varying resource mix within the family.

*Table 2:* **Artix-7 FPGA Resource Information**

| | Part Number | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Resources** | XC7A12T | XC7A15T | XC7A25T | XC7A35T | XC7A50T | XC7A75T | XC7A100T | XC7A200T |
| Logic Cells (k) | 12,800 | 16,640 | 23,360 | 33,280 | 52,160 | 75,520 | 101,440 | 215,360 |
| Total Block RAM (Kb) | 720 | 900 | 1,620 | 1,800 | 2,700 | 3,780 | 4,860 | 13,140 |
| I/O | 150 | 250 | 150 | 250 | 250 | 300 | 300 | 500 |
| DSP Slices | 40 | 45 | 80 | 90 | 120 | 180 | 240 | 740 |
| PCIe® Gen2(1) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Analog Mixed Signal | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Max. Memory Interface (Mb/s) | 1,066 | 1,066 | 1,066 | 1,066 | 1,066 | 1,066 | 1,066 | 1,066 |
| Transceiver (6.6 Gb/s Max Rate)(2) | 2 | 4 | 4 | 4 | 4 | 8 | 8 | 16 |

**Notes:**

1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers.

## Low Power in a Scalable Optimized Architecture

Based on TSMC's 28 nm high performance, low power (HPL) process, Xilinx 7 series FPGAs offer the ideal balance of power, performance, and capacity. The 7 series consists of:

- Artix-7 devices for low power and low cost
- Kintex®-7 devices for an optimal balance of price and performance
- Virtex®-7 devices for highest performance and capacity

Careful comparisons to TSMC's low power (LP) and high power (HP) processes indicate that the HPL process achieves the lowest power and highest performance when considering the operating range of an FPGA. In principle, an HP process sees performance gains over an HPL process but at levels of static power that are often unacceptable for programmable devices. Conversely, at low leakage points, 28 HPL offers a better performance-power metric than 28 LP, as shown in Figure 1. The ability to extend into a lower leakage region enables a low-power Artix-7 device, for example, to be substituted without switching to a different process.

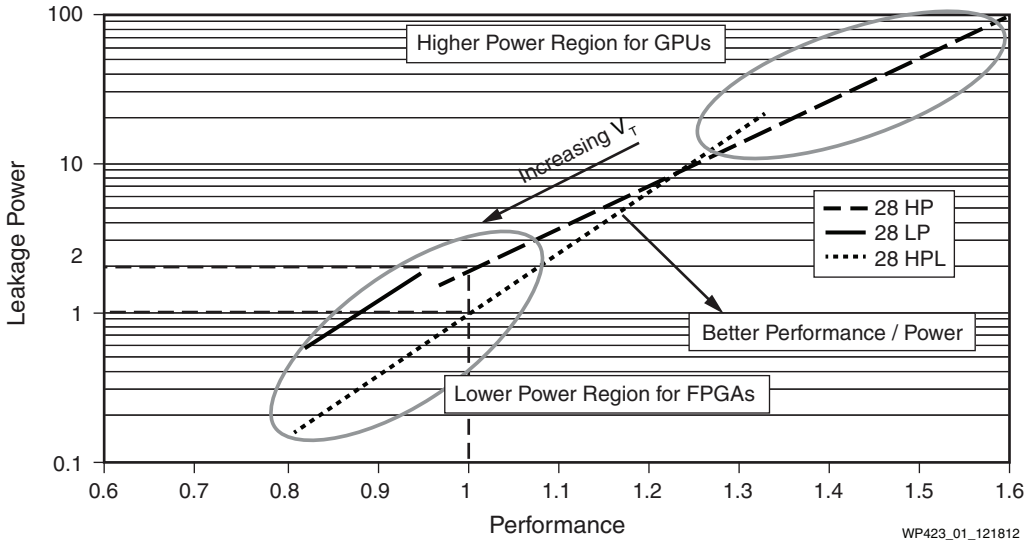


*Figure 1:* **HPL Process Enables Low Power and High Performance in the Artix-7 FPGA**

By using the HPL process and the same architectural building blocks for the Virtex-7, Kintex-7, and Artix-7 families of FPGAs, the 7 series provides easy design migration across families, eliminating time-consuming reoptimization. Targeting an Artix-7 device for an existing product ensures scalability for next-generation systems. Conversely, a high-performance Virtex-7 or Kintex-7 FPGA-based system can be migrated to an Artix-7 FPGA if an application needs to be scaled down to reduce power, cost, and size. For more information on the 7 series scalable optimized architecture, refer to the Xilinx white paper: WP373, *Xilinx Redefines Power, Performance, and Design Productivity with Three Innovative 28 nm FPGA Families: Virtex-7, Kintex-7, and Artix-7 Devices*.

The breakthrough of combining the HPL process with the Xilinx 7 series architecture cuts total power consumption by 50% compared to the previous generation (see Figure 2). This provides headroom for additional performance, logic density, I/O bandwidth, and signal processing. Designers have the flexibility to either lower power by 50% or take advantage of greater performance and capacity at previous power budgets.

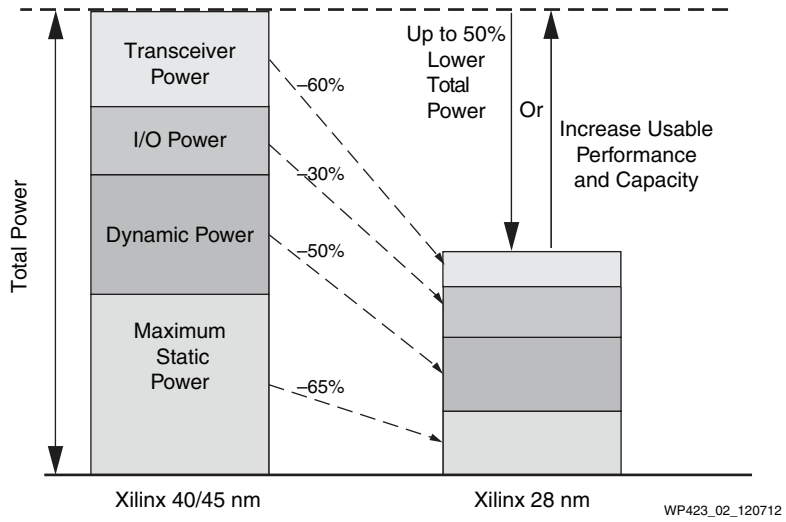


*Figure 2:* **The 28 nm HPL Process Reduces Power Consumption by 50 Percent**

## Low Power Speed-Grades with Artix-7 FPGAs

Voltage scaling and power binning—while available in all 7 series FPGAs and SoCs—is especially versatile in the Artix-7 family. This process of screening for devices that can operate at lower voltages yet retain optimal performance can significantly reduce static and dynamic power. This is made possible by the headroom gained with the 28 HPL process. This is similar to the power strategy first introduced in Virtex-6 and Spartan®-6 devices.

In particular, Artix-7 FPGAs that can run at 0.95V are designated -1LI, delivering equivalent performance to regular -1 speed grades at 1.0V. Industrial-grade (I-grade) devices provide a much wider operating temperature range. Xilinx screens these devices for performance and tighter leakage specifications relative to standard devices. Only the lower leakage and higher performance FPGAs are selected for the -1LI speed-grade. When compared to standard speed-grades and commercial temperature range devices, this screening method yields a 65% reduction in static power and 10% lower dynamic power without any drop in performance, as shown in Table 3. This is particularly useful for industrial, aerospace and defense, and other applications that are thermally challenged and hence power constrained.

For applications that need even greater performance than a -1 speed grade but without the industrial operating range requirement, -2LE devices deliver -2 speed grade performance with 45% lower static power than commercial grade parts. A summary of these low-power speed grades is shown in Table 3.

*Table 3:* **Voltage Scaling and Power Binning**

| | C-Grade Devices | I-Grade Devices | -1LI (0.95V) | -2LE (1.0V) |
|---|---|---|---|---|
| Voltage ($V_{CCINT}$) | 1.0V | 1.0V | 0.95V | 1.0V |
| Static Power | Nominal | -30% | –65% | –45% |
| Dynamic Power | Nominal | Nominal | –10% | 0% |
| Performance | Nominal | No degradation | No degradation | No degradation |

## Reducing Cost through System Integration

Artix-7 FPGAs enable BOM cost reduction by eliminating the need for additional components on the board. For example, the Artix-7 family features a fully programmable analog sub-system that includes 12-bit Analog-to-Digital Converters (ADCs), a 17-channel front-end, and on-chip monitors and sensors. The system is ideal for simple analog monitoring or complex signal conditioning and processing.

The integration with FPGA logic allows for microprocessors, controllers, and DSP functions to handle monitoring and “housekeeping” functions on a single device. An Artix-7 device leveraging on-chip Analog Mixed Signal (AMS) can be used for applications such as industrial programmable logic controllers, multi-function printers, and digital SLR cameras, among others, where component and board cost savings are imperative. For more on programmable analog, refer to the Xilinx white paper: WP392, *Xilinx Analog Mixed Signal Solutions*.

Collectively, these on-chip components reduce overall system cost. By enabling multi-chip functionality on a single device, designers require fewer components, minimize the number of board layers and simplify PCB development — reducing not just the BOM but development cost. Secondary benefits include smaller form factor, faster development cycles, and lower power due to fewer components and less chip-to-chip communication.

For more information on BOM cost reduction and integration capabilities of Artix-7 FPGAs and other cost-optimized devices, refer to Xilinx white paper: WP460, *Reducing System BOM Cost with Xilinx's Cost-Optimized Portfolio*.

## Logic Fabric Optimized for Performance

As part of its scalability, the 7 series architecture uses the same flexible logic across all families. Configurable logic blocks (CLBs) consist of two slices, each comprised of four 6-input look-up tables (LUTs), four flip-flops, carry-chain logic, and four additional flip-flops that can be configured as latches. There are also dedicated resources that can be used to build large high-speed multiplexers (as opposed to utilizing LUTs). For more information, refer to the Xilinx white paper: WP405, *Xilinx 7 Series FPGAs: The Logical Advantage*.

The 7 series slice architecture is based closely on that in the Virtex-6 and Spartan-6 families, using the same LUT structure, control logic, enables, and outputs. These similarities between the Spartan-6 and Artix-7 devices provide an easy migration path.

## Highest DSP Bandwidth in a Cost-Optimized Device

With a block RAM-to-logic ratio of up to 13.1 Mb within 215K logic cells, and 740 DSP48E1 slices for the same capacity, the Artix-7 FPGA rivals the logic density of mid-range products while still benefiting from lower power and cost. The DSP resources provide up to 930 GMACs of DSP performance— 3X that of the competition — useful for imaging and communication applications that require extensive processing capacity.

## High-Speed Interfaces

Supporting up to sixteen 6.6 Gb/s transceivers that have been optimized for low power, the Artix-7 family offers the fastest line rates for cost-sensitive markets. These transceivers support pre-emphasis and continuous time linear equalization (CTLE) to compensate for signal distortion across transmission channels. With up to 211 Gb/s of total throughput, the Artix-7 family is a low-cost alternative for bandwidth-sensitive applications that would otherwise require mid-range solutions.

Because memory read/write bandwidth can affect overall system performance, the Artix-7 family offers up to 1,066 Mb/s DDR3 data rates, the highest in the industry for FPGAs in its class. The memory solution consists of a flexible controller and physical layer (PHY) for interfacing designs and AMBA® advanced extensible interface (AXI4) slave interfaces to DDR3 and DDR2 SDRAM devices. The controller supports an array of external memories for flexible system design, such as streamlined access to video and data storage.

## MicroBlaze Processor for Embedded Applications

More than just a data processing or high-speed interface engine, an Artix-7 FPGA can serve as a microcontroller, a real-time processor, or a complete SoC for cost-sensitive applications. Xilinx's proprietary MicroBlaze™ soft IP processor can be implemented in programmable logic while achieving competitive DMIPS performance and consuming minimal real estate. Rather than opting for an ASSP with companion FPGA, an embedded designer can implement an SoC on a single Artix-7 FPGA while integrating ASSP functionality, as well as capabilities typically not possible in many low-cost ASSPs and microcontrollers.

With multiple configurations for multiple use models, a MicroBlaze processor can be instantiated any number of times to distribute tasks and workloads across the FPGA logic, and

easily instantiated through "presets" within the Vivado Design Suite (Release 2017.3 or later). Use models and related DMIPS/MHz performance are shown below.

*Table 4:* **MicroBlaze Processor Presets and Relative Performance**

| Vivado Preset | Use Model | $F_{MAX}$ | Performance | Logic Cells |
|---|---|---|---|---|
| Microcontroller | Basic Control Applications | 200 MHz | 1.1 DMIPS/MHz | 1,000 LCs |
| Real-Time Processor | RTOS Applications | 160 MHz | 1.3 DMIPS/MHz | 4,500 LCs |
| Application Processor | Linux Applications | 120 MHz | 1.4 DMIPs/MHz | 6,500 LCs |

### Small Form Factor

The Artix-7 family features a 50% smaller package at equivalent density compared to the Spartan-6 family. As low-cost devices move into more compact applications, such as hand-held software-defined radios, feasibility largely depends on the device's form factor and the restrictions caused by limited PCB area. Artix-7 devices are offered in various types of low-cost wire-bond packages — from chip-scale packaging with 0.5 mm ball spacing, the smallest form factor, to BGA packaging with 1.0 mm ball spacing, ideal for low-cost PCB manufacturing. Refer to the Artix-7 Product Table for more information on packaging.

## Market Applications

The following examples demonstrate how the Artix-7 FPGA enables cost-sensitive applications to deliver high processing power and bandwidth while benefiting from low power consumption.

### Military Software-Defined Radio

One of the most ideal fits for the Artix-7 FPGA is in military software-defined radio (SDR). A military SDR network can comprise permanent military bases, mobile command centers, ground and airborne vehicles, manpack, and hand-held devices for individual foot soldiers. Mobile SDR systems in worst-case use locations often require higher transmit power — which typically leads to higher battery drain, increased size and weight (often driven by the need for bigger batteries), and ultimately, higher costs.

In addition, extensive DSP processing capacity is needed to support a variety of radio protocols (each with unique waveform characteristics) for voice, data, and video communication modes. Supporting many protocols is challenging, as is maintaining the required level of security in all protocols. The SDR must also be able to operate reliably from worst-case radio locations within a complex strategic topology as well as in dense radio frequency (RF) spectrum environments that can exacerbate undesired cross-channel interference and receiver desensitization.

SDRs must be designed for:

- The capability to recognize and support encoding/decoding of many different communications protocols
- High-performance waveform processing in all supported protocols
- Small form factors, permitting a high degree of designed-in portability
- Minimal power consumption by the FPGA, providing extended use periods between battery replacement/recharge

## DSP Processing Capacity for Wideband Protocol Support

Critical to an SDR is the modem that performs baseband signal preprocessing and RF signal improvements. Because of its parallel processing-based architecture and reconfigurability, an FPGA implementation of the modem is common — and the Artix-7 FPGA is an ideal fit, as shown in Figure 3. With up to 740 DSP slices, the Artix-7 device can provide up to 930 GMACs of DSP performance — three times that of competing FPGAs, and far greater than any stand-alone DSP processor or GPU.

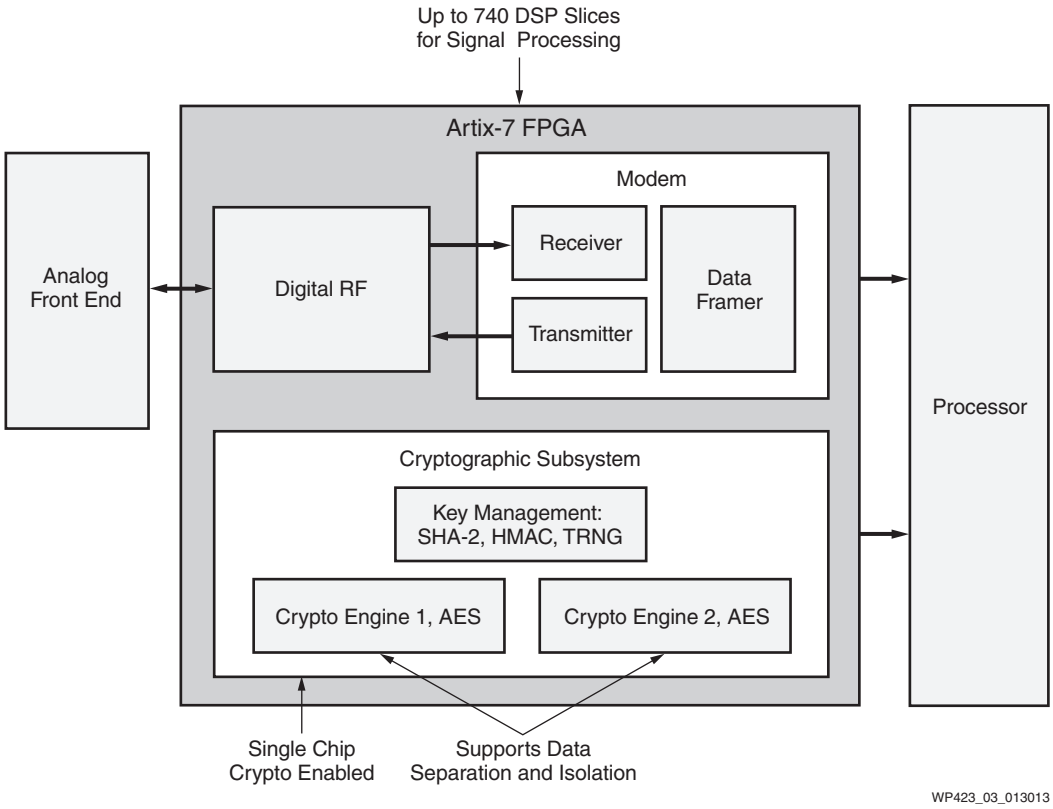


*Figure 3:* **System Integration for Software-Defined Radio**

## Small Form Factor for Hand-Held Radio

Size and weight are high priorities when deploying SDRs for foot soldiers. The Artix-7 A100T FPGA is available in a 15x15 mm package with 101,440 logic cells, the industry's smallest FPGA for its capacity. With 215,360 logic cells in a 19x19 mm package, the Artix-7 A200T FPGA is an ideal solution for implementing an SDR modem as well as a cryptographic engine, as represented in Figure 3.

## Single-Chip Cryptographic Solution for System Integration

Because security is a major concern in SDR, a key requirement is the compartmentalization of encrypted and unencrypted data. Typically, this would require two separate devices, but Xilinx supports an Isolation Design Flow (IDF) that enables multiple physically isolated functions to be implemented within a single FPGA. IDF utilizes a “fence” of unused device components between each function, ensuring the system meets security requirements while still benefiting from single-chip integration.

### Low Power for Long Battery Life

While DSP processing is critical, limitations of battery operation demand just the right performance-to-power balance. The Artix-7 FPGA's performance per watt ensures long battery life while still providing the needed processing capacity. As a matter of comparison, a typical ASSP-based implementation is comprised of a DSP processor and ASSP for the modem function, along with a three-device cryptographic engine. The Artix-7 A200T device consumes up to 35% less power than such an implementation.

## Wireless Backhaul: High Bandwidth in Urban Locations

Mobile backhaul has come to the forefront within cellular communications networks due to the rapid growth in data traffic. Because the majority of the growth in cellular traffic is happening in urban and suburban areas where fiber media is often not practical, operators plan to boost capacity by deploying small cells at street level in places like lamp posts, traffic lights, and walls of adjoining buildings. To interconnect these small cells in clusters and to connect them to the nearest aggregation points, operators must deploy low-power, low-cost backhaul units, whose microwave radio links can span up to tens of miles.

### High-Speed Transceivers for Bandwidth Support

A traditional mobile backhaul unit typically supports several Ethernet links. In wireless mobile backhaul, the traffic is forwarded between Ethernet links and radio channels using an internal Ethernet switch. High-speed transceivers are required at both ends of the unit. As a low-cost alternative, the Artix-7 family delivers maximal bandwidth with its sixteen 6.6 Gb/s transceivers for both Ethernet and RF links using JEDEC JESD204B connectivity to data converters.

### Integrating Multi-Chip Functionality onto a Single Device

One half of the backhaul unit contains packet processing, traffic management, and timing synchronization functions. The other half of the unit supports modem channels for signal processing. For modem functionality, two requirements are key:

- Adequate high-performance DSP processing
- High-speed transceivers that interconnect with the data converters to produce high rates of data throughput

The Artix-7 devices have the right mix of logic density, IP support, and DSP resources to support these functions. The Artix-7 A200T device, for example, with 215,360 logic cells, can integrate a backhaul solution composed of all the needed packet processing, traffic management, and timing/synchronization blocks as well as a single high-speed radio channel.

A typical two-channel ASIC/ASSP-based solution needs a stand-alone Ethernet switch, a traffic manager function in an FPGA, an external timing and synchronization device, one modem device per channel, external PHY for serial connectivity, and a control plane CPU.

This is a seven-device solution. The Xilinx solution requires only *two* devices for its programmable implementation of the same functionality, as shown in Figure 4.

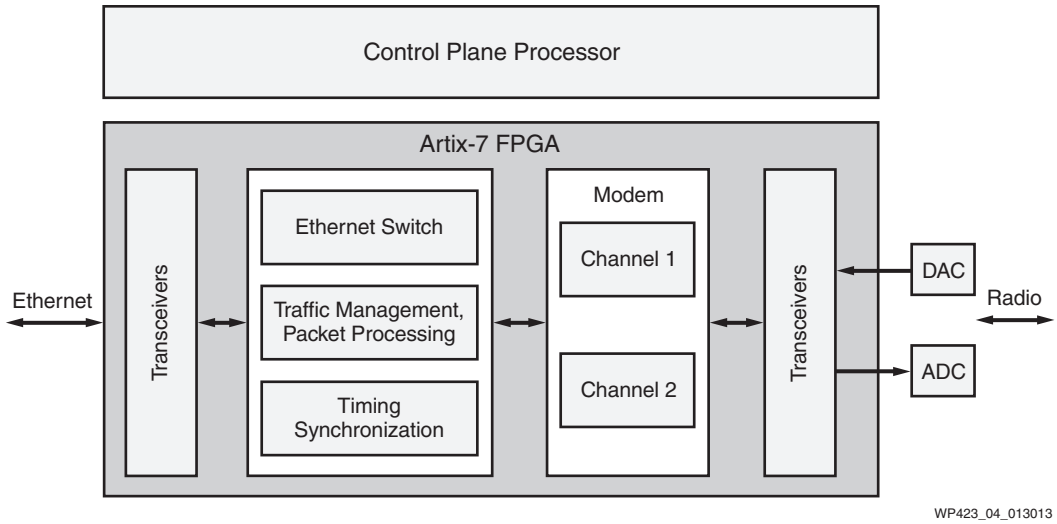


*Figure 4:* **Integrating Multi-Device Functionality for Microwave Mobile Backhaul**

### Low Power in a Small Form Factor

To maintain low visual impact, backhaul units are typically compact, making it challenging to dissipate the heat they generate. By integrating much of the system on a single FPGA, the Artix-7 FPGA solution minimizes dissipation needs, not just by reducing device count, but also by reducing inter-device I/O dissipation. An Artix-7 FPGA-based design can reduce power by up to 50% compared to a multi-device solution.

## Programmable Logic Controllers

Programmable logic controllers (PLCs) are commonly used in industrial settings for packaging, printing, assembly, and other processes. The controller itself manages the coordination of I/O devices, motor drives, and machine vision systems to ensure all the components are tightly synchronized and are operating efficiently. This requires fast computation, real-time processing, and high-speed I/O interfacing. Furthermore, because these PLC modules are of standard size, form factor is equally critical.

### Re-Programmability for Scalability

Traditionally, PLCs have been implemented via microprocessors in conjunction with an ASIC or ASSP and dedicated plug-in modules. While the main processor runs an OS with the PLC run-time software, motion control, and Human Machine Interface (HMI) user interface, the ASIC- or ASSP-based plug-in cards manage safety functions and communication. PLCs of this architecture are customized for use in different applications by selecting which plug-in modules to insert into the PLC. FPGAs make it possible to maintain the versatility of plug-in cards, but with lower cost and a smaller form factor. With an FPGA-based architecture, plug-in modules themselves can become scalable and reconfigurable, enabling PLC suppliers to maximize economy of scale. A single hardware platform can be configured to support different Industrial Ethernet or fieldbus protocols, or perform virtually any application from motion control to custom I/O functions. As communication standards evolve, FPGA-based communication cards can be remotely upgraded to take advantage of the latest protocols without changing hardware, thus, offering suppliers the ability for end-customers to future-proof their systems.

## On-Chip Real-Time Processing and High-Speed I/O Interfaces

FPGAs provide an advantage over ASICs not just for re-programmability and easier upgradeability but also for their ability to perform real-time processing. Because the control algorithms have become increasingly complex, in many cases the FPGA can fully integrate major control functions via its on-chip processor while coordinating and synchronizing other systems on the factory floor. With a 32-bit MicroBlaze™ processor for real-time control and 52,160 logic cells, the Artix-7 A50T FPGA is ideal for smaller capacity but compute intensive controllers. The larger Artix-7 A75T FPGA is ideal for modules with multiple communication ports combined with additional functions. With FreeRTOS support in Xilinx SDK tool suites, embedded designers can implement these real-time functions in a familiar eclipse-based design environment.

As mentioned, the key to PLC functionality is rapid communication with neighboring control systems. The Artix-7 A50T provides up to four 6.25 Gb/s transceivers, supporting PCIe® x4 Gen2 for communication with the processor. The high transceiver count relative to package size makes the Artix-7 A50T device ideal for integrating multiple networking standards across multiple slave devices.

## Isolation of Safety Functions

To satisfy the strict requirements for functional safety in industrial applications and comply with industrial safety standards such as SIL3, Xilinx's Isolation Design Flow (IDF) enables multiple physically isolated functions to be implemented within a single FPGA. The safety design can be isolated from other critical functions in the device to ensure that potential errors in non-critical circuitry do not impact the safety application. By completely isolating the safety application from other parts of the design, suppliers can achieve safety certification much faster by reusing the safety design across platforms. See Figure 5.

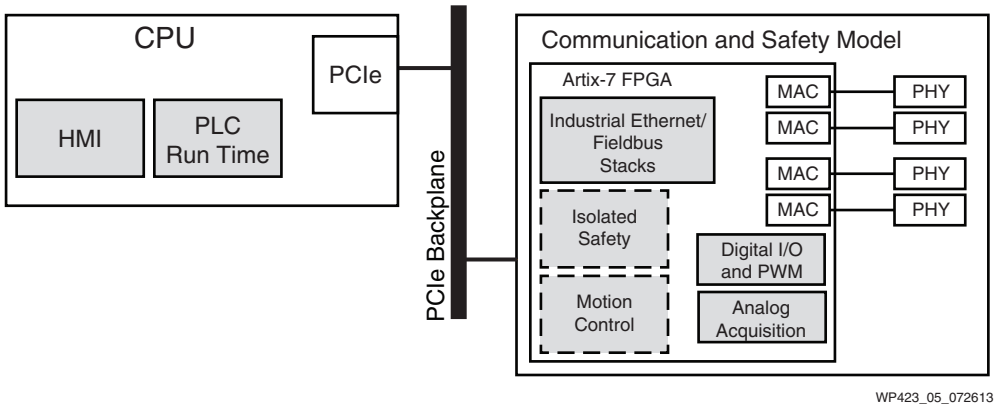


*Figure 5:* **Artix-7 FPGA Used for a Programmable Logic Controller**

# Conclusion: High-End Value in a Low-Cost Platform

The applications described in this white paper are only a few examples. Because end-users in cost-competitive markets continue to demand more functionality and greater bandwidth, the Artix-7 family of FPGAs fits into many other market segments, such as consumer, wired infrastructure, and broadcasting.

System architects are compelled to examine every component on their bill of materials to minimize system cost while still meeting performance requirements. Not only does the Artix-7 family deliver the greatest performance per watt in its class, but its integration of analog mixed-signal capabilities reduces BOM cost and overall system power. By leveraging the Artix-7 family, designers can deliver high-end value in these highly competitive, cost-sensitive markets.

For more information, visit www.xilinx.com/artix7.

# Additional Resources

1. DS180, *7 Series FPGA Overview*
2. WP312, *Xilinx Next Generation 28 nm FPGA Technology Overview*
3. WP389, *Lowering Power at 28 nm with Xilinx 7 Series FPGAs*

# Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 07/16/12 | 1.0 | Initial Xilinx release. |
| 12/18/12 | 2.0 | Changed document title and introductory text section on page 1. Deleted section **Edge Applications for Market Expansion**. Added new Table 1. In section Low Power in a Scalable Optimized Architecture, updated Figure 1 and Figure 2. Added new section Reducing Cost through System Integration, including new Figure 3 (BOM Cost). Updated Market Applications. In sections Logic Fabric Optimized for Performance and Military Software-Defined Radio, updated various Artix-7 FPGA numeric parameters, both in text and in Figure 3. Added new section Industrial Motor Control, including new Figure 5. Updated Conclusion: High-End Value in a Low-Cost Platform. |
| 02/07/13 | 2.1 | Updated page 1, Reducing Cost through System Integration, High-Speed Interfaces, High-Speed Transceivers for Bandwidth Support, and On-Chip Components and Analog Mixed Signal for System Integration. |
| 07/31/13 | 2.2 | Updated High Performance with Reduced System Power and Cost. Removed Industrial Motor Control. Added Programmable Logic Controllers. |
| 12/17/14 | 2.3 | Added Low Power Speed-Grades with Artix-7 FPGAs. |
| 09/27/16 | 2.4 | Updated High Performance with Reduced System Power and Cost. |
| 01/24/18 | 2.5 | Updated title and abstract. Updated High Performance with Reduced System Power and Cost and Reducing Cost through System Integration. Added MicroBlaze Processor for Embedded Applications. Updated On-Chip Real-Time Processing and High-Speed I/O Interfaces and Isolation of Safety Functions, and made other minor typographical edits. |
| 03/16/18 | 2.5.1 | Updated URLs. |

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