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# Simulating FPGA Power Integrity Using S-Parameter Models

*By: Hany Fahmy and Colin Warwick of Agilent Technologies, Inc.*
*and Jack Carrel, Ray Anderson, Harry Fu, and Romi Mayder of Xilinx, Inc.*

The purpose of a Power Distribution Network (PDN) is to provide power to electrical devices in a system. Each device in a system not only has its own power requirements for its internal operation, but also a requirement for the input voltage fluctuation of that power rail. For Xilinx Kintex™-7 and Virtex®-7 FPGAs, the analog power rails have an input voltage fluctuation requirement of not more than 10 mV peak-to-peak from the 10 kHz to the 80 MHz frequency range. The self- generated voltage fluctuation on the power rails is a function of frequency and can be described by Ohm's Law: Voltage (frequency) = Current (frequency) * Self-Impedance (frequency).

Thus, if the user determines the self-impedance (frequency) and knows the current (frequency) of the PDN, then the voltage (frequency) can be determined. The self-impedance (frequency) can easily be determined by simulating the frequency domain self-impedance profile of the PDN and is, thus, the subject of this white paper.

# Overview

Before simulating the frequency domain self-impedance profiles of a PDN, it is important to establish expectations for the simulation results. To do this, an understanding of the fundamental concepts must be attained:

- Series-Resonance Circuit and Impedance Minimums
- Parallel-Resonance Circuit and Impedance Maximums
- Frequency Components of Electrical Signals
- S-Parameter Model vs. Lumped RLC Model for Decoupling Capacitors

## Series-Resonance Circuit and Impedance Minimums

A series-resonant circuit is defined by a capacitor (C) and inductor (L) that are connected in series. When the $X_C$ (capacitive reactance) and $X_L$ (inductive reactance) are equal in magnitude and opposite in phase, the current is at maximum. This condition gives rise to an impedance minimum. The frequency at which this equality occurs is called the series-resonant frequency and is described by Equation 1:

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \textit{Equation 1}$$

A common series-resonant circuit is formed by the *capacitance* (C) and the *parasitic inductance* (L) of a given capacitor mounted on a printed circuit board. Figure 1 shows the schematic circuit representation while Figure 2 shows the frequency domain impedance profile.

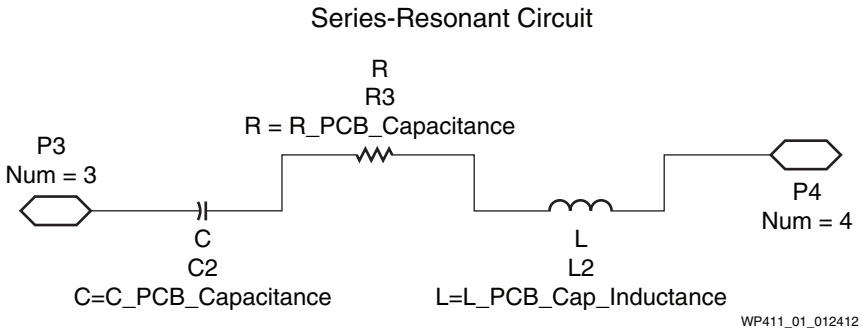


*Figure 1:* **Series-Resonant Components of a PCB-Mounted Capacitor**

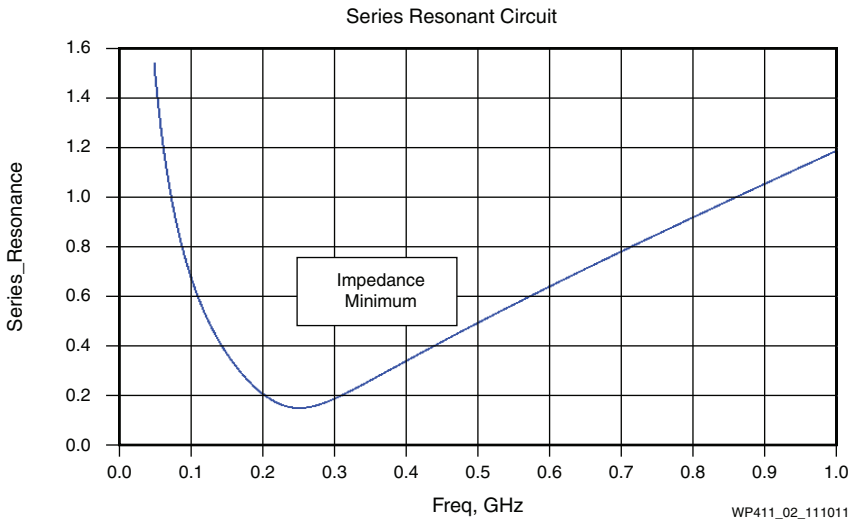


*Figure 2:* **Frequency-Domain Impedance Profile of PCB-Mounted Capacitor**

## Parallel-Resonance Circuit and Impedance Maximums

A parallel anti-resonant circuit is defined by a capacitor (C) and inductor (L) that are connected in parallel. When the $X_C$ (capacitive reactance) and $X_L$ (inductive reactance) are equal in magnitude and opposite in phase, the reactive branch currents are also equal in magnitude and opposite in phase. This gives rise to a minimum total current and thus, a maximum total impedance is created. The frequency at which this condition occurs is called the parallel anti-resonant frequency and is described by Equation 2:

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \textit{Equation 2}$$

A common parallel anti-resonant circuit is one formed by the die capacitance and package inductance. Figure 3 shows a schematic circuit representation while Figure 4 shows the frequency domain impedance profile.

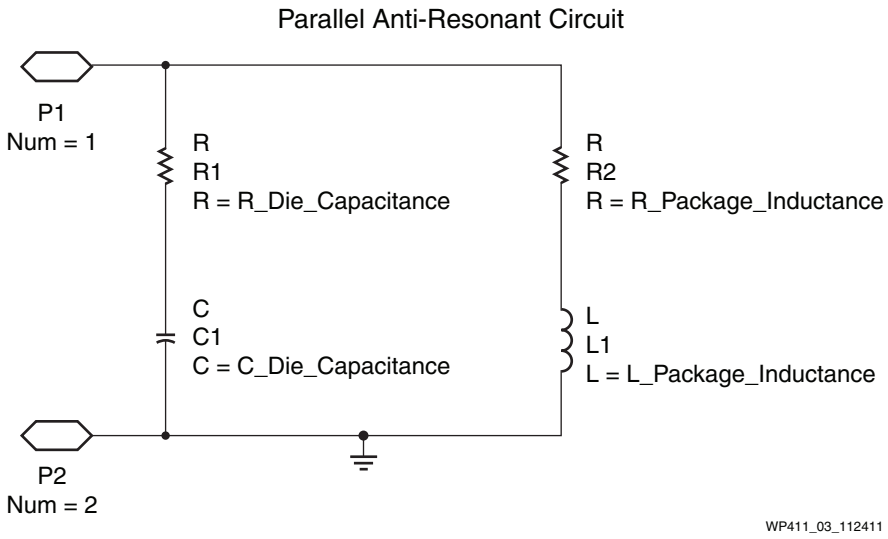


*Figure 3:* **Parallel Anti-Resonant Components of Die and Package Properties**

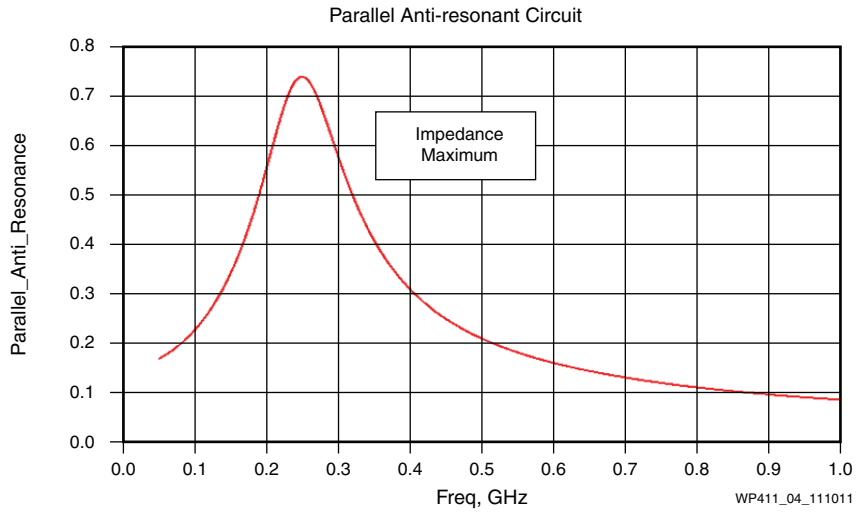


*Figure 4:* **Frequency-Domain Impedance Profile of Die and Package Properties**

## Frequency Components of Electrical Signals

The frequency domain current profile of $V_{CCO}(f)$ is shown in Figure 5 and Figure 6 as simulated at the BGA power balls of the Xilinx Virtex-7 XC7VX485T FPGA in the FFG1761 pin package.

In the example, the simulation is running a memory interface at 1.866 Gb/s with a PRBS15 data pattern. The power spectral density of $V_{CCO}(t)$ is wide-banded, extending from 10 MHz up to the 10 GHz. As the data traffic pattern and activity change, the simulations demonstrate that the dominant frequency components of the power spectral density *also* change. Therefore, the simulations show that PDN noise is a wide-band phenomenon; PDN simulations must, therefore, be run over a wide-band frequency range.

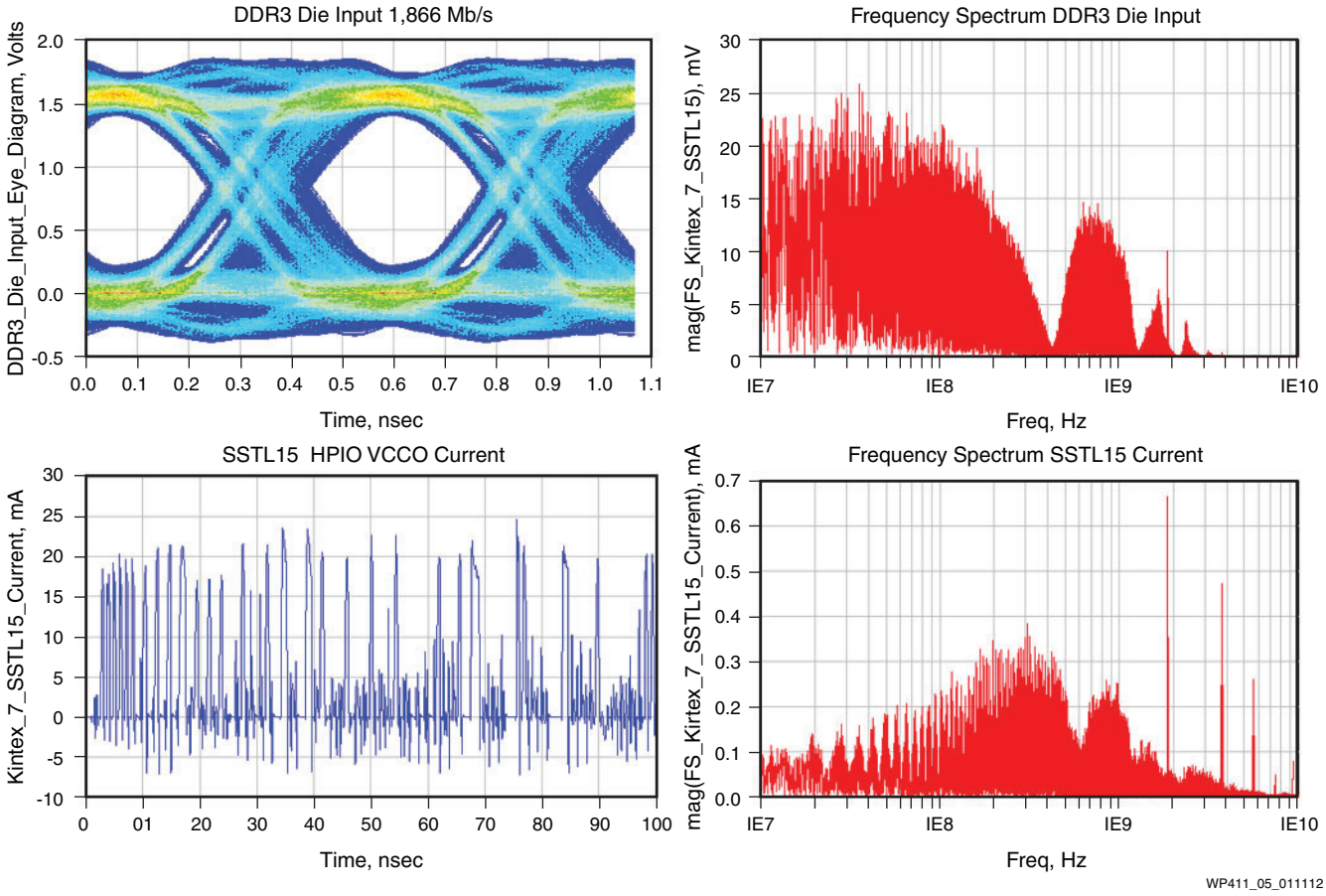


*Figure 5:* **Memory Interface Simulation Activity Patterns**

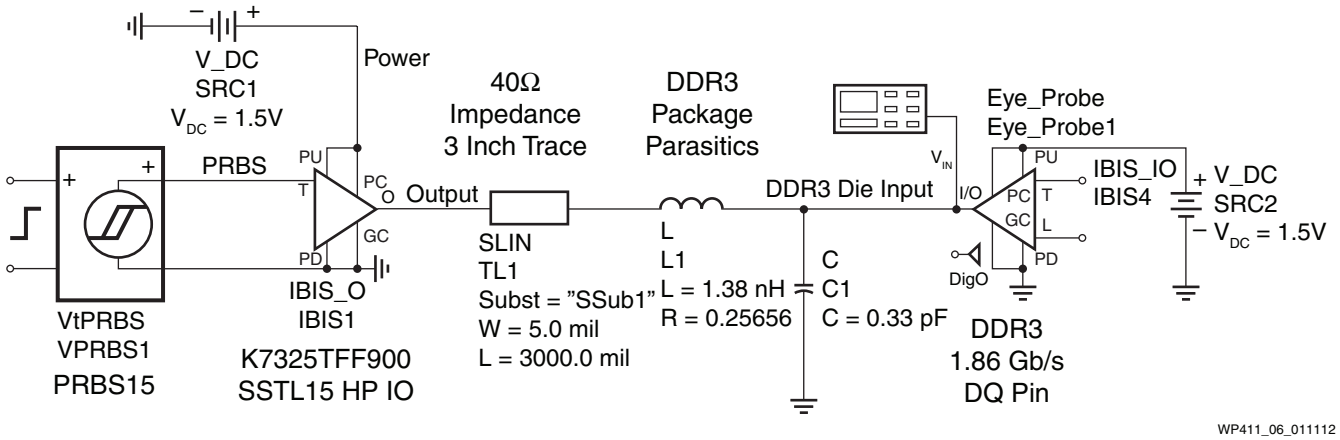


*Figure 6:* **Simulation Test Setup**

Because the power spectral density is of a wide band, the frequency domain self-impedance profile must be simulated over a wide range. Below 1 kHz, the voltage regulator module (VRM) dominates the frequency domain self-impedance profile. Above 10 GHz, the on-die capacitance dominates the impedance profile. Thus, Xilinx recommends running the simulations from 1 kHz to 10 GHz.

## S-Parameter Model vs. Lumped RLC Model for Decoupling Capacitors

As a comparison between using lumped RLC circuits and S-parameters to run PDN simulations, the decoupling capacitors portion of the PDN circuit is examined first.

In this simulation, an attempt is made to curve-fit an S-parameter model for common X5R capacitors in the following EIA case sizes: 0201, 0402, 0603, 0805, 1206, and 1610. After matching the capacitive reactance and the series-resonant frequency given in Equation 1,the percentage error of the inductive reactance at 100 MHz is measured.

These simulations are done at room temperature (25°C) with no applied DC bias. Figure 7 through Figure 9 show the circuit schematic representations. Figure 10 and Figure 11 show the simulation results.

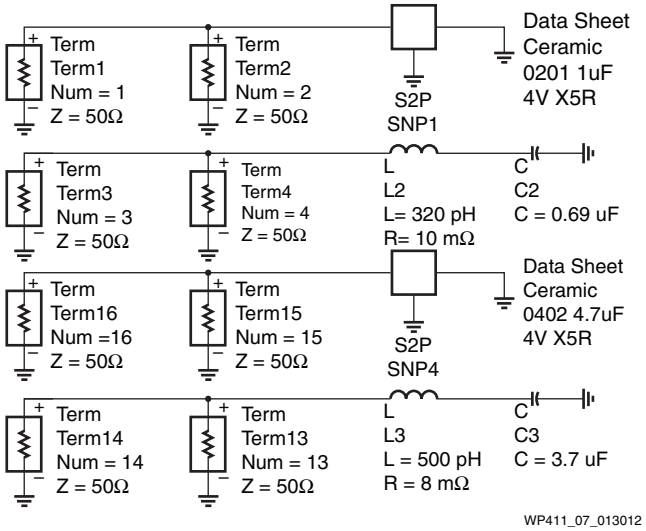


*Figure 7:* **Decoupling Capacitors Simulation, Schematic Representation 1**

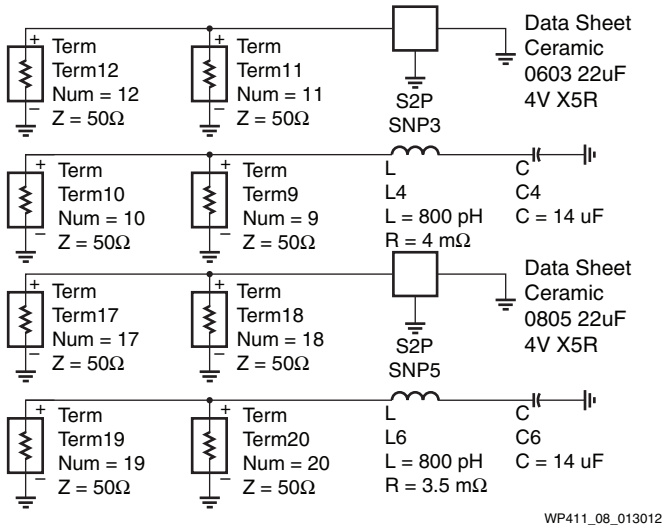


*Figure 8:* **Decoupling Capacitors Simulation, Schematic Representation 2**

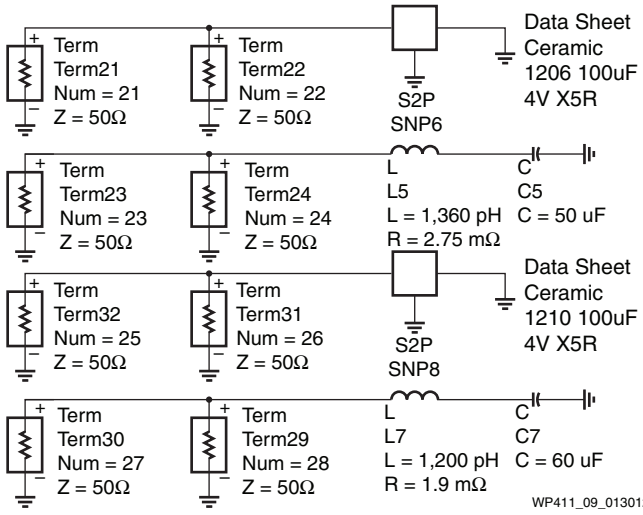


*Figure 9:* **Decoupling Capacitors Simulation, Schematic Representation 3**

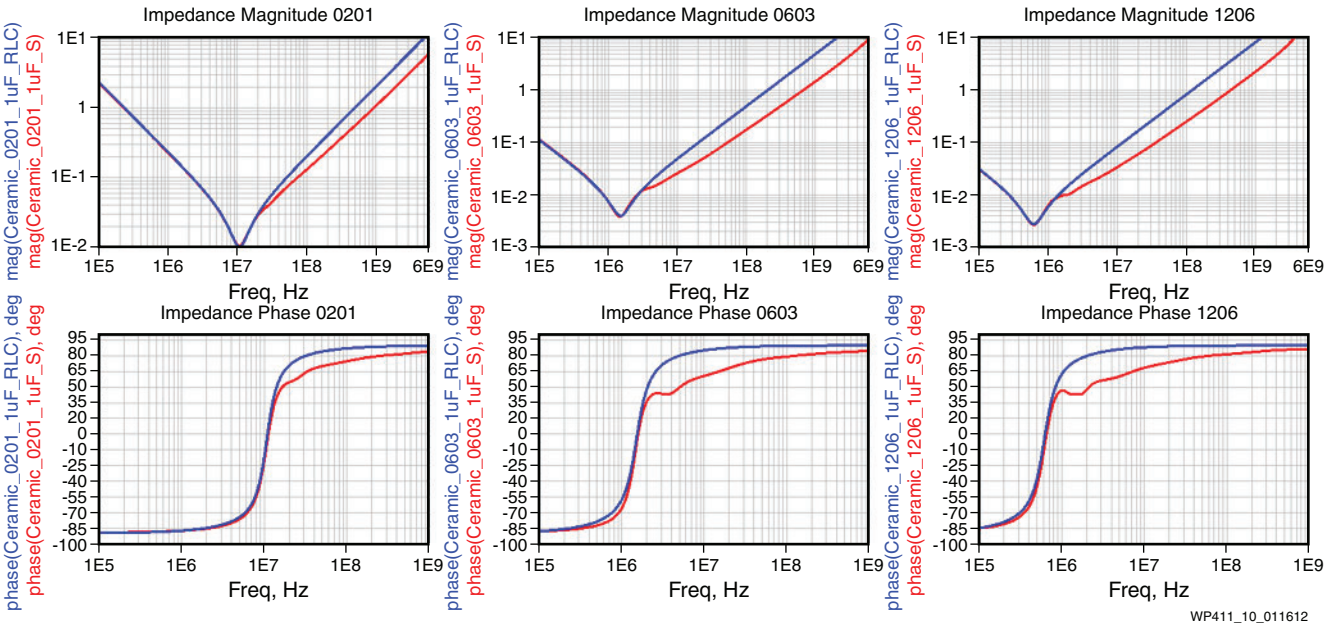


*Figure 10:* **Simulation Results (EIA Case Sizes 0201 / 0603 / 1206)**

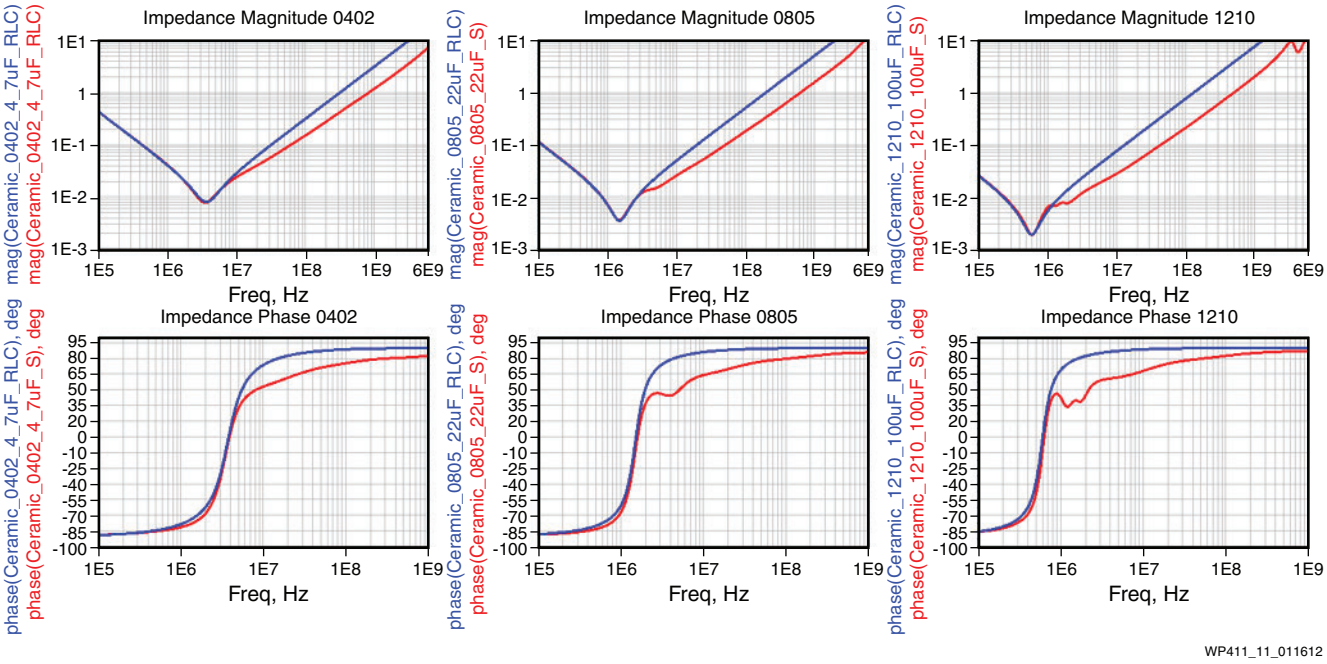


*Figure 11:* **Simulation Results (EIA Case Sizes 0402 / 0805 / 1210)**

A summary of the data is shown below in Table 1:

*Table 1:* **Summary of Result Data, Decoupling Capacitors Simulation**

| Size | Capacitance (µF) | | | Impedance Magnitude @ 100 MHz | | | Series-Resonant Frequency |
|---|---|---|---|---|---|---|---|
| EIA Code | S-Parameter | Data Sheet | % Error | S-Parameter | RLC Model | % Error | |
| 1210 | 60 | 100 | 66.7 | 0.209 | 0.751 | 259.3 | 600 KHz |
| 1206 | 50 | 100 | 100.0 | 0.255 | 0.845 | 231.4 | 700 KHz |
| 805 | 14 | 22 | 57.1 | 0.18 | 0.501 | 178.3 | 1.5 MHz |
| 603 | 14 | 22 | 57.1 | 0.178 | 0.501 | 181.5 | 1.5 MHz |
| 402 | 3.7 | 4.7 | 27.0 | 0.15 | 0.313 | 108.7 | 3.5 MHz |
| 201 | 0.69 | 1 | 44.9 | 0.129 | 0.198 | 53.5 | 10 MHz |

It is known that the typical capacitor manufacturer specifies the capacitance of a capacitor with zero DC bias and 0.5 Vrms AC voltage, while the s-parameter models are typically measured with a 0 dbm AC signal.

In S-Parameter Models for Decoupling Capacitors section, the various methods for generating the S-parameter model of a capacitor are examined.

## S-Parameter Models for Decoupling Capacitors

At first glance, the measurement of the capacitor's PDN impedance profile (the impedance with respect to frequency) seems to be a simple task, but several subtle details are required to ensure the measured data is accurate.

The frequency domain measurement is usually accomplished by utilizing a Vector Network Analyzer (VNA). The obvious method is to probe the PDN making an S11 measurement, and then convert the measured s-parameters to impedance by means of the Equation 3 relationship:

$$Z_{dut} = 50\,\frac{1 + S11}{1 - S11} \qquad \textit{Equation 3}$$

An impedance measurement using this method, however, has inherent inaccuracies due to the fact that the instrument typically has a 50Ω input impedance and the PDN has a very low impedance (typically in the milliohm range). The accuracy of the measured VNA data inherently has errors because the typical uncertainty of S11 (when rho, the reflection coefficient, is near 1) can be in the 1%–2% range.

This equates to an impedance uncertainty in the 0.3Ω-to-0.4Ω range. If PDN impedances in the milliohm range are being measured, it quickly becomes obvious that the desired impedance measurement is lost in the measurement uncertainty.

A second factor to consider is that the inductive parasitics of the probing arrangement can easily exceed the value of the DUT inductance. There is no easy way to back out the probe parasitics from the measured data.

Fortunately, an S21 measurement is a good alternative to an S11 measurement to determine the PDN impedance. In this method, it is found that $Z_{dut} = 25(S21)$. With this measurement technique, the solder of the decoupling capacitor is included in the measurement. By utilizing the S21 measurement, the impedance uncertainty is reduced into the 10s-of-milliohms range. In addition, the probe parasitics are in series with 50Ω as opposed to being in series with the DUT impedance, which reduces their effects to near negligible levels. For a more complete discussion of this topic, see *Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency*

*Range* presented at DesignCon 2010 by Istvan Novak of SUN Microsystems and Yasuhiro Mori and Mike Resso of Agilent Technologies (http://www.home.agilent.com/upload/cmc_upload/All/DC10_ID2696_Novak-Mori-Resso.pdf).

## RLC Models for Decoupling Capacitor

Decoupling capacitors are often characterized by vendors by means of three parameters: R (resistance), L (inductance), and C (capacitance). The C parameter is the decap's intrinsic capacitance; the L is its intrinsic inductance; and the R is the ESR of the decoupling capacitor. When this simple RLC model for a decoupling capacitor is utilized in a simulation along with a good PDN model, the mounting inductance and spreading inductance associated with the package or PCB combines with the decap's intrinsic inductance to effectively model the loop inductance. This loop inductance plus the package inductance resonates with the die capacitance to form a parallel anti-resonant circuit with a unique impedance profile.

Series RLC models of decoupling capacitors are easy to understand, and they simulate quickly as both frequency domain and transient simulations with a minimum of issues. As noted previously, the RLC values for the model can come from a vendor's data sheet; alternatively, they can be derived from measured s-parameter data by fitting the values of a simple series RLC circuit to the response of the s-parameters. In some cases, particularly at low frequencies, the simple series RLC circuit works adequately. However, when it is required to determine the impedance profile of a PDN accurately over a wide bandwidth of DC to several gigahertz, things usually do not work out so simply.

Two main issues make simple series RLC models inadequate for accurate PDN simulations. Due to the stacked layers of the decoupling capacitor construction, there is distributed inductance and resistance in the Z axis of the plate stack. This causes the L parameter of the series RLC representation to be frequency dependent. In most simulators, there is no frequency-dependent L element. First, a reasonably accurate series RLC model can be constructed at either low frequencies or high frequencies, but cannot model both simultaneously. Second, while a complex multi-element model can be constructed to more accurately model the frequency-dependent L effect, such models are very difficult to design and manage.

Therefore, rather than use a simple series RLC circuit that is known to be inaccurate over a wide bandwidth, or attempt to synthesize a more complex multi-element model, the simulation work done at Xilinx suggests that it is much easier and more accurate to utilize a measured wideband s-parameter decoupling capacitor model when simulating PDNs.

***Note:*** Ceramic decoupling capacitor models are strongly voltage dependent. Therefore, it is important to obtain the s-parameter model from the capacitor manufacturer that has been measured at the operating voltage of interest—for both DC and AC voltages.

# Running the PDN Simulations with the Agilent ADS 2011.10

To simulate the frequency domain self-impedance profile of a Power Distribution Network, Xilinx recommends using the **Agilent ADS 2011 software bundle**. This software bundle provides the high-speed-digital (HSD) designer with a wide range of tools. Every aspect of the power integrity problem requires a specific technique for solving it. For example, PDN analysis requires the following:

1. True frequency-domain simulation of the PDN parallel anti-resonances and series resonances with solid S-parameter handling and assurance of "Passivity and Causality"
2. Patented convolution (Kramers-Kronig) to bring frequency-domain models (measurement-based models and EM-based models) into the time domain (eye diagrams, BER contours, and jitter decomposition)
3. Using an extraction technique, such as Method-of-Moment, which has excellent accuracy from DC to GHz range

## PDN Simulation Example

In this simulation example, the simulation performed is the PDN of the MGTAVCC and MGTAVTT analog power rails for the Xilinx 7 series XC7VX485T FPGA in the FFG1761 pin package.

Two cases are simulated here. Case 1 uses the PCB capacitors listed in Table 2, which are similar to the recommended PCB caps for the Xilinx Virtex-6 devices.

*Table 2:* **Case 1 Capacitors**

| QTY per Group | | | Capacitance (µF) |
|---|---|---|---|
| MGTAVCC | MGTAVTT | MGTVCCAUX | |
| 4 | 4 | 2 | 0.022 |
| 4 | 4 | 0 | 0.47 |
| 2 | 2 | 1 | 1 |
| 2 | 2 | 1 | 4.7 |

Case 2 uses the PCB capacitors described in Table 3.

*Table 3:* **Case 2 Capacitors**

| QTY per Group | | | Capacitance (µF) |
|---|---|---|---|
| MGTAVCC | MGTAVTT | MGTVCCAUX | |
| 0 | 0 | 0 | 0.022 |
| 0 | 0 | 0 | 0.47 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 4.7 |

Figure 12 is the schematic for both cases (1) and (2) listed above for the MGTAVCC and MGTAVTT power rails. For case 2 (with no PCB capacitors), there is still one bulk capacitor mounted on the PCB specified by the manufacturer of the voltage regulator module.

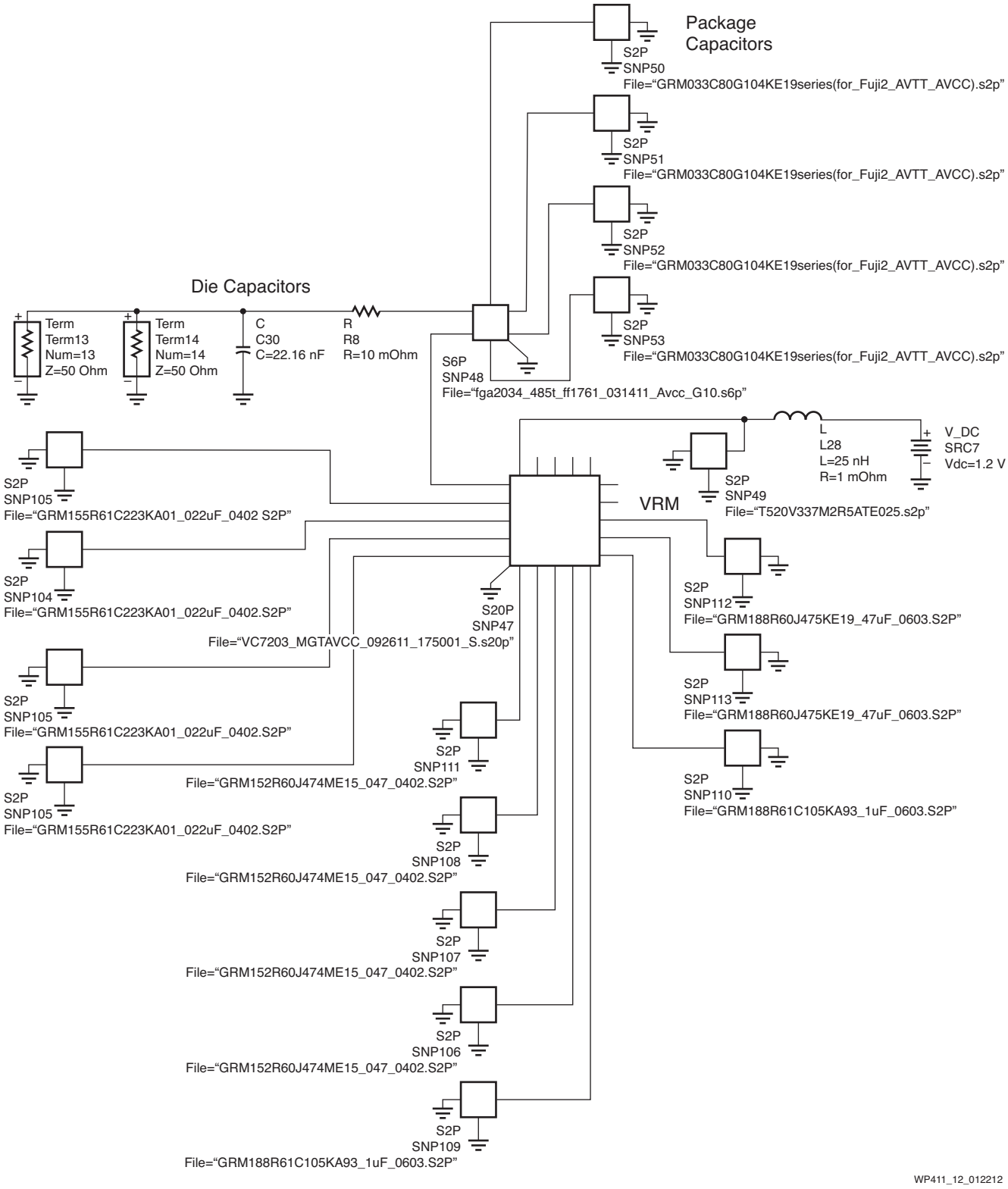


*Figure 12:* **Power Rails Simulation Schematic Representation**

Figure 13 show the simulations results.

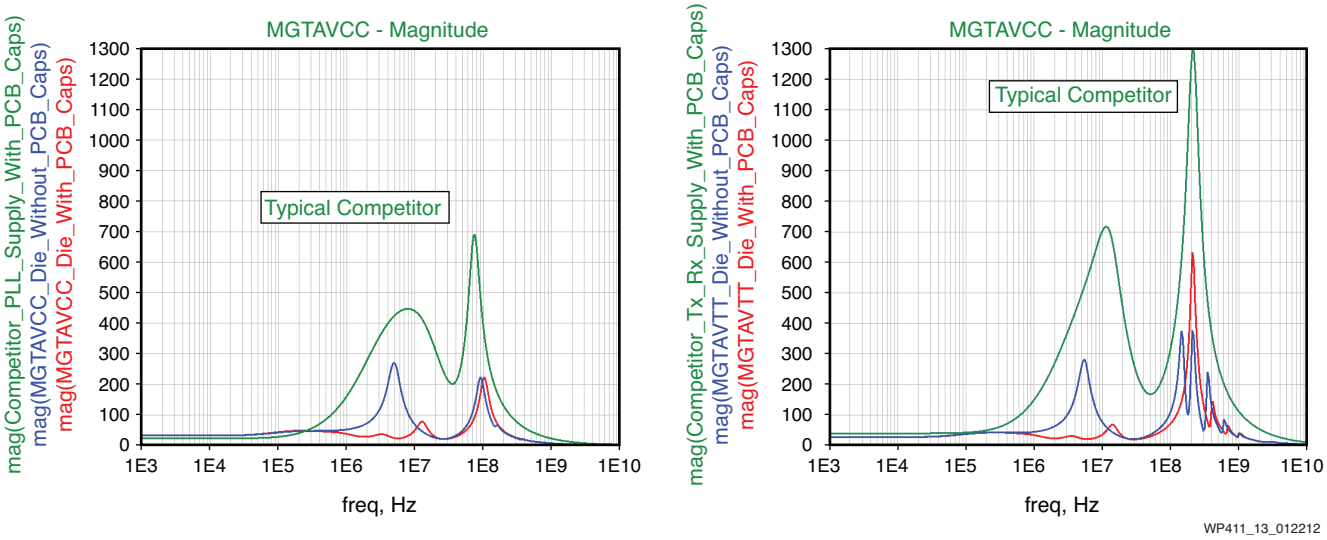


*Figure 13:* **Power Rails Simulation Results**

Figure 14 shows the complete simulation time using a typical laptop computer running the Windows-7 64-bit operating system is only 11.68 seconds!

```
hpeesofsim (*) 371.400 May 13 2011 (64-bit built: 05/25/11 12:47:43)
Copyright Agilent Technologies, 1989-2011.

SP SP1[1] <White_Paper_PI_lib:AVCC_and_AVTT:schematic>   freq=(1 kHz->10 GHz)
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''

Resource usage:
  Total stopwatch time     =    11.68 seconds.

-------------------------------------------------------------------------------
Simulation finished: dataset `AVCC_and_AVTT' written in:
  `C:\Agilent\Workspaces\White_Paper_PI/data'
-------------------------------------------------------------------------------
```

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*Figure 14:* **Complete Simulation Time, Windows-7 64-bit OS**

Because the simulation results for both cases result in almost identical frequency domain self-impedance profiles for the MGTAVCC and MGTAVTT power rails, and because the MGTVCCAUX power rail has an internal low drop out regulator integrated on the die, similar performance between the two cases should be expected. As a simple reference, the impedance profiles were simulated on a competitive device with 0 PCB capacitors beyond the 1 bulk PCB capacitor typically required by the voltage regulator manufacturer. Profiles representing the VCCH_GXBL0, VCCT_GXBL0, and VCCR_GXBL0 power rails were run.

As can easily be seen in the PDN profiles of a typical competitive device, the analog rails would have a peak impedance of well over 2Ωif the PCB caps were removed!

## Transmitter Hardware Measurements

Figure 15 through Figure 18 contain a series of eye diagrams at 10.3125 Gb/s using the QPLL and 6.25 Gb/s using the CPLL with PRBS15 data pattern measured on the Agilent Infiniium DCA-J Wide-Bandwidth Oscilloscope. This Agilent 86100C with the 86108A precision waveform analyzer has been selected to make these hardware measurements because of the following key attributes:

1. High bandwidth, low noise, and ultra-low residual jitter
2. Simple one connection "triggerless" operation
3. PLL characterization including loop BW/jitter transfer
4. Integrated hardware clock recover with adjustable loop BW/Peaking—exceeds industry standards

Figure 15 shows the eye diagram and associated jitter decomposition when using the CPLL running at 6.25 Gb/s for case 1.

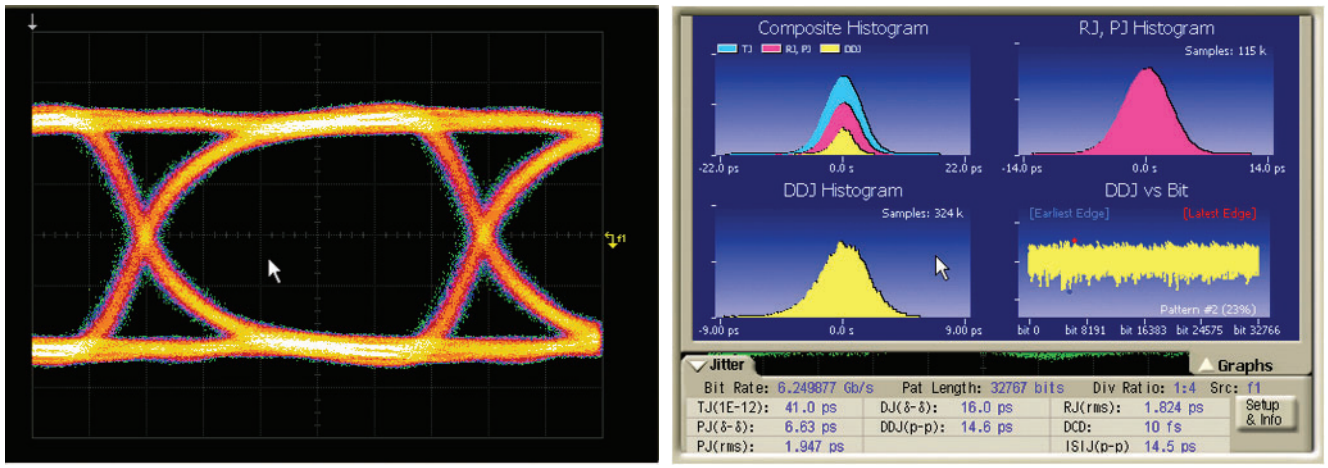


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*Figure 15:* **Case 1 Eye Diagram, 6.25 Gb/s**

Figure 16 shows the eye diagram and associated jitter decomposition when using the CPLL running at 6.25 Gb/s for case 2 (no PCB caps).

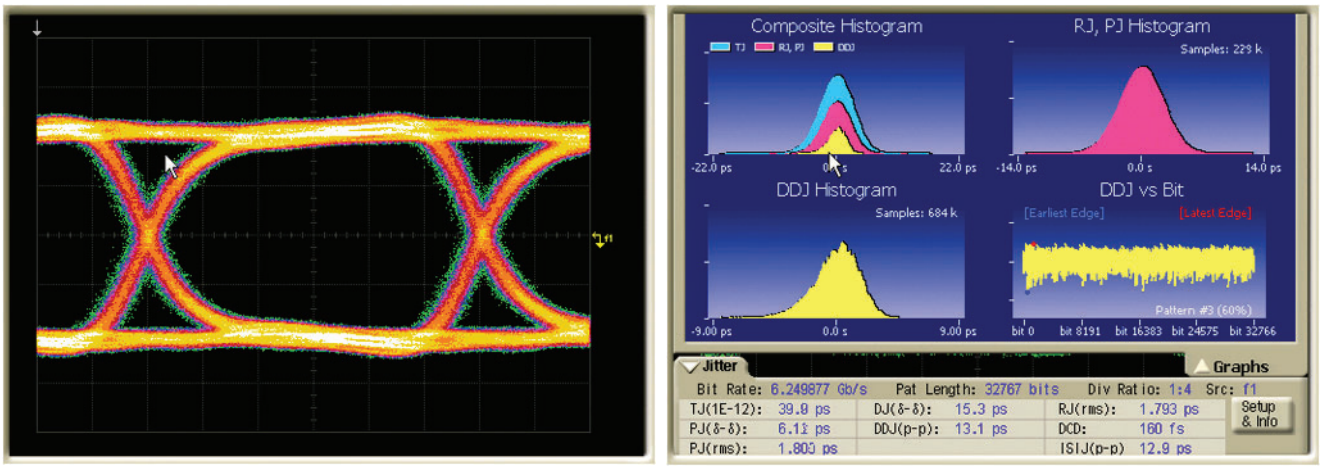


*Figure 16:* **Case 2 Eye Diagram, 6.25 Gb/s**

Figure 17 shows the eye diagram and associated jitter decomposition when using the QPLL running at 10.3125 Gb/s for case 1.

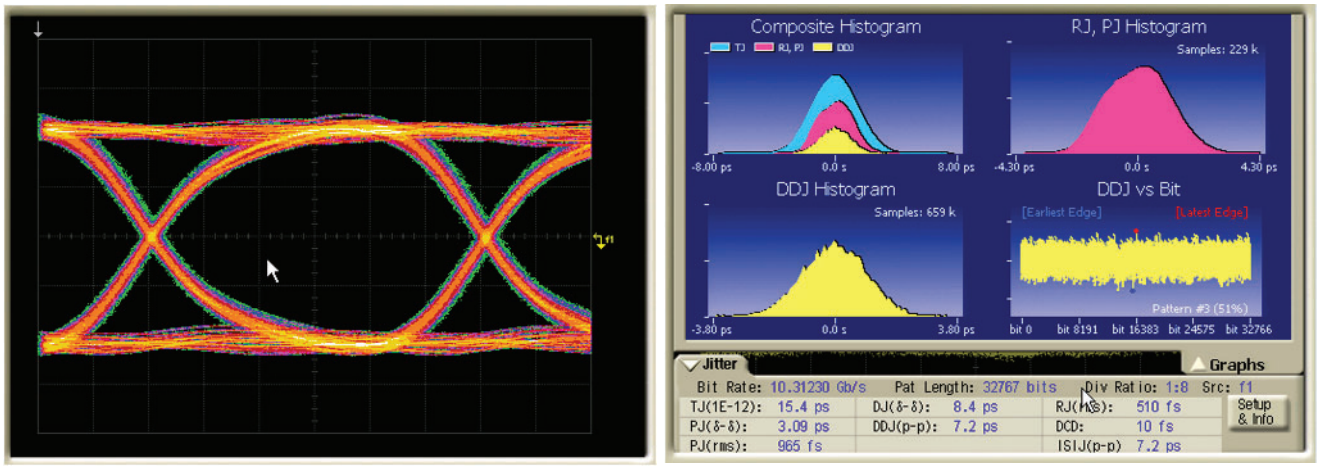


*Figure 17:* **Case 1 Eye Diagram, 10.3125 Gb/s**

Figure 18 shows the eye diagram and associated jitter decomposition when using the QPLL running at 10.3125 Gb/s for case 2 (no PCB caps).

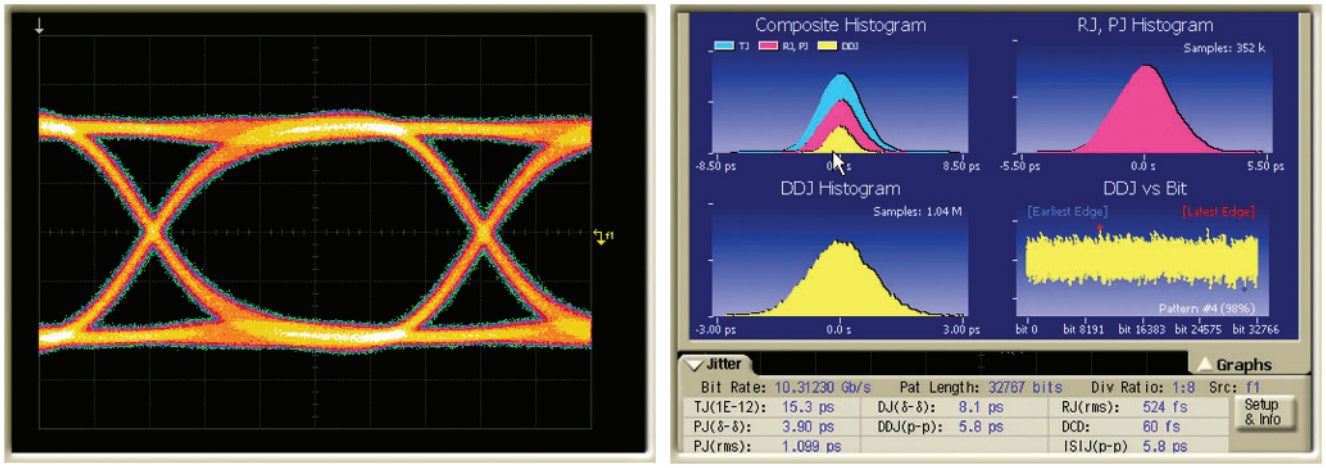


*Figure 18:* **Case 2 Eye Diagram, 10.3125 Gb/s**

As seen in the scope screenshots in Figure 15 through Figure 18, the total jitter is both cases 1 and 2 is within the measurement tolerance of the setup. Thus, hardware measurements have confirmed the simulation results showing that 0 PCB caps are required for proper operation of the transmitter.

## Receiver Measurements

Table 4 is a summary of the receiver hardware measurements based on a loopback test using eyescan. The data recorded in Table 4 is the voltage amplitude noise with all transceivers in the package running asynchronously. As shown by the data, the voltage amplitude noise is the same or less after all the PCB caps have been removed when using either the CPLL or the QPLL.

*Table 4:* **Comparison of Voltage Amplitude Noise with/without Decoupling Caps**

| PLL | CPLL | | QPLL | |
|---|---|---|---|---|
| Bit Rate | 6.25 Gb/s | | 10.3125 Gb/s | |
| MGTAVCC | All Caps | No Caps | All Caps | No Caps |
| MGTAVTT | All Caps | No Caps | All Caps | No Caps |
| MGTVCCAUX | All Caps | No Caps | All Caps | No Caps |
| **% Full Scale** | **3.6%** | **3.3%** | **5.0%** | **4.5%** |

Figure 19 is a summary of the receiver's jitter tolerance analysis with all transceivers in the package running asynchronously for both cases 1 and 2.

As shown by the data, the jitter tolerance is the same or less after all the PCB caps have been removed. The jitter tolerance analysis was done at $10^{-12}$ BER threshold and a data rate of 10.3125 Gb/s.

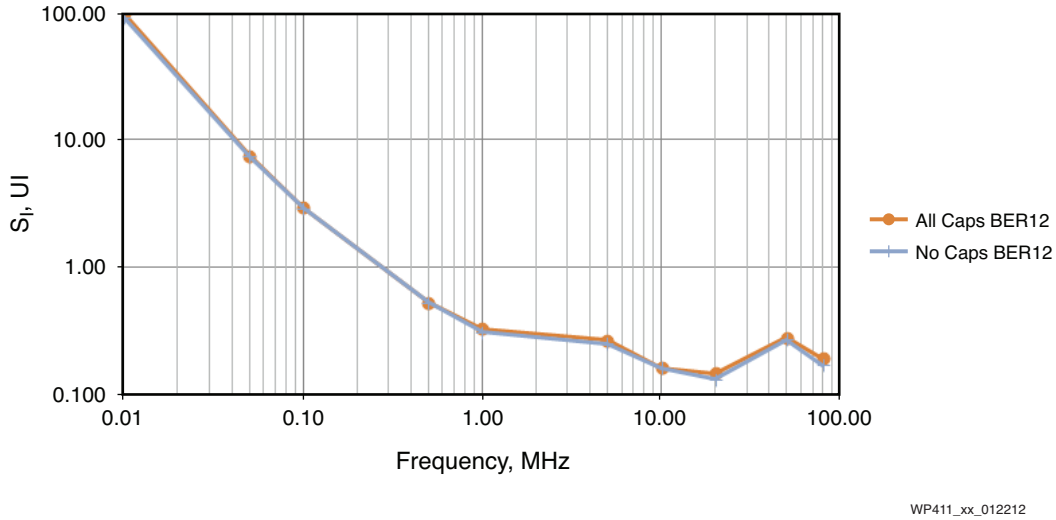


*Figure 19:* **Comparison of Jitter Tolerance with/without Decoupling Caps**

# Summary

PDN simulations, confirmed by hardware measurements, have shown that no PCB caps beyond that recommended by the voltage regulator manufacturer are required for the MGTAVTT, MGTAVCC, and MGTVCCAUX power rails for proper operation of the transceivers in Xilinx's Kintex-7 and Virtex-7 devices.

While the PCB capacitors are not needed for proper operation of the transceivers, however, proper filtering can be required on the PCB to achieve the input voltage ripple noise specification of 10 mV peak-to-peak (10 kHz to 80 MHz) when measured at the BGA ball of the package.

Currently, Xilinx has several Agilent ADS Power Integrity Design Kits available for 7 series FPGAs that support all device power supplies (digital and analog). Contact your local Xilinx field application engineer to obtain these Agilent ADS Design Kits.

To obtain a 30-day free license of Agilent ADS2011, please visit the following link:

https://software.business.agilent.com/TrialLicense/TrialLicenseRequest.aspx?ProdNum=W2200F-1U1-TRL

# Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 01/30/12 | 1.0 | Initial Xilinx release. |

# Notice of Disclaimer