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Accelerating Design Productivity with 7 Series FPGAs and DSP Platforms

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Designers tasked with delivering more capability and performance in today's sophisticated DSP applications are increasingly turning to programmable logic for their hardware solutions. Xilinx® 7 series FPGAs meet this demand with a family of devices uniquely developed to address specific market needs, such as highest performance, lowest cost, or lowest power. Xilinx 7 series DSP Targeted Design Platforms accelerate development of DSP applications by reducing schedule risk, enabling design reuse, and introducing new high-level design methodologies.

7 Series FPGAs for DSP

With 7 series FPGAs, Xilinx introduced a new high-k metal gate (HKMG), high-performance, low-power (HPL) variant of 28 nm process technology. The resulting Artix™-7, Kintex™-7, and Virtex®-7 FPGAs allow designers to achieve both low power consumption and high DSP performance without compromise (Figure 1). The 7 series devices are built around a scalable, optimized structural concept that eliminates architectural differences between device families. This makes it easy to target designs towards the 7 series device that most perfectly meets the designer's requirements.
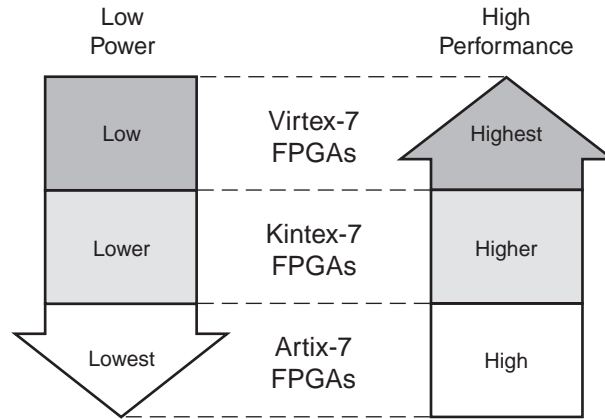
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Figure 1: **7 Series FPGAs Optimized, Scalable Architecture**

Fourth Generation DSP48E1 Slice

High DSP performance in the 7 series FPGAs is achieved through the capabilities of the DSP48E1 slice, the fourth generation of this innovative embedded block in 7 series FPGAs. The DSP48E1 slice provides designers with dynamic control input signals that can select different arithmetic operations on a clock-by-clock basis. The slice is implemented in fully customized silicon, and as a result, delivers superior power and performance.The structural elements of the slices and tile are illustrated in Figure 2.
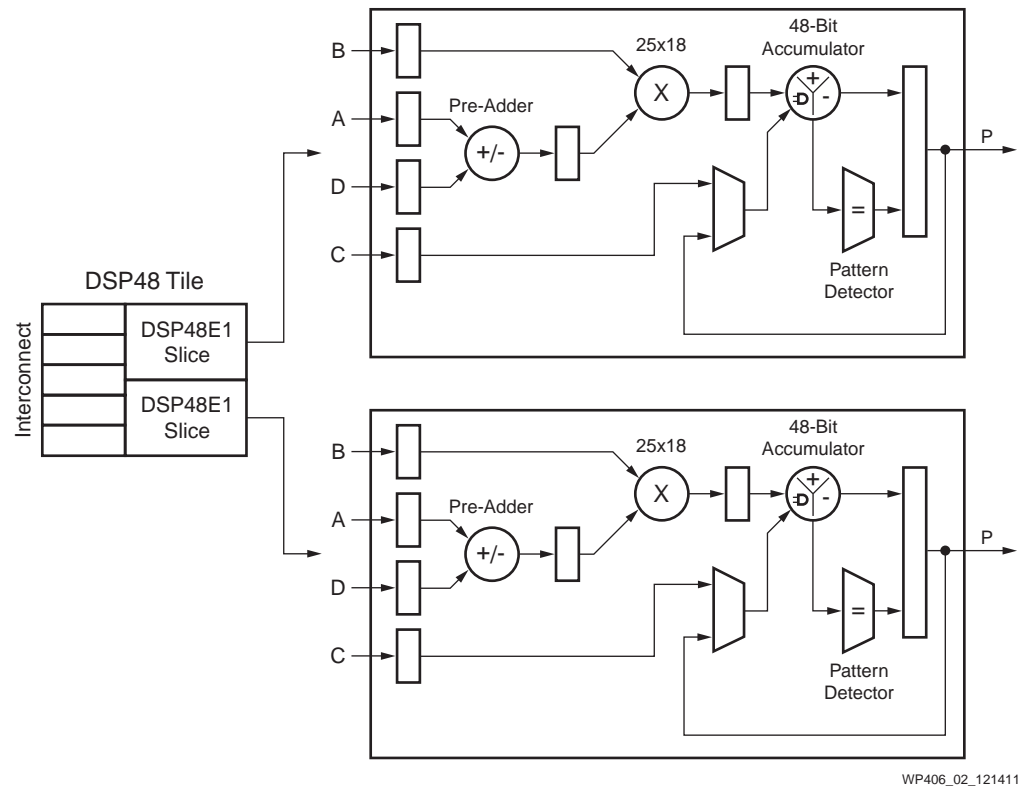
*Figure 2:* **DSP48E1 Tile (Two DSP48E1 Slices and Interconnects)**

Five high-speed interconnects are used to combine two DSP48E1 slices into a single DSP48E1 tile that can be used to implement a variety of arithmetic operations of variable precision with no loss of F_{MAX} performance.

This enables high-resolution applications such as radar, medical imaging, and wireless to take full advantage of the 7 series FPGAs' industry-leading 28 nm DSP performances.

The Independent Multiplier and Accumulator Access section compares the capabilities of the 7 series DSP48E1 tile to the Altera Stratix V DSP block for a variety of arithmetic operations commonly used in DSP algorithms.

Independent Multiplier and Accumulator Access

The DSP48E1 slice allows for greater flexibility by providing independent access to each multiplier and accumulator compared to the Altera Stratix V DSP block that limits access to one. See Figure 3.
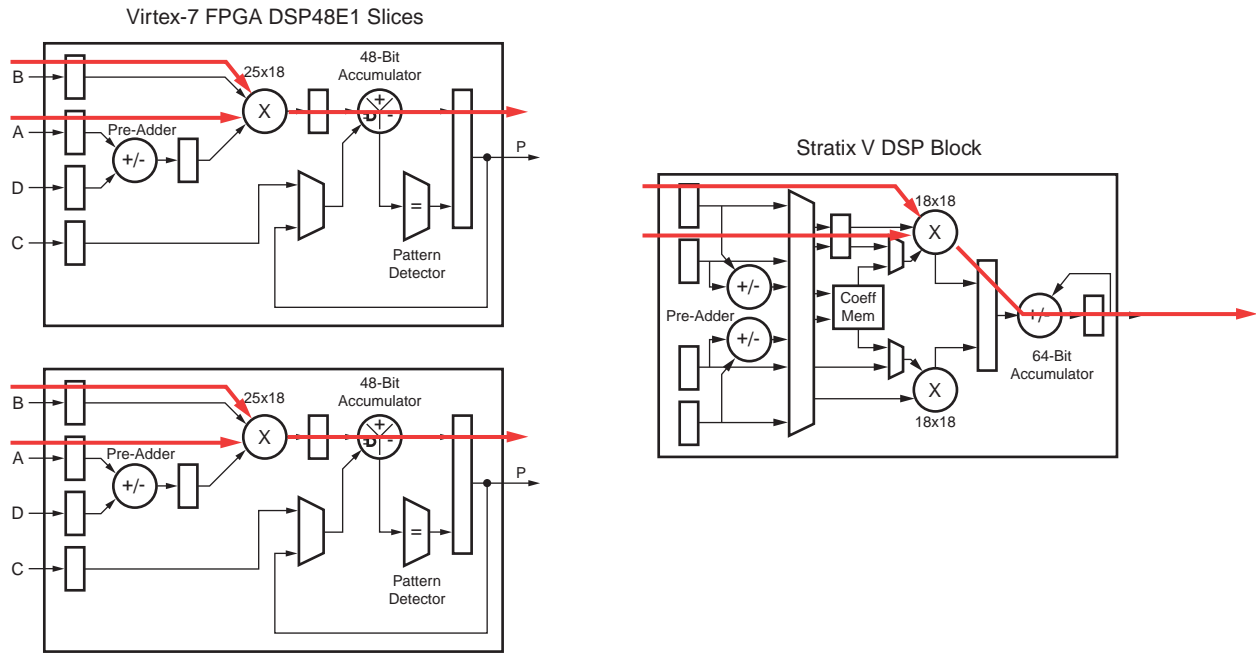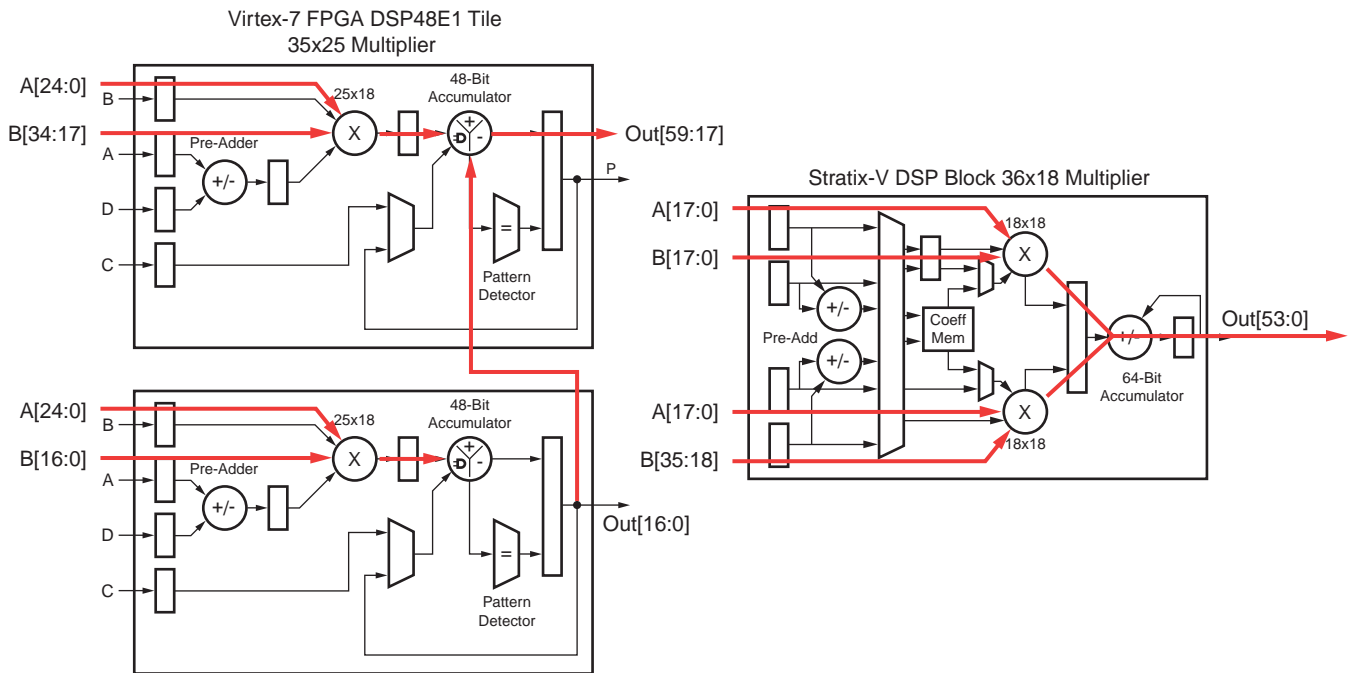
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Figure 3: **Independent Multipliers in the DSP48E1 Tile**

Support for Wider Multiply Operations

Each multiplier in the DSP48E1 slice supports up to 18x25 bits that allow the DSP48E1 tile to implement wider multiply operations up to 35x24 with pre-add and 35x26 without pre-add. See Figure 4 and Table 1.

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Figure 4: **Wide Multiplier Comparison**

Table 1: **DSP Resource Comparison for Wide Multipliers**

Configuration	Xilinx DSP48E1 Tile	Altera Stratix V DSP Block
Independent Multipliers	Two 25x18 with full 43-bit resolution	Two 18x18 with limited 32-bit resolution
With Pre-add	35x24	26x22
Without Pre-add	35x25 or 42x18	27x27 or 36x18
Without Pre-add (Cport ext)	35x26 or 42x19	N/A

Symmetric Filter Coefficients Not Limited to 8 Values

The DSP48E1 slice provide complete flexibility to support coefficients of any length using the input ports for each accumulator. See Figure 5.
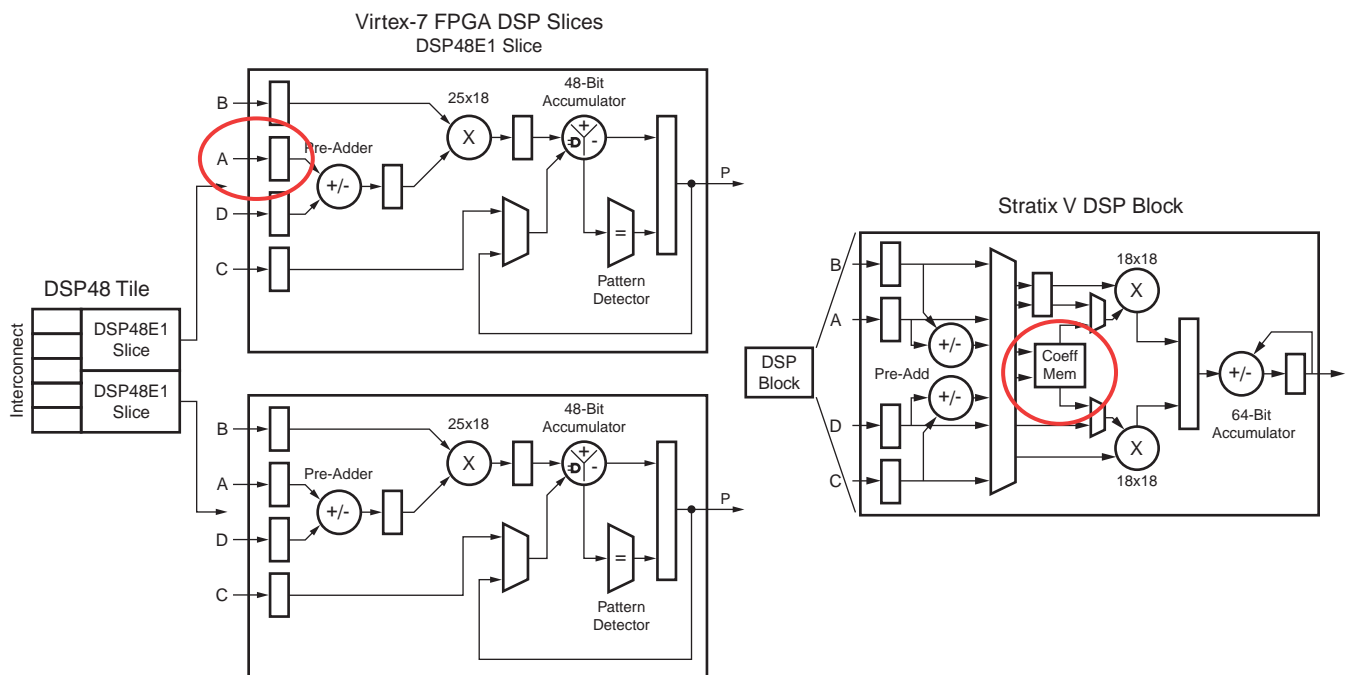

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Figure 5: **Support for Filter Coefficients**

ALU Block for Efficient Rounding

Each DSP48E1 slice supports advanced functions, such as an ALU and pattern detection block, which allow more efficient hardware implementations for common rounding modes, including convergent, symmetric, and random rounding. See Figure 6.
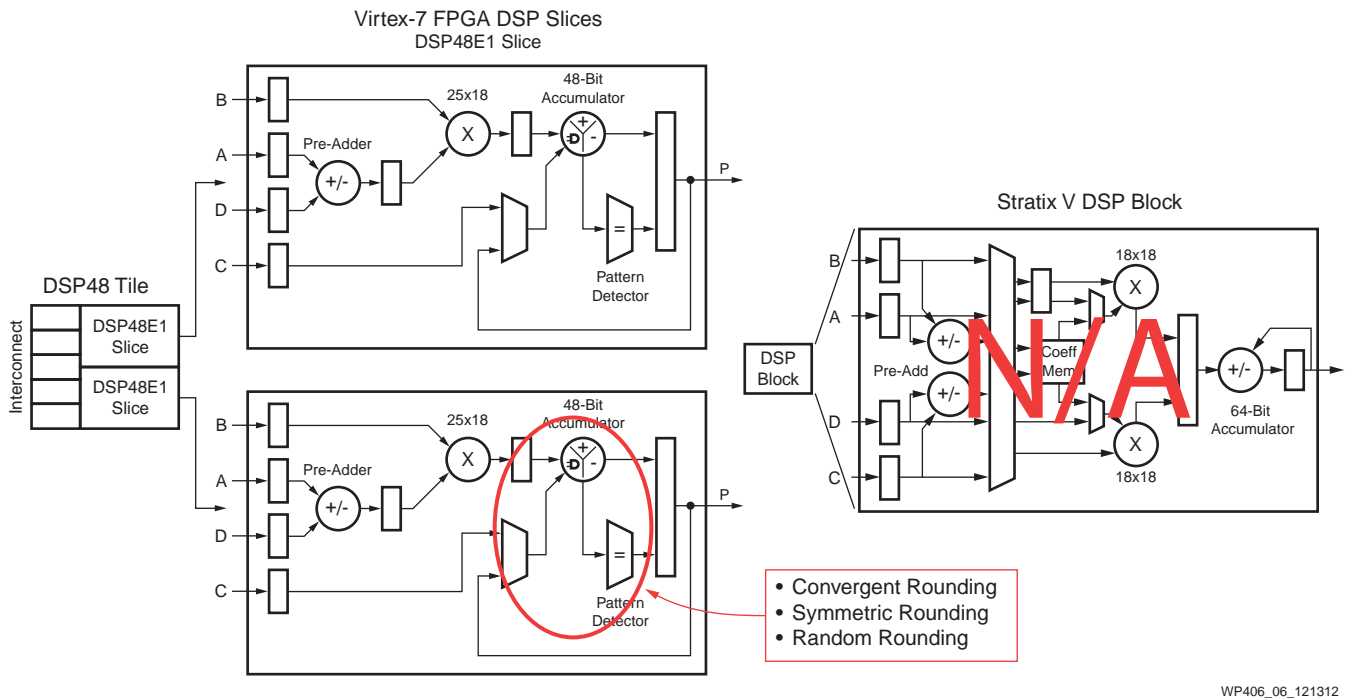
Figure 6: **Hardware Support for Fixed-Point Rounding**

Larger, More Flexible Accumulators

The DSP48E1 tile offers the flexibility to use two 48-bit accumulators independently or to combine them into a single 96-bit accumulator. See Figure 7. See Table 2.
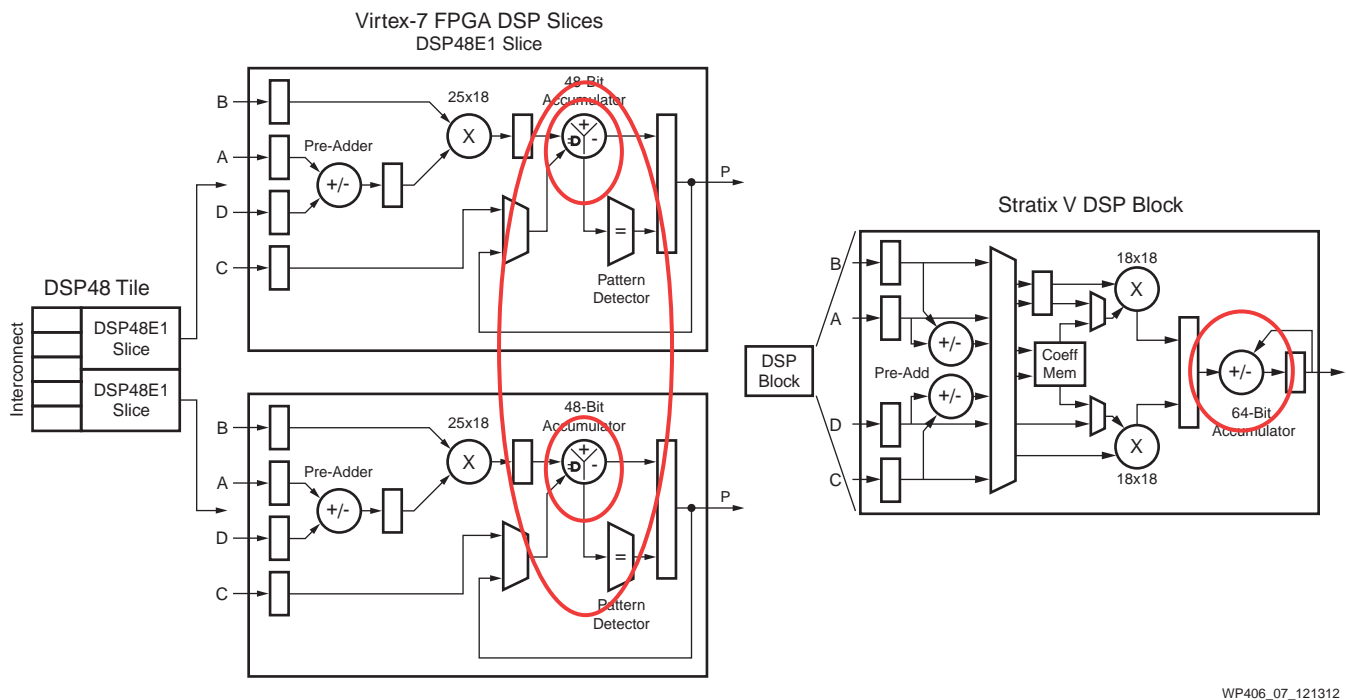

Figure 7: **Wide Accumulator Comparison**

Table 2: **DSP Resource Comparison for Wide Accumulators**

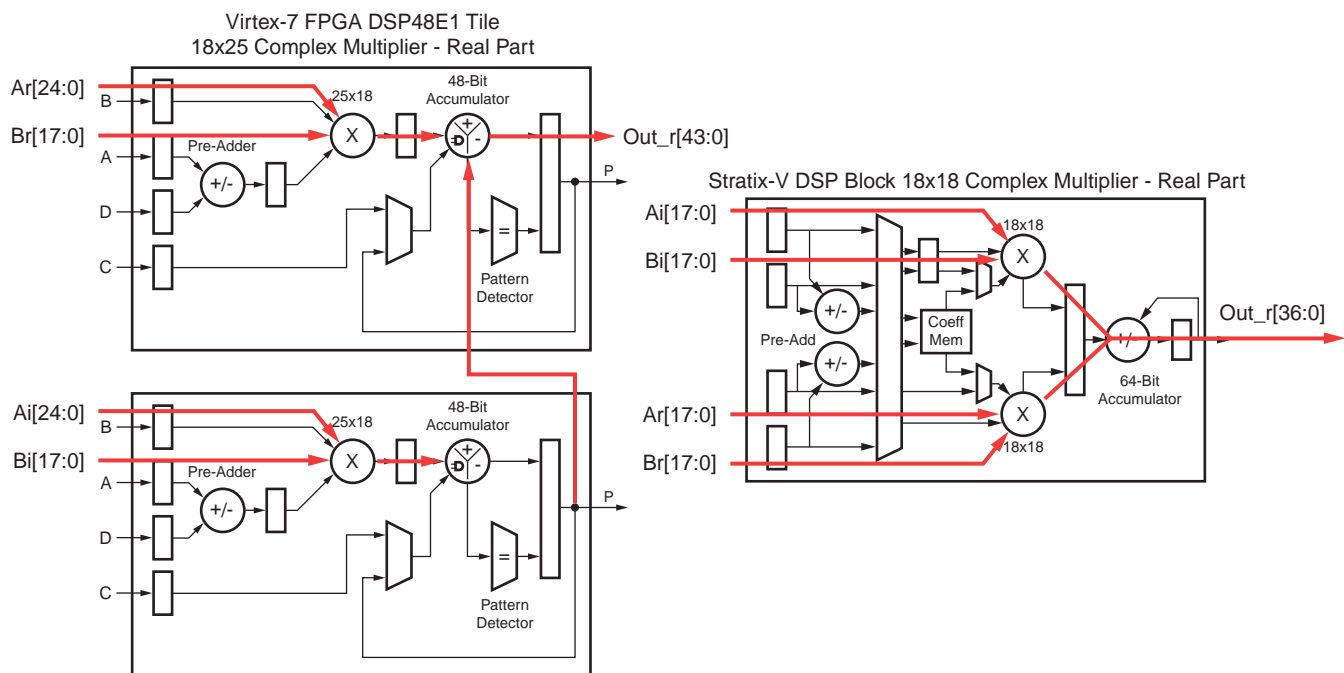| Configuration	Xilinx	Altera
One Accumulator	96-bit	64-bit
Two Accumulators	48-bits	N/A

More Efficient Complex Multiply Implementations

The DSP48E1 tile can be configured to implement two 25x18 multiply-add operations that can be used to build complex multipliers with 30% less logic:

out_r = (ar*br) - (ai*bi)

out_i = (ar*bi) + (ai*br)

See Figure 8.

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Figure 8: **Comparison of Complex Multiply Real Output**

Note: Figures only show configuration for the real output of the complex multiply.

Table 3 compares the DSP hardware resources for wide complex multiply operations commonly used in wireless and A&D applications

Table 3: **Wide Complex Multiply Operations**

Operation	Xilinx	Altera
18x18 complex multiplier	3 DSP48 slices (1.5 DSP tiles)	2 DSP blocks
18x25 complex multiplier	2 DSP48 tiles	3 DSP blocks
18x25 complex multiplier F_{MAX}	741 MHz	400 MHz

Virtex-7 FPGAs: Highest Performance in a Programmable Device

Virtex-7 FPGAs address a need for a hardware solution in applications that require the highest levels of DSP performance. Virtex-7 FPGAs include up to 3,600 DSP48E1 slices, capable of clocking at over 741 MHz, that combine to deliver over 5,000 GMAC/s of peak DSP performance, satisfying even the most demanding applications, as illustrated in Figure 9.
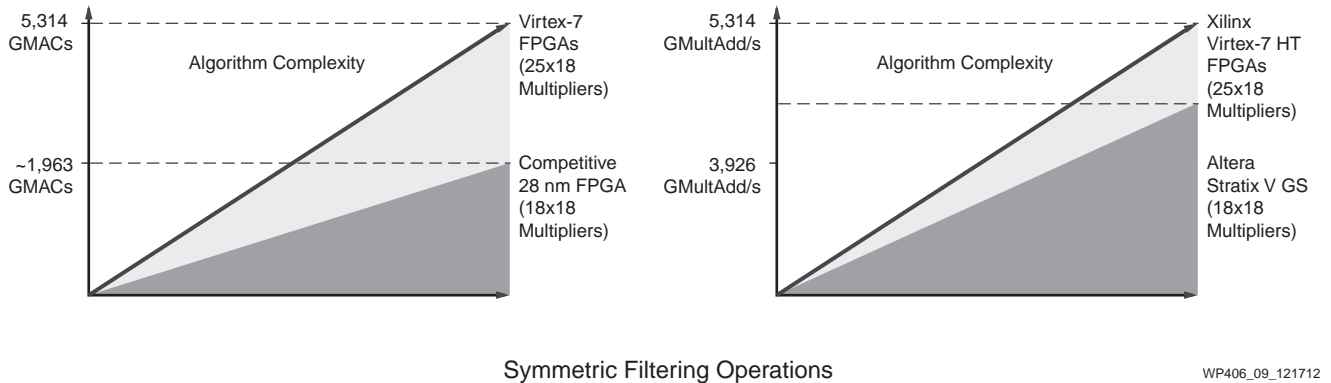

Figure 9: **High-End FPGA DSP Performance**

Virtex-7 FPGAs deliver over 2X the peak DSP processing bandwidth of other leading 28 nm alternatives for symmetric filtering operations typical of wireless, radar, and medical applications.

Kintex-7 FPGAs: Highest DSP Performance per Dollar

The Kintex-7 FPGA shares the same high-performance silicon process and DSP48E1 slice as the Virtex-7 FPGA, but the amounts and ratios of these resources have been optimized to lower costs for high-volume applications. These applications include wireless infrastructure, broadcast, and medical, which previously required a high-performance class device; they can now use the Kintex-7 FPGA to reduce cost and power by half. In fact, Kintex-7 devices offer over twice the DSP processing bandwidth of competing mid-range 28 nm programmable devices, as shown in Figure 10.
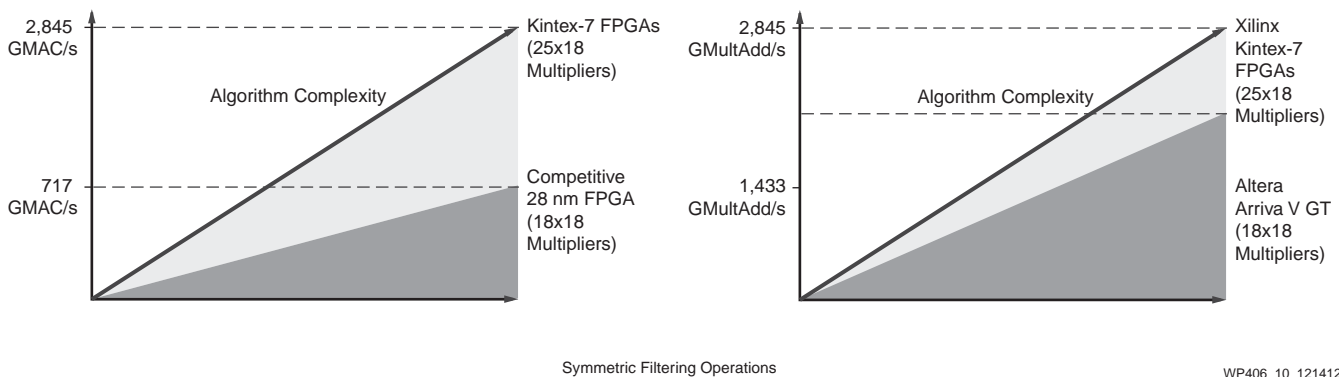

Figure 10: **High-Volume FPGA DSP Performance**

Artix-7 FPGAs: Highest DSP Performance per Watt in a High-Volume Device

The Artix-7 device offers the lowest power and lowest cost in an FPGA, addressing the high-volume market. The Artix-7 device shares a scalable, optimized architecture with Kintex-7 and Virtex-7 FPGAs, including the DSP48E1 slice, but the Artix-7 FPGA silicon processes have been further optimized for maximum power efficiency. The 50% power reduction achieved by 7 series FPGAs is the cumulative effect of multiple power optimizations, including an advanced, low-power (HPL) HKMG process that delivers a 65% reduction in static power. Additional architectural and process improvements have lowered dynamic power in the Artix-7 device by 25%, while I/O power has been reduced by 30%. See Figure 11.
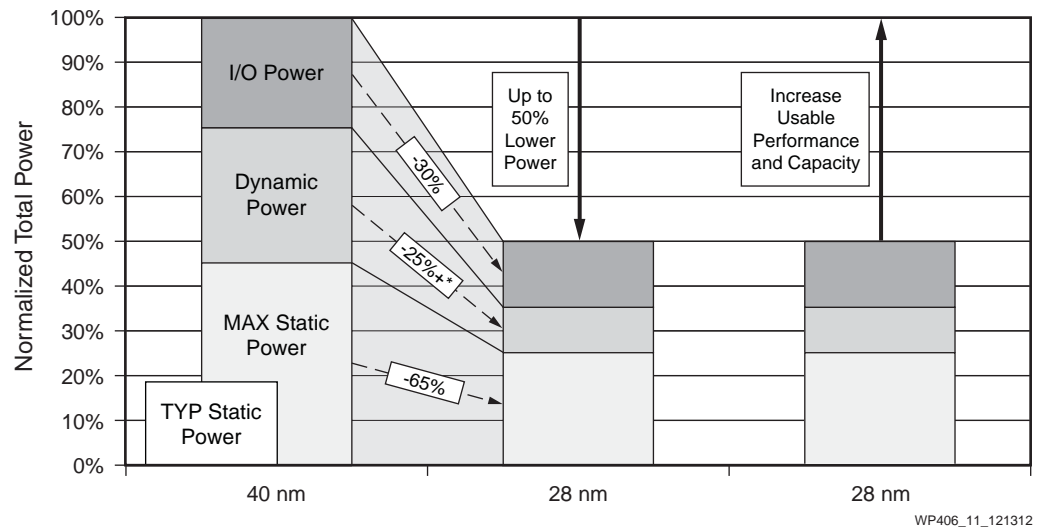

Figure 11: **7 Series Power Reduction**

Power-sensitive, high-volume applications can be implemented on Artix-7 devices with over 3X the DSP processing bandwidth and up to 87% less power than competitive devices, enabling more DSP processing bandwidth per clock and per watt.

Additionally, Artix-7 FPGAs offer up to a 5X performance-per-watt advantage compared to multi-core DSPs. For example, a TI TMC320C6678 multi-core DSP consumes an estimated 12.3 watts to deliver a peak DSP performance of 320 GMAC/s, which normalizes to 26 GMAC/s per watt. The Artix-7 FPGA can deliver up to 140 GMAC/s per watt, making it the ideal device for applications that demand both high performance and low power. Refer to Figure 12.
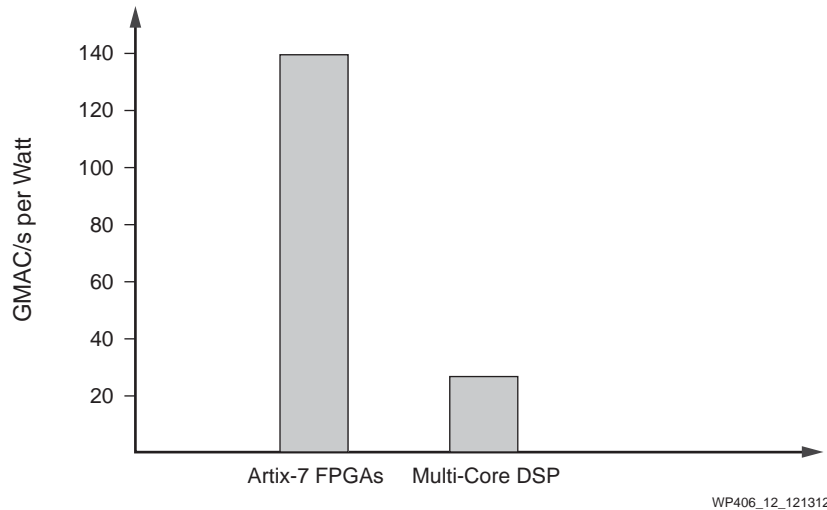
Figure 12: **DSP Performance per Watt**

When compared against competing 28 nm high-volume devices, the Artix-7 family offers over a 3X performance advantage, delivering up to 929 GMAC/s of DSP processing bandwidth for symmetric filters, as shown in Figure 13.

Artix-7 FPGAs offer both performance and flexibility advantages over off-the-shelf ASSP solutions and over 2X the performance of competitive devices.
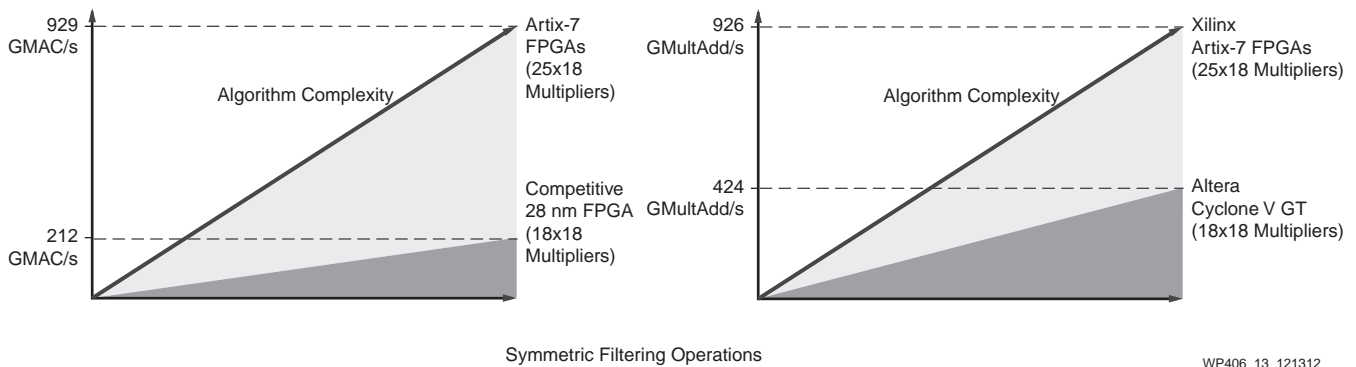
Figure 13: **Low Power, High Volume DSP Performance**

Accelerate Development with DSP Targeted Design Platforms

Designers with a variety of technical backgrounds can use the leading DSP Targeted Design Platforms from Xilinx (see Figure 14) to evaluate the benefits of 7 series FPGAs in their designs. Targeted Design Platforms provide development hardware, FPGA Mezzanine Card (FMC) I/O daughter cards, reference designs, IP and domain-specific design methodologies, and tools that reduce schedule risk and accelerate development of new designs.
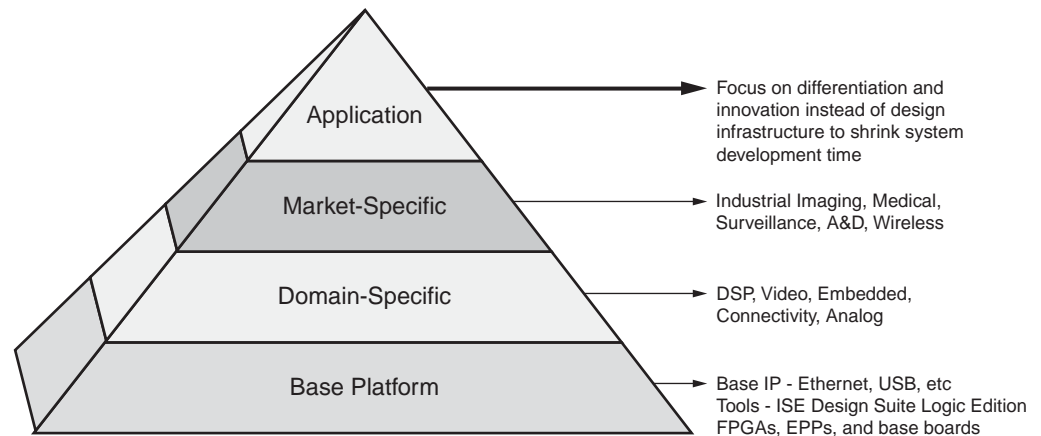
Figure 14: **Xilinx Targeted Design Platforms**

The Kintex-7 FPGA DSP Kit is the first DSP domain platform available from Xilinx for DSP development in 7 series devices. Technical highlights of this kit include:

- Kintex-7 FPGA KC705 Evaluation Kit equipped with the Kintex-7 XC7K325T device, featuring 840 DSP48E1 slices that can deliver up to 1,245 GMAC/s of DSP processing bandwidth
- 4DSP FMC150 ADC/DAC high-speed FMC mezzanine card that includes:
  - Dual-channel 16-bit 800 MSPS DAC
  - Dual-channel 14-bit 250 MSPS ADC data converters
  - Clock generation/clock conditioning
- ISE® Design Suite: System Edition/Vivado™ Design Suite — Targeted to the KC705 board
  - Includes System Generator for DSP
- DSP "Getting Started" Reference Design with digital up/down conversion and high-speed analog interface logic
- RTL DSP design tutorial
- Model-based design tutorial with MATLAB® and Simulink® software

Additional RF and High-Speed analog cards are available from the Xilinx FMC ecosystem.

Reduce Schedule Risk with Proven DSP Targeted Reference Designs

Xilinx DSP Development kits serve as a validation platform for DSP development that reduces schedule risk. Prior to release, each reference design shipped with the kits is thoroughly tested for functional correctness, design efficiency, timing closure, and high quality of results.

The digital signal processing logic and high-speed analog interfaces are designed to fully leverage the performance of the FPGA, including the DSP48E1 slice and the I/O. These reference designs are provided as precompiled bitstreams that can be directly downloaded onto the FPGA and executed in hardware. The reference designs reduce schedule risk by validating working devices at full performance. After silicon has been validated, step-by-step design tutorials are provided that take users through the process of regenerating IP cores and recompiling design source files through the ISE Design Suite tool to generate new programming files. Validating working silicon,

working IP, and working tool flows ensures that time-critical projects start with confidence.

The DSP reference design fully leverages the performance capability of the Kintex-7 FPGA. The programmable logic used to implement the DUC/DDC functionality is overclocked at 491.52 MHz to allow resource sharing of the DSP48E1 slices. The DUC output sampling rate supports 245.76 MSPS with a 2X interpolation through the ISERDES to achieve a final DAC output sampling rate of 491.52 MSPS. The ISERDES ADC data capture is configured to support either a single stream of 245.76 MSPS (per ADC channel) or a dual stream, where each stream is decimated by 2X at 122.88 MSPS.

An example of an initial design is shown in Figure 15.
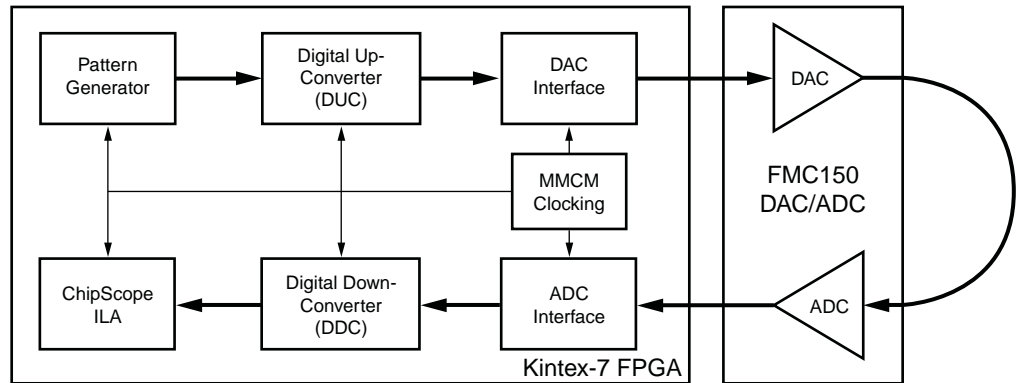
Figure 15: **Kintex-7 FPGA DSP Kit Targeted Reference Design Block Diagram**

DSP Targeted Reference Designs are fully supported designs that are updated for each design tool release. Portions of these designs are often reusable in end-user designs, saving weeks or even months of design effort recreating non-proprietary design infrastructure. For example, the targeted reference design for the Kintex-7 FPGA DSP Kit includes signal generation, digital up/down conversion blocks, and interface blocks to the high-speed data converters.
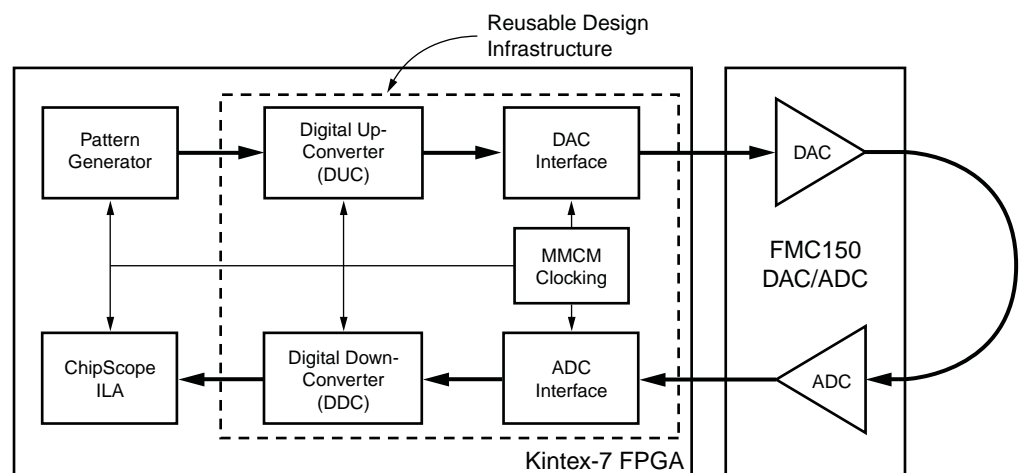
Figure 16: **Kintex-7 FPGA DSP Kit Design Reuse**

Extend DSP Platform Capabilities through the FMC Ecosystem

Developed by a consortium of companies ranging from FPGA vendors to end users, the FPGA Mezzanine Card (FMC) is compliant to an ANSI standard that provides a standard form factor, connectors, and modular interface to an FPGA located on a base board. Decoupling the I/O interfaces from the FPGA simplifies I/O interface module design while maximizing carrier card reuse. See Figure 17. Today, roughly 30 FMC high-speed analog FMC daughter cards are available through Xilinx ecosystem partners.

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Figure 17: **FMC Mezzanine Cards for Xilinx Development Boards**

Key Benefits of FMCs:

- **Data throughput:** Support of individual signaling speeds up to 10 Gb/s, with potential overall bandwidth of 40 Gb/s between mezzanine and carrier card
- **Latency:** Elimination of protocol overhead removes latency and ensures deterministic data delivery
- **Design simplicity:** Expertise in protocol standards such as PCI™, PCI Express®, or Serial RapidIO not required
- **System overhead:** Power consumption, IP core costs, engineering time, and material costs reduced through simplification of system design
- **Design reuse:** Whether using a custom in-house board design or a commercial off-the-shelf (COTS) mezzanine or carrier card, the FMC standard promotes the ability to retarget existing FPGA/carrier card designs to a new I/O. All that is required is swapping out the FMC module and slightly adjusting the FPGA design.

Over 30 high-speed analog FMC cards are currently available through the FMC ecosystem. A complete list of can be found at: www.xilinx.com/fmc.

Summary

Xilinx DSP design platforms reduce schedule risk and accelerate productivity for any new DSP design that targets FPGAs. Xilinx 7 series FPGAs deliver high levels of DSP performance at half the cost and power compared to previous generation devices. The device family shares an optimized, scalable silicon architecture that enables designs to migrate across device families, and thus to highlight the device that offers the best combination of performance, cost, and power.

As more designers turn to programmable logic to solve their design challenges, an amazing synergy is taking place. Designers are discovering that these many evolving technologies support and facilitate each other:

- Greater confidence in the working silicon
- Greater confidence in the design tools
- Easier design reuse
- Increased design efficiency
- Easier-to-use high-level design flows

All these advances, working together, enable more designers and product managers to get better products to market in record time.

For more information, go to http://www.xilinx.com/innovation/7-series-fpgas.htm.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/17/12	1.0	Initial Xilinx release.
02/22/13	1.1	Updated Support for Wider Multiply Operations, Table 1, Figure 4, Figure 8, and Table 3.

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