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Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits

Hardness to atmospheric neutrons continues to improve as process architectures as small as 16nm have come online. Longer beam test times have therefore been implemented.

ABSTRACT

The September 2005 issue of **IEEE Transactions on Device and Materials Reliability** featured an article entitled "The Rosetta Experiment: Atmospheric Soft Error Rate Testing in Differing Technology FPGAs" [Ref 1]. The article described real-time experiments that evaluated large Xilinx® FPGAs for their sensitivity to radiation-induced single event upsets (SEUs).

This white paper clarifies some open issues from the original Xilinx Rosetta experiments conducted in 2005.

The devices under test represent several CMOS technologies, from 150nm, current at the time of this white paper's original publication (v1.0), to 16nm, current at the time of publication of this revision (v2.0). Detailed experimental results derived from simulation, beam testing, and atmospheric testing are presented.

Introduction

The Stone of Rosette by Ulrich Schade and Richard Wäsch [Ref 2] defines Rosetta as follows:

> *Rosetta refers to the crucial breakthrough in the research regarding Egyptian hieroglyphs. It especially represents the "translation" of "silent" symbols into a living language, which is necessary in order to make the whole content of information of these symbols accessible.*"

Just as the Rosetta Stone enabled researchers to decode the unsolvable and mysterious Egyptian hieroglyphs by comparing them to the same text written in a known language, the Xilinx Rosetta experiments link two prior known and well-documented techniques of estimating atmospheric neutron single event upsets (SEUs) with the real effects of atmospheric neutrons on integrated circuits. The known techniques are accelerated testing in a neutron or proton beam and software simulation of the circuit to determine the critical charge a particular node or latch can handle before it changes state. These Xilinx experiments determine the actual upset rate of Xilinx FPGAs due to an atmospheric neutron cascade, which resulted from a cosmic ray. With a good understanding of the real effect(s) that these atmospheric neutrons have on today's integrated circuits, Xilinx can validate the design and technology choices being used to mitigate these effects.

Predicting atmospheric neutron flux is not an exact science. In the JEDEC89A standard, there is a methodology that uses models and magnetic latitude data to predict the flux at any given location on the earth. The 2005 Rosetta results clearly did not agree with the original JEDEC89 standard, and the committee worked in collaboration with Xilinx to resolve this issue. Three corrections were made to the JEDEC89A standard:

- Realization that the proton flux is not insubstantial (it is approximately an additional 7% in San Jose and as much as an additional 32% at Mauna Kea).
- The attenuation by the building must be more accurately calculated (28% of the flux is lost to the ground floor of a typical Silicon Valley, two-story, tilt-up, concrete structure).
- A more automated model can be developed to aid investigators (a new prototype web-based tool): http://www.seutest.com/cgi-bin/FluxCalculator.cgi.

The JEDEC89A revision also proposes a new atmospheric spectral model, based on work done by Goldhagen, et al. [Ref 3].

Thermal neutrons were not considered at the time to have sufficient energy to upset devices. Since the 28nm technology node, thermal neutrons are now considered, because they do contribute to the overall upset rate.

Alpha particles (contamination) to fabrication and packaging have led to ultra-low alpha manufacturing processes utilized by Xilinx, and verified by below-ground (shielded) testing.

Experiments

Each Rosetta experiment consisted of multiple sets of 100 of the largest available Xilinx FPGAs using differing technologies, located at different altitudes. All tested components were fabricated by Xilinx foundry partners, using their planar or FinFET technologies.

Table 1 lists the locations of the experiments, and Table 2 and Table 3 list the device type, technology, and quantity.

Table 1: **Locations of Xilinx Rosetta Experiments**

Location	Altitude (Feet)	Adjusted Altitude Factor(1)
Lead, SD	–5800 See note (2)	0.00
Rustrel, France	–1600 See note (2)	0.00
San Jose, CA	257	0.75
Marseilles, France	359	1.08
Longmont, CO	4958	4.11
Albuquerque, NM	5145	3.34
Pic du Bure, France	8196	6.00
Pic du Midi, France	9298	8.62
Echo Lake, CO	10600	11.38
Aiguille du Midi, France	11289	12.45
White Mountain, CA	12442	19.48
Mauna Kea, HI	13000	11.35

Notes:
1. Adjustments have been made for the influence of minimum solar sunspots on cosmic ray flux.
2. Underground facilities.

Table 2: **Devices Previously Tested (WP286 v1.x)**

Device Family	Device Number	Technology	Quantity
Virtex®-II FPGAs	XC2V6000	150nm	300
Virtex-II Pro FPGAs	XC2VP50	130nm	600
Spartan®-3 FPGAs	XC3S1500	90nm	200
Virtex-4 FPGAs	XC4VLX25	90nm	400
Virtex-4 FPGAs	XC4VLX60	90nm	300
Virtex-5 FPGAs	XC5VLX110	65nm	300

Table 3: **Devices Presently Under Test (WP286 v2.0)**

Device Family	Device Number	Technology	Quantity
Spartan-6 FPGAs	XC6SLX150	45nm	200
Virtex-6 FPGAs	XC6VLX240T	40nm	300
Kintex®-7 FPGAs	XC7K325T	28nm	300
Kintex UltraScale™ FPGAs	XCKU040	20nm	400
Kintex UltraScale+™ FPGAs	XCKU9P	16nm	400

Over the years, the Rosetta program has changed to include prediction of error rates using TCAD modeling, fabrication and beam testing of test devices, beam testing of production devices, and testing using the atmospheric placement of arrays, as well as underground arrays.

In the IC design of the Xilinx FPGAs, the individual memory cells (implemented as static latches) used for configuration, look-up tables, and block RAM were all simulated for their sensitivity to single event upsets.

To detect alpha contamination in packaging and assembly, the experimental groups were rotated through the three altitudes in addition to using the underground facility. Any evidence of a constant upset rate due to alpha particles would be observed as a non-altitude, non-latitude dependent factor in the resulting upsets, or measured directly underground.

Atmospheric Test Results

All atmospheric and alpha information is present in UG116, *Device Reliability Report*, which is updated twice per year. The report summarizes the atmospheric and beam test results for all Xilinx FPGA device technologies. The error rate is stated either in failures in time (FIT) per billion hours or in mean time between events in hours, days, or years. A functional failure of the user data due to the single event upset rate then becomes mean time between functional failure in hours, days, or years. *Estimation of Single Event Upset Probability Impact of FPGA Designs* [Ref 4] describes the relationship between the mean time between failure (MTBF) configuration bit and mean time between functional failure, which is based in estimating the Device Vulnerability Factor (DVF). Not every upset results in a functional failure because upsets can be masked in either time or space by a user's design. The DVF factor has been shown to be commonly from 2%, to no more than 10%, in actual device beam testing. A reasonable DVF estimate when the design is not known is 5%.

Since on average, it takes from 10 to 50 upsets to actually cause a functional failure, determining the field failure rate of any design needs to be appropriately derated. The recommended worst-case estimate is to use a factor of ten (10) as the derating factor.

An *essential bits* feature of the Xilinx bitstream generation tools provides a design-specific estimate of the derating for any design. In addition to the *Device Reliability Report,* Xilinx also provides a pre-design failures-in-time (FIT) estimator that helps customers determine if SEU mitigation is needed, given their design specifications.

Q_{CRIT} Simulation

The Xilinx IC design group uses models and methods from Xilinx fabrication partners to estimate the potential sensitivity of the memory cells to upsets. These models and methods have been used in their production of other standard products. Their prediction of Q_{CRIT} to atmospheric upsets is used to compare with Xilinx observations in the Rosetta experiment.

Xilinx then models candidate layouts because they differ in some cases from the foundry layout. After that, Xilinx fabricates test devices so that beam testing can be done to confirm predictions prior to making a selection of a candidate cell for use in a Xilinx product.

Accelerator Test Facilities

In the past, the best resource available to simulate atmospheric neutrons had been the high-energy Neutron Testing Facility at the Los Alamos Neutron Science Center (LANSCE). At LANSCE, high-energy neutrons are produced by spallation. A linear accelerator produces an 800MeV pulsed proton beam that strikes a water-cooled tungsten target. The impact produces a spectrum of neutrons whose energy distribution and intensity is precisely measured. This spectrum is very similar in shape to the atmospheric spectrum.

The flight path consists of a small building for the irradiation that also encloses the testing equipment, isolated from the beam by a substantial concrete barrier. The devices to be tested are placed in the neutron beam line (in air) in the irradiation building. The experimenters control the neutron beam by opening and closing a shutter external to the irradiation building, and the number of neutrons on the sample is continuously monitored and recorded. Corrections to flux for the $1/R^2$ distance from the source must be included.

Additional tests are performed at other facilities for thermal neutrons and protons.

Accuracies are calculated either by variations in the results over many visits (more than 30 for LANSCE), and represent the 95% confidence intervals. All tests had more than 5,000 actual upsets each, so that the inaccuracies due to counting of the number of events are less than ±1% for 95% confidence interval.

LANSCE Results

Testing is performed at LANSCE on a regular basis. See UG116, *Device Reliability Report*.

Conclusion

As the hardness to atmospheric neutrons improves, fewer upsets in the beam testing also occur, which affect the accuracy of the results, requiring longer beam exposures or resulting in higher statistical uncertainty.

It is not possible to make a statement about foundry, process, voltage, or temperature effects without side-by-side experiments in the same beam, at the same time, with a few thousand upsets on each. All data in UG116, *Device Reliability Report*, meets these criteria.

For more information, go to:

http://www.xilinx.com/support/quality/single-event-upsets.html

References

1. Lesea, Austin, Saar Drimer, Joseph Fabula, Carl Carmichael, and Peter Alfke. *The Rosetta Experiment: Atmospheric Soft Error Rate Testing in Differing Technology FPGAs*. IEEE Transactions on Device and Materials Reliability, Volume 5, Number 3, September 2005.
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3. Goldhagen, Paul, J.M. Clem, and J.W. Wilson, *Recent Results from Measurements of the Energy Spectrum of Cosmic-Ray Induced Neutrons Aboard an ER-2 Airplane and on the Ground*. Preprint: Advances in Space Research 32 (1) pp. 35-40 (2003), Proceedings of the 34th COSPAR Scientific Assembly, Houston, TX, October 10-19, 2002.
4. Sundararajan, Prasanna, Scott McMillan, Brandon Blodget, Carl Carmichael, and Cameron Patterson. *Estimation of Single Event Upset Probability Impact of FPGA Designs*. MAPLD 2003.

Related Reading

1. Roche, Philippe and Gilles Gasiot. *Impacts of Front-End and Middle-End Process Modifications on Terrestrial Soft Error Rate*. IEEE Transactions on Device and Materials Reliability, Volume 5, Number 3, September 2005.
2. Castellani, Karine. *3-D Modeling of Bulk and Multi-gate Transistors and SRAM* (summary of research), Laboratoire Matériaux et Microélectronique de Provence (L2MP), UMR/CNRS.
3. Swift, Gary (editor). *Xilinx Single Event Effects, 1st Consortium Report, Virtex-II Static SEU Characterization*. JPL website, http://parts.jpl.nasa.gov/tag/parts-technology.
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The California Institute of Technology Submillimeter Observatory at Mauna Kea, Hawaii.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/22/2016	2.0	Updated document to reflect additional technology nodes to 16nm and clarify historical versus ongoing experiments.
10/13/2011	1.1	Updated document to reflect 40nm technology node and added Virtex-6 and Spartan-6 FPGA data. Updated "Introduction," Table 2, Experiments, Atmospheric Test Results, Q_{CRIT} Simulation, Accelerator Test Facilities, Conclusion, Acknowledgments, and References sections.
05/22/2009	1.0.1	Changed footnote 1 on page 3. Was: FIT/Mb = failures per million hours per Megabit. Is: FIT/Mb = failures per billion hours per Megabit.
03/10/2008	1.0	Initial Xilinx release.

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