Device Reliability Report

Second Half 2020

UG116 (v10.14) April 23, 2021

XILINX

Revision History

The following table shows the revision history for this document.

Date	Revision
04/23/2021 Version 10.14	
Chapter 1: The Reliability Program	Removed XCVxxxE from Table 8. Removed 180 nm (Virtex-E) row from Table 19 and Table 20. Added KU19P, VU23P, ZU43DR, ZU46DR, ZU47DR, ZU48DR, and ZU49DR to Table 17. Updated device hours for 16 nm, 20 nm, 28 nm, 40 nm, 45 nm, 65 nm, 130 nm, 180 nm, 220 nm/180 nm, and 350 nm/250 nm in Table 18. Updated soft error rates for 20 nm and 16 nm process technologies in Table 19 and Table 20.
Chapter 3: Results by Package Type	Updated tables with the latest test results.
Chapter 2: Results by Product Family	Updated tables with the latest test results.
10/30/2020 Version 10.13	
Chapter 1: The Reliability Program	Removed note about HTS stress from Table 6. Added VU19P to Table 17. Updated device hours for 16 nm, 20 nm, 28 nm, 40 nm, 45 nm, 90 nm, and 180 nm in Table 18. Updated soft error rates for 20 nm and 16 nm process technologies in Table 19 and Table 20.
Chapter 2: Results by Product Family	Updated tables with the latest test results.
Chapter 3: Results by Package Type	Updated tables with the latest test results.
04/06/2020 Version 10.12	
Chapter 1: The Reliability Program	Updated ESD and latch-up data for UltraScale+ devices (Table 17), summary failure rates (Table 18) and soft error rates (Table 19, Table 20, and Table 21) for 28 nm, 20 nm, and 16 nm process technologies.
Chapter 2: Results by Product Family	Updated tables with the latest test results.
Chapter 3: Results by Package Type	Updated tables with the latest test results.
09/18/2019 Version 10.11	
Chapter 1: The Reliability Program	Updated summary failure rates (Table 18) and soft error rates (Table 19 and Table 20) for 28 nm, 20 nm, and 16 nm process technologies.
Chapter 2: Results by Product Family	Updated tables with the latest test results.
Chapter 4: Board-Level Reliability Tests	Updated tables with the latest test results.
03/22/2019 Version 10.10	
Chapter 1: The Reliability Program	Updated summary failure rates (Table 18) and soft error rates (Table 19 and Table 20) for 28 nm, 20 nm, and 16 nm process technologies.
Chapter 2: Results by Product Family	Updated tables with the latest test results.
Chapter 4: Board-Level Reliability Tests	Updated tables with the latest test results. Added device type XCVU7P.
09/10/2018 Version 10.9	
Chapter 1: The Reliability Program	Added devices for Spartan®-7 FPGAs to Table 15. Added a column for RF-ADC and RF-DAC HBM and CDM data to Table 17. Updated Table 18, Table 19, and Table 20.

Date	Revision
Chapter 2: Results by Product Family	Updated tables with the latest test results. Added tables for *TH Test Results for Si Gate CMOS Device Types in the UltraScale Family* and the UltraScale+ family. Removed device types XC2Sxxx, XC3Sxxx, and XC3SDxxxA. Added Table 2-43, *HAST Test Results for Si Gate CMOS Device Type XC6Sxxx*. Removed the section *Unbiased High Accelerated Stress Test*.
Chapter 4: Board-Level Reliability Tests	Updated tables with the latest test results. Added packages CPG196, SFV625, SFV784, FBV900, FBV484, FFG323, FFG324, FFG363, FFG1513, FFG1696, FFG1704, FFG1738, FFG1759, FFV901, FFV1136, FFV1148, FFV1152, FFV1153, FFV1154, FFV1156, FFV1156, FFV1157, and FFV1158. Removed packages CSG144, FFG900, FGG256, FGG320, FGG484, FGG400, FGG1156, FLV1517, FLV1924, FLV2104, HCG1932, PQG160, PQG208, PQG240, QFG32, and QFG48.
07/12/2018 Version 10.8.2	
Throughout	Editorial updates only. No technical content updates.
05/03/2018 Version 10.8.1	
Chapter 2: Results by Product Family	Corrected UltraScale and UltraScale+ device rows in Table 2-17.
03/22/2018 Version 10.8	
Chapter 1: The Reliability Program	Added device XC7S50 to Table 15. Added PS-GTR transceivers to Table 17. Updated Table 18, Table 19, and Table 20.
Chapter 2: Results by Product Family	Updated tables with the latest test results.
Chapter 4: Board-Level Reliability Tests	Updated tables with the latest test results. HTS failures for device type XCVU9P in Table 3-37 changed to 0. Added test results for package FTG196 for device type XA7S50 (Table 3-54).
11/17/2017 Version 10.7.1	
	Updated the SEU link above Table 19.
11/13/2017 Version 10.7	
Chapter 1: The Reliability Program	Updated Table 7 and Table 18 for 0.016 µm devices. Added Table 17 for UltraScale+ devices. Updated SEU and Soft Error Rate Measurements, Table 19, and Table 20.
Chapter 2: Results by Product Family	Updated tables for 0.016 µm devices. Updated Updated Table 2-1 and Table 2-14. Added Table 2-16, Table 2-25, Table 2-40, and Table 2-55.
Chapter 4: Board-Level Reliability Tests	Adjusted Weibull plots for clarity and accuracy. Added device types (Table 3-16 and Table 3-37). FFV1927 was corrected to FFG1928. Updated FFG1928 characteristic life in Table 119.
07/11/2017 Version 10.6.1	
Throughout	Made typographical changes.
07/10/2017 Version 10.6	
Chapter 1: The Reliability Program	Updated ESD and LU test data. Added a definition of *obsolete*.
Chapter 2: Results by Product Family	Updated many tables and deleted tables for obsolete products. Added new tables for CMOS device types XC4Vxxx, XC5Vxxx, and XC6Vxxx (Table 2-48 through Table 2-50). Added a note to Table 2-21.

Date	Revision
Chapter 4: Board-Level Reliability Tests	Updated many tables and deleted tables for obsolete products containing data more than 2 years old. Deleted data for non-hermetic packages BG352, BG432, and BG560 (device types XCV1000E, XCV1600E, and XCV300). Deleted data for package FB676 (device type XC7K410T). Deleted data for package SF363 (device type XC4VLX15). Deleted data for Pb-free packages BGG256 (device type XCS30XL), BGG352, BGG432, and BGG560 (device types XCV300E (Shrink), XCV600E (Shrink), and XCV1000E (Shrink)), CPG196 (device types XC6SLX4 and XC6SLX16), CPG236 (device type XC7A50T), FLG1155 (device type XC7V11580T), HCG1155 (device type XC7VH580T), and SFG363 (device type XC4VLX15). Added a note to Table 3-2 and Table 3-23.
04/04/2017 Version 10.5.2	
Table 2-15	XCVU440 equivalent device hours were corrected to be 34,592.
12/19/2016 Version 10.5.1	
FFVB2104	Updated the plot.
10/31/2016 Version 10.5	
Changed many tables to show test data for the first half of 2016. Added new product and package reliability data for XCVU440, XCVU190, XCVU125, XCVU095, and XCKU115 with respective packages of FFV1517, FFV1924, and FFV2104, FLV1517, FLV1924, and FLV2104 , FLG2104, FLG2377, and FLG2892. Removed the reliability data for these obsolete devices and packages: XCE06L24T, XC17SxxxA, XC17Vxxx, XCE0104, XC9572XL (PCG44 only), and PG120.	
Chapter 1: The Reliability Program	Changed the title of Table 8 to ESD and Latch-up Data for PROMs, CPLDs, and Older FPGAs. Added devices to Table 16. Changed nomenclature for degrees Kelvin to K. Updated Table 18. Updated Table 19 and Table 20 data for the 28nm and 20nm nodes. (The former Table 1-18, Beam Testing and Real-Time Soft Error Rates, was divided into two tables: Experimental Beam Testing and Real-Time Soft Error Rates for CRAM and Experimental Beam Testing and Real-Time Soft Error Rates for BRAM.)
Chapter 2: Results by Product Family	Updated Table 2-1, Summary of HTOL Test Results and many tables. Updated CPLD Products.
Chapter 4: Board-Level Reliability Tests	Updated tables for non-hermetic and hermetic packages. Added SFVA784 and SBVA784 to Pb-Free BGA.
04/01/2016 Version 10.4	
Changed many tables to show test data for the second half of 2015.	
Chapter 1: The Reliability Program	Updated Table 18 and Table 1-18.
Chapter 2: Results by Product Family	Updated most of the tables in this chapter. Added a footnote to Table: THB Test Results for Si Gate CMOS Device Type UltraScale FPGAs. Added Table: High-Temperature Storage Life Test Results for Si Gate CMOS Device Type UltraScale FPGAs.
Chapter 4: Board-Level Reliability Tests	Updated Table 111: Summary of Test Results. Added FBVA900, FFVB2104, and FLVA1924 package types to Pb-Free BGA, Table 112.
09/08/2015 Version 10.3.1	
Table 1-18	Corrected two numbers in 20nm tech node row, FIT/Mb (Real-Time Soft Error Rate Per Event) column.

Date	Revision
09/02/2015 Version 10.3	
Changed many tables to show test data for the first half of 2015. No devices were removed.	The UltraScale FPGA KU040 device was added. Test results for new package FFVA1156 were added. FFV1927 package details were added to Pb-Free BGA.
03/09/2015 Version 10.2.1	
	Corrected typo in Table 18 and High-Temperature Operating Life (HTOL) Test from 1.43,104 to 1,143,104.
02/11/2015 Version 10.2	
This report will now be issued biannually (twice a year). Changed many tables to show second quarter 2014 test data.	
Chapter 1: The Reliability Program	Added UltraScale device data. Added Table 1-16: ESD and Latch-up Data for UltraScale Series.
Chapter 2: Results by Product Family	Added Table 2-27: THB Test Results for Si Gate CMOS Device Type XC2Vxxx. Deleted Table 2-29: THB Test Results for Si Gate CMOS Device Type XC2Sxxx. Deleted Table 2-39: TH Test Results for Si Gate CMOS Device Type XC3Sxxx. Deleted Table 2-40: TH Test Results for Si Gate CMOS Device Type XC3SxxxE. Deleted Table 2-41: TH Test Results for Si Gate CMOS Device Type XC3SxxxA. Deleted Table 2-42: TH Test Results for Si Gate CMOS Device Type XC3SDxxxA. Table 2-78: HASTU Test Results for Si Gate CMOS Device Type XC6Sxxx. Added Table 2-90: High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC6Sxxx. Table 2-91: High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC6Sxxx. Added Table 2-119: Summary of THB Test Results. Added Table 2-120: THB Test Results for Si Gate CMOS Device Type XC95xxxXL (replaced data for XC2Cxxx/A). Added Table 2-121: THB Test Results for Si Gate CMOS Device Type XC2Cxxx/A.
Chapter 4: Board-Level Reliability Tests	Deleted package test results for PC44, PD8, and Table 3-29: Tests of Package Type DD8 (obsolete package). Added package test results for BGG256, FFVA1156, CPG236, FLG1155, FGG400, and added Figure 3-14: Cycles to Failure in the Second-Level Reliability Tests for FFG1928.
08/07/2014 Version 10.1	
Changed many tables to show second quarter 2014 test data.	
Chapter 1: The Reliability Program	Updated Table 18 and Table 19. Updated SEU and Soft Error Rate Measurements.
Chapter 2: Results by Product Family	Data was updated in many tables. The Autoclave Test section was removed for CPLDs. HASTU has substituted Autoclave for the reliability monitor program.
Chapter 4: Board-Level Reliability Tests	Added packages for PQ208 and FBG484.
05/02/2014 Version 10.0	
Changed many tables to show first quarter 2014 test data.	Removed obsolete 0.22 μm Virtex® FPGA product data. Added package data for CLG400, FLG1926, FLG1928, and HCG1932. In Chapter 3, removed tables for packages CS280, CS484, FF1513, FF1517, PQ100, PQ160, PQ208, PQ240, CSG280, and PCG84. Added data for packages CLG400, FLG1926, FLG1928, and HCG1932. Added *Appendix A: Additional Resources and Legal Notices*.
03/18/2014 Version 9.8	
	Replaced reliability data for package FFG1928. Added reliability data for package FLG1925. Revised the Revision History section for readability.

Date	Revision
02/14/2014 Version 9.7	
Changed many tables to show fourth quarter, 2013 test data. Removed reliability data for the obsolete XCSxxxXL 0.25 µm device. Removed Spartan®-3 FPGA Autoclave data. HASTU has substituted Autoclave for the reliability monitor program.	
Chapter 1: The Reliability Program	Updated Table 8, Table 15, Table 18, and Table 1-18 Beam Testing and Real-Time Soft Error Rates.
Chapter 2: Results by Product Family	Updated and moved existing tables. Updated test results in Temperature Cycling Test, High Accelerated Stress Test, and High Temperature Storage Life. Updated test results in Temperature Humidity with Bias Test, Unbiased High Accelerated Stress Test, and Data Retention Bake Test.
Chapter 4: Board-Level Reliability Tests	Alphabetized Non-Hermetic packages SO20, VO20, VO48, PC44, PC84, PC20, PQ100, PQ160, PQ208, PQ240, TQ100, TQ144, VQ44, VQ100, HQ208, and HQ240. Removed package BGG256 from Reliability Data for Pb-Free Packages.
11/19/2013 Version 9.6	
Changed many tables to show third quarter, 2013 test data. Removed reliability data for the obsolete XC95xxx 0.5 µm device. Removed Spartan-3 FPGA Autoclave data. HASTU has substituted Autoclave for the reliability monitor program.	
Chapter 1: The Reliability Program	Updated Table 7, Wafer Process Technology Family, Table 8, Product ESD and Latch-up Data, Table 15, ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs, Table 18, Summary of the Failure Rates, and Table 1-18, Real-Time Soft Error Rates. Added devices XC7V2000T, XC7VH580T, XC7VX1140T, and XC7Z100 to Table 15.
Chapter 2: Results by Product Family	Deleted the Autoclave Test section in Temperature cycling Test.
Chapter 4: Board-Level Reliability Tests	Added packages BG352, BG432, and BG560, FB676, FF484, FG320, FF900, BGG256, FBG900, FFG1513, FFG1517 FFG1696 FFG1704, FFG1738, FFG1759, FFG1738, FFG1760, FFV900, FFV901, FLG1925, FLG1926 FLG1928, FLG1932, FLG2104, FLG2377, FLG2892, and FLG48. Added FBG900, SBG484, FFG1928 and their plots to Pb-Free BGA.
08/16/2013 Version 9.5	
Changed many tables to show second quarter, 2013 test data. Removed reliability data for obsolete devices: XC17(S)xxx/XL/E 0.6 µm, XC4xxx/LE 0.5 µm, XC4xxxE 0.5 µm, XC4xxxXL 0.35 µm, XCSxxx 0.35 µm, XC4xxxXLA 0.25 µm, and XC95xxxXV 0.25 µm	
Chapter 1: The Reliability Program	Updated Table 7, Wafer Process Technology Family, Table 8, Product ESD and Latch-up Data, Table 9, ESD and Latch-up Data for XC2VPxxx, Table 18, Summary of the Failure Rates, and Table 1-18, Real-Time Soft Error Rates. Added XC7VX980T to Table 15, ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs.
Chapter 2: Results by Product Family	Deleted tables for obsolete devices. Updated data in many tables. Added Table 2-23, THB Test Results for Si Gate CMOS Device Type XC3SxxxAN and Table 2-86, THB Test Results for Si Gate CMOS Device Type XC17SxxxA.

Date	Revision
Chapter 4: Board-Level Reliability Tests	Deleted these tables: Table 3-24, Tests of Package Type DD8 Table 3-25, Tests of Package Type Chip Scale CC44 Table 3-61, Test Results for Device Types XC7VX485T, XC7VX690T under heading FFG1927. Deleted PG132 and PG175 from Table 3-7, Tests of Package Type PG223. Deleted CB-100 and CB164 from and added CB196 to Table 3-8, Tests of Package Type CB228. Updated data in many tables. Added package CS484. Added packages FF1924, FF1926, FF1927, FF1928, FF1929, and FF1930. Added packages FFG1924, FFG1926, FFG1926, FFG1927, FFG1928, and FFG1930.
05/13/2013 Version 9.4	
Changed many tables to show first quarter, 2013 test data.	
Chapter 1: The Reliability Program	Added 7 series devices XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T and Zynq-7000 SoC devices XC7Z010, XC7Z030, and XC7Z045 to Table 15, ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs. Updated data for 0.25 µm, 0.35 µm, and 0.5 µm process technologies in Table 18, Summary of the Failure Rates. Updated data for 40 nm, 45 nm, and 28 nm technology nodes in SEU and Soft Error Rate Measurements.
Chapter 2: Results by Product Family	Data in many tables was updated. Removed duplicate Table 2-17, HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCE2Vxxx. Deleted Table 2-69, Temperature Cycling Test Results for Si Gate CMOS Device Type XC4xxxXLA. Added Table 2-67, Temperature Cycling Test Results for Si Gate CMOS Device Type XCE4VxXxxx.
Chapter 4: Board-Level Reliability Tests	Data in many tables was updated. Added packages and test results for FFV900, FFV901 and FFG1927.
04/02/2013 Version 9.3	
Changed many tables to show fourth quarter, 2012 test data. Added Xilinx 7 series FPGAs and Zynq-7000 SoCs.	
Chapter 1: The Reliability Program	Added XC7A100T, XC7A200T, XC7K70T, and XC7Z020 devices to Table 1-15 ESD and Latch-up Data for 7 Series FPGAs. Failure rate data changed in Table 1-16 Summary of the Failure Rates. Text and data changed in SEU and Soft Error Rate Measurements.
Chapter 2: Results by Product Family	Data in many tables was updated. Added Table 2-33 THB Test Results for Si Gate CMOS Device Type XCVxxx, Table 2-35 THB Test Results for Si Gate CMOS Device Type XC2Vxxx, Table 2-32 THB Test Results for Si Gate CMOS Device Type XC2SxxxE, Table 2-81 HAST Test Results for Si Gate CMOS Device Type XC4xxxE, and Table 2-104 HASTU Test Results for Si Gate CMOS Device Type XC4xxxXLA. Deleted Table 2-167, Summary of the Test Results for device XC2Cxxx/A from Temperature Humidity Test, page 68.
Chapter 4: Board-Level Reliability Tests	Data in many tables was updated. Added packages CS144, CS324, CLG400 and CLG484, FBV676 and their respective test results in Table 3-9 Test Results for Device Types XCV50, XC2V80, Table 3-11 Test Results for Device Types XC6SLX45, XC6SLX45T, Table 3-29 Test Results for Device Types XC2V1000, XC2V1500, and Table 3-49 Test Results for Device Types XC5VLX50. Note: Table numbers are accurate as of the version 9.3 printing.

Date	Revision
02/12/2013 Version 9.2	
Changed many tables to show the third quarter, 2012 test data. Added Xilinx 7 series FPGAs.	
Chapter 1: The Reliability Program	Added XC7K160T, XC7K410T, XC7K420T, XC7K480T, XC7V585T, and XC7VX485T devices to Table 1-15, ESD and Latch-up Data for 7 Series FPGAs.
Chapter 2: Results by Product Family	Added Table 2-34, THB Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-95, HAST Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-103, HASTU Test Results for Si Gate CMOS Device Type XC4xxxE, Table 2-110, HASTU Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-111, HASTU Test Results for Si Gate CMOS Device Type XCVxxxE (Shrink), Table 2-120, HASTU Test Results for Si Gate CMOS Device Type XCE4VxXxxx, Table 2-125, High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XC4xxxXLA, Table 2-126, High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XCSxxx, Table 2-141, High-Temperature Storage Life Test Results for Si Gate CMOS Device Type XCE4VxXxxx, and Table 2-160, Autoclave Test Results for Si Gate CMOS Device Type XCFxxxS/P.
Chapter 4: Board-Level Reliability Tests	Added packages FF665, FF672, FF676, FFG665, FFG672, and FFG896. Added Table 3-47, Test Results for Device Types XC5VLX30T and Table 3-56, Test Results for Device Type XC2V1000. Note: Table numbers are accurate as of the version 9.2 printing.
08/22/2012 Version 9.1	
Changed many tables to show the second quarter, 2012 test data.	
Chapter 1: The Reliability Program	Added entries for devices XC6SLX4 and XC6SLX9. Removed obsolete reliability data for devices XC4VSX25, XC4VSX55, and XCV600E.
Chapter 2: Results by Product Family	Added entries for devices XC17S150A, XC3S250E, XC6VLX195T, XC7K410T, XC7VX485T, and XC9536. Removed obsolete reliability data for the following devices: XC17(S)xxx, XC17(S)xxx(X)L, XC17(S)xxxE, XC1702L, XC17S15A, XC17S200A, XC17S50XL, XC17Sxxx, XC17SxxxA, XC17SxxxXL, XC17Vxxx, XC18V01, XC18V02, XC18V04, XC18V512, XC18Vxxx, XC2C64, XC2S100E, XC2S150E, XC2V1500, XC2V3000, XC2VP100, XC2VP70, XC2VPxxx, XC2Vxxx, XC3S1000, XC3S100E, XC3S1400AN, XC3S200A, XC3SD1800A, XC3SDxxxA, XC3SxxxA, XC3SxxxAN, XC4013XLA, XC4VLX15, XC4VLX200, XC4VLX80, XC4VSX25, XC4VSX55, XC4xxxXLA, XC5VLX50T, XC6SLX150T, XC6SLX45, XC6SLX45T, XC6VLX130T, XC6VLX760, XC95144XL, XC95144XV, XC95288XV, XC95xxxXL, XC95xxxXV, XCF01S, XCF04S, XCF08P, XCF16P, XCF32P, XCFxxx, XCFxxxP, XCFxxxS, XCS20, XCS40XL, XCSxxx, XCSxxxXL, XCV1000E, XCV1600E, XCV400, XCV400E, XCV405E, XCV600E, XCV812E, XCVxxx (shrink), XCVxxxE, XCVxxxE (shrink)

Date	Revision
Chapter 4: Board-Level Reliability Tests	Added entries for devices XC7K410T and XC7VX485T. Removed obsolete reliability data for the following devices: XC17256E, XC17S100A, XC17S100XL, XC17S200A, XC17S50A, XC18V01, XC2C128, XC2C256, XC2S300E, XC2V1000, XC2V250, XC2V500, XC2V6000, XC2V80, XC2VP100, XC2VP50, XC2VP70, XC3S1500, XC3S4000, XC3S5000, XC4085XLA, XC4VLX100, XC4VLX25, XC5215, XC5VLX50, XC6SLX150T, XC6SLX16, XC6SLX45, XC6SLX45T, XC6VLX130T, XC6VLX240T, XC6VLX475T, XC6VLX760, XCE2VP50, XCF01S, XCF02S, XCF04S, XCF08P, XCF16P, XCF32P, XCR3064XL, XCS40XL, XCV1000E (shrink), XCV1600E, XCV2000E, XCV2000E (shrink), XCV300E (shrink), XCV600, XCV600E
05/08/2012 Version 9.0	
	Changed many tables to show the first quarter, 2012 test data. Added Xilinx 7 series FPGAs.
01/27/2012 Version 8.1	
Chapter 1: The Reliability Program	Added XCE6VxXxxx to Table 1-7. Added XC5VSX240T to Table 1-12.
Chapter 2: Results by Product Family	Added XCE6VxXxxx to Table 2-1. Deleted XC2S150 from Table 2-8. Added XCV100 to Table 2-9. Added XC6SLX45 and XC6SLX100 to and deleted XC6SLX16 from Table 2-23. Added XC4VLX160 and XC4VFX12 and modified Note 1 in Table 2-24. Added Note 1 to Table 2-25 and Table 2-26. Inserted new table: Table 2-29. Added XC5VLX85T to table Table 2-45. Added XC6VLX365T to Table 2-46. Added XCS20XL to and deleted XCS10XL from Table 2-71. Added XC3S200AN to Table 2-84. Added XC6SLX4 to Table 2-85. Added XC2S100E to and deleted XC2S400E from Table 2-93. Added XCS20XL and XCSxxxX to Table 2-105. Added XC6SLX4 and XC6SLX9 to Table 2-117. Deleted XCR3064XL from Table 2-178. Added XC2C64 to Table 2-194. Added XCR3128XL to Table 2-214. Added XC2C64 to Table 2-215.
Chapter 4: Board-Level Reliability Tests	Added HTS to Table 3-3 and Table 3-47. Added HAST to Table 3-56. Note: Table numbers are accurate as of the version 8.1 printing.
11/07/2011 Version 8.0	
Changed most tables to show the third quarter, 2011 test data.	
Chapter 1: The Reliability Program	Updated Acceptance Criteria and added note 3 to Table 1-3.

Date	Revision
Chapter 2: Results by Product Family	Added XCV600E to Table 2-12. Added XC2VP7 to and deleted XC2VP80 from Table 2-15. Deleted XC3S2000 from Table 2-18. Deleted XC4VLX15 from Table 2-24. Added XC6VLX130T to Table 2-28. Added XC4VLX80 to Table 2-43. Added XC2V6000 to Table 2-77. Deleted XC4VFX100 and XC4VLX85T from Table 2-85. Added XC5VLX330T device to Table 2-86. Added XC6VLX195T device to Table 2-87. Added XC6SLX25T to Table 2-99. Added XCV100 to Table 2-123. Added XC6SLX16 to Table 2-136. Added XC4VLX80 to Table 2-137. Deleted XC17S150XL from Table 2-146. Deleted XCF128X from Table 2-148. Deleted XC17S30XL from Table 2-152. Deleted XCF01S, XCF04S, XCF08P, and XCF128X from Table 2-155. Deleted XC17S30XL from Table 2-163. Deleted XC17V16 from Table 2-164. Deleted XC17S30XL from Table 2-169. Deleted XC17V16 from Table 2-170. Deleted XCF01S, XCF04S, XCF08P, and XCF128X from Table 2-172. Deleted XC95216 from Table 2-174. Added XCR3256XL and deleted XCR384XL and XCR3512XL from Table 2-192. Added XCR3256XL and deleted XCR384XL and XCR3512XL from Table 2-201. Added XCR3256XL and deleted XCR3128XL XCR3512XL from Table 2-213.
Chapter 4: Board-Level Reliability Tests	Added HASTU to Table 3-11. Deleted HTS from Table 3-12. Deleted HASTU from Table 3-15. Deleted Temperature cycling –40 to +125°C row from Table 3-26. Added HASTU to Table 3-29. Added HTS to Table 3-43. Added HAST to Table 3-47. Added Temperature cycling -55 to +125°C row and HTS to Table 3-49. Added HTS to Table 3-66. Added Temperature humidity 85°C, 85% RH with bias row to Table 3-74. Note: Table numbers are accurate as of the version 8.0 printing.
08/02/2011 Version 7.0	
Changed most tables to show the **second** quarter, 2011 test data.	
06/17/2011 Version 6.0.1	
Revised last sentence in SEU and Soft Error Rate Measurements for clarity.	
05/09/2011 Version 6.0	
Changed most tables to show the first quarter, 2011 test data.	
02/01/2011 Version 5.12	
Changed most tables to show the fourth quarter, 2010 test data.	
11/01/2010 Version 5.11	
Changed most tables to show the third quarter, 2010 test data.	
08/10/2010 Version 5.10	
Changed most tables to show the second quarter, 2010 test data.	
05/04/2010 Version 5.9	
Changed most tables to show the first quarter, 2010 test data.	
03/15/2010 Version 5.8	
Changed most tables to show the fourth quarter, 2009 test data.	
10/27/2009 Version 5.7	
Updated most tables to include third quarter, 2009 test data. Added alpha particle FIT/Mb data for Spartan®-6 and Virtex®-6 FPGAs to Table 1-14, page 19. Note: Table number is accurate as of the version 5.7 printing.	

Date	Revision
08/03/2009 Version 5.6	
Changed most tables to show the second quarter, 2009 test data.	
06/15/2009 Version 5.5	
Added SF363 (Lot 2) data to Table 3-62, page 102. Replaced Figure 3-1, page 103, Figure 3-2, page 103, and Figure 3-3, page 104. Revised FFG1704 data in Table 3-64, page 108. Note: Table and Figure numbers are accurate as of the version 5.5 printing.	
05/07/2009 Version 5.4	
Changed most tables to show the first quarter, 2009 test data. Added second paragraph to SEU and Soft Error Rate Measurements.	
02/11/2009 Version 5.3	
Changed most tables to show the fourth quarter test data. Added single event upset and soft error rate data. See Table 1-14, page 19. Note: Table number is accurate as of the version 5.3 printing.	
11/14/2008 Version 5.1	
Changed most tables to show the third quarter test data. Updated legal disclaimer.	
08/15/2008 Version 5.0	
Changed most tables to show the second quarter test data.	
07/07/2008 Version 4.3	
Changed most tables to show the first quarter test data.	
02/06/2008 Version 4.2	
Changed most tables to show the fourth quarter test data.	
10/31/2007 Version 4.1.2	
Changed most tables to show the third quarter test data.	
09/18/2007 Version 4.1.1	
Corrected omission in this history table.	
08/24/2007 Version 4.1	
Changed most tables to show the second quarter test data.	
06/04/2007 Version 4.0	
Changed most tables to show the first quarter test data.	
03/28/2007 Version 3.3.2	
Corrected typos in four tables.	
02/20/2007 Version 3.3.1	
Corrected typos in three tables.	
02/12/2007 Version 3.3	
Changed most tables to show the fourth quarter test data.	
12/01/2006 Version 3.2	
Changed most tables to show the third quarter test data.	
10/06/2006 Version 3.1.2	
Corrected values in tables 1-12, 2-87, 2-90, and 2-91.	
08/29/2006 Version 3.1.1	
Changed typos in tables 2-91, 3-44, and 3-55.	

Date	Revision
08/11/2006 Version 3.1	
Changed most tables to show the second quarter test data.	
06/20/2006 Version 3.0.1	
Corrected two transposed figures in Table 1-10.	
05/05/2006 Version 3.0	
Changed most tables to show the first quarter test data.	
02/24/2006 Version 2.9	
Updated most tables to reflect the fourth quarter test data.	
11/17/2005 Version 2.8	
Updated most tables to include the third quarter test data.	
08/19/2005 Version 2.7	
Changed most tables to show the second quarter test values.	
05/20/2005 Version 2.6	
Corrected data in tables 2-61 and 3-32.	
03/01/2005 Version 2.5	
Changed most tables to show the fourth quarter test values. Removed packaging information from Chapter 1 and added a reference to the packaging website.	
01/04/2005 Version 2.4	
Added third quarter data.	
08/18/2004 Version 2.3	
Added second quarter data.	
05/24/2004 Version 2.2	
Changed Tables 1-1, 2-1, 2-15, 3-44, 3-46, 3-48, 3-50, 3-52 and a heading on page 75.	
05/24/2004 Version 2.1	
Changed FIT rate on page 7 for 0.5 μm from 89 to 8.	
05/10/2004 Version 2.0	
First quarter 2004 revision.	
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Chapter 1

The Reliability Program

Overview

Xilinx publishes this report to provide customers with insight regarding the reliability of Xilinx® products. Reliability is defined as product performance to specification over time in response to varied (specified) environmental stress conditions. The goal of the reliability program is to achieve continuous improvement in the robustness of each product being evaluated.

As part of this program, finished product reliability is measured periodically to ensure that the product performance meets or exceeds reliability specifications. Reliability programs are executed in response to internal programs.

The reliability qualifications of new devices, wafer processes, and packages are designed to ensure that Xilinx products satisfy internal requirements before transfer into production. The reliability qualification and monitoring requirements are outlined in Table 1 through Table 18. The reliability stress tests are conducted according to the conditions specified in JEDEC Solid State Technology Association's reliability test methods for packaged devices, JESD22, except Group B and D tests in which it follows DSCC test methods, MIL-STD-883.

In this report, *obsolete* refers to Xilinx products for which a Product Discontinuation Notice (PDN) has been issued to cease the shipment and to data more than two years old that is no longer valid due to a process change.

Product Qualification

The reliability tests used for wafer process qualification are summarized in the following table.

Table 1: **Wafer Process Qualification Tests**

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
High-temperature operating life (HTOL)	$T_J \geq 125°C$, V_{DD} Max	1,000 hours	3	77	200 FIT[1] 50 FIT[2]

Table 1: **Wafer Process Qualification Tests** *(cont'd)*

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
THB[3] or High-accelerated stress test (HAST)[3]	85°C, 85% RH, VDD	1,000 hours	3	25	0 failures
	130°C, 85% RH, VDD	96 hours			
	110°C, 85% RH, VDD	264 hours			
Temperature humidity (TH)[3] or Unbiased high accelerated stress test (UHAST)[3]	85°C, 85% RH	1,000 hours	3	25	0 failures
	130°C, 85% RH	96 hours			
	110°C, 85% RH	264 hours			
Temperature cycling (TC)[3, 4, 5, 6,]	–65°C to +150°C	500 cycles	3	25	0 failures
	–55°C to+125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Data Retention Bake[7] or High Temperature Storage (HTS)	T_A = 150°C	1,000 hours	3	25	0 failures
Program Erase[8]	TA = 25°C	10,000 cycles	1	32	0 failures

Notes:

1. FIT is *failure in time*. Phase I production is released as the qualification data demonstrates, meeting the required 200 FIT failure rate and other test requirements.
2. Phase II production is released as the qualification data demonstrates, meeting the required 50 FIT failure rate and other test requirements.
3. Package preconditioning is performed prior to THB, HAST, temperature cycling, TH, and UHAST tests.
4. For plastic QFP packages: –65°C to +150°C and 500 cycles or –55°C to +125°C and 1,000 cycles.
5. For plastic BGA packages: –55°C to +125°C and 1,000 cycles.
6. For flip chip packages: –55°C to +125°C and 1,000 cycles or –40°C to +125°C and 1,000 cycles.
7. For CPLD and EPROM products.
8. This is not a mandatory test and only for CPLD and EPROM products.

Non-Hermetic and Hermetic Packages

Moisture sensitivity and reflow temperature information can be found in *Device Package User Guide* (UG112).

The non-hermetic package/assembly qualification is outlined in the following table. However, for hermetic package qualification, a full group B and D test per MIL-STD-833, *Test Methods*, is required.

Table 2: **Non-Hermetic Package/Assembly Qualification**

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
THB[1] or HAST[1]	85°C, 85% RH, V_{DD}	1,000 hours	3	25	0 failures
	130°C, 85% RH, V_{DD}	96 hours			
	110°C, 85% RH, V_{DD}	264 hours			
Temperature cycling[1, 2, 3, 4]	–65°C to +150°C	500 cycles	3	25	0 failures
	–55°C to +125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Autoclave[1] or temperature humidity unbiased[1] or UHAST[1]	121°C, 100% RH	96 hours	3	25	0 failures
	85°C, 85% RH	1,000 hours			
	130°C, 85% RH or 110°C, 85% RH	96 hours or 264 hours			
High-Temperature Storage (HTS)	TA=150°C	1,000 hours	3	25	0 failures

Notes:

1. Package preconditioning is performed prior to THB, HAST, temperature cycling, autoclave, TH, and UHAST tests.
2. For plastic BGA packages: –55°C to +125°C and 1,000 cycles.
3. For flip chip packages: –55°C to +125°C and 1,000 cycles or –40°C to +125°C and 1,000 cycles.
4. For plastic QFP packages: –65°C to +150°C and 500 cycles or –55°C to +125°C and 1,000 cycles.

The qualification process for new devices is shown in the following table.

Table 3: **Device Qualification**

Reliability Test	Conditions	Lot Quantity	Sample Size per Lot	Target Criteria
ESD	HBM[1]	1	3	1,000V
ESD	CDM[2]	1	3	250V[3]
Latch-up	Current injection	1	3	±100 mA

Notes:

1. HBM = Human Body Model.
2. CDM = Charge Device Model.
3. CDM level of 20 nm and below process node is specified per JEP157.

Reliability Monitor Program

The wafer process reliability monitor program is based on the maturity of the wafer process, the number of device hours, and the failure in time (FIT) rate. All processes are divided into one of two classes to determine how often the process is monitored annually. Class 1 processes are monitored every quarter; Class 2 processes are monitored every other quarter. FIT Rate calculations for both classes are based on approximately one million device hours (at T_J = 125°C) per fab if the data is available. Processes that are four years old or less are monitored every quarter regardless of the FIT rate. Mature processes older than four years are monitored based on the FIT Rate. The following table summarizes the classification criteria and monitoring frequency for both classes.

Table 4: **Monitoring Process Classes**

	Class 1	Class 2
Classification Criteria	Process Age ≤ 4 years or FIT > 26 (for FPGAs), 55 (for Flash PROM)	Process Age > 4 years and FIT < 26 (for FPGAs), 55 for Flash PROMs)
Monitor Frequency	4 times per year	2 times per year

The following table shows the reliability tests used to monitor the wafer process.

Table 5: **Tests Used to Monitor Wafer Processes**

Reliability Test	Condition	Duration	Lot Quantity	Sample Size per Process per Family per Quarter
HTOL	T_j > 125°C, V_{DD} Max	1,000 hours	1	45
Data Retention Bake[1]	T_A = 150°C	1,000 hours	1	45

Notes:

1. For CPLD and PROM products.

The package reliability monitor program takes into consideration the following factors:

- Package construction (wire-bond lead frame, wire-bond BGA, or flip chip)
- Factory location (assembly site, or wafer fabrication site)
- Substrate vendor
- Die size
- Technology maturity
- Past history

Based on these factors and availability, representative packages are drawn from inventory for the stress tests defined in the following table. These tests are typically conducted on a quarterly basis, but the number of tests can be reduced or eliminated based on the maturity of the package technology, understanding of failure mechanisms, and their dependency on the stress test.

Table 6: **Tests Used by the Reliability Package Monitor Program**

Reliability Test	Stress Conditions	Stress Duration	Sample Size	Frequency
THB[1] or HAST[1]	85°C, 85% RH, V_{DD}	1,000 hrs	45	WBLF[2] every even quarter WBBGA[3] every odd quarter Flip Chip [4] every quarter
	130°C, 85% RH, V_{DD}	96 hrs		
	110°C, 85% RH, VDD	264 hrs		
Temperature cycling[1, 5]	–55°C to +125°C or –40°C to +125°C	1,000 cycles	45	WBLF every quarter WBBGA every quarter Flip Chip every quarter
Autoclave[1, 6] or Temperature humidity unbiased[1, 6] or UHAST[1, 6]	121°C, 100% RH	96 hrs	45	WBLF every odd quarter WBBGA every even quarter
	85°C, 85% RH	1,000 hrs		
	130°C, 85% RH or 110°C, 85% RH	96 hrs or 264 hrs		
HTS	TA=150°C	1,000 hrs	45	WBLF every quarter WBBGA every quarter

Notes:

1. Package preconditioning is performed prior to THB, HAST, temperature cycling, autoclave, TH, and UHAST tests.
2. For matured WBLF packages (PLCCs, SOICs, and DIPs packages), reliability monitoring is performed once a year.
3. For matured WBBGA packages (S-BGA Cavity-down BGA), reliability monitoring is performed once a year.
4. For flip chip packages, THB testing is performed every quarter and replaces the need for temperature humidity testing.
5. For plastic QFP and BGA packages: –55°C to +125°C and 1,000 cycles; for flip chip packages: –55°C to +125°C and 1,000 cycles or 40°C/+125°C and 1,000 cycles.
6. Refer to the device-specific qualification report for complete autoclave, temperature humidity, and UHAST reliability test data.

Process Technology Family

The following table lists the Xilinx devices that support various process technologies.

Table 7: **Wafer Process Technology Family**

Process Technology	Device
16 nm	UltraScale+ devices
20 nm	UltraScale devices
28 nm	7 series FPGAs and Zynq®-7000 SoCs
40 nm	XC6VxXxxx
45 nm	XC6Sxxx
65 nm	XC5VxXxxx

Table 7: **Wafer Process Technology Family** *(cont'd)*

Process Technology	Device
90 nm	XC3Sxxx, XC3SxxxA, XC3SxxxAN, XC3SxxxE, XC3SDxxxA, XC4VxXxxx, XCE4VxXxxx
130 nm	XC2VPxxx
150 nm	XC18Vxxx, XCFxxxS/P
180 nm	XC2Cxxx
220 nm/180 nm	XC2Sxxx
350 nm/250 nm	XC95xxxXL
350 nm	XCRxxxXL

ESD and Latch-up Summary

ESD results are obtained according to specifications ANSI/ESDA/JEDEC JS-001-2010 and JEDEC JESD22-C101. Latch-up results are obtained by using specification EIA/JESD78. ESD tests are performed at 25°C. In general, the latch-up data for newer products such as Zynq-7000 SoCs, 7 series, Virtex®-4, Virtex®-5, Virtex®-6, Spartan®-3, and Spartan®-6 devices are collected at 125°C unless specified otherwise.

ESD and latch-up data are summarized by family in these tables:

- Table 8: PROMs, CPLDs, and older FPGAs
- Table 9: Virtex-II Pro devices
- Table 10 and Table 11: Virtex-4 devices
- Table 12: Virtex-5 devices
- Table 13: Spartan-6 devices
- Table 14: Virtex-6 devices
- Table 15: 7 series FPGAs and Zynq-7000 SoCs
- Table 16: UltraScale devices
- Table 17: UltraScale+ devices

Table 8: **ESD and Latch-up Data for PROMs, CPLDs, and Older FPGAs**

Device	Latch-up	Human Body Model	Charge Device Model
XC18Vxxx/XCFxx	+200 mA	+2,000V	+500V[1]
XC2Sxxx	+210 mA	+2,000V	+500V[4]
XC95xxxXL	+200 mA	+2,000V to +3,000V	+1,000V[5]
XCRxxxL	+200 mA	+2,000V to +3,000V	+500V[6]
XC2Cxxx	+200 mA	+2,000V	+500V

Table 8: **ESD and Latch-up Data for PROMs, CPLDs, and Older FPGAs** *(cont'd)*

Device	Latch-up	Human Body Model	Charge Device Model
XC3Sxxx	+200 mA	+2,000V	+500V
XC3SxxxE	+200 mA	+2,000V	+500V
XC3SxxxA	+200 mA	+2,000V	+500V

Notes:

1. Measured on XC18V04 and XCF32P
2. Only XCV100E and XCV812E have ESD threshold below 2KV, (XCV100E passed at 1.5KV and XCV812E passed at 1KV)
3. Measured on XCV50E
4. Measured on XC2S200
5. Measured on XC9536XL
6. Measured on XCR3064XL

The ESD results in the following table do not include DXN and DXP temperature sensing pins.

Table 9: **ESD and Latch-up Data for XC2VPxxx**

Device	Latch-up ±200 mA	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		Regular I/O and Power	MGT	Regular I/O and Power	MGT
XC2VP2	Pass	+1,500V	+2,000V	+500V	+300V
XC2VP4	Pass	+2,000V	+1,500V	+500V	+300V
XC2VP7	Pass	+2,000V	+1,000V	+500V	+500V
XC2VP20	Pass	+2,000V	+2,000V	+500V	+300V
XC2VP30	Pass	+2,000V	+2,000V	+500V	+300V
XC2VP40	Pass	+2,000V	+2,000V	+500V	+300V
XC2VP50	Pass	+2,000V	+2,000V	+500V	+300V
XC2VP70	Pass	+2,000V	+2,000V	+500V	+300V
XC2VP100	Pass	+2,000V	+1,000V	+500V	+300V

Table 10: **ESD and Latch-up Data for XC4VFXxxx**

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		STDIO	MGT	STDIO	MGT
XC4VFX12	Pass	+2,000V	N/A	+450V	N/A
XC4VFX60	Pass	+2,000V	+1,000V	+500V	+300V
XC4VFX40	Pass	+2,000V	+1,000V	+500V	+300V
XC4VFX20	Pass	+2,000V	+1,000V	+500V	+300V
XC4VFX100	Pass	+2,000V	+1,000V	+450V	+300V
XC4VFX140	Pass	+2,000V	+1,000V	+500V	+300V

Table 11: **ESD and Latch-up Data for XC4VLXxxx and XC4VSXxxx**

Device	Latch-up	Human Body Model Passing Voltage	Charge Device Mode Passing Voltage
XC4VLX15	Pass	+2,000V	+500V
XC4VLX25	Pass	+2,000V	+450V
XC4VLX40	Pass	+2,000V	+450V
XC4VLX60	Pass	+2,000V	+400V
XC4VLX80	Pass	+2,000V	+450V
XC4VLX100	Pass	+2,000V	+350V
XC4VLX160	Pass	+2,000V	+450V
XC4VLX200	Pass	+2,000V	+350V
XC4VSX25	Pass	+2,000V	+500V
XC4VSX35	Pass	+2,000V	+450V
XC4VSX55	Pass	+2,000V	+400V

Table 12: **ESD and Latch-up Data for XC5VxXxxx/T**

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		SelectIO[1]	Transceiver	SelectIO	Transceiver
XC5VLX20T	Pass	+2,000V	+1,000V	+400V	+250V
XC5VLX30	Pass	+2,000V	N/A	+400V	N/A
XC5VLX30T	Pass	+2,000V	+1,000V	+400V	+250V
XC5VLX50	Pass	+2,000V	N/A	+400V	N/A
XC5VLX50T	Pass	+2,000V	+1,000V	+400V	+250V[2]
XC5VLX85	Pass	+2,000V	N/A	+400V	N/A
XC5VLX85T	Pass	+2,000V	+1,000V	+400V	+250V[2]
XC5VLX110	Pass	+2,000V	N/A	+400V[3]	N/A
XC5VLX110T	Pass	+2,000V	+1,000V	+400V[3]	+250V[2]
XC5VLX155	Pass	+2,000V	N/A	+400V	N/A
XC5VLX155T	Pass	+2,000V	+1,000V	+400V	+250V[4]
XC5VLX220	Pass[5]	+2,000V	N/A	+400V	N/A
XC5VLX220T	Pass[5]	+2,000V	+1,000V	+400V	+250V[4]
XC5VLX330	Pass[6]	+2,000V	N/A	+400V	N/A
XC5VLX330T	Pass[6]	+2,000V	+1,000V	+400V	+250V[2]
XC5VFX30T	Pass	+2,000V	+1,000V	+400V	+250V
XC5VFX70T	Pass	+2,000V	+1,000V	+400V	+250V
XC5VFX100T	Pass	+2,000V	+1,000V	+400V	+250V
XC5VFX130T	Pass	+2,000V	+1,000V	+400V	+250V
XC5VFX200T	Pass	+2,000V	+1,000V	+400V	+250V
XC5VSX35T	Pass	+2,000V	+1,000V	+400V	+250V
XC5VSX50T	Pass	+2,000V	+1,000V	+400V	+250V[2]
XC5VSX95T	Pass	+2,000V	+1,000V	+400V	+250V
XC5VSX240T	Pass	+2,000V	+1,000V	+400V	+250V[2]
XC5VTX150T	Pass	+2,000V	+1,000V	+400V	+250V

Table 12: **ESD and Latch-up Data for XC5VxXxxx/T** *(cont'd)*

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		SelectIO[1]	Transceiver	SelectIO	Transceiver
XC5VTX240T	Pass	+2,000V	+1,000V	+400V	+250V

Notes:

1. Human body model passing voltage for VBATT pin is 1,000V. This data is updated based on the data collected after the HBM tester was upgraded to remove the HBM-ESD trailing pulse.
2. If an internal AC coupling capacitor is used in the GTP receiver input (RX) pin, charge device model passing voltage is 200V. Compliance to ANSI/ESD S20.20 (ESD Association standard for the electrostatic discharge control program) is necessary.
3. Charge device model passing voltage for VBATT pin is 300V.
4. If an internal AC coupling capacitor is used in the GTP receiver input (RX) pin, the CDM level is 150V. Compliance to ANSI/ESD S20.20 (ESD Association standard for the electrostatic discharge control program) is necessary.
5. The D_IN and CS_B pins on XC5VLX220 and XC5VLX220T devices pass at 150 mA.
6. The D_IN, CS_B, and RDWR_B pins on XC5VLX300 and XC5VLX330T devices pass at 150 mA.

Table 13: **ESD and Latch-up Data for XC6Sxxx**

Device	Latch-up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO	GTP	SelectIO	GTP
XC6SLX4	Pass	±2,000V	N/A	±500V	N/A
XC6SLX9	Pass	±2,000V	N/A	±500V	N/A
XC6SLX16	Pass	±2,000V	N/A	±500V	N/A
XC6SLX25	Pass	±2,000V	N/A	±500V	N/A
XC6SLX25T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX45	Pass	±2,000V	N/A	±500V	N/A
XC6SLX45T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX75	Pass	±2,000V	N/A	±500V	N/A
XC6SLX75T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX100	Pass	±2,000V	N/A	±500V	N/A
XC6SLX100T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX150	Pass	±2,000V	N/A	±500V	N/A

Table 13: **ESD and Latch-up Data for XC6Sxxx** *(cont'd)*

Device	Latch-up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO	GTP	SelectIO	GTP
XC6SLX150T	Pass	±2,000V	±2,000V	±500V	±450V

Table 14: **ESD and Latch-up Data for XC6VxXxxx**

Device	Latch-up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC6VLX75T	Pass	±2,000V[1]	±1,000V	±500V[2]	±250V
XC6VLX130T	Pass	±2,000V[1]	±1,000V	±500V[2]	±250V
XC6VLX195T	Pass	±2,000V[1]	±1,000V	±500V[2]	±250V
XC6VLX240T	Pass	±2,000V[1]	±1,000V	±500V[2]	±250V
XC6VLX365T	Pass	±2,000V[1]	±1,000V	±500V[2]	±250V
XC6VLX550T	Pass	±2,000V[1]	±1,000V	±500V[2]	±250V
XC6VLX760	Pass	±2,000V[1]	N/A	±500V[2]	N/A
XC6VSX315T	Pass	±2,000V[1]	±1,000V	±500V[2]	±200V
XC6VSX475T	Pass	±2,000V[1]	±1,000V	±500V[2,3]	±250V
XC6VHX250T	Pass	±2,000V[1]	±1,000V	±500V[2,3]	±250V
XC6VHX255T	Pass	±2,000V[1]	±1,000V	±500V[2,3]	±250V
XC6VHX380T	Pass	±2,000V[1]	±1,000V	±500V[2]	±250V
XC6VHX565T	Pass	±2,000V[1]	±1,000V	±500V[2,3]	±250V

Notes:

1. If the system monitor function is used, HBM passing voltage is: ±1,000V for all of the devices.
2. If the system monitor function is used, CDM passing voltage for the AVDD, AVSS, VN, VP, VREFN, VREFP, DXN and DXP pins is: ±200V for XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VSX315T, XC6VHX250T, XC6VHX255T, and XC6VHX565T devices; ±150V for XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380Tdevices. The DXN and DXP pins can withstand CDM voltages up to 500V without impacting the temperature sensing function.
3. The CDM passing voltage for the CCLK pin of the XC6VSX475T, XC6VHX250T, XC6VHX255T, and XC6VHX565T devices is 450V.

Table 15: **ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs**

Device	Latch-up	HBM Passing Voltage[1]		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC7A12T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A15T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A25T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A35T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A50T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A75T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A100T	Pass	±1,000V	±1,000V	±350V	±300V
XC7A200T	Pass	±1,000V	±1,000V	±350V	±250V
XC7S6	Pass	±1,000V[2]	N/A	±350V	N/A
XC7S15	Pass	±1,000V[2]	N/A	±350V	N/A
XC7S25	Pass	±1,000V	N/A	±350V	N/A
XC7S50	Pass	±1,000V	N/A	±350V	N/A
XC7S75	Pass	±1,000V	N/A	±350V	N/A
XC7S100	Pass	±1,000V	N/A	±350V	N/A
XC7K70T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K160T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K325T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K355T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K410T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K420T	Pass	±1,000V	±1,000V	±350V	±300V
XC7K480T	Pass	±1,000V	±1,000V	±350V	±300V
XC7V585T	Pass	±1,000V	±1,000V	±350V	±250V
XC7V2000T	Pass	±1,000V	±1,000V	±350V	±250V
XC7VH580T	Pass	±1,000V	±1,000V	±350V	±200V
XC7VH870T	Pass	±1,000V	±1,000V	±350V	±200V

Table 15: **ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 SoCs** *(cont'd)*

Device	Latch-up	HBM Passing Voltage[1]		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC7VX330T	Pass	±1,000V	±1,000V	±350V	±250V
XC7VX415T	Pass	±1,000V	±1,000V	±350V	±250V
XC7VX485T	Pass	±1,000V	±1,000V	±350V	±250V
XC7VX550T	Pass	±1,000V	±1,000V	±350V	±200V
XC7VX690T	Pass	±1,000V	±1,000V	±350V	±200V
XC7VX980T	Pass	±1,000V	±1,000V	±350V	±200V
XC7VX1140T	Pass	±1,000V	±1,000V	±350V	±200V
XC7Z007S	Pass	±1,000V	N/A	±350V	N/A
XC7Z010	Pass	±1,000V	N/A	±350V	N/A
XC7Z012S	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z014S	Pass	±1,000V	N/A	±350V	N/A
XC7Z015	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z020	Pass	±1,000V	N/A	±350V	N/A
XC7Z030	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z035	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z045	Pass	±1,000V	±1,000V	±350V	±300V
XC7Z100	Pass	±1,000V	±1,000V	±350V	±300V

Notes:

1. HBM passing voltage levels have been revised based on latest calibration data.
2. All pins pass ±1000V except for HR I/O pins which pass ±900V.

Table 16: **ESD and Latch-up Data for UltraScale Devices**

Device	Latch-up	HBM Passing Voltage		CDM Passing Voltage		
		SelectIO and Special Functions	Transceivers	SelectIO and Special Functions	Transceivers	
					GTH	GTY
XCKU025	Pass	±1,250V	±1,250V	±250V	±200V	N/A
XCKU035	Pass	±1,250V	±1,250V	±250V	±200V	N/A
XCKU040	Pass	±1,250V	±1,250V	±250V	±200V	N/A
XCKU060	Pass	±1,250V	±1,250V	±250V	±200V	N/A
XCKU085	Pass	±1,250V	±1,250V	±250V	±150V	N/A
XCKU095	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCKU115	Pass	±1,250V	±1,250V	±250V	±150V	N/A
XCVU065	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCVU080	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCVU095	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCVU125	Pass	±1,250V	±1,250V	±250V	±200V	±150V
XCVU160	Pass	±1,000V	±1,000V	±250V	±200V	±150V
XCVU190	Pass	±1,000V	±1,000V	±250V	±200V	±150V
XCVU440	Pass	±1,250V	±1,250V	±250V	±200V	N/A

Table 17: **ESD and Latch-up Data for UltraScale+ Devices**

Device	Latch-up	HBM Passing Voltage Levels						CDM Passing Voltage Levels					
		FPGA Logic and SelectIO Interface	Transceivers					FPGA Logic and SelectIO Interface	Transceivers				
			PS-GTR	GTH	GTY	GTM	RF-ADC RF-DAC		PS-GTR	GTH	GTY	GTM	RF-ADC RF-DAC
KU3P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
KU5P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
KU9P	Pass	±1,500V	N/A	±1,500V	N/A	N/A	N/A	±150V	N/A	±150V	N/A	N/A	N/A

Table 17: **ESD and Latch-up Data for UltraScale+ Devices** *(cont'd)*

Device	Latch-up	HBM Passing Voltage Levels						CDM Passing Voltage Levels					
		FPGA Logic and SelectIO Interface	Transceivers					FPGA Logic and SelectIO Interface	Transceivers				
			PS-GTR	GTH	GTY	GTM	RF-ADC RF-DAC		PS-GTR	GTH	GTY	GTM	RF-ADC RF-DAC
KU11P	Pass	±1,500V	N/A	±1,500V	±1,500V	N/A	N/A	±150V	N/A	±150V	±150V	N/A	N/A
KU13P	Pass	±1,500V	N/A	±1,500V	N/A	N/A	N/A	±150V	N/A	±150V	N/A	N/A	N/A
KU15P	Pass	±1,500V	N/A	±1,500V	±1,500V	N/A	N/A	±150V	N/A	±150V	±150V	N/A	N/A
KU19P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU3P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU5P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU7P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU9P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU11P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU13P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU19P	Pass	±1,250V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU23P	Pass	±1,500V	N/A	N/A	±1,500V	±1,500V	N/A	±150V	N/A	N/A	±150V	±150V	N/A
VU27P	Pass	±1,500V	N/A	N/A	±1,500V	±1,500V	N/A	±150V	N/A	N/A	±150V	±150V	N/A
VU29P	Pass	±1,500V	N/A	N/A	±1,500V	±1,500V	N/A	±150V	N/A	N/A	±150V	±150V	N/A
VU31P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU33P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU35P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU37P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU45P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
VU47P	Pass	±1,500V	N/A	N/A	±1,500V	N/A	N/A	±150V	N/A	N/A	±150V	N/A	N/A
ZU2	Pass	±1,500V	±1,500V	N/A	N/A	N/A	N/A	±150V	±150V	N/A	N/A	N/A	N/A
ZU3	Pass	±1,500V	±1,500V	N/A	N/A	N/A	N/A	±150V	±150V	N/A	N/A	N/A	N/A
ZU4	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	N/A	±150V	±150V	±150V	N/A	N/A	N/A

Table 17: **ESD and Latch-up Data for UltraScale+ Devices** *(cont'd)*

Device	Latch-up	HBM Passing Voltage Levels						CDM Passing Voltage Levels					
		FPGA Logic and SelectIO Interface	Transceivers					FPGA Logic and SelectIO Interface	Transceivers				
			PS-GTR	GTH	GTY	GTM	RF-ADC RF-DAC		PS-GTR	GTH	GTY	GTM	RF-ADC RF-DAC
ZU5	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	N/A	±150V	±150V	±150V	N/A	N/A	N/A
ZU6	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	N/A	±150V	±150V	±150V	N/A	N/A	N/A
ZU7	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	N/A	±150V	±150V	±150V	N/A	N/A	N/A
ZU9	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	N/A	±150V	±150V	±150V	N/A	N/A	N/A
ZU11	Pass	±1,500V	±1,500V	±1,500V	±1,500V	N/A	N/A	±150V	±150V	±150V	±150V	N/A	N/A
ZU15	Pass	±1,500V	±1,500V	±1,500V	N/A	N/A	N/A	±150V	±150V	±150V	N/A	N/A	N/A
ZU17	Pass	±1,500V	±1,500V	±1,500V	±1,500V	N/A	N/A	±150V	±150V	±150V	±150V	N/A	N/A
ZU19	Pass	±1,500V	±1,500V	±1,500V	±1,500V	N/A	N/A	±150V	±150V	±150V	±150V	N/A	N/A
ZU21DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	N/A	±150V	±150V	N/A	±150V	N/A	N/A
ZU25DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V
ZU27DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V
ZU28DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V
ZU29DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V
ZU39DR	Pass	±1,250V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V
ZU43DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V
ZU46DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V
ZU47DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V
ZU48DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V
ZU49DR	Pass	±1,500V	±1,500V	N/A	±1,500V	N/A	±1,500V	±150V	±150V	N/A	±150V	N/A	±150V

Failure Rate Determination

The failure rate is typically defined in FIT units. One FIT equals 1 failure per 1 billion device hours. For example, 5 failures expected out of 1 million components operating for 1,000 hours have a failure rate of 5 FIT. The following is the failure rate calculation method:

$$Failure\ Rate = \frac{x^2 10^9}{2(No.\ of\ Devices)(No.\ of\ Hours)(Acc.\ Factor)}$$

where:

x^2 = Chi-squared value at a desired confidence level and (2f + 2) degrees of freedom, where f is the number of failures.

The acceleration factor is calculated using the Arrhenius relationship:

$$A = \exp\left\{\frac{E_a}{k} \bullet \left(\frac{1}{T_{J1}} - \frac{1}{T_{J2}}\right)\right\}$$

where:

E_a = Thermal activation energy (0.7 eV is assumed and used in failure rate calculation except EPROM in which 0.58 eV is used).

A = Acceleration factor

k = Boltzmann's constant, 8.617164 x 10^{-5} eV/K

T_{J1} = Use junction temperature in Kelvin (K = °C + 273.16)

T_{J2} = Stress junction temperature in Kelvin (K = °C + 273.16)

Failure Rate Summary

Table 18: **Summary of the Failure Rates**

Process Technology	Device Hours at TJ = 125°C	FIT[1]
16 nm	1,121,613	10
20 nm	1,089,902	11
28 nm	1,038,272	11
40 nm	1,082,906	11
45 nm	1,152,629	10
65 nm	1,175,529	10

Table 18: **Summary of the Failure Rates** *(cont'd)*

Process Technology	Device Hours at TJ = 125°C	FIT[1]
90 nm	7,433,858	2
130 nm	1,462,448	8
150 nm	2,032,788	6
180 nm	1,084,504	11
220 nm/180 nm	1,040,291	11
350 nm/250 nm	1,143,653	10
350 nm	1,014,559	12

Notes:

1. FIT is calculated based on 0.7 eV (0.58 eV for EPROM), 60% C.L. and TJ of 55°C.

SEU and Soft Error Rate Measurements

Table 19, Table 20, and Table 21 show the soft error rates caused by single event upsets (SEUs) affecting memory cells used as configuration RAM, block RAM, and UltraRAM. Neutron cross-sections are determined from LANSCE beam testing according to JESD89A/89-3A. Soft error rates (in FIT/Mb) are determined from real-time (system level) measurements in various locations and altitudes and corrected for New York City, according to JESD89A/89-1A. Also refer to *Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits* (WP286). All data is current as of the date of this report.

An upset in any configuration bit does not create a soft functional error per se. The bit has to be one that is critical to the function in order for a soft functional error to occur. The number of unused bits and non-critical bits reduces the effective soft error rate by what is known as the device vulnerability factor (DVF). The DVF for a typical design is 5% (one in 20 upsets, on average, cause a functional soft error). In the worst case, the DVF is never larger than one in ten, or never more than 10% of the upsets cause a soft functional error. Therefore, the functional soft error rate of a design running in programmable logic is far lower than what is predicted by calculation from the data in Table 19, Table 20, and Table 21. The significant factor contributing to low DVF is that most programmable logic routing resources are unused within any particular implementation.

Xilinx offers a significant portfolio of SEU analysis and mitigation solutions to help you understand and interpret soft error rates and manage SEU rates in any given design. Consult your Xilinx sales and field support for assistance in understanding these capabilities, and visit our Single Event Upsets website to obtain the Xilinx SEU Estimator tool for modeling device-level SEU rates based on operating environment and the data in Table 19, Table 20, and Table 21. The Xilinx SEU Estimator tool models total SEU rate in terrestrial environments by scaling the real-time data based on operating environment and adding the alpha particle data.

In Table 19, Table 20, and Table 21, Tech Node is technology node, CRAM is configuration RAM, BRAM is block RAM, and URAM is UltraRAM. The data in these tables is not a specification but is for reference only, under the stated conditions for each experiment.

All experiments are performed at ambient temperature with typical power supply voltages.

Table 19: **Experimental Beam Testing and Real-Time Soft Error Rates for CRAM[1]**

Tech Node	Product Family	LANSCE Neutron Cross-Section per Bit[2]		FIT/Mb (Thermal Neutrons)		FIT/Mb (Alpha Particle)[3]		FIT/Mb[4] (Real-Time Soft Error Rate Per Event)[5, 7]	
		CRAM	Error	CRAM	Error[6]	CRAM	Error[6]	CRAM	Error[6]
150 nm	Virtex-II	2.56×10^{-14}	±18%					405	±8%
130 nm	Virtex-II Pro	2.74×10^{-14}	±18%					437	±8%
90 nm	Virtex-4	1.55×10^{-14}	±18%					263	±11%
90 nm	Spartan-3	2.40×10^{-14}	±18%					190	–50% +80%
90 nm	Spartan-3E, Spartan-3A	1.31×10^{-14}	±18%					104	–80% +90%
65 nm	Virtex-5	6.70×10^{-15}	±18%					165	–13% +15%
45 nm	Spartan-6	1.00×10^{-14}	±18%	21	–11% +13%	88	–50% +100%	177	–10% +11%
40 nm	Virtex-6	1.26×10^{-14}	±18%	0.7	–11% +13%	7	–45% +97%	105	–10% +11%
28 nm	Artix-7, Spartan-7, and Zynq-7000	6.99×10^{-15}	±18%	29	–10% +10%	50	–34% +56%	74	–8% +9%
28 nm	Kintex-7 and Virtex-7	5.69×10^{-15}	±18%	1.1	–15% +18%	50	–34% +56%	40	–17% +21%
20 nm	UltraScale	2.55×10^{-15}	±18%	0.5	–13% +16%	9	–64% +374%	31	–11% +12%
16 nm	UltraScale+	2.67×10^{-16}	±18%	0.35	–16% +20%	0.1	–20% +20%	5	–20% +25%

Notes:

1. Experiments are performed at ambient temperature with typical power supply voltages.
2. Data from Los Alamos Neutron Science Center (LANSCE).
3. Spartan-6 and UltraScale+ FPGA alpha data is based on alpha foil testing and package alpha emissivity of 0.001 counts/cm^2/hr. Virtex-6, 7 series, and UltraScale FPGA alpha data estimated using real-time underground cave testing.
4. One FIT equals 1 failure per 1 billion device hours. Mb = 1e6 memory bits.
5. Data compiled from Rosetta experiment which includes upsets from neutron, proton, and thermal neutron secondaries. Based on experimental methodology, upsets from alpha particles are not included. Modeling of the total SEU rate in terrestrial environments requires use of alpha particle data in addition to real-time data. Xilinx advises use of the SEU Estimator tool to model total SEU rates.
6. 90% confidence interval.
7. Soft error rates (in FIT/Mb) are determined from real-time (system level) measurements in various locations and altitudes and corrected for New York City, according to JESD89A/89-1A.

Table 20: **Experimental Beam Testing and Real-Time Soft Error Rates for BRAM[1]**

Tech Node	Product Family	LANSCE Neutron Cross-Section per Bit[2]		FIT/Mb (Thermal Neutrons)		FIT/Mb (Alpha Particle)[3]		FIT/Mb[4] (Real-Time Soft Error Rate Per Event) [5, 7]	
		BRAM	Error	BRAM	Error[6]	BRAM	Error[6]	BRAM	Error[6]
150 nm	Virtex-II	2.64×10^{-14}	±18%					478	±8%
130 nm	Virtex-II Pro	3.91×10^{-14}	±18%					770	±8%
90 nm	Virtex-4	2.74×10^{-14}	±18%					484	±11%
90 nm	Spartan-3	3.48×10^{-14}	±18%					373	–50% +80%
90 nm	Spartan-3E, Spartan-3A	2.73×10^{-14}	±18%					293	–80% +90%
65 nm	Virtex-5	3.96×10^{-14}	±18%					692	–13% +15%
45 nm	Spartan-6	2.20×10^{-14}	±18%	83	–11% +13%	172	–50% +100%	370	–10% +11%
40 nm	Virtex-6	1.14×10^{-14}	±18%	1.4	–11% +13%	120	–45% +97%	213	–10% +11%
28 nm	Artix-7, Spartan-7, and Zynq-7000	6.32×10^{-15}	±18%	41	–10% +10%	45	–34% +56%	72	–8% +9%
28 nm	Kintex-7 and Virtex-7	5.57×10^{-15}	±18%	1.8	–15% +18%	45	–34% +56%	42	–23% +31%
20 nm	UltraScale	4.43×10^{-15}	±18%	1.1	–13% +16%	16	–64% +374%	59	–18% +23%
16 nm	UltraScale+	9.82×10^{-16}	±18%	4.7	–12% +13%	7	–20% +20%	19	–16% +19%

Notes:

1. Experiments are performed at ambient temperature with typical power supply voltages.
2. Data from Los Alamos Neutron Science Center (LANSCE).
3. Spartan-6 and UltraScale+ FPGA alpha data is based on alpha foil testing and package alpha emissivity of 0.001 counts/cm^2/hr. Virtex-6, 7 series, and UltraScale FPGA alpha data is estimated using real-time underground cave testing.
4. One FIT equals 1 failure per 1 billion device hours. Mb = 1e6 memory bits.
5. Data compiled from Rosetta experiment which includes upsets from neutron, proton, and thermal neutron secondaries. Based on experimental methodology, upsets from alpha particles are not included. Modeling of the total SEU rate in terrestrial environments requires use of alpha particle data in addition to real-time data. Xilinx advises use of the SEU Estimator tool to model total SEU rates.
6. 90% confidence interval.
7. Soft error rates (in FIT/Mb) are determined from real-time (system level) measurements in various locations and altitudes and corrected for New York City, according to JESD89A/89-1A.

Table 21: **Experimental Beam Testing and Real-Time Soft Error Rates for URAM[1]**

Tech Node	Product Family	LANSCE Neutrons Cross-Section per Bit[2]		FIT/Mb[3, 5] (Thermal Neutrons)		FIT/Mb (Alpha Particle)[4, 5]		FIT/Mb (Real-Time Soft Error Rate Per Event)[2, 5, 7]	
		URAM	Error	URAM	Error[6]	URAM	Error[6]	URAM	Error
16 nm	UltraScale+	8.06×10^{-16}	±20%	4.1	±50%	6.2	±20%	10.2	±20%

Notes:

1. Experiments are performed at ambient temperature with typical power supply voltages.
2. Data from Los Alamos Neutron Science Center (LANSCE).
3. Estimate based on BRAM/URAM neutron ratio.
4. UltraScale+ FPGA alpha data is based on alpha foil testing and package alpha emissivity of 0.001 counts/cm^2/hr.
5. One FIT equals 1 failure per 1 billion device hours. Mb = 1e6 memory bits.
6. 90% confidence interval.
7. Soft error rates (in FIT/Mb) are determined from real-time (system level) measurements in various locations and altitudes and corrected for New York City, according to JESD89A/89-1A.

Results by Product Family

FPGA Products

High-Temperature Operating Life (HTOL) Test

The HTOL test is conducted under the conditions of $T_J \geq 125°C$ temperature, maximum V_{DD} and either dynamic or static operation. The FIT failure rate calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level (CL).

Summary

Table 22: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC2Sxxx	12	0	484	925,079	1,040,291	11
XC2VPxxx	7	0	314	605,545	1,462,448	8
XC3Sxxx	10	0	445	802,610	1,018,021	12
XC3SxxxE	9	0	435	742,485	1,010,057	12
XC3SxxxA	8	0	359	696,082	1,075,977	11
XC3SxxxAN	10	0	656	793,753	1,072,137	11
XC3SDxxxA	7	0	293	565,731	1,020,659	12
XC4VxXxxx	6	0	270	544,500	1,002,226	12
XC5VxXxxx	7	0	309	506,524	1,175,529	10
XCE4VxXxxx	9	0	402	583,597	1,234,781	10
XC6Sxxx	8	0	359	673,450	1,152,629	10
XC6VxXxxx	7	0	314	516,000	1,082,906	11
7 series FPGAs and Zynq-7000 SoCs	9	0	403	806,000	1,038,272	11
UltraScale devices	10	0	444	626,772	1,089,902	11
UltraScale+ devices	10	0	371	587,000	1,121,613	10

Data

Table 23: **HTOL Test Results for 220/180 nm Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC2S100	7	0	315	585,855	660,323	11
XC2S150	3	0	81	162,162	172,345	
XC2S30	1	0	45	90,000	100,498	
XC2S50	1	0	43	86,387	93,972	
XC2Sxxx	12	0	484	924,404	1,027,138	

Table 24: **HTOL Test Results for 130 nm Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC2VP40	7	0	314	605,545	1,462,448	8
XC2VPxxx	7	0	314	605,545	1,462,448	

Table 25: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC3S1000	4	0	180	361,080	463,500	12
XC3S1500	2	0	90	135,495	180,261	
XC3S400	4	0	175	306,035	374,260	
XC3Sxxx	10	0	445	802,610	1,018,021	

Table 26: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC3S1600E	3	0	167	245,605	366,995	12
XC3S250E	2	0	90	183,060	221,125	
XC3S500E	4	0	178	313,820	421,937	
XC3SxxxE	9	0	435	742,485	1,010,057	

Table 27: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC3S1400A	8	0	359	696,082	1,075,977	11
XC3SxxxA	8	0	359	696,082	1,075,977	

Table 28: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC3S1400AN	7	0	416	553,753	787,200	11
XC3S700AN	3	0	240	240,000	284,937	
XC3SxxxAN	10	0	656	793,753	1,072,137	

Table 29: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC3SD1800A	2	0	90	180,135	277,026	12
XC3SD3400A	5	0	203	385,596	743,633	
XC3SDxxxA	7	0	293	565,731	1,020,659	

Table 30: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC4VFX20	2	0	90	182,565	267,185	12
XC4VLX100	1	0	45	90,585	270,878	
XC4VLX15	1	0	45	91,080	114,538	
XC4VLX40	1	0	45	90,090	140,131	
XC4VLX80	1	0	45	90,180	209,494	
XC4VxXxxx	6	0	270	544,500	1,002,226	

Table 31: **HTOL Test Results for 65 nm Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC5VLX110T	7	0	309	506,524	1,175,529	10
XC5VxXxxx	7	0	309	506,524	1,175,529	

Table 32: **HTOL Test Results for 90 nm Si Gate CMOS Device Type XCE4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XCE4VLX40	4	0	177	289,522	461,250	10
XCE4VLX80	5	0	225	294,075	773,531	
XCE4VxXxxx	9	0	402	583,597	1,234,781	

Table 33: **HTOL Test Results for 45 nm Si Gate CMOS Device Type XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC6SLX45T	8	0	359	673,450	1,152,629	10
XC6Sxxx	8	0	359	673,450	1,152,629	

Table 34: **HTOL Test Results for 40 nm Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC6VLX240T	7	0	314	516,000	1,082,906	11
XC6VxXxxx	7	0	314	516,000	1,082,906	

Table 35: **HTOL Test Results for 28 nm Si Gate CMOS Device Type 7 series FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC7K325T	1	0	45	90,000	115,936	11
XC7Z020	8	0	358	716,000	922,336	
7 series FPGAs and Zynq-7000 SoCs	9	0	403	806,000	1,038,272	

Table 36: **HTOL Test Results for 20 nm Si Gate CMOS Device Type UltraScale Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XCKU040	10	0	444	626,772	1,089,902	11
UltraScale devices	10	0	444	626,772	1,089,902	

Table 37: **HTOL Test Results for 16 nm Si Gate CMOS Device Type UltraScale+ Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XCVU35P	1	0	28	28,000	41,980	10
XCZU3EG	3	0	134	223,500	431,660	
XCZU5EV	1	0	42	42,000	81,117	
XCZU9EG	5	0	167	293,500	566,856	
UltraScale+ devices	10	0	371	587,000	1,121,613	

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C and 85% RH and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

The failures listed in the following table are also listed by device with failure analysis results in the footnotes.

Summary

Table 38: **THB Test Results for Si Gate CMOS Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3Sxxx	2	0	85	85,000
XC3SxxxE	11	0	484	703,000
XC5VxXxxx	2	0	87	108,500
XC6VxXxxx	5	0	159	193,500
7 series FPGAs and Zynq-7000 SoCs	2	0	90	135,000
UltraScale devices	18	0	612	721,584
UltraScale+ devices	13	0	551	786,684

Data

Table 39: **THB Test Results for Si Gate CMOS Devices XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S400	2	0	85	85,000
XC3Sxxx	2	0	85	85,000

Table 40: **THB Test Results for Si Gate CMOS Devices XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1200E	3	0	132	264,000
XC3S250E	8	0	352	439,000
XC3SxxxE	11	0	484	703,000

Table 41: **THB Test Results for Si Gate CMOS Devices XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX110T	2	0	87	108,500
XC5VxXxxx	2	0	87	108,500

Table 42: **THB Test Results for Si Gate CMOS Devices XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VHX565T	2	0	25	37,500
XC6VLX240T	3	0	134	156,000
XC6VxXxxx	5	0	159	193,500

Table 43: **THB Test Results for Si Gate CMOS Devices 7 series FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7S25	1	0	45	67,500
XC7S50	1	0	45	67,500
7 series FPGAs and Zynq-7000 SoCs	2	0	90	135,000

Table 44: **THB Test Results for Si Gate CMOS Devices UltraScale Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCKU040	8	0	299	350,608
XCKU115	7	0	234	272,346
XCVU190	3	0	79	98,630
UltraScale devices	18	0	612	721,584

Table 45: **THB Test Results for Si Gate CMOS Devices UltraScale+ Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCVU37P	1	0	24	24,264
XCZU3EG	5	0	222	361,500
XCZU5EV	1	0	35	40,740
XCZU9EG	6	0	270	360,180
UltraScale+ devices	13	0	551	786,684

Temperature Cycling Test

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 46: **Summary of Temperature Cycling Test Test Results**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3Sxxx	TCB	4	0	165	229,000
XC3SxxxE	TCB	11	0	450	692,000
XC3SxxxA	TCB	4	0	164	211,500
XC5VxXxxx	TCB	4	0	180	295,560
XC6Sxxx	TCB	7	0	241	462,000
XC6VxXxxx	TCB	7	0	227	304,500
7 series FPGAs and Zynq-7000 SoCs	TCB	9	0	368	588,500
UltraScale devices	TCB, TCG	16	0	713	1,074,900
UltraScale+ devices	TCB, TCG	24	0	998	1,636,500

Data

Table 47: **Summary of Temperature Cycling Test Results XC3Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S1000	TCB	1	0	40	60,000
XC3S400	TCB	3	0	125	169,000
XC3Sxxx	TCB	4	0	165	229,000

Table 48: **Summary of Temperature Cycling Test Results XC3SxxxE**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S1200E	TCB	3	0	120	242,000
XC3S250E	TCB	8	0	330	450,000
XC3SxxxE	TCB	11	0	450	692,000

Table 49: **Summary of Temperature Cycling Test Results XC3SxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S200A	TCB	4	0	164	211,500
XC3SxxxA	TCB	4	0	164	211,500

Table 50: **Summary of Temperature Cycling Test Results XC5VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC5VLX110T	TCB	4	0	180	295,560
XC5VxXxxx	TCB	4	0	180	295,560

Table 51: **Summary of Temperature Cycling Test Results XC6Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6SLX150T	TCB	3	0	81	162,000
XC6SLX45T	TCB	4	0	160	300,000
XC6Sxxx	TCB	7	0	241	462,000

Table 52: **Summary of Temperature Cycling Test Results XC6VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6VHX565T	TCB	3	0	47	70,500
XC6VLX240T	TCB	4	0	180	234,000
XC6VxXxxx	TCB	7	0	227	304,500

Table 53: **Summary of Temperature Cycling Test Results 7 series FPGAs**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC7A100T	TCB	3	0	125	165,000
XC7K325T	TCB	1	0	45	67,500
XC7S25	TCB	1	0	40	60,000
XC7S50	TCB	1	0	40	60,000
XC7Z020	TCB	3	0	118	236,000
7 series FPGAs and Zynq-7000 SoCs	TCB	9	0	368	588,500

Table 54: **Summary of Temperature Cycling Test Results UltraScale Devices**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCKU040	TCB	7	0	315	459,000
XCKU115	TCG	3	0	133	209,100
XCVU095	TCB	6	0	265	406,800
UltraScale devices	TCB, TCG	16	0	713	1,074,900

Table 55: **Summary of Temperature Cycling Test Results UltraScale+ Devices**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCVU13P	TCG	2	0	68	102,000
XCVU37P	TCG	3	0	80	80,000
XCZU3EG	TCB	7	0	314	628,000
XCZU5EV	TCB	1	0	45	90,000
XCZU7EV	TCB	1	0	45	67,500
XCZU9EG	TCB	10	0	446	669,000
UltraScale+ devices	TCB, TCG	24	0	998	1,636,500

High Accelerated Stress Test

The HAST test is conducted under the conditions of 130°C, 85% RH and V_{DD} bias or 110°C, 85% RH and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the HAST test.

Summary

Table 56: **Summary of High Accelerated Stress Test Test Results**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3SxxxA	110°C / 85%RH	4	0	180	71,280
XC6Sxxx	110°C / 85%RH	4	0	180	95,040
7 series FPGAs and Zynq-7000 SoCs	110°C / 85%RH, 85°C / 85%RH	7	1	330	156,720

Data

Table 57: **Summary of HAST Test Results XC3SxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S200A	110°C / 85%RH	4	0	180	71,280
XC3SxxxA	110°C / 85%RH	4	0	180	71,280

Table 58: **Summary of HAST Test Results XC6Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6SLX45T	110°C / 85%RH	4	0	180	95,040
XC6Sxxx	110°C / 85%RH	4	0	180	95,040

Table 59: **Summary of HAST Test Results 7 series FPGAs**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC7A100T	110°C / 85%RH, 85°C / 85%RH	4	1[1]	195	85,440
XC7Z020	110°C / 85%RH	3	0	135	71,280
7 series FPGAs and Zynq-7000 SoCs	110°C / 85%RH, 85°C / 85%RH	7	1	330	156,720

Notes:

1. One unit failed due to substrate copper residues. A corrective action is in place.

High Temperature Storage Life

The High-Temperature Storage Life test is conducted under the conditions of 150°C and with the device unbiased.

Summary

Table 60: **Summary of High Temperature Storage Life Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3Sxxx	4	0	180	225,000
XC3SxxxE	11	0	494	719,000
XC3SxxxA	4	0	180	225,000
XC5VxXxxx	4	0	179	246,500
XC6Sxxx	6	0	233	395,000
XC6VxXxxx	7	0	202	303,000
7 series FPGAs and Zynq-7000 SoCs	8	0	357	581,000
UltraScale devices	14	0	500	785,000
UltraScale+ devices	18	1	719	1,183,500

Data

Table 61: **Summary of High-Temperature Storage Life Test Results XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1000	1	0	45	45,000
XC3S400	3	0	135	180,000
XC3Sxxx	4	0	180	225,000

Table 62: **Summary of High-Temperature Storage Life Test Results XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1200E	4	0	179	314,000
XC3S250E	7	0	315	405,000
XC3SxxxE	11	0	494	719,000

Table 63: **Summary of High-Temperature Storage Life Test Results XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200A	4	0	180	225,000
XC3SxxxA	4	0	180	225,000

Table 64: **Summary of High-Temperature Storage Life Test Results XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX110T	4	0	179	246,500
XC5VxXxxx	4	0	179	246,500

Table 65: **Summary of High-Temperature Storage Life Test Results XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6SLX150T	2	0	54	81,000
XC6SLX45T	4	0	179	314,000
XC6Sxxx	6	0	233	395,000

Table 66: **Summary of High-Temperature Storage Life Test Results XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VHX565T	4	0	68	102,000
XC6VLX240T	3	0	134	201,000
XC6VxXxxx	7	0	202	303,000

Table 67: **Summary of High-Temperature Storage Life Test Results 7 series FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7A100T	3	0	133	177,500
XC7S25	1	0	44	66,000
XC7S50	1	0	45	67,500
XC7Z020	3	0	135	270,000
7 series FPGAs and Zynq-7000 SoCs	8	0	357	581,000

Table 68: **Summary of High-Temperature Storage Life Test Results UltraScale Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCKU040	6	0	270	405,000
XCKU115	8	0	230	380,000
UltraScale devices	14	0	500	785,000

Table 69: **Summary of High-Temperature Storage Life Test Results UltraScale+ Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCVU13P	1	0	44	66,000
XCVU37P	3	0	52	52,000
XCZU3EG	7	0	312	579,000
XCZU5EV	1	1(1)	44	86,000
XCZU9EG	6	0	267	400,500
UltraScale+ devices	18	1	719	1,183,500

Notes:

1. One unit failed due to abnormal substrate via shape issue. A corrective action is in place.

Flash PROM Products

High-Temperature Operating Life (HTOL) Test

The HTOL test is conducted under the conditions of $T_J \geq 125°C$ temperature, maximum V_{DD}, and either dynamic or static operation. The FIT failure rate calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level (CL).

Summary

Table 70: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC18Vxxx	3	0	167	337,291	356,425	33

Data

Table 71: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XC18Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC18V01	1	0	77	154,231	164,637	33
XC18V04	1	0	45	92,835	99,755	
XC18V512	1	0	45	90,225	92,033	
XC18Vxxx	3	0	167	337,291	356,425	

CPLD Products

High-Temperature Operating Life (HTOL) Test

The HTOL test is conducted under the conditions of $T_J \geq 125°C$ temperature, maximum V_{DD}, and either dynamic or static operation. The FIT calculations in Table 41 through Table 43 are based on the assumption of 0.7 eV activation energy and 60% confidence level.

Summary

Table 72: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC95xxxXL	13	0	542	1,048,447	1,143,653	10
XCRxxxXL	12	0	538	1,012,585	1,014,559	12
XC2Cxxx/A	12	0	539	1,079,573	1,084,504	11

Data

Table 73: **HTOL Test Results for 0.35 µm Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC95144XL	2	0	87	175,442	308,284	10
XC9572XL	11	0	455	873,005	835,369	
XC95xxxXL	13	0	542	1,048,447	1,143,653	

Table 74: **HTOL Test Results for 0.35 µm Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XCR3064XL	1	0	45	22,500	22,738	12
XCR3128XL	3	0	135	270,855	271,487	
XCR3256XL	4	0	176	352,540	353,286	
XCR3384XL	3	0	134	270,114	270,472	
XCR3512XL	1	0	48	96,576	96,576	
XCRxxxXL	12	0	538	1,012,585	1,014,559	

Table 75: **HTOL Test Results for 0.35 µm Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and TJ = 55°C (FIT)
XC2C128	10	0	449	899,573	904,504	11
XC2C64A	2	0	90	180,000	180,000	
XC2Cxxx/A	12	0	539	1,079,573	1,084,504	

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C, 85% RH, and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test

Summary

Table 76: **Summary of THB Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95xxxXL	3	0	135	225,000
XC2Cxxx/A	2	0	88	176,000

Data

Table 77: **THB Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9572XL	3	0	135	225,000
XC95xxxXL	3	0	135	225,000

Table 78: **THB Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C64A	2	0	88	176,000
XC2Cxxx/A	2	0	88	176,000

Temperature Cycling Test

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test

Summary

Table 79: **Summary of Temperature Cycling Test Results**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95xxxXL	TCB	3	0	125	214,000
XC2Cxxx/A	TCB	4	0	160	280,000

Data

Table 80: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC9572XL	TCB	3	0	125	214,000
XC95xxxXL	TCB	3	0	125	214,000

Table 81: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2C256	TCB	2	0	80	120,000
XC2C64A	TCB	2	0	80	160,000
XC2Cxxx/A	TCB	4	0	160	280,000

Data Retention Bake Test

The Data Retention Bake Test is conducted at 150°C. The devices are programmed prior to the bake test

Summary

Table 82: **Summary of Data Retention Bake Test Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95xxxXL	3	0	134	268,000
XC2Cxxx/A	4	0	180	315,000

Data

Table 83: **Data Retention Bake Test XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9572XL	3	0	134	268,000
XC95xxxXL	3	0	134	268,000

Table 84: **Data Retention Bake Test XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C256	2	0	90	135,000
XC2C64A	2	0	90	180,000
XC2Cxxx/A	4	0	180	315,000

Chapter 3

Results by Package Type

Reliability Data for Non-Hermetic Packages

FF1136, FF1148, FF1152, FF1156, FF1157, and FF1158

Table 85: **Test Results for Device Type XC2VP40, XC5VLX110T, XC6VLX240T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	8	0	360	529,560
HTS	7	0	313	447,500
THB 85°C, 85% RH with bias	5	0	221	264,500

FG324, FG456, and FG484

Table 86: **Test Results for Device Type XC2VP2, XC2VP4, XC3S1000, XC3S1400A, XC3S1500, XC3S1600E, XC3S2000, XC3S400, XC3S700A, XC3S700AN, XC6SLX150T, XC6SLX45T, XC7A100T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HAST	8	1 [(1)]	375	180,480
Temperature cycling –55°C to +125°C	11	0	406	691,000
HTS	10	0	413	620,000
THB	2	0	85	85,000
Temperature humidity	1	0	45	45,000

Notes:

1. One unit failed due to substrate copper residues. A corrective action is in place.

Reliability Data for Hermetic Packages

Reliability Data for PGA Packages

Table 87: **Tests of Package Type PG223**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	15	0	
B3	Solderability	15	0	
B5	Bond strength	24	0	
D1	Physical dimension	30	0	
D2	Lead integrity	30	0	
	Seal			
D3	Thermal shock	30	0	450
	Temperature cycle			
	Seal			
	Visual examination			
	End-point electrical			
	Parametrics			
D4	Mechanical	30	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			
D5	Salt atmosphere	30	0	
	Seal			
	Visual examination			
D6	Internal water-vapor content	30	0	
D7	Adhesion of lead finish	30	0	
D8	Lid torque	30	0	

Reliability Data for CB Packages

Table 88: **Tests of Package Type CB228**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	48	0	
B3	Solderability	27	0	
B5	Bond strength	36	0	
D1	Physical dimension	60	0	
D2	Lead integrity	60	0	
	Seal			
D3	Thermal shock	60	0	
	Temperature cycle			
	Seal			
	Visual examination			
	End-point electrical			
	Parametrics			
D4	Mechanical	60	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			
D5	Salt atmosphere	60	0	
	Seal			
	Visual examination			
D6	Internal water-vapor content	60	0	
D7	Adhesion of lead finish	60	0	
D8-LID	Lid torque	30	0	
HTOL	Life Test	45	0	

Reliability Data for CF1144 Package

Table 89: **Tests of Package Type CF1144**

Code	Test	Sample Quantity	Failures	Total Device Cycles
D3	Thermal shock	15	0	225
	Parametrics			
D4	Mechanical	15	0	
	High temperature storage	22		2,112
	Temperature cycling 65 to +155°C	15		1,500
	HAST (130°C, 85% RH)	18	0	1,728
TCB	Temperature cycling –55 to +125°C	14	0	28,260

Reliability Data for CG717 Package

Table 90: **Tests of Package Type CG717**

Code	Test	Sample Quantity	Failures	Total Device Cycles
	Thermal shock	15	0	225
	Mechanical shock	15	0	
	Vibration	15	0	225
	High temperature storage	22	0	2,112
	Temperature cycling 65 to +155°C	15	0	1,500
	HTOL	44	0	44,000

Reliability Data for Pb-Free Packages

CLG400 and CLG484

Table 91: **Test Results for Device Type XC7Z020**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	3	0	118	236,000
HTS	3	0	135	270,000
HAST	3	0	135	71,280

CPG132

Table 92: **Test Results for Device Type XC2C128, XC2C256, XC3S250E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	4	0	165	225,000
HTS	4	0	180	225,000
THB 85°C, 85% RH with bias	4	0	178	222,000

CSG324

Table 93: **Test Results for Device Type XC6SLX16, XC6SLX45, XC7S25, XC7S50**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	2	0	80	120,000
HTS	2	0	89	133,500
THB 85°C, 85% RH with bias	2	0	90	135,000

SFV625

Table 94: **Test Results for Device Type XCZU3EG**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
THB	5	0	222	361,500
Temperature cycling	7	0	314	628,000
HTS	7	0	312	579,000

SFV784

Table 95: **Test Results for Device Type XCZU5EV**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling	1	0	45	90,000
HTS	1	1 (1)	44	86,000
THB	1	0	35	40,740

Notes:

1. One unit failed due to abnormal substrate via shape issue. A corrective action is in place.

FBG900,FBV900

Table 96: **Test Results for Device Type XC7K325T, XCZU7EV**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	2	0	90	135,000

FFG1136, FFG1148, FFG1152, FFG1153, FFG1154, FFG1155, FFG1156, FFG1157, and FFG1158

Table 97: **Test Results for Device Type XC2VP40, XC5VLX110T, XC6VLX240T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	8	0	360	529,560
HTS	7	0	313	447,500
THB 85°C, 85% RH with bias	5	0	221	264,500

FFV900 and FFV901

Table 98: **Test Results for Device Type XCZU9EG**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	6	0	269	403,500

FFV1136, FFV1148, FFV1152, FFV1153, FFV1154, FFV1156, FFV1156, FFV1157, and FFV1158

Table 99: **Test Results for Device Type XCKU040, XCZU9EG**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	11	0	492	724,500
THB	13	0	528	649,288
HTS	12	0	537	805,500

FFV1517, FFV1924, and FFV2104

Table 100: **Test Results for Device Type XCVU095, XCVU3P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling	6	0	265	406,800

FFV1923 and FFV1928

Table 101: **Test Results for Device Type XC6VHX565T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	4	0	68	102,000
THB	2	0	25	37,500
Temperature cycling	3	0	47	70,500

FGG676

Table 102: **Test Results for Device Type XC7A100T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	3	0	125	165,000
HTS	3	0	133	177,500

FHG1761, FHG2104

Table 103: **Test Results for Device Type XC7V2000T, XCVU13P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	67,500
HTS	1	0	44	66,000

FLV1517, FLV1924, and FLV2104

Table 104: **Test Results for Device Type XCKU040, XCKU115, XCVU125, XCVU7P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
THB 85°C, 85% RH with bias	8	0	275	333,846
Temperature cycling –40°C to +125°C	3	0	133	209,100
HTS	8	0	230	380,000

FLG1925, FLG1926, FLG1928, FLG1932, FLG2104, FLG2377, and FLG2892

Table 105: **Test Results for Device Type XC7V2000T, XC7VX1140T, XCVU13P, XCVU190, XCVU440**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
THB 85°C, 85% RH with bias	3	0	79	98,630
Temperature cycling –40°C to +125°C	1	0	23	34,500

FSV2892

Table 106: **Test Results for Device Type XCVU37P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	3	0	52	52,000
Temperature cycling	3	0	80	80,000
THB	1	0	24	24,264

FTG256

Table 107: **Test Results for Device Type XC2C256, XC2S50, XC3S1000, XC3S1200E, XC3S200A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	9	0	364	573,500
HTS	10	0	449	674,000
HAST	4	0	180	71,280
THB 85°C, 85% RH with bias	3	0	132	264,000

TQG44, TQG100, TQG144, TQG160 and TQG176

Table 108: **Test Results for Device Type XC2C256, XC2C384, XC2S100, XC2S30, XC3S400, XC95144XL, XC9572XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	3	0	125	214,000
HTS	3	0	134	268,000

VQG44, VQG64, and VQG100

Table 109: **Test Results for Device Type XC18V512, XC2C128, XC2C64A, XC3S250E, XC9572XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	6	0	245	385,000
HTS	5	0	225	360,000
THB	9	0	397	618,000

XILINX

Chapter 4

Board-Level Reliability Tests

SnPb Eutectic

FG676, FG680, FG900, FG1156, BF957, FF672, FF896, FF1152, FF1704, SF363, and CF1144

Table 110: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8 x 17.8 x 0.3	0.56 thick, 4-layer
FG680	40 x 40	680	1.00	0.60	0.46	SMD	20.3 x 20.3 x 0.3	0.98 thick, 3-layer
FG900	31 x 31	900	1.00	0.60	0.46	SMD	17.0 x 17.0 x 0.3	0.56 thick, 4-layer
FG1156	35 x 35	1,156	1.00	0.60	0.46	SMD	23 x 21 x 0.3	0.56 thick, 4-layer
BF957	40 x 40	957	1.27	0.75	0.61	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FF672	27 x 27	672	1.00	0.60	0.53	SMD	12 x 10 x 0.7	1.152 thick, 6-layer
FF896	31 x 31	896	1.00	0.60	0.53	SMD	10 x 10 x 0.7	1.152 thick, 6-layer
FF1152	35 x 35	1,152	1.00	0.60	0.53	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FF1704	42.5 x 42.5	1,704	1.00	0.60	0.53	SMD	26 x 22 x 0.7	1.152 thick, 6-layer
SF363	17 x 17	363	0.8	0.50	0.40	SMD	10 x 10 x 0.3	0.60 thick, 4-layer
CF1144	35 x 35	1,144	1.00	0.52	0.80	SMD	22 x 20 x 0.7	1.59 thick, 10-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.3622 mm size, HASL finish
- 0.5 mm pad diameter/0.65 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power/GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.1524 mm laser cut stencil, 0.50 mm aperture, alpha metals WS609 paste

Test Condition

- 0°C – 100°C, 10-minutes dwell, 5-minute ramps, 2 cycles/hour

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- OPEN: Resistance of net > threshold resistance (300Ω)
- FAIL: At least 2 opens within one cycle, log 15 failures for each net

Table 111: **Summary of Test Results**

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FG676	7,027	30	30	4,686	6,012
FG680	4,000	30	0	NA	NA
FG900	7,027	28	28	4,405	5,344
FG1156	5,000	32	25	2,786	4,892
BF957	4,145	35	35	1,958	3,662
FF672	5,840	30	30	3,764	4,881
FF896	7,027	12	10	5,607	6,783
FF1152	4,158	30	30	2,668	3,822
SF363 (Lot 1)	2,370	24	21	1,642	2,048
SF363 (Lot 2)	2,288	24	24	1,555	1,999
FF1704	4,150	35	35	3,003	3,389
CF1144	5,000	21	0	NA	NA

Weibull Plots

Figure 1: **Cycles to Failure in the Second-Level Reliability Tests for FG676**

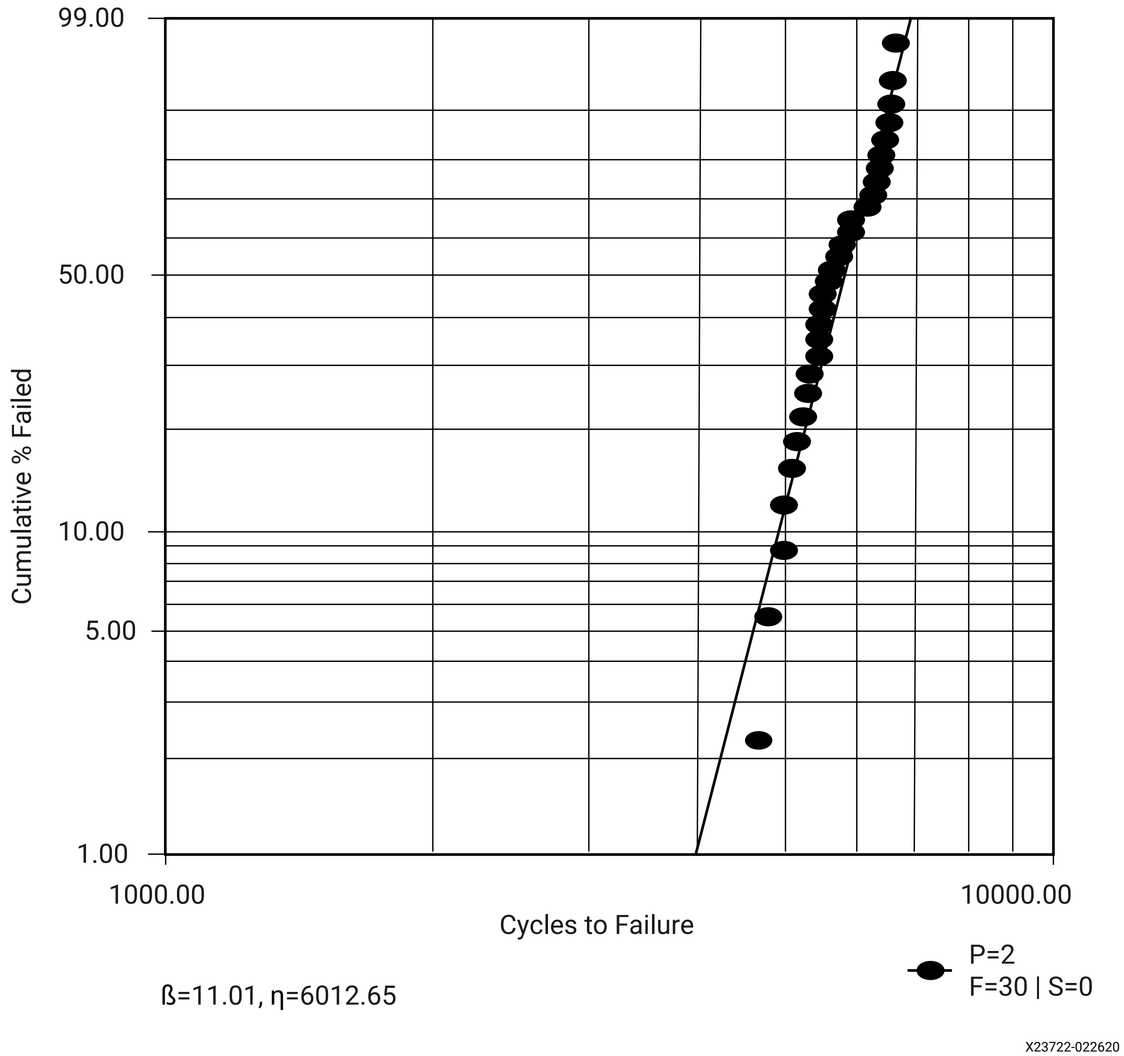


Figure 2: **Cycles to Failure in the Second-Level Reliability Tests for FG900**

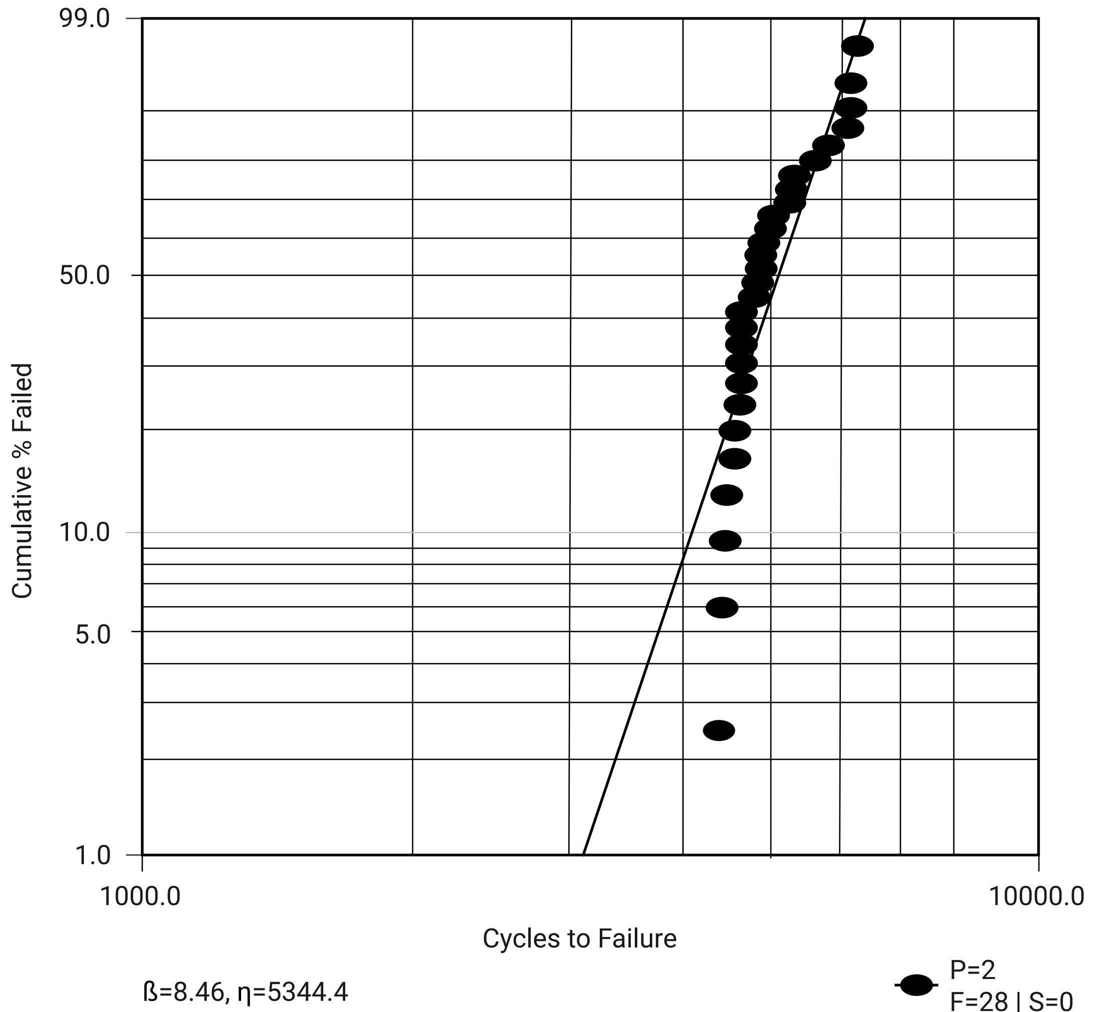


Figure 3: **Cycles to Failure in the Second-Level Reliability Tests for FG1156**

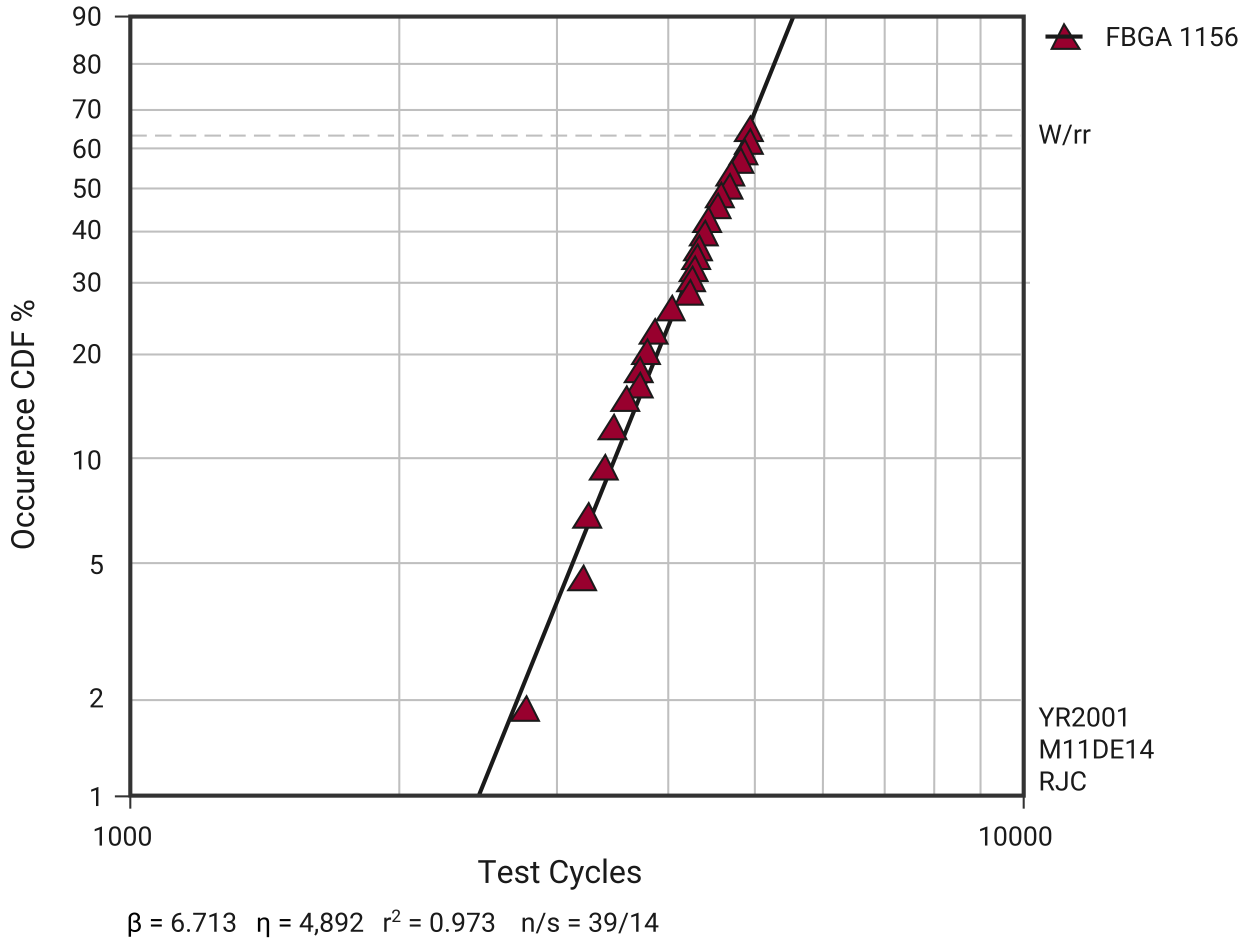


Figure 4: **Cycles to Failure in the Second-Level Reliability Tests for BF957**

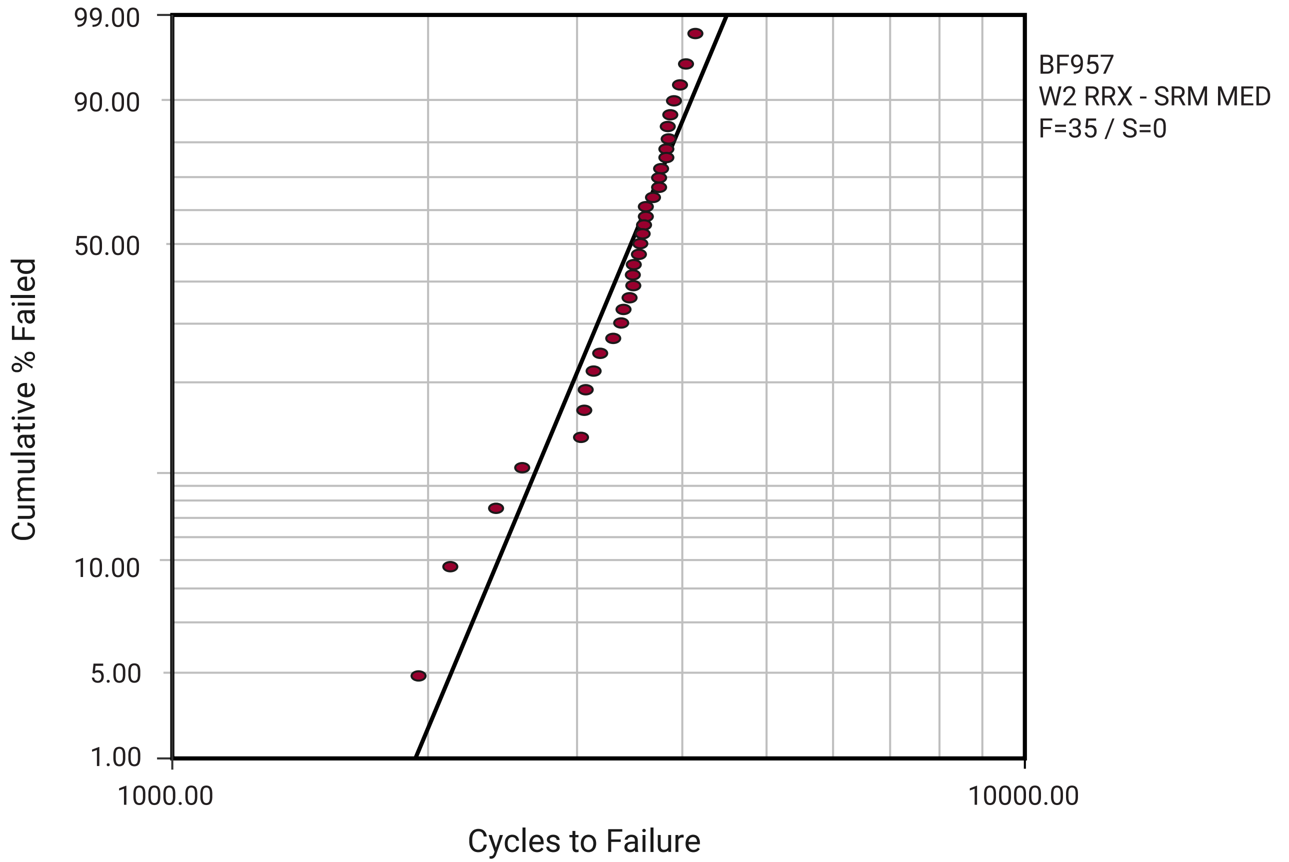


Figure 5: **Cycles to Failure in the Second-Level Reliability Tests for FF672**

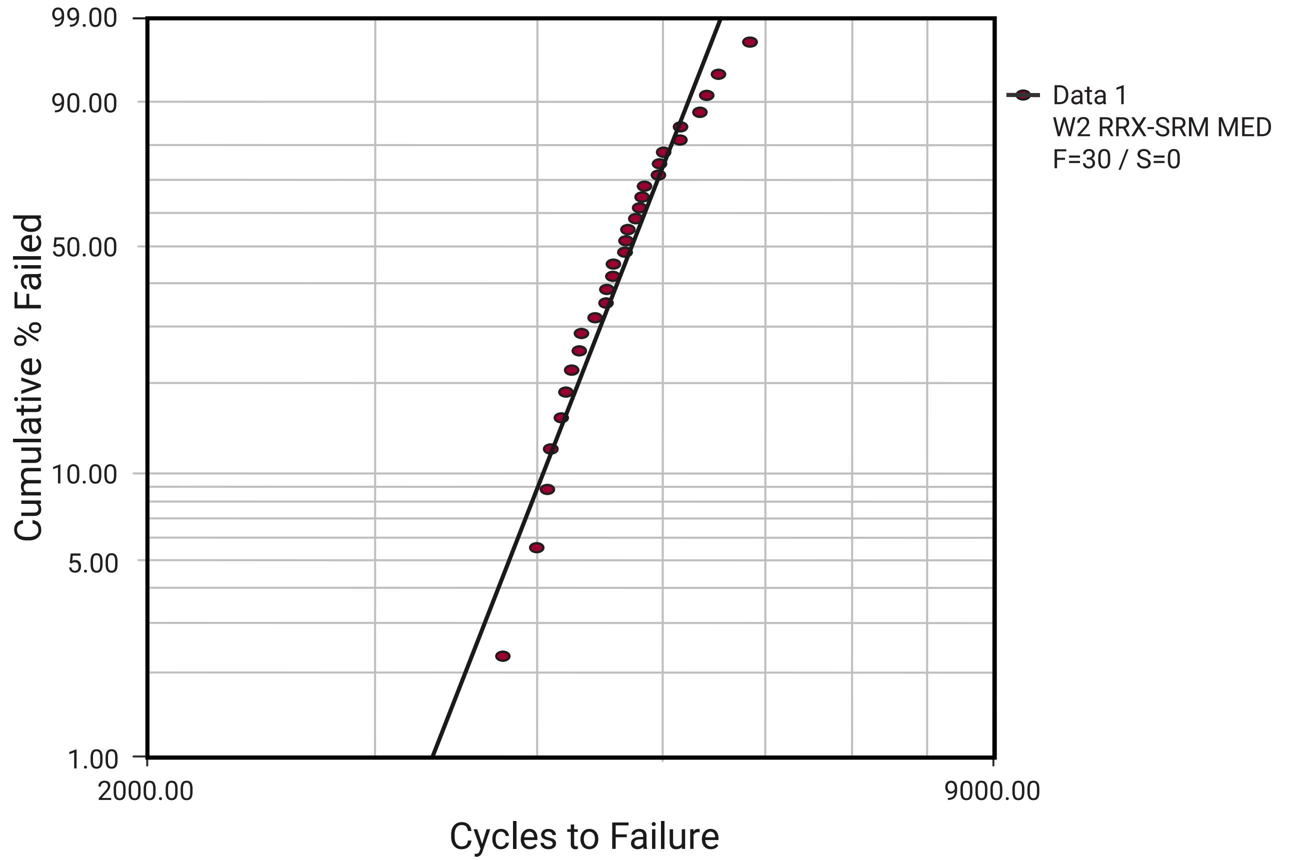


Figure 6: **Cycles to Failure in the Second-Level Reliability Tests for FF896**

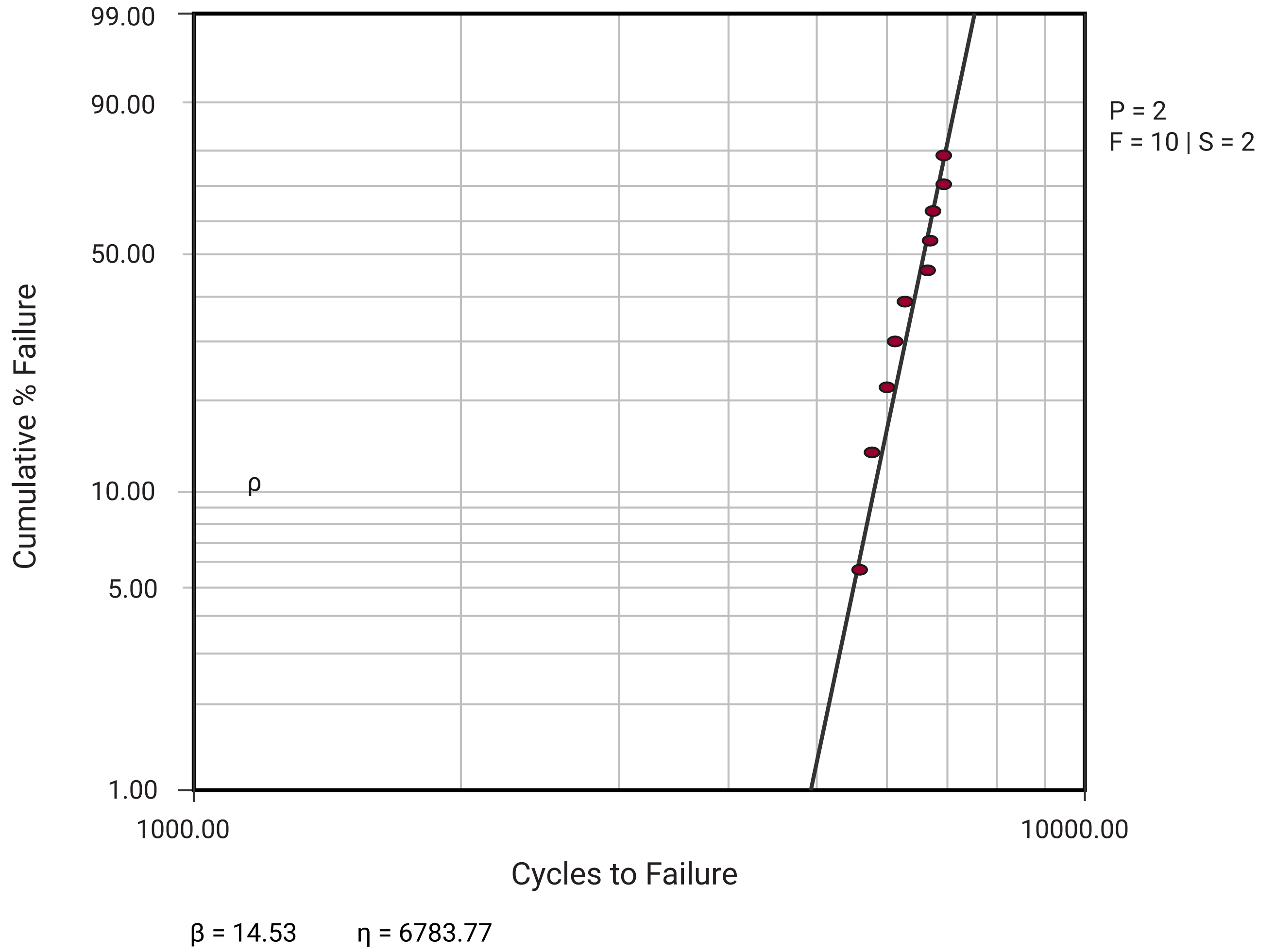


Figure 7: **Cycles to Failure in the Second-Level Reliability Tests for FF1152**

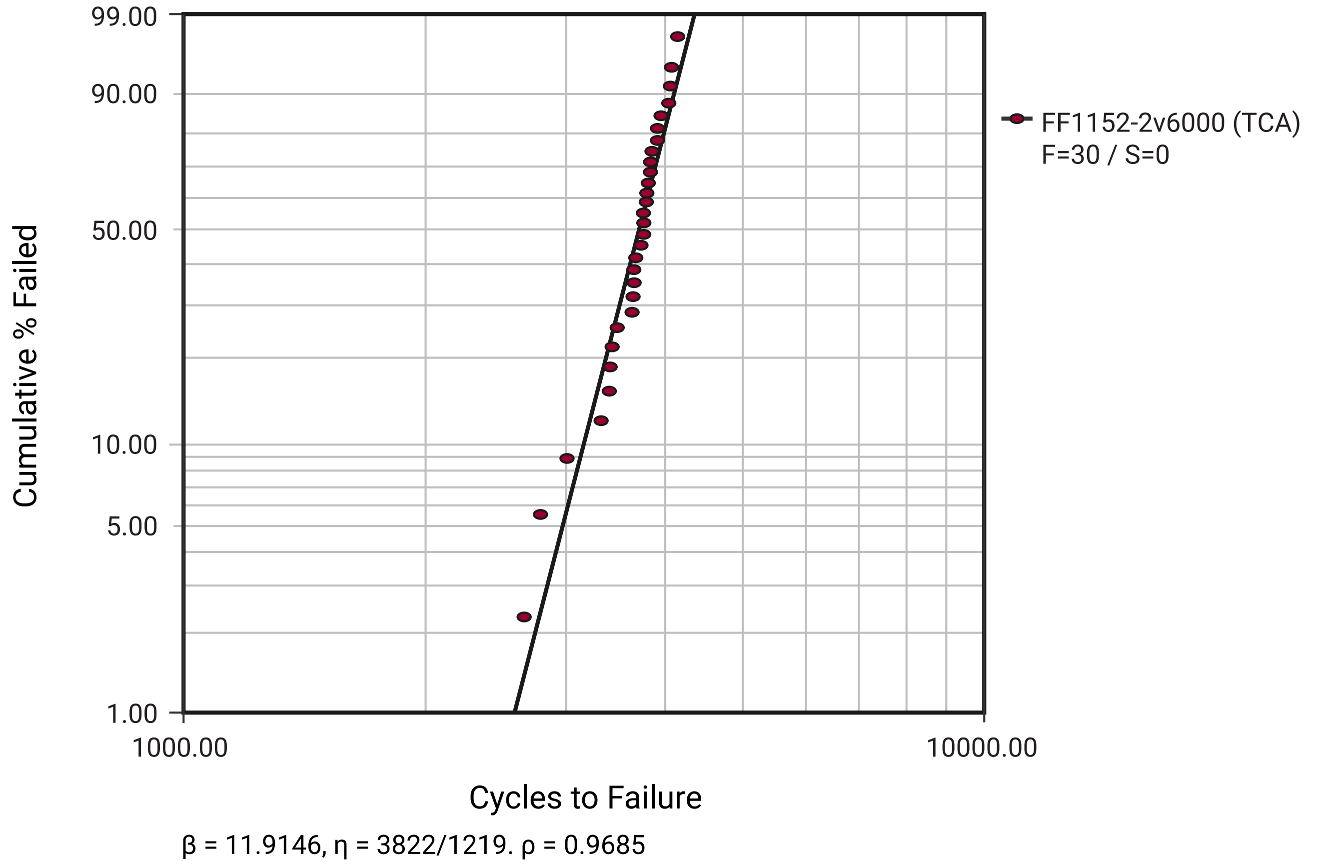


Figure 8: **Cycles to Failure in the Second-Level Reliability Tests for SF363**

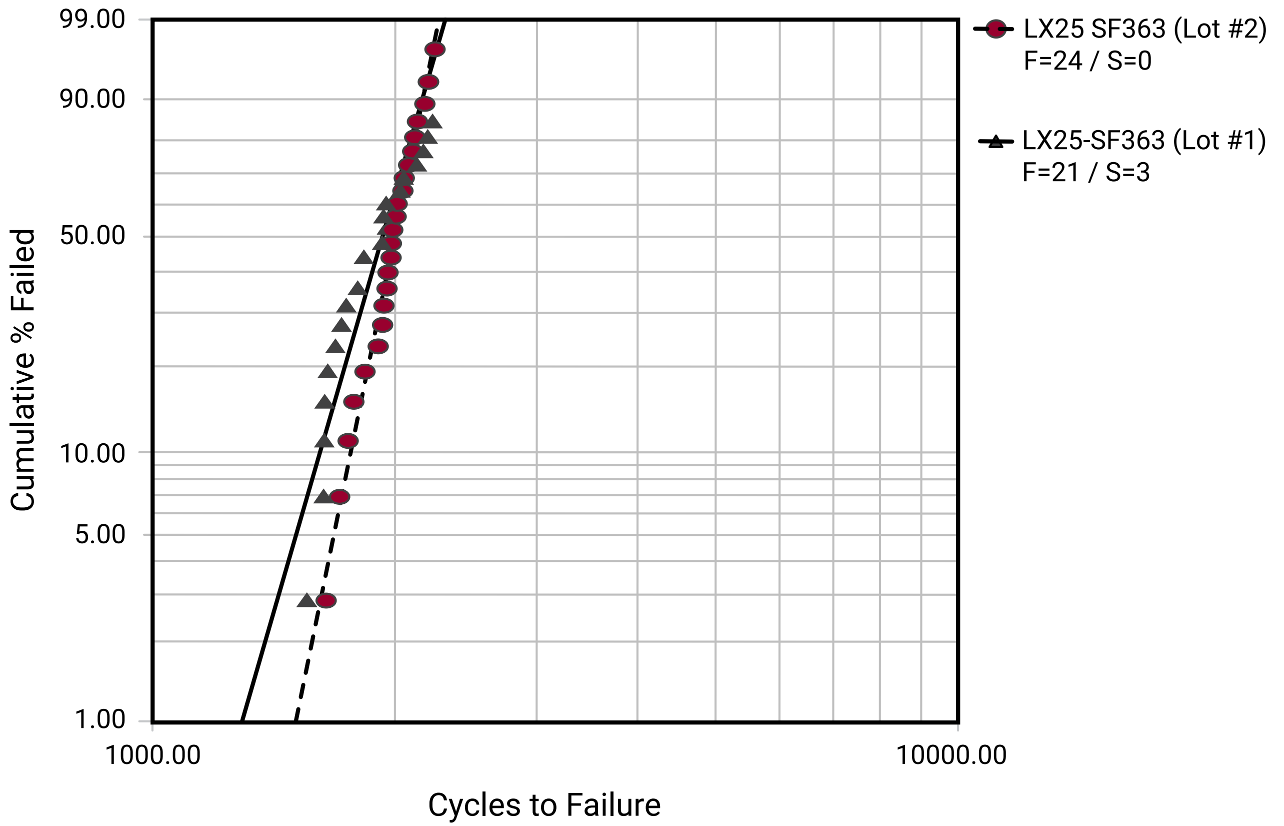
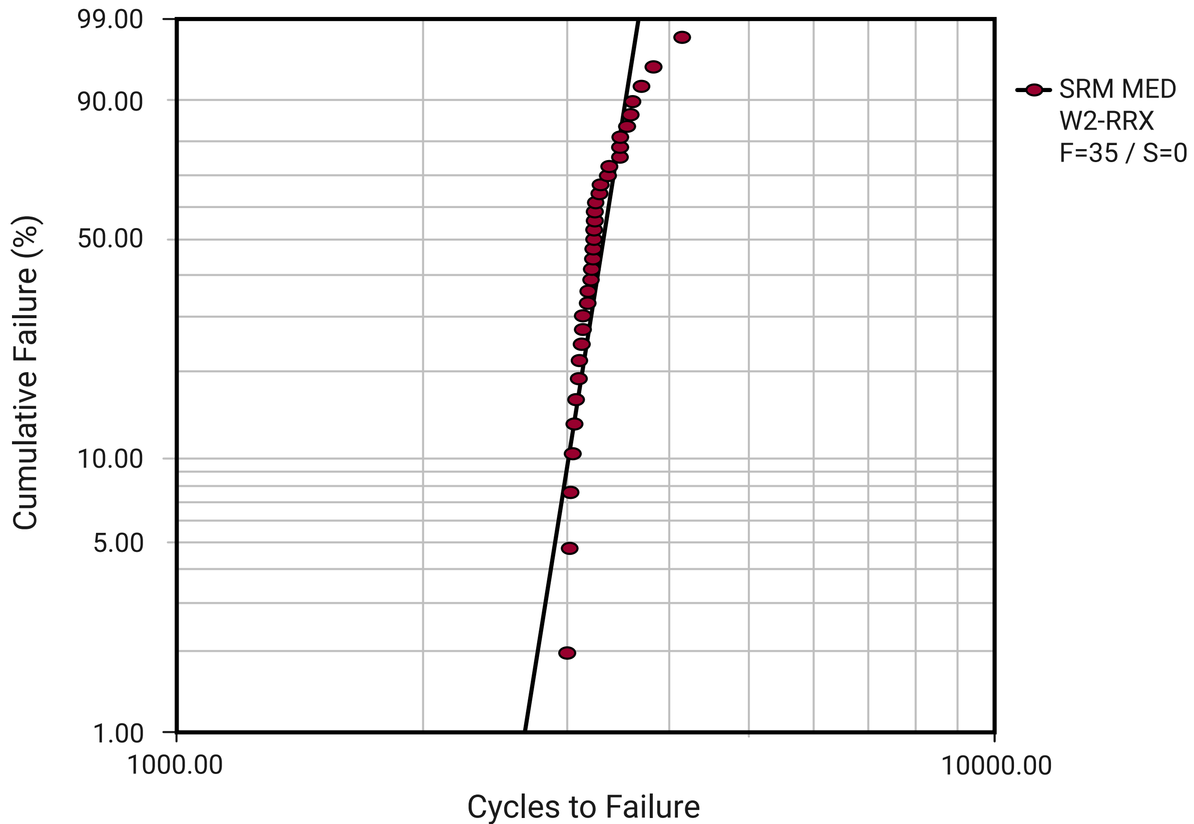


Figure 9: **Cycles to Failure in the Second-Level Reliability Tests for FF1704**



Pb-Free BGA

FGG676, FFG1152, FBVA900, FFVB2104, FLVA1924, SFVA784, and SBVA784

Table 112: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FGG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8 x 17.8 x 0.3	0.56 thick, 4-layer
FFG1704	42.5 x 42.5	1,704	1.00	0.60	0.53	SMD	23 x 23	1.152 thick, 6-layer
FFG1152	35 x 35	1,152	1.00	0.60	0.53	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FBVA900	31 x 31	900	1.00	0.60	0.53	SMD	16.30 x 11.36	1.24 thick, 10-layer

Table 112: **Package Details (All Dimensions in mm)** *(cont'd)*

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FFVB2104	47.5 x 47.5	2104	1.00	0.6	0.53	SMD	18 x 22.5	1.42 thick, 14-layer
FLVA1924	45 x 45	1924	1.00	0.6	0.53	SMD	25 x 31	1.33 thick, 12-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.3622 mm size, OSP finish
- 0.5 mm pad diameter/0.65 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.1524 mm laser cut stencil, 0.50 mm aperture, alpha metals WS609 paste

Test Condition

- FGG676: 0°C – 100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate
- FFG1152: 0°C – 100°C, 10-minute dwells, 5-minute ramps, 2 cycles/hour

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- OPEN: Resistance of net > threshold resistance (300Ω)
- FAIL: At least 2 opens within one cycle, log 15 failures for each net

Table 113: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FGG676	7,027	35	27	4,390	5,974
FFG1704	5,000	32	0	NA	NA
FFG1152	4,640	28	26	3,186	4,121
FBVA900	8,737	32	28	7,181	8,260
FFVB2104	8,568	32	14	5,205	9,351
FLVA1924	4,605	32	25	2,759	4,222

Weibull Plots

Figure 10: **Cycles to Failure in the Second-Level Reliability Tests for FGG676**

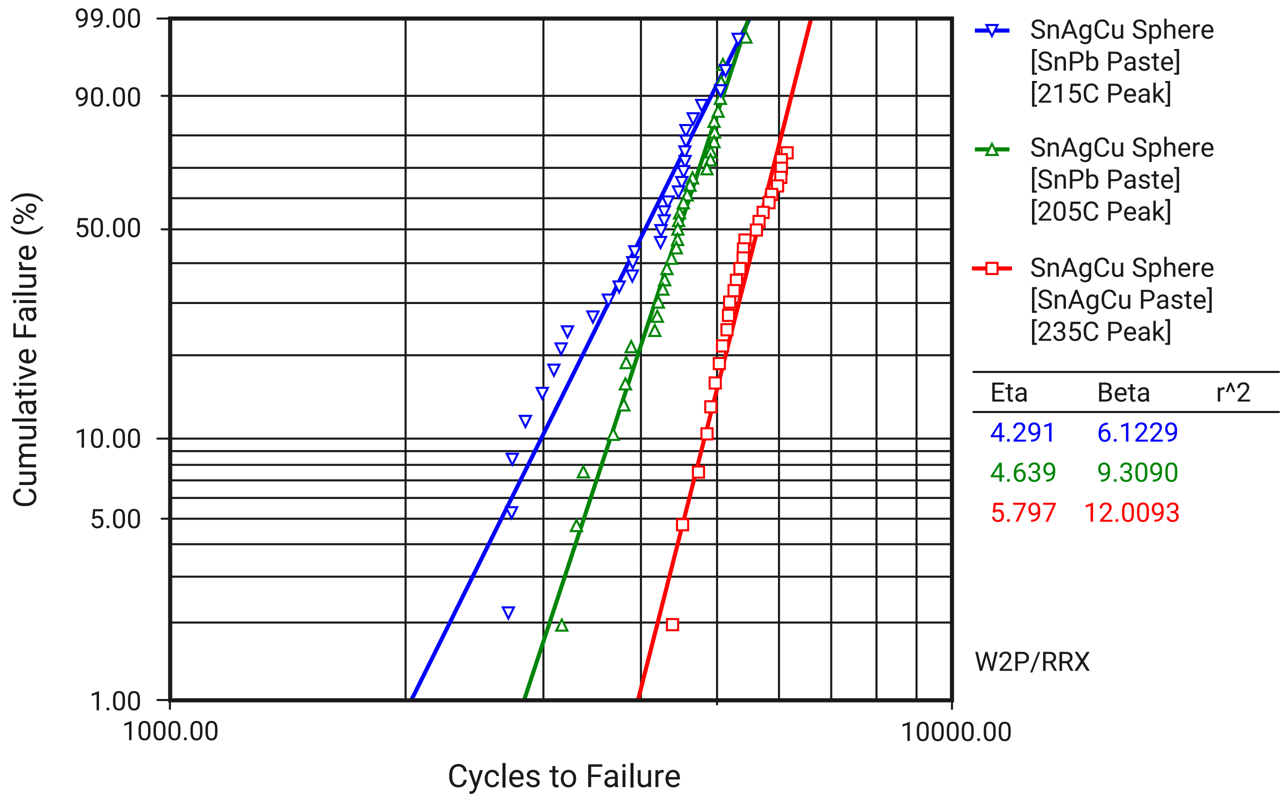
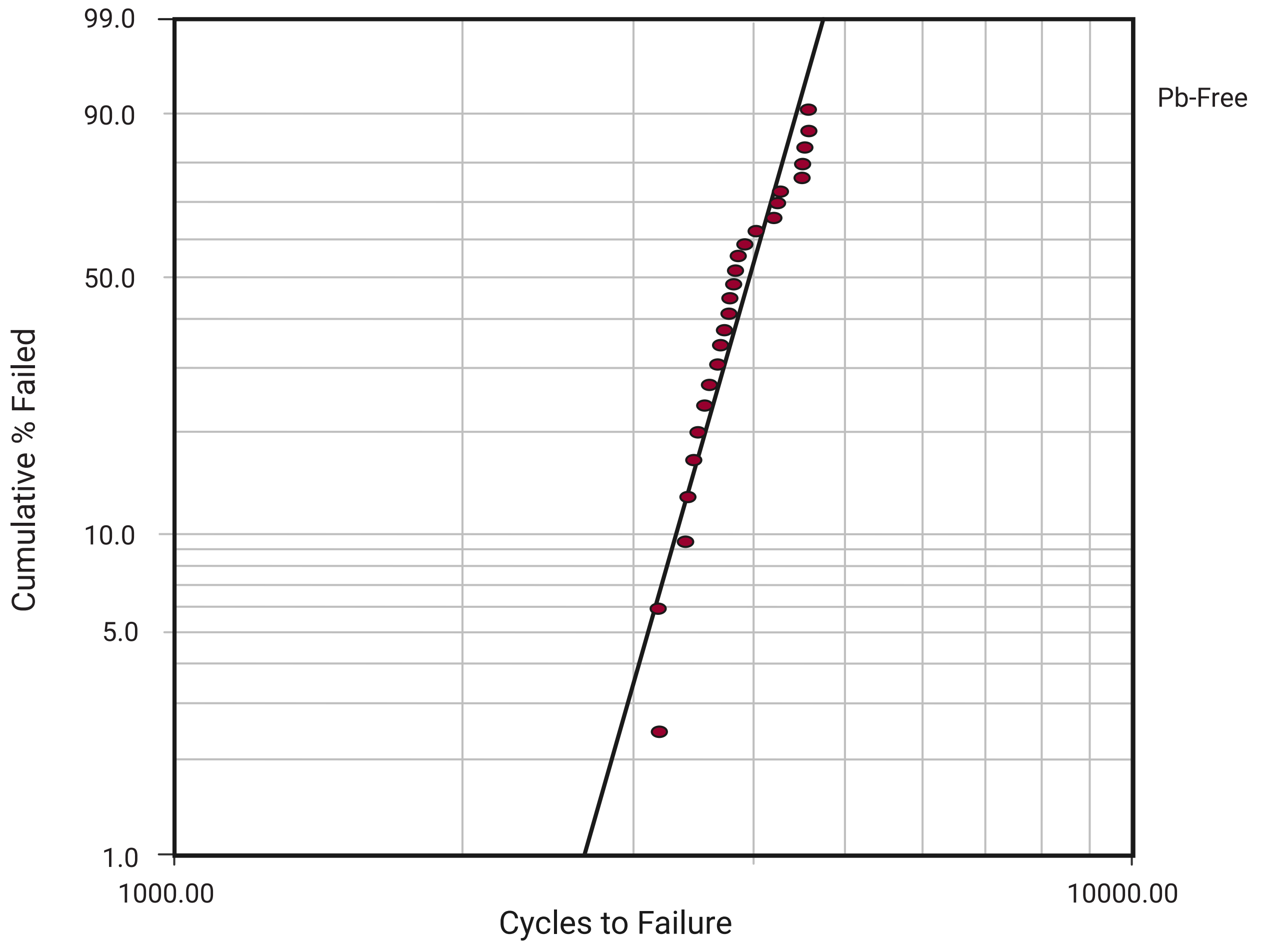


Figure 11: **Cycles to Failure in the Second-Level Reliability Tests for FFG1152**



FBG900

Table 114: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FBG900	31 X 31	900	1.00	0.60	0.53	SMD	12.93 x 16.91	0.95 thick, 8-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.36 mm size, ENIG finish
- 0.45 mm pad diameter/0.55 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.

- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

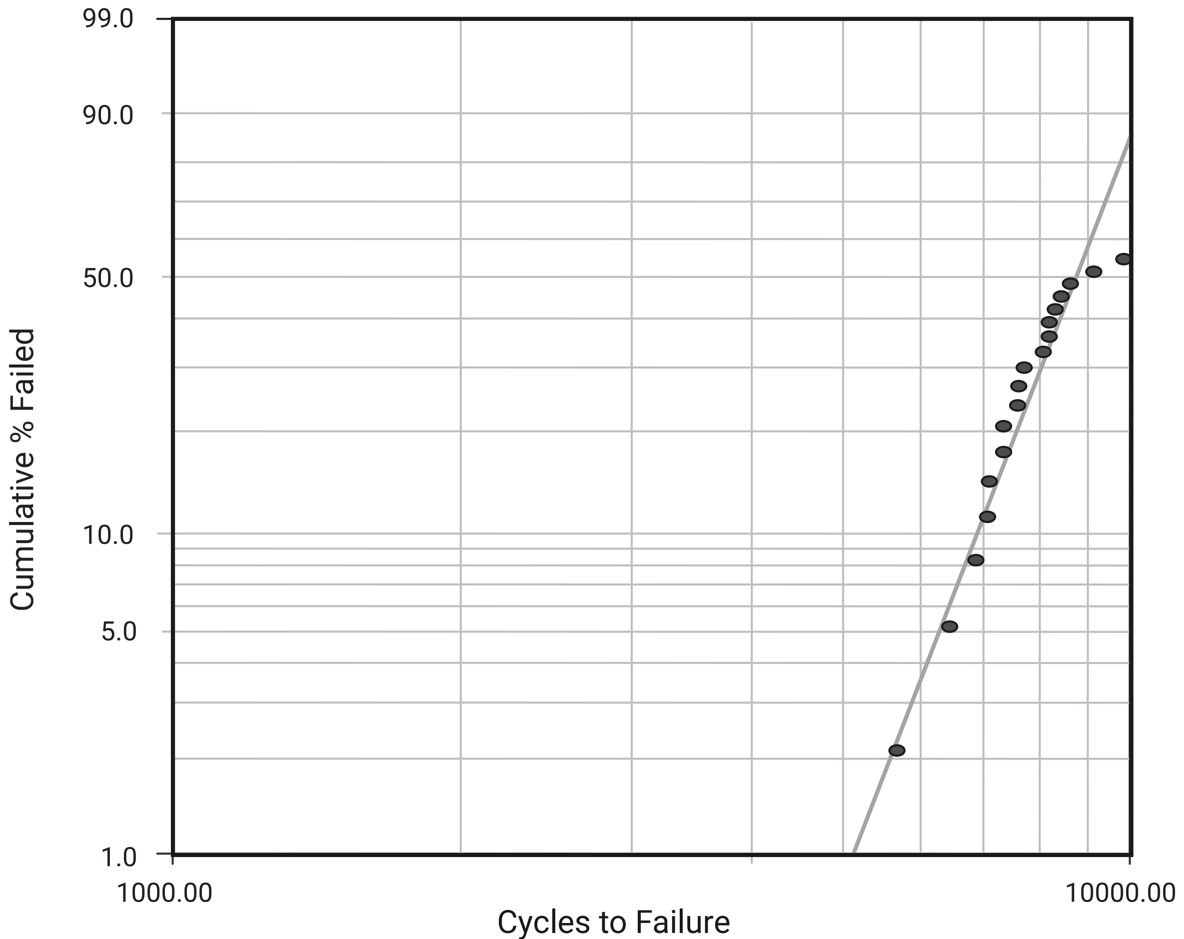
- Continuous scanning of daisy chain nets with event detection
- FAIL: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 115: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FBG900	10,085	32	18	5,674	9,148

Weibull Plots

Figure 12: **Cycles to Failure in the Second-Level Reliability Tests for FBG900**



SBG484

Table 116: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
SBG484	19 X 19	484	0.8	0.50	0.40	SMD	10.82 x 12.04	0.98 thick, 8-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.36 mm size, ENIG finish
- 0.33 mm pad diameter/0.50 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power

- Power, GND layer has 70% metal. Internal signal layer has 40% metal.

Test Condition

- 0°C – 100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

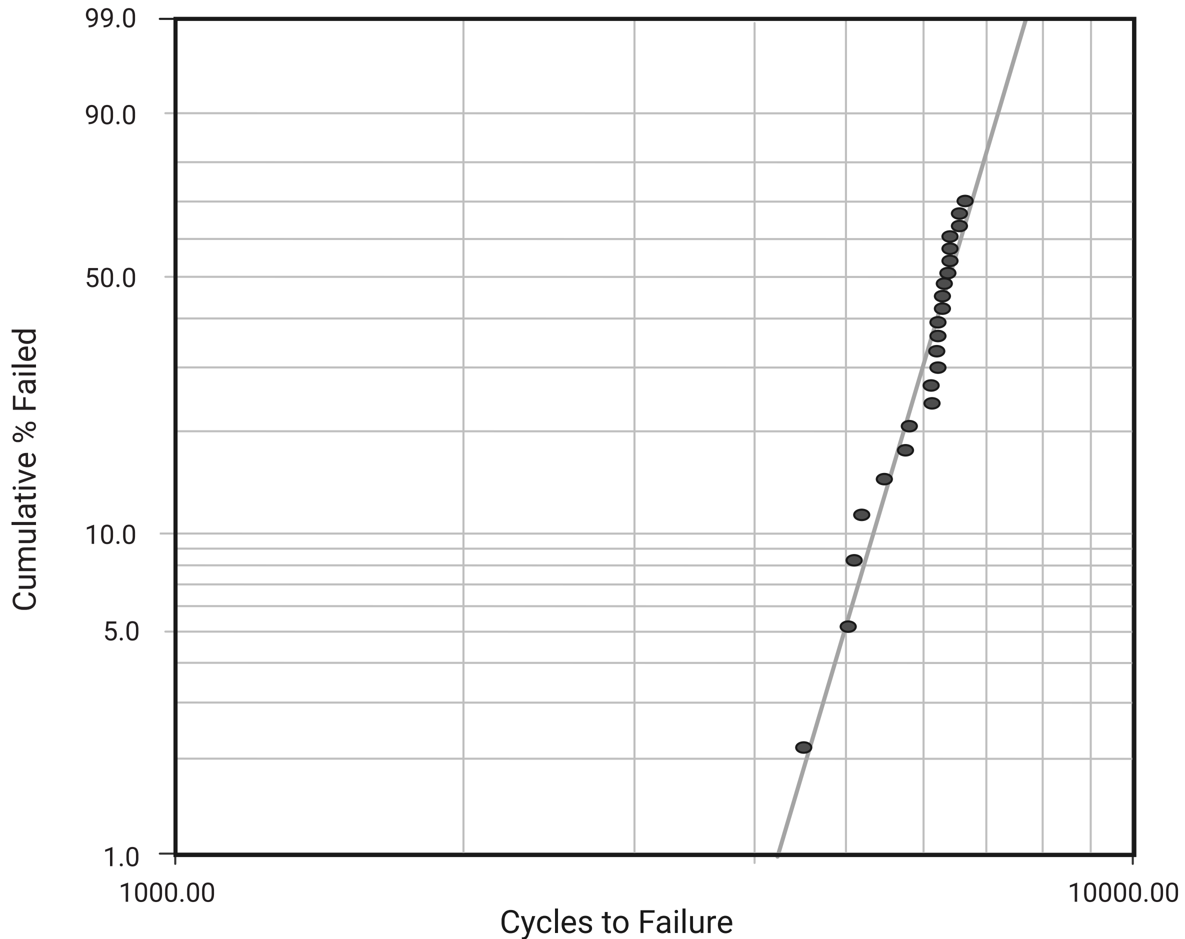
- Continuous scanning of daisy chain nets with event detector
- FAIL: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 117: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
SBG484	6,827	32	23	4,499	6,608

Weibull Plots

Figure 13: **Cycles to Failure in the Second-Level Reliability Tests for SBG484**



FFG1928

Table 118: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FFG1928	45 X 45	1924	1.00	0.60	0.53	SMD	23.85 x 21.65	1.33 thick, 12-layer

Mother Board Design and Assembly Details

- 16-layer, FR-4, 220 x 140 x 2.4 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power

- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

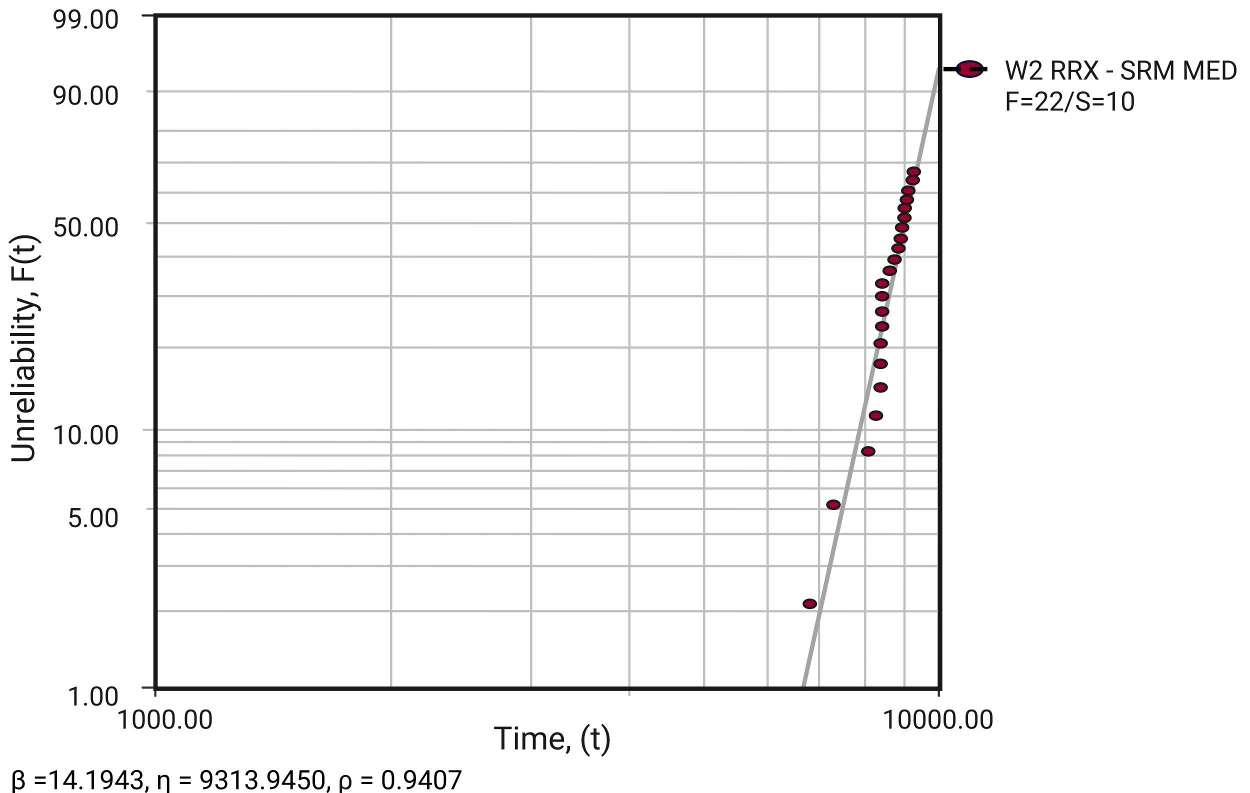
- Continuous scanning of daisy chain nets with event detector
- FAIL: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 119: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FFG1928	9,520	32	22	6,861	9,313

Weibull Plots

Figure 14: **Cycles to Failure in the Second-Level Reliability Tests for FFG1928**



FLG1925

Table 120: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FLG1925	45 X 45	1924	1.00	0.635	0.53	SMD	23.85 x 21.65	1.42 thick, 12-layer

Mother Board Design and Assembly Details

- 16-layer, FR-4, 220 x 140 x 3.2 size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

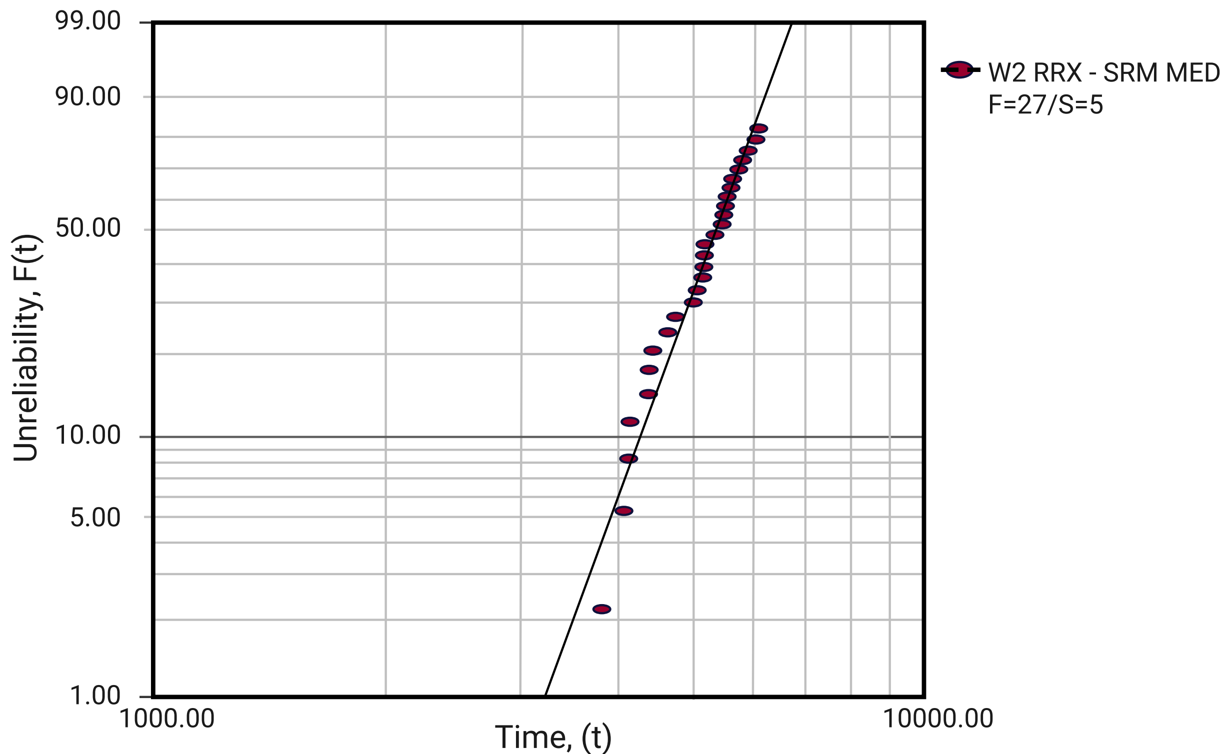
- Continuous scanning of daisy chain nets with event detector
- FAIL: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 121: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FLG1925	6,043	32	27	3,789	5,548

Weibull Plots

Figure 15: **Cycles to Failure in the Second-Level Reliability Tests for FLG1925**



FFV1928

Table 122: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FFV1928	45 X 45	1924	1.00	0.60	0.53	SMD	23.85 x 21.65	1.33 thick, 12-layer

Mother Board Design and Assembly Details

- 16-layer, Megtron 6, 220 x 140 x 2.4 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.50 mm aperture, alpha metals WS820 paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

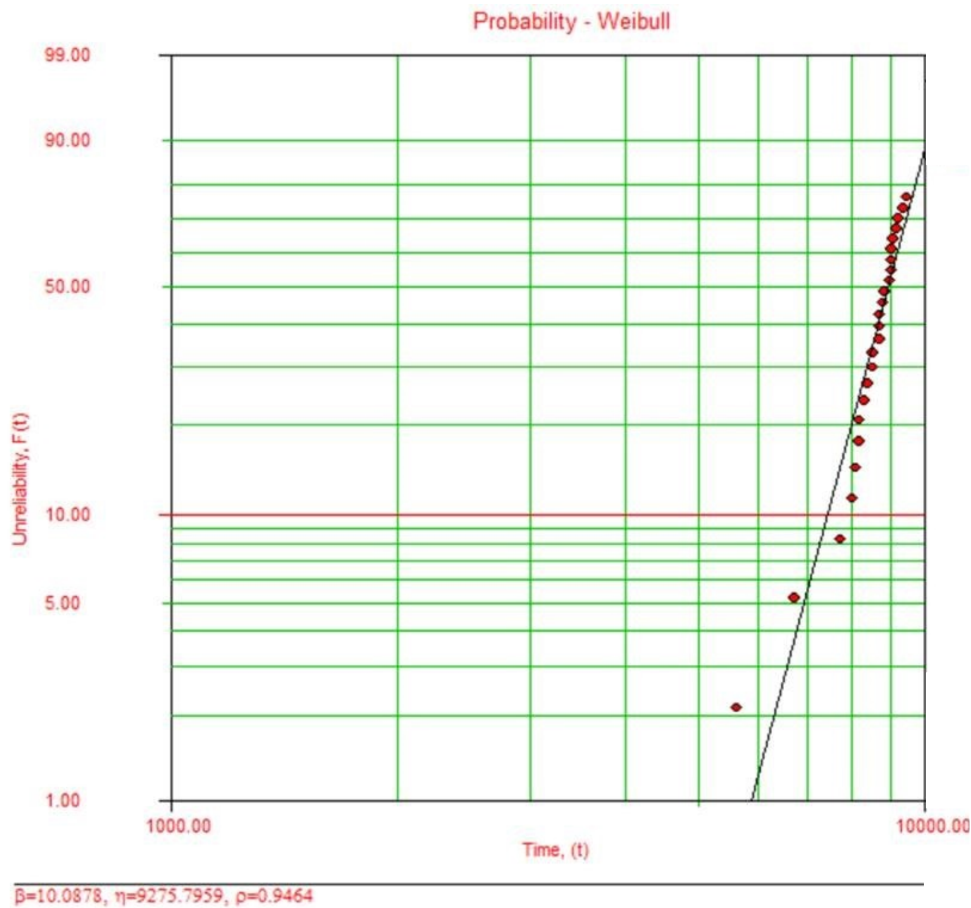
- Continuous scanning of daisy chain nets with event detector
- FAIL: Resistance of net > threshold resistance (500Ω) and lasting longer than 1 µs, followed by >9 events within 10% of the cycles to initial failure.

Table 123: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FFV1928	9,490	32	25	5,635	9,275

Weibull Plots

Figure 16: **Cycles to Failure in the Second-Level Reliability Tests for FFV1928**



FBVA900

Table 124: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FBVA900	31 X 31	900	1.00	0.60	0.53	SMD	16.30 x 11.36 x 0.762	1.24 thick, 10-layer

Mother Board Design and Assembly Details

- 16-layer, Megtron-6, 290 x 140 x 3.2 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: 16 layer with simulated power, ground (70% metal), and signal (40% metal) layer
- 0.127 mm laser cut stencil, 0.530 mm aperture, Indium 8.9HF paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

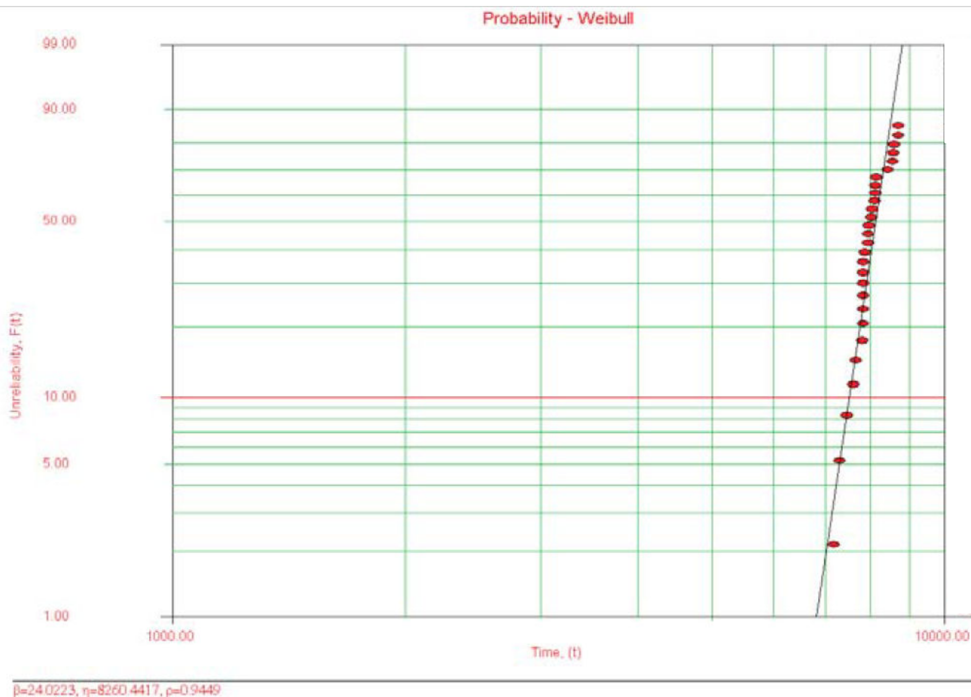
- Continuous scanning of daisy chain nets with event detection
- FAIL: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 125: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FBVA900	8737	32	28	7181	8260

Weibull Plots

Figure 17: **Cycles to Failure in the Second-Level Reliability Tests for FBVA900**



FFVB2104

Table 126: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FFVB2104	47.5 x 47.5	2104	1.00	0.60	0.53	SMD	18 x 22.5 x 0.762	1.42 thick, 14-layer

Mother Board Design and Assembly Details

- 28-layer, Megtron-6, 290 x 140 x 3.4 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: 28 layer with simulated power, ground (70% metal), and signal (40% metal) layer
- 0.127 mm laser cut stencil, 0.530 mm aperture, Indium 8.9HF paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

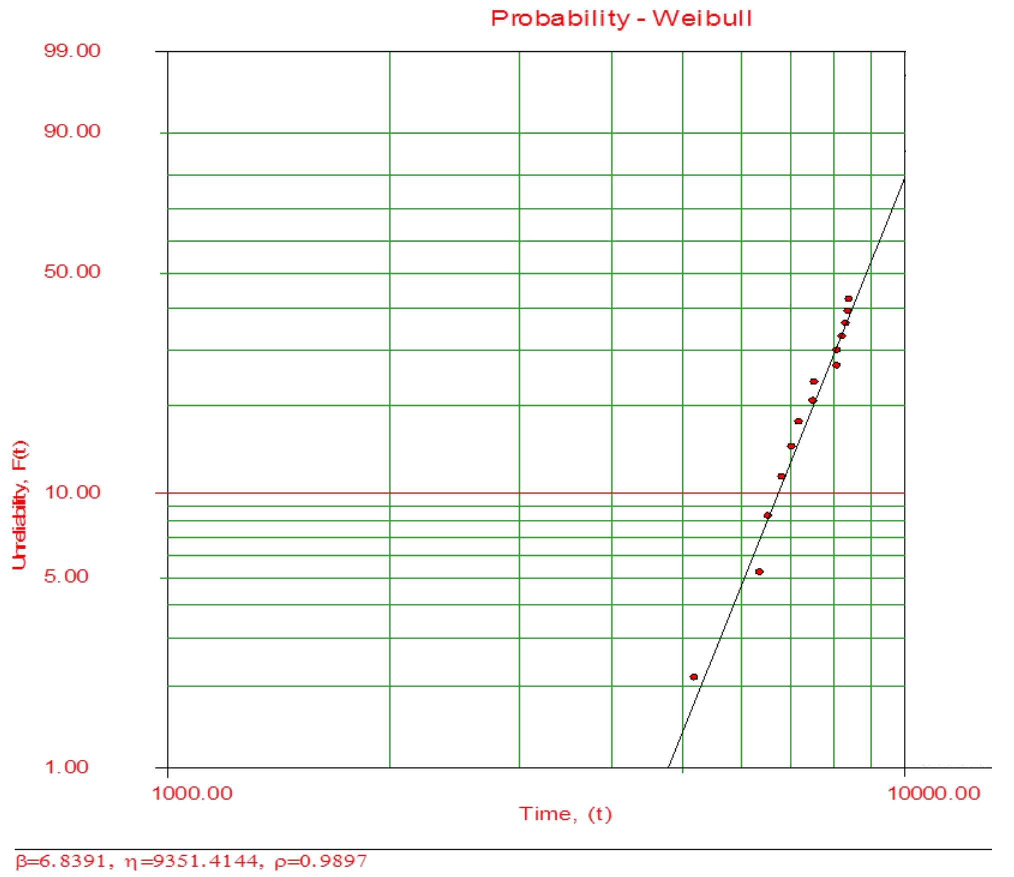
- Continuous scanning of daisy chain nets with event detector
- FAIL: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 127: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FFVB2104	8568	32	14	5205	9351

Weibull Plots

Figure 18: **Cycles to Failure in the Second-Level Reliability Tests for FFVB2104**



FLVA1924

Table 128: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FLVA1924	45 x 45	1924	1.00	0.60	0.53	SMD	14.4 x 23 x 0.10 (2 pcs) 25 x 31 x 0.50	2.00 thick, 18-layer

Mother Board Design and Assembly Details

- 28-layer, Megtron-6, 290 x 140 x 3.4 mm size, OSP finish
- 0.53 mm pad diameter/0.63 mm solder mask opening (NSMD pads)
- Board layer structure: 28 layer with simulated power, ground (70% metal), and signal (40% metal) layer
- 0.127 mm laser cut stencil, 0.530 mm aperture, Indium 8.9HF paste

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

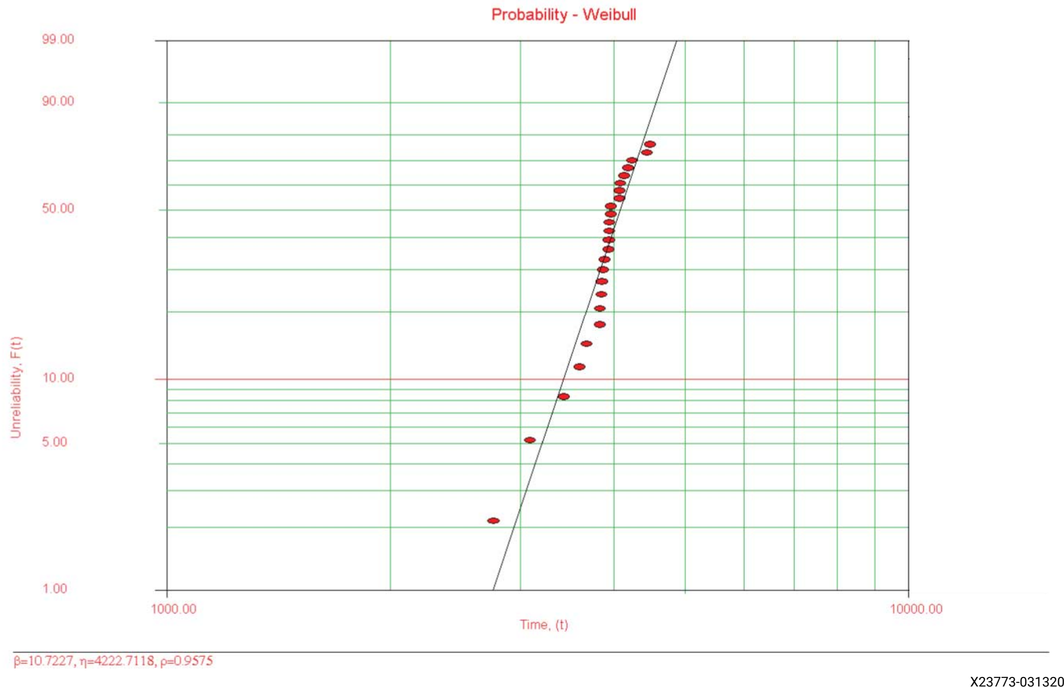
- Continuous scanning of daisy chain nets with event detector
- FAIL: Resistance of net > threshold resistance (500Ω), 10 events (maximum), 1 µs duration (maximum)

Table 129: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FLVA1924	4605	32	25	2759	4222

Weibull Plots

Figure 19: **Cycles to Failure in the Second-Level Reliability Tests for FLVA1924**



SFVA784 and SBVA784

Table 130: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
SFVA784	23 x 23	784	0.8	0.50	0.40	SMD	16.3 x 11.36	1.33 thick, 12-layer
SBVA784	23 x 23	784	0.8	0.50	0.40	SMD	16.3 x 11.36	1.33 thick, 12-layer

Mother Board Design and Assembly Details

- 28-layer, Megtron-6, 305 x 140 x 3.4 mm size, OSP finish
- 0.40 mm pad diameter/0.50 mm solder mask opening (NSMD pads)
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.127 mm laser cut stencil, 0.40 mm aperture, SAC305 solder paste.

Test Condition

- 0°C–100°C, 40-minute thermal cycle, 10-minute dwells, 10°C/minute ramp rate

Failure Criteria

- Continuous scanning of daisy chain nets with event detector
- FAIL: Resistance of net > threshold resistance (500Ω) and lasting greater than 1 µs, followed by >9 events within 10% of the cycles to initial failure.

Table 131: **Summary of Test Results**

Package	Cycles Completed	Number Tested	Number Failed	First Failure (Cycle)	Characteristic Life (Cycle)
SFVA784	6800	32	25	5049	6540
SBVA784	6140	32	25	4120	5718

Weibull Plots

Figure 20: **Cycles to Failure in the Second-Level Reliability Tests for SFVA784**

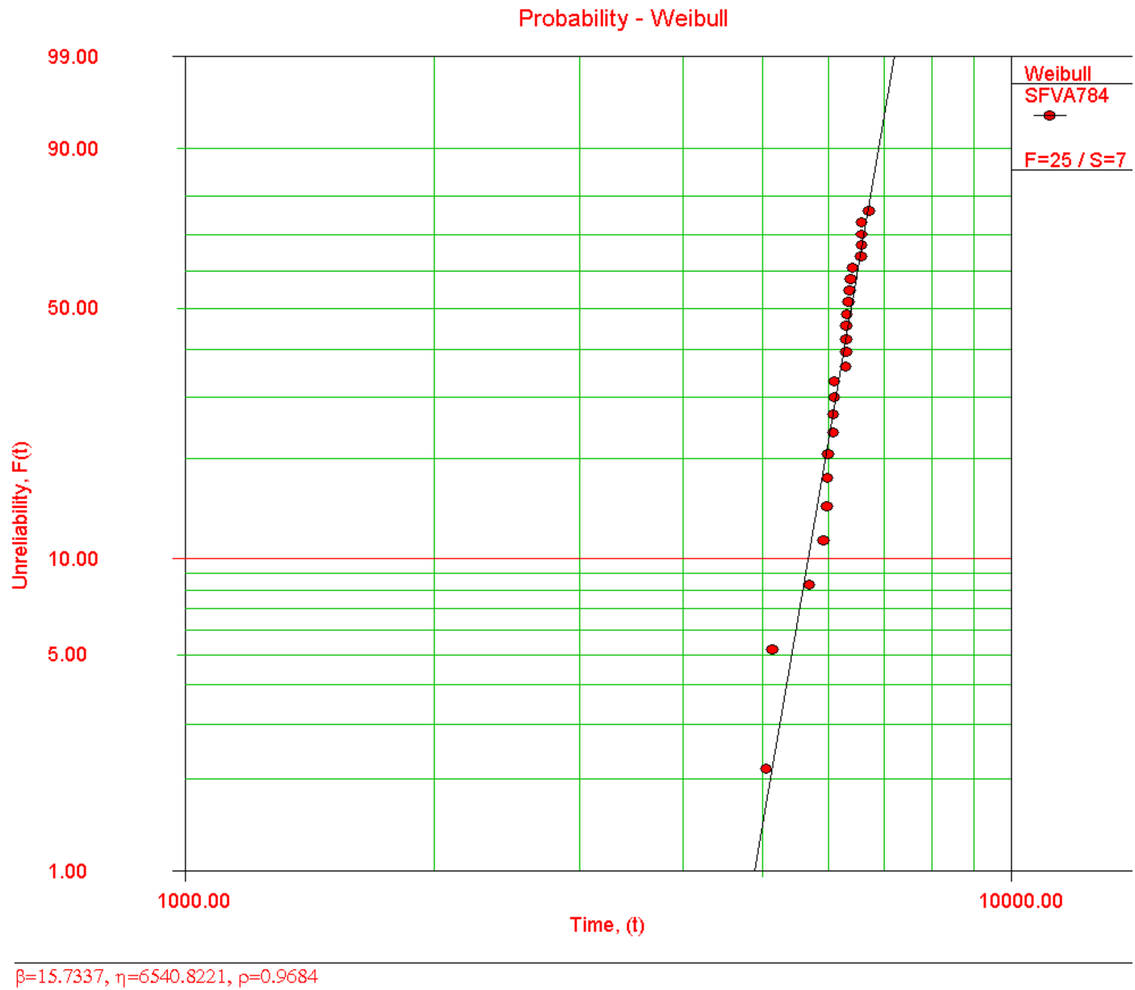
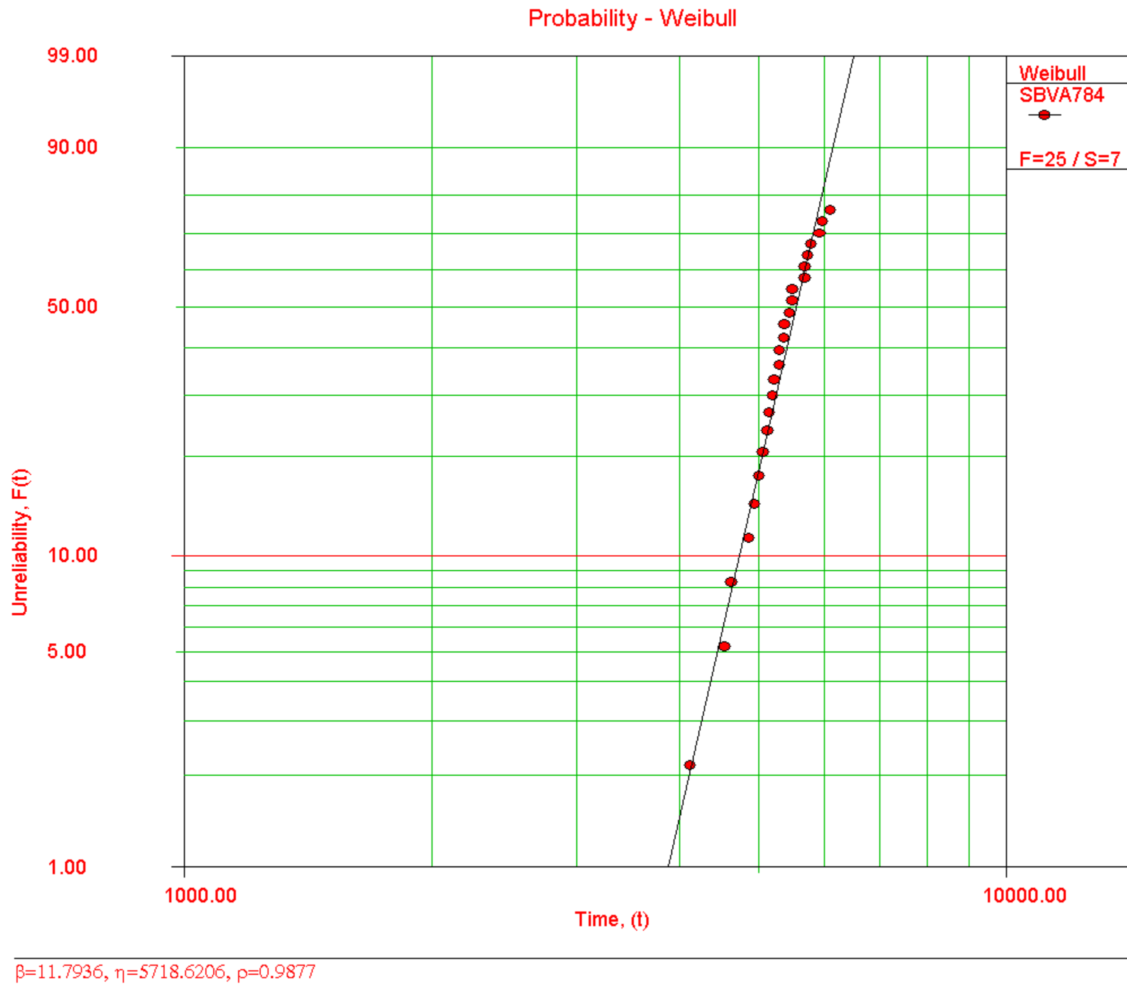


Figure 21: **Cycles to Failure in the Second-Level Reliability Tests for SBVA784**



XILINX

Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

***Note*:** For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *Device Package User Guide* (UG112)
2. *Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits* (WP286)
3. *Virtex-4 FPGA Packaging and Pinout Specification* (UG075)
4. *Virtex-5 FPGA Packaging and Pinout Specifications* (UG195)
5. *Virtex-6 FPGA Packaging and Pinout Specifications* (UG365)
6. *Spartan-6 FPGA Packaging and Pinouts Product Specification* (UG385)
7. *7 Series FPGAs Packaging and Pinout Product Specification* (UG475)
8. *Zynq-7000 SoC Packaging and Pinout Product Specifications* (UG865)
9. *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575)
10. *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075)

Training Resources

1. Designing FPGAs Using the Vivado Design Suite 1 Training Course
2. Vivado Design Suite QuickTake Video Tutorials

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