Sequential System Design Using ASM Charts

Introduction

Control unit designs may range from simple to highly complex. There are number of methods to design and realize control units. Simple control units can be designed using state graphs and state table methods. Complex control units may be designed using algorithmic charts just like flowcharts are used in software development. In this lab, you will be introduced to the Algorithmic State Machine (ASM) chart technique. *Please refer to the Vivado tutorial on how to use the Vivado tool for creating projects and verifying digital circuits*.

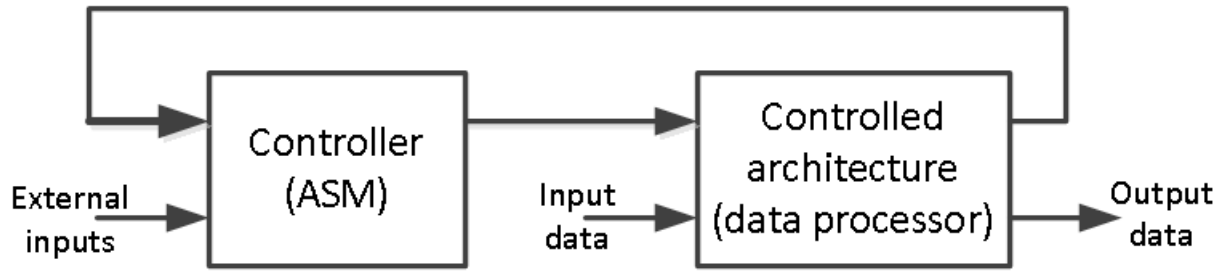
Objectives

After completing this lab, you will be able to:

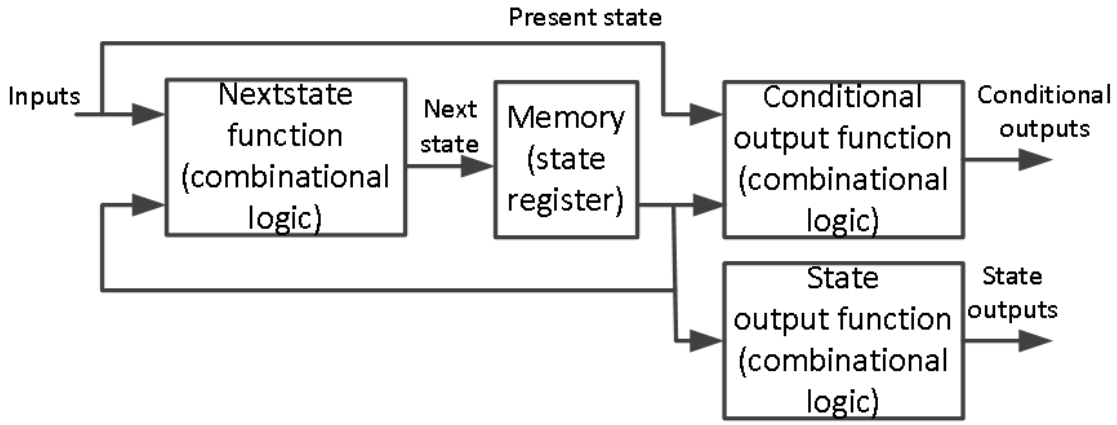
- Use the ASM charts to design sequential systems

ASM Charts Part 1

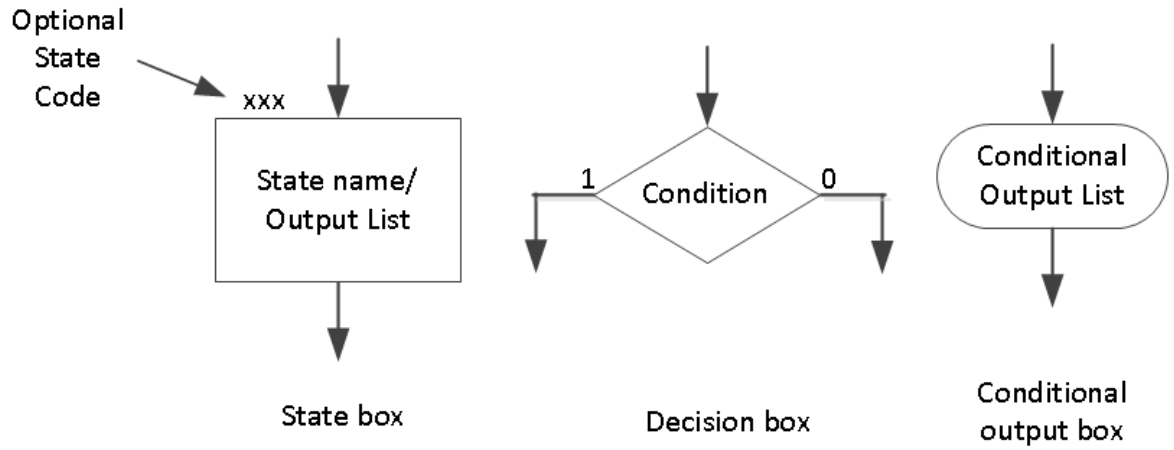
Just as flowcharts are useful in software design, special flowcharts called Algorithmic State Machines (ASM) are useful in digital systems hardware design. Digital systems typically consist of datapath processing and the control path. The control path is implemented using state machines which can be realized using state graphs. As the control path (behavior) of the system becomes complex, it becomes increasingly difficult to design the control path using the state graph technique. The ASM charts technique becomes useful and handy in designing complex and algorithmic circuits. The following diagram shows a complex digital system, partitioned into a controller (to generate the control signals) and the controlled architecture (data processor).



The model of the Controller (ASM) block in the above figure can be viewed as the combination of Mealy and Moore machines as shown below.

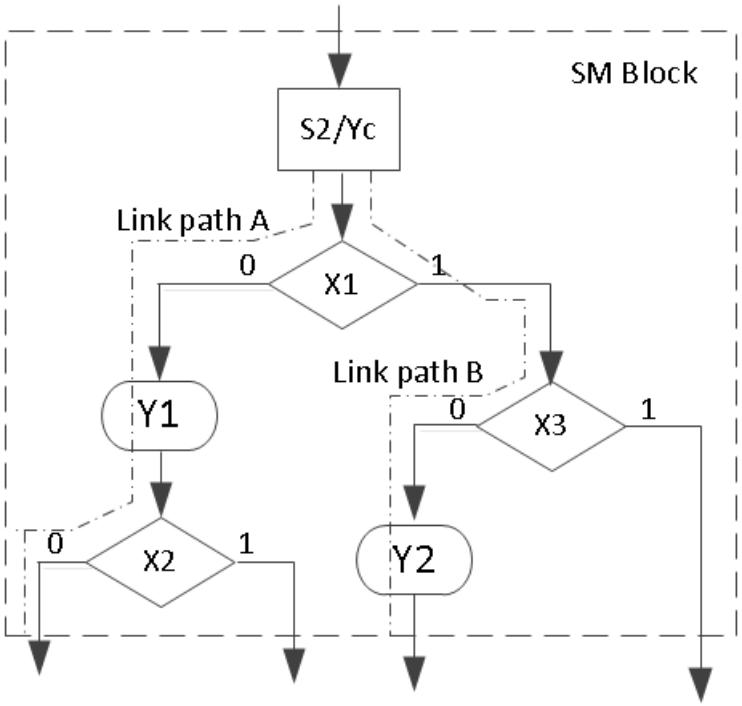


The ASM chart differs from an ordinary flowchart in that specific rules must be followed in constructing the chart. When these rules are followed, the ASM chart is equivalent to a state graph, and it leads directly to a hardware realization. The following diagram shows the three main components of an ASM chart.



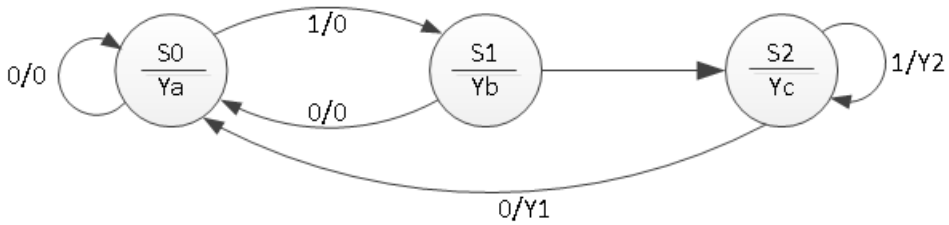
The state of the system is represented by a *state box*. The *state box* contains a state name, and it may contain an *output list* (just like in a state graph of the Moore machine). A *state code* may be placed outside the box at the top (if you want to assign a state code). A *decision box* always has true and false branches. The condition placed in the *decision box* must be a Boolean expression that is evaluated to determine which branch to take. The conditional output box contains a *conditional output list*. The conditional outputs depend on both the state of the system and the inputs (just like in the Mealy machine).

The ASM chart is constructed from SM blocks. Each SM block contains exactly one state box together with decision boxes and conditional output boxes associated with that state as shown below. An SM block has exactly one entrance path and one or more exit paths. Each SM block describes the machine operation during the time that the machine is in that state. A path through an SM block from entrance to exit is referred to as a link path.

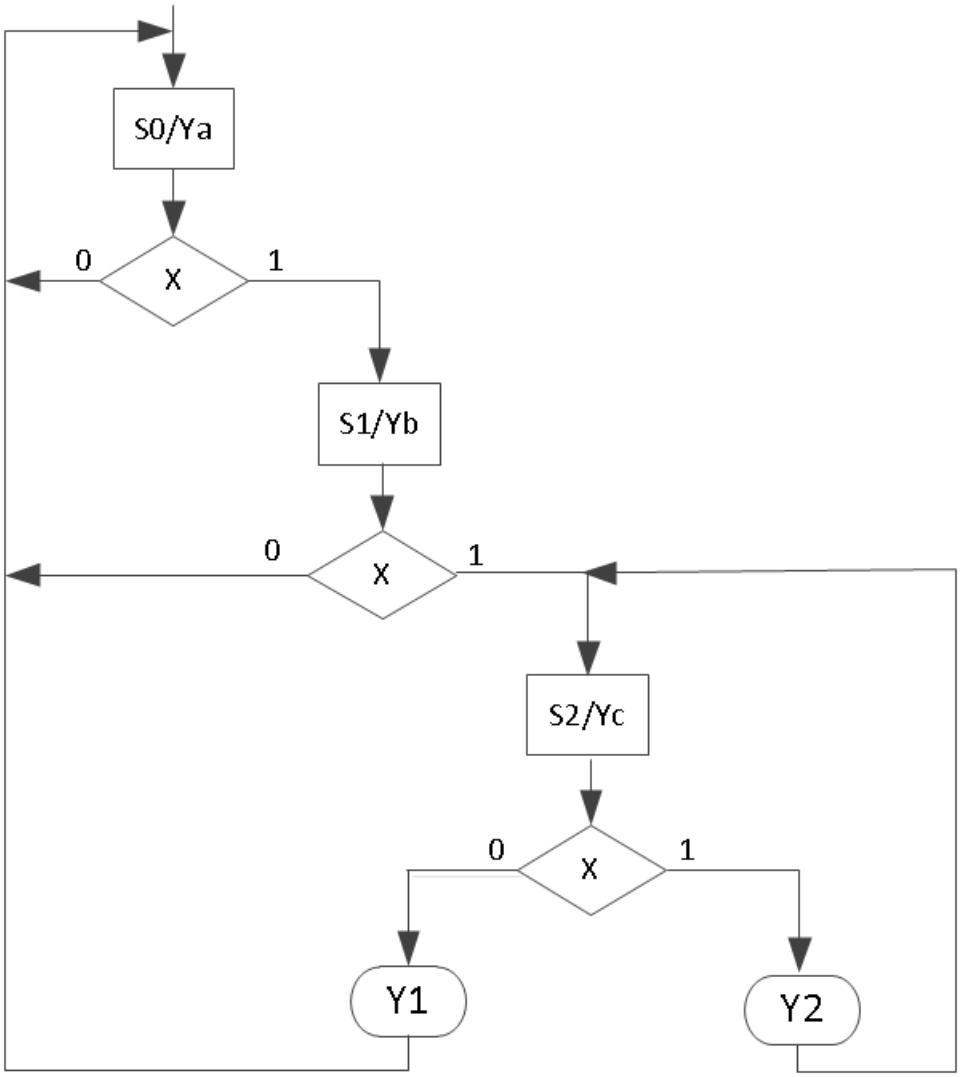


Let us consider an example of a state graph of a sequential network shown below. This state graph has both Mealy and Moore outputs. The outputs Y1 and Y2 are the Mealy outputs and so should be

conditional outputs. The Ya, Yb, and Yc are the Moore outputs so they should be part of state box. Input X can either be “0” or “1” and hence it should be part of the decision box.



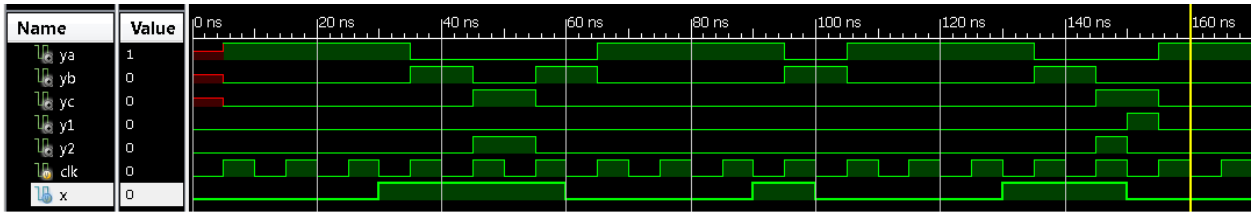
The ASM chart of the above state graph is as shown below.



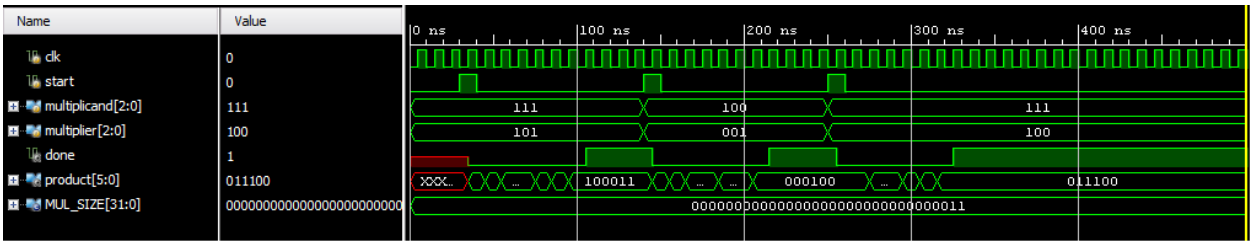
Once the ASM chart is determined, the conversion to HDL is straight forward. A `case` statement can be used to specify what happens in each state. Each condition box corresponds directly to an *if* statement (or an `else if`). The following code represents the functionality of the above ASM chart.

```
module asm_chart(input clk, input x, output reg ya, output reg yb, output reg
yc, output reg y1, output reg y2);
    reg [1:0] state, nextstate;
    parameter [1:0] S0=0, S1=1, S2=2;
always @(posedge clk)   // always block to update state
    state <= nextstate;
always @(state or x) // always block to compute both Mealy output & nextstate
begin
    y1 = 1'b0;
    y2 = 1'b0;
    case(state)
       S0: if(x)
                nextstate = S1;
             else
                nextstate = S0;
       S1: if(x)
                nextstate = S2;
           else
                nextstate = S0;
       S2: if(x)
           begin
                y2 = 1'b1;
                nextstate = S1;
           end
           else
           begin
                y1 = 1'b1;
                nextstate = S0;
           end
       default:
           nextstate = S0;
    endcase
end
always @(state) // always block to compute Moore output
begin
    ya = 1'b0;
    yb = 1'b0;
    yc = 1'b0;
    case(state)
       S0: ya = 1'b1;
       S1: yb = 1'b1;
       S2: yc = 1'b1;
       default: begin
           ya = 1'b0;
           yb = 1'b0;
           yc = 1'b0;
      end
    endcase
end
endmodule
```

The following behavioral simulation result shows the above model functionality.



1-1. Design a 3-Bit x 3-Bit binary multiplier. The multiplier will output 6-Bit product. The data processor unit will consist of a 3-Bit accumulator, a 3-Bit multiplier register, a 3-Bit adder, a counter, and a 3-bit shifter. The control unit will consist of a least-significant-bit (*lsb*) of the multiplier, a *start* signal, a *cnt_done* signal, and *clk* as an input. It will generate *start*, *shift*, a*dd*, and *done* signals. Develop an ASM chart for the control unit. Develop models for the data processor and the control unit. Develop a testbench to validate the design using the behavioral simulation.



1-2. Implement the design of 1-1 using SW7:SW5 as a *multiplier* input, SW4:SW2 as a *multiplicand* input, SW15 as a *clk* input, BTNU as a *start* input. Use LED7:LED2 as the *product* output, and LED0 as a *done* signal output. Go through the design flow, generate the bitstream, and download it into the Basys3 or the Nexys4 DDR board. Verify the functionality. Hint: You will have keep the BTNU pushed while switching (generating clock pulse) SW15 for the first time.

Sequential System Design Using ASM Chart — Part 2

We saw how the ASM chart technique can be used in designing control units of sequential machine. Now we will use the ASM chart technique along with the sequential design principles to design complex systems.

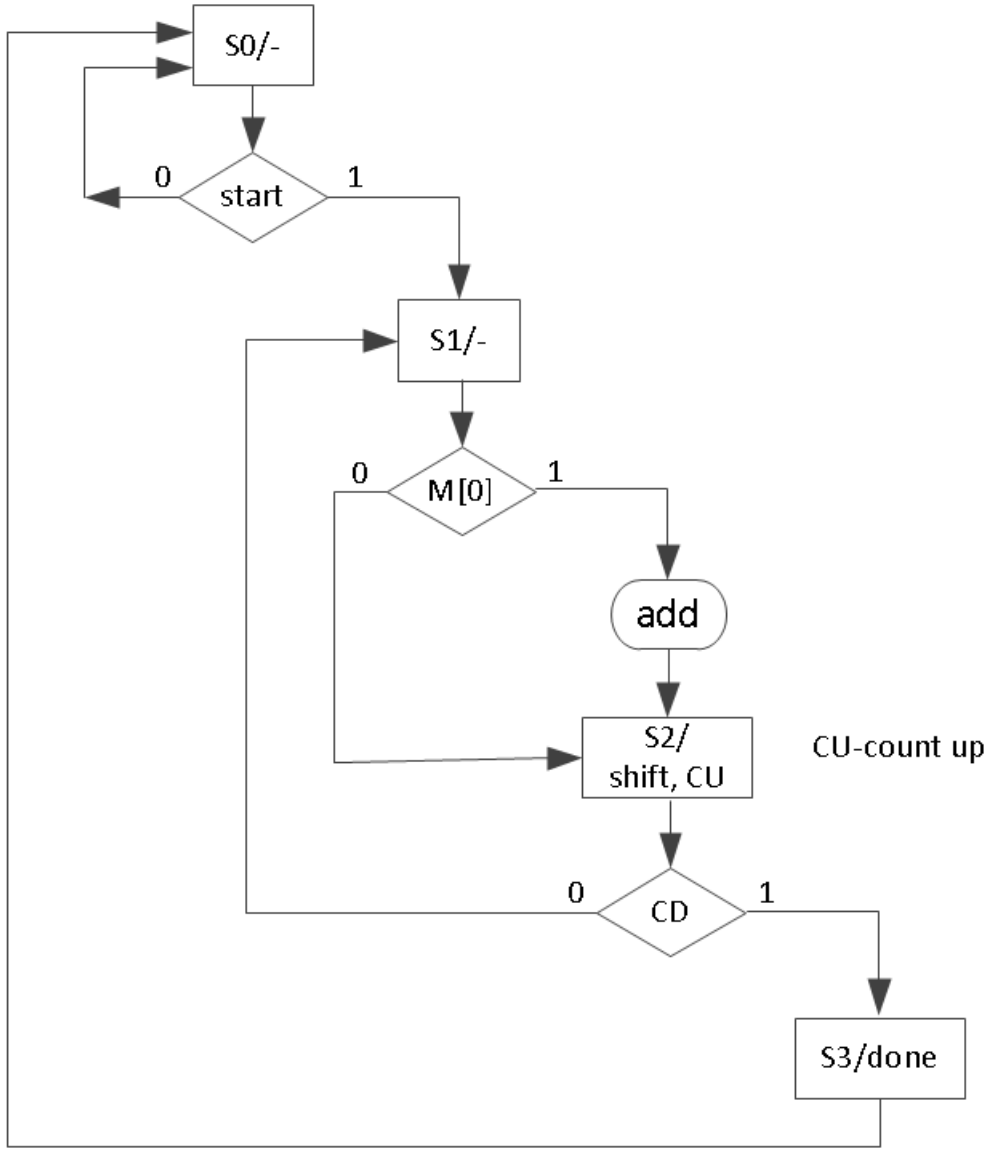
2-1. Modify the design of 1-2 to perform 4-Bit x 4-Bit unsigned multiplication. You will store the 4-Bit multiplicand and multipliers in 32x4 ROM (first 16 locations holding multiplicands and the other 16 locations holding multipliers). You will input multiplicand and multiplier operand addresses using switches. Use the clocking wizard to generate 5 MHz clock. Use the on-board clock source of 100 MHz, the BTNU button to start the calculation, SW7:SW4 to input the multiplicand address, SW3:SW0 to input the multiplier address, LED0 to output the done signal, and right most three 7-segment displays to show the result. Go through the design flow, generate the bitstream, and download it into the Basys3 or the Nexys4 DDR board. Verify the functionality.

Conclusion

In this lab, you learned how ASM charts can be used to design complex control units. You also designed digital system to perform binary multiplication using the ASM chart technique to develop the control unit which interfaced to the datapath processing unit.

Solution

ASM chart for 1-2



Block Diagram of 2-1