XILINX

Versal™ ACAP HBM Series Product Selection Guide

Industry's First Adaptive Compute Acceleration Platform (ACAP)

Versal™ HBM Series – Resources

			VH1522	VH1542	VH1582	VH1742	VH1782
Adaptable Engines	System Logic Cells (K)		3,837	3,837	3,837	5,631	5,631
	LUTs		1,753,984	1,753,984	1,753,984	2,574,208	2,574,208
	NoC Master / NoC Slave Ports		52	52	52	76	76
	Distributed RAM (Mb)		54	54	54	79	79
Memory	Total Block RAM (Mb)		89	89	89	132	132
	UltraRAM (Mb)		366	366	366	541	541
	Total PL Memory (Mb)		509	509	509	752	752
	HBM DRAM (GB)		8	16	32	16	32
	DDR Memory Controllers		4	4	4	4	4
	DDR Bus Width		256	256	256	256	256
Intelligent Engines	DSP Engines		7,392	7,392	7,392	10,848	10,848
Scalar Engines	APU		Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC				
	RPU		Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC				
	Memory		256KB On-Chip Memory w/ECC				
	Connectivity		Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)				
Serial Transceivers	GTYP[1] 32G		68	68	68	68	68
	GTM[2] 56G (112G)		20 (10)	20 (10)	20 (10)	60 (30)	60 (30)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM5)		2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX
	PCI Express (PLPCIE5)		8 x Gen5x4	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4
	100G Multirate Ethernet MAC		4	4	4	6	6
	600G Ethernet MAC		1	1	1	3	3
	600G Interlaken		0	0	0	1	1
	400G High-Speed Crypto Engines		2	2	2	3	3
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTYP, GTM (112G)				
VSVA3697	57.5x57.5	0.92	132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 20 (10)		
LSVA4737	70x70	1.0		132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 60 (30)	132, 570 0, 78 68, 60 (30)

Versal HBM Series

Notes:
1. GTY transceivers operate at data rates up to 32.75Gb/s
2. GTM transceivers can operate at data rates up to 112Gb/s by combining two transceivers together

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.

Versal™ HBM Series – Figures of Merit

			VH1522	VH1542	VH1582	VH1742	VH1782
Adaptable Engines	Adaptable Engine Peak Perf – INT1	TOPs	1834	1834	1834	2691	2691
	Adaptable Engine Peak Perf – INT2	TOPs	840	840	840	1233	1233
	Adaptable Engine Peak Perf – INT4	TOPs	218	218	218	320	320
	Adaptable Engine Peak Perf – INT8	TOPs	56	56	56	82	82
	NoC Cross-sectional Bandwidth	Tb/s	2.2	2.2	2.2	2.2	2.2
Memory	Total Bandwidth - Block RAM	Tb/s	366	366	366	539	539
	Total Bandwidth - Ultra RAM	Tb/s	138	138	138	205	205
	Total SRAM Bandwidth	Tb/s	504	504	504	743	743
	DDR4 Memory Bandwidth	GB/s	102.4	102.4	102.4	102.4	102.4
	LPDDR4 Memory Bandwidth	GB/s	136.5	136.5	136.5	136.5	136.5
Intelligent Engines	DSP Engine Peak Perf – INT8	TOPs	51.0	51.0	51.0	74.9	74.9
	DSP Engine Peak Perf – INT24	TOPs	17.0	17.0	17.0	25.0	25.0
	DSP Engine Peak Perf – CINT18	Complex TOPs	7.3	7.3	7.3	10.7	10.7
	DSP Engine Peak Perf – FP32	TFLOPs	11.9	11.9	11.9	17.5	17.5
Scalar Engines	Arm® Cortex-A72 Performance	DMIPs	15980	15980	15980	15980	15980
	Arm Cortex-R5 Performance	DMIPs	2505	2505	2505	2505	2505
I/O	Transceiver Bandwidth	Tb/s	6.77	6.77	6.77	11.41	11.41
Connectivity Throughput	PCIe Gen5 Throughput	GT/s	1536	1536	1536	1536	1536
	Interlaken Throughput	Gb/s	0	0	0	*600*	*600*
	Ethernet Throughput	Gb/s	1000	1000	1000	2400	2400
	Cryptographic (AES-256) Throughput	Gb/s	800	800	800	1200	1200
Connectivity Ports	10G Ethernet Ports	#	16	16	16	24	24
	25G Ethernet Ports	#	16	16	16	24	24
	40G Ethernet Ports	#	4	4	4	6	6
	50G Ethernet Ports	#	8	8	8	12	12
	100G Ethernet Ports	#	10	10	10	24	24
	200G Ethernet Ports	#	3	3	3	9	9
	400G Ethernet Ports	#	1	1	1	3	3

Versal HBM Series

Versal™ ACAP Ordering Information

Device Name				Device Attributes				Package Definition			
XC	V	C	1902	-1	M	S	E	V	S	V	D1760
Xilinx XC: Commercial XA: Automotive XQ: Defense	**Architecture** Versal	**Series Name** E: AI Edge C: AI Core M: Prime P: Premium H: HBM	**Device Number** Digits 1-3: Value Identifier Digit 4: # of Primary Cores	**Speed Grade** -1: Slowest -2: Mid -3: Highest	**Voltage** L: Low (0.7V) M: Mid (0.80V) H: High (0.88V)	**Static Screen** S: Standard L: Low Static	**Temp Grade** E: 0 to 110°C(1) I: –40 to 110°C(1) Q: –40 to +125°C M: –55 to +125°C	**Ball Pitch** V: 0.92mm, w/LSC N: 0.92mm, no LSC S: 0.8mm L: 1.0mm	**Lid** S: Lidless, w/Stiffener Ring F: Lidded B: Lidless, no Stiffener Ring H: Lidded Overhang I: Lidless, w/Stiffener Ring & Overhang	**RoHS6 Code** (2) V: Pb-free Ball Q: Eutectic Ball R: Ruggedized, Eutectic Ball	**Footprint**

Note:
1. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime—except -1E and -3E (standard 0–100°C).
2. All packages have Pb-free bumps.