LogiCORE IP Utility Reduced Logic (v2.0)

PB045 (v2.0) April 9, 2018 **Product Brief**

Introduction

The Utility Reduced Logic core applies a logic reduction function over an input vector to generate a single bit result. The core is intended as glue logic between peripherals. The logical operations supported are AND, OR, XOR and NOT.

Additional Information

See the product page.

Features

- Configurable size of the input vector
- Configurable reduced logic operation over the input vector

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale+™, UltraScale™, Zynq® -7000, Artix®-7, Virtex® -7, Kintex®-7
Supported User Interfaces	N/A
Provided with Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	None
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	N/A
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Figure 1 shows a Utility Reduced Logic in a system.

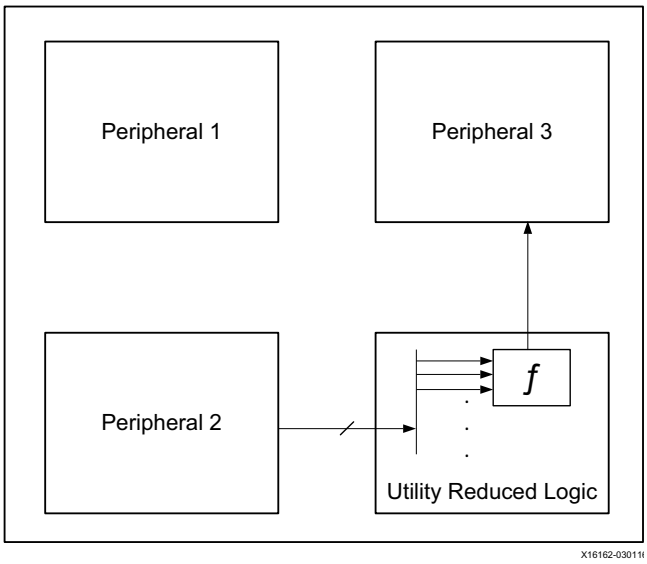

Figure 1: **Utility Reduced Logic in a System**

Block Diagram

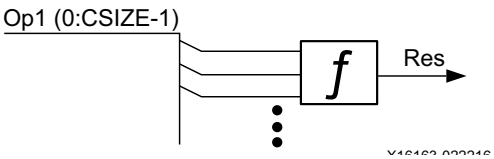

Figure 2: **Utility Reduced Logic Block Diagram**

I/O Signals

Table 1: **I/O Signals**

Signal	Interface	I/O	Description
Op1	None	I	Input bus [0: C_SIZE-1]
Res	None	O	One bit output signal. Result from the reduced logic operation.

Design Parameters

Table 2: **Design Parameters**

Parameter	Description	Type
C_SIZE	The vector size of input bus. Minimum value is 1.	Integer
C_OPERATION	The vector operation to perform. The supported functions (f) are: and, or, xor, not	String

There are no restrictions on allowed parameter combinations for this core.

Parameter-Port Dependencies

Table 3: **Port and Parameter Dependencies**

Name	Affects	Depends	Relationship Description
Design Parameters			
C_SIZE	Op1	0 to C_SIZE-1	Scale width of input bus
Port Signals			
Op1		C_SIZE	Scale width of input bus

Design Implementation

Design Tools

Note: This IP can only be used in the Vivado® IP integrator. It is not designed to be used in an RTL-only design flow within the Vivado Design Suite.

HDL code is generated by the Vivado IP integrator.

Target Technology

The target technologies are UltraScale+™, UltraScale™, Zynq®-7000, and 7 series devices.

Device Utilization and Performance Benchmarks

Table 4: **Resource Utilization**

Parameter Value		Device Resources		
C_OPERATION	C_SIZE	Slices	Slice Flip-Flops	Slice LUTs
"and"	8	2	0	2
"or"	8	2	0	2
"xor"	8	2	0	2

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

Date	Version	Revision
04/09/2018	2.0	• Changed the minimum value of the C_SIZE parameter to 1 in Table 2. • Updated the legal notices.
04/16/2016	2.0	Initial Xilinx release of this product brief

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