Reset Verification IP v1.0

LogiCORE IP Product Guide

Vivado Design Suite

PG298 (v1.0) October 30, 2019

Table of Contents

IP Facts

The Xilinx® Reset Verification IP (VIP) core has been developed to support the simulation of customer designed test bench or design which requires a reset signal.

The Reset VIP is unencrypted SystemVerilog source that is comprised of a SystemVerilog interface and synthesizable RTL. You can use APIs from the embedded reset RTL interface to assert/deassert reset.

Features

- Sets interface into master/pass-through mode
- Asserts/deasserts reset
- Asynchronous/synchronous reset

IP Facts

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family[1]	UltraScale+, UltraScale, Zynq®-7000 SoC, 7 series
Supported User Interfaces	Reset
Resources	N/A
Provided with Core	
Design Files	N/A
Example Design	SystemVerilog
Test Bench	N/A
Constraints File	N/A
Simulation Model	Unencrypted SystemVerilog
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.

LogiCORE™ IP Facts Table	
Synthesis	N/A
Support	
Release Notes and Known Issues	Master Answer Record: 69565
All Vivado IP Change Logs	Master Vivado IP Change Logs: 72775
Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of third-party tools, see the Xilinx Design Tools: Release Notes Guide.

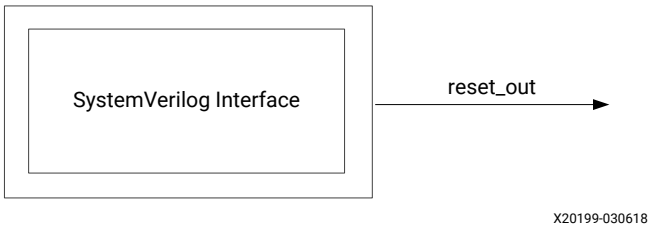
Overview

The Reset VIP core generates different kinds of reset signals during simulation. The Reset VIP can be configured in two different modes:

- Reset master VIP
- Reset pass-through VIP

The following figure shows the Reset master VIP which generates a reset signal and sends it to the reset system. The asynchronous reset is set to YES.

Figure 1: **Reset Master VIP**



The following figure shows the Reset master VIP with `sync_clk_in`. The asynchronous reset is set to NO.

Figure 2: **Reset Master VIP (sync_clk_in)**

The following figure shows the Reset pass-through VIP passing the reset signal which it receives. It can be configured in simulation to be pass-through or master. The asynchronous reset is set to YES.

Figure 3: **Reset Pass-Through VIP**

The following figure shows the Reset pass-through VIP with `sync_clk_in`. The asynchronous reset is set to NO.

Figure 4: **Reset Pass-Through VIP (sync_clk_in)**

Feature Summary

The Reset VIP core can be configured in master or in pass-through mode.

Applications

The Reset VIP core is for verification and system engineers who want to generate reset signals.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado® Design Suite under the terms of the Xilinx End User License.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx® LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

This chapter includes information on performance, parameters, and port descriptions.

Performance

The Reset VIP core synthesizes to wires and does not impact performance.

User Parameters

The following table shows the Reset VIP core user parameters.

Table 1: **Reset VIP User Parameters**

Parameter Name	Format/Range	Default Value	Description
INTERFACE_MODE	Type: string Value range: PASS_THROUGH, MASTER	PASS_THROUGH	Used to control the mode of protocol to be configured as master or pass-through.
RST_POLARITY	Type: string ACTIVE_LOW, ACTIVE_HIGH	ACTIVE_LOW	Used to control the polarity of the reset pin.
ASYNCHRONOUS	Type: string Value range: YES, NO	NO	Used to control whether reset is asynchronous/ synchronous to clock.

Port Descriptions

The table shows the Reset VIP independent port descriptions.

Table 2: **Reset VIP Independent Port Descriptions**

Signal Name	I/O	Default	Width	Description	Enablement
rst_in	I		1	Reset input	In pass-through mode only

Table 2: **Reset VIP Independent Port Descriptions** *(cont'd)*

Signal Name	I/O	Default	Width	Description	Enablement
rst_out	O		1	Reset output	Always ON
sync_clk	I	OFF	1	Synchronous clk input	When ASYNCHRONOUS is NO

Chapter 4

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

The Reset VIP core should be inserted into a system as shown in the following figures for Reset master VIP and Reset pass-through VIP.

Note: When the Reset VIP is configured with Asynchronous mode set to NO, `sync_clk` is added to the figures below.

Figure 5: **Reset Master VIP Example Topology**

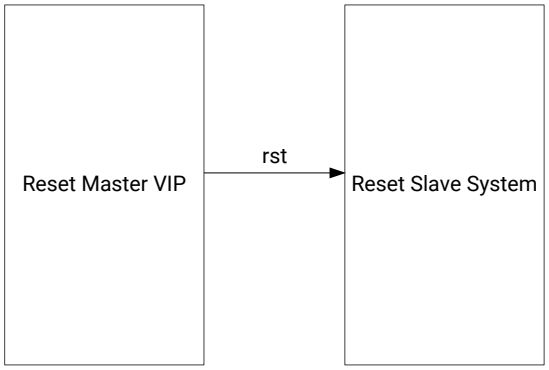
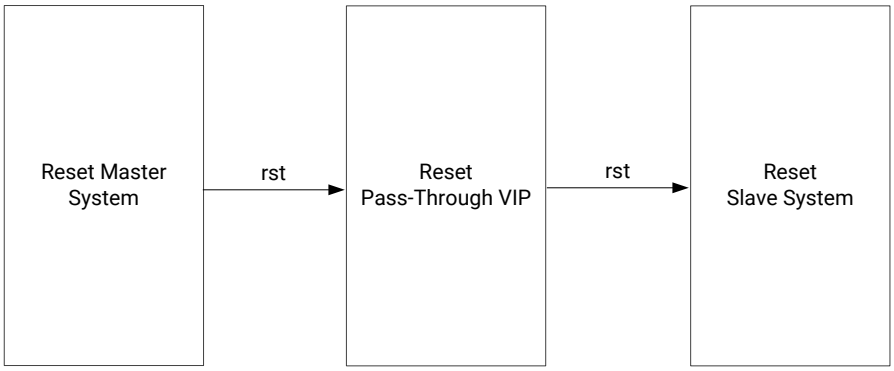


Figure 6: **Reset Pass-Through VIP Example Topology**



Clocking

This section is not applicable for this IP core.

Resets

This section is not applicable for this IP core.

Design Flow Steps

This section describes customizing and generating the core, constraining the core, and the simulation, synthesis, and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
- *Vivado Design Suite User Guide: Designing with IP* (UG896)
- *Vivado Design Suite User Guide: Getting Started* (UG910)
- *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado® Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

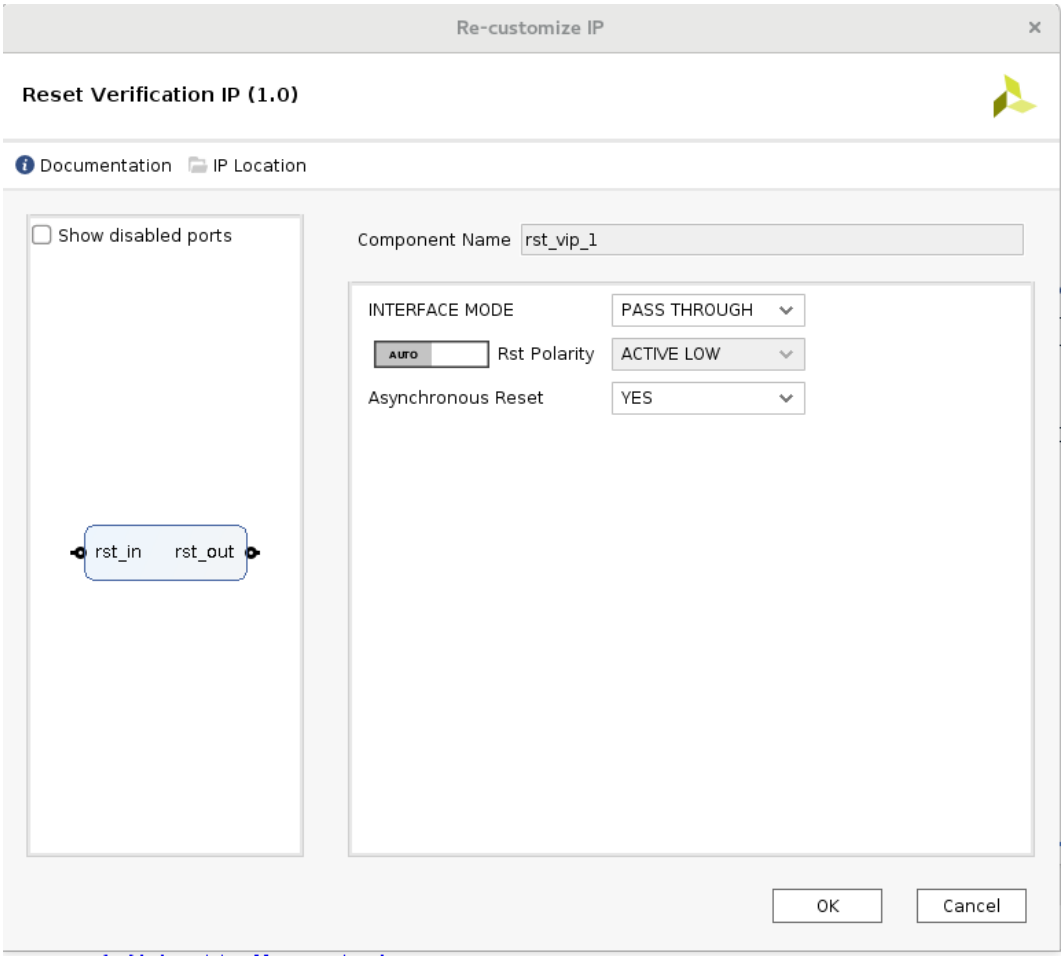
For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the *Vivado Design Suite User Guide: Getting Started* (UG910).

Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Customize IP Window

The figure shows the Reset VIP Vivado IDE Component Name screen.

Figure 7: **Customize IP Window**



Note: For the runtime parameter descriptions, see the User Parameters table in the Product Specification.

- **Component Name:** The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, 0 to 9 and "_".
- **Interface Mode:** Controls the mode of protocol to be configured as master or pass-through.
- **Rst Polarity:** Selects the specific reset polarity specification.
- **Asynchronous Reset:** Selects whether the reset is synchronous/asynchronous to the clock.

User Parameters

For the relationship between the fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl Console), see the User Parameters table in the Product Specification chapter.

Related Information

User Parameters

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

The Reset VIP core deliverables are organized in the directory `<project_name>/<project_name>.srcs/sources_1/ip/<component_name>` and are designated as the `<ip_source_dir>`. The relevant contents or directories are described in the following sections.

Vivado Design Tools Project Files

The Vivado design tools project files are located in the root of the `<ip_source_dir>`.

Table 3: **Vivado Design Tools Project Files**

Name	Description
<component_name>.xci	Vivado tools IP configuration options file. This file can be imported into any Vivado tools design and be used to generate all other IP source files.
<component_name>.{veo|vho}	Reset VIP instantiation template.

IP Sources

The IP sources are held in the subdirectories of the `<ip_source_dir>`.

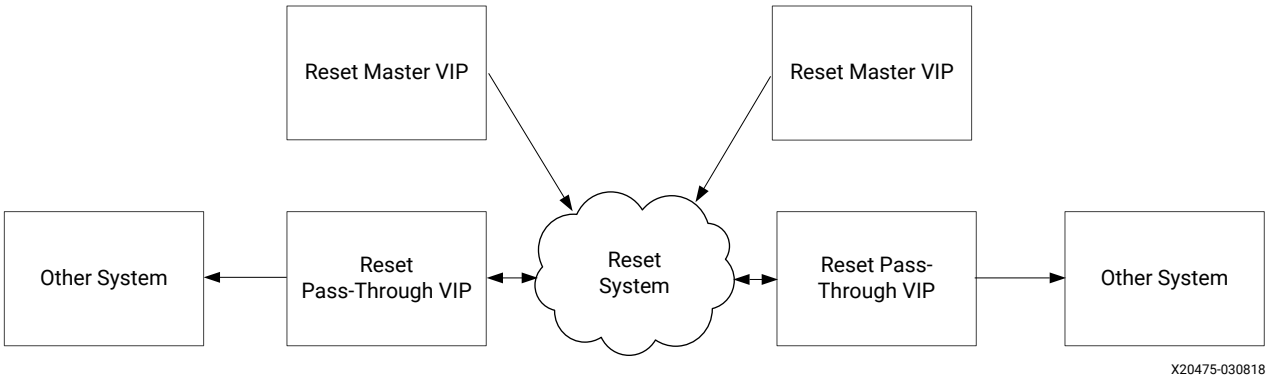
Table 4: **IP Sources**

Name	Description
hdl/*.sv	Reset VIP source files.
synth/<component_name>.sv	Reset VIP generated top-level file for synthesis. Optional, generated if synthesis target selected.
sim/<component_name>.sv	Reset VIP generated top-level file for simulation. Optional, generated if simulation target selected.

Reset VIP in Vivado IP Integrator

This section contains information about how to use the Reset VIP in a design and test bench environment. The following figure shows a possible design with the Reset VIPs.

Figure 8: **Reset VIP Design**



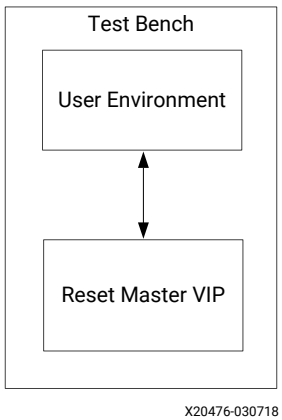
The Reset VIP consists of an interface which is used to generate reset signal which is needed in any design.

Reset Master VIP

The figure shows the Reset master VIP with its test bench. The test bench has two parts:

- User environment
- Reset master VIP

Figure 9: **Reset Master VIP Test Bench**



Finding the Reset VIP Hierarchy Path in IP Integrator

As mentioned earlier, the Reset VIP interface has to be passed to the user environment for use. The following guidelines describe how to find the hierarchy path of the Reset VIP in the IP integrator.

The best method to identify the VIP instance in the hierarchy is after the connection of all the IPs and the validation check. Click the **Simulation Settings**, set up the tool, and then click **Run Simulation**. The figure shows the Mentor Graphics Questa Advanced Simulator results. After the hierarchy is identified, it is used in the SystemVerilog test bench to drive the Reset VIP APIs.

Figure 10: **Reset VIP Instance in IP Integrator Design Hierarchy**

After the Reset VIP is instantiated in the IP integrator design and its hierarchy path found, the next step is using the Reset VIP to generate reset in master mode or produce pass-through VIP in runtime master mode.

Related Information

Example Design

Constraining the Core

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900).

IMPORTANT! *For cores targeting 7 series or Zynq®-7000 devices, UNIFAST libraries are not supported. Xilinx IP is tested and qualified with UNISIM libraries only.*

Synthesis and Implementation

The Reset VIP core is a verification IP set to synthesize as wires. There is no implementation for the Reset VIP.

Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

IMPORTANT! *The example design of this IP is customized to the IP configuration. The intent of this example design is to demonstrate how to use the Reset VIP core.*

Overview

The following figure shows the Reset VIP core example design with an asynchronous reset.

Figure 11: **Reset VIP Example Design**

This section describes the example tests used to demonstrate the abilities of the Reset VIP core. Example tests are delivered in SystemVerilog. When the core example design is open, the example files are delivered in a standard path test bench and bd design are under directory imports. The packages are under the directory `example.srcs/sources_1/bd/ex_sim/ipshared`.

The example design consists of two components:

- Reset VIP in master mode
- Reset VIP in pass-through mode

In the Reset master VIP, it creates a reset signal and sends it to the Reset pass-through VIP. In the Reset pass-through VIP, it receives a reset signal from the Reset master VIP and sends it out.

The Reset VIP core is not fully autonomous. If the tests are written using the APIs, there are different methods from the user environment to set up the reset signal. Xilinx recommends obtaining all of the members through the APIs instead of accessing them directly.

When the Reset VIP is configured in pass-through mode, it can be changed to master mode in the runtime and then be changed back to pass-through mode based on your requirements. When it is switched to runtime master mode, it behaves exactly as a Reset master VIP.

Test Bench

This chapter contains information about the test bench for the example design provided in the Vivado® Design Suite.

To open the example design either from the Vivado IP catalog or Vivado IP integrator design, follow these steps:

1. Open a new project and click **IP Catalog**.
2. Search for **Reset Verification IP**. Double-click the IP, configure, and generate the IP.
3. Right-click the IP and choose **Open IP Example Design...**.

   Note: If you have the Reset VIP as one component in the IP integrator design, right-click Reset VIP and click **Open IP Example Design...**.

In both scenarios, a new project with the example design is created. The example design has the master and pass-through VIP connected directly to each other as shown in the figure in the Example Design chapter. The configuration of the example design matches the original VIP configuration.

Related Information

Example Design

Reset VIP Example Test Bench and Test

The following scenarios are covered in the example design:

- Reset pass-through VIP in pass-through mode. The Reset master VIP generates a simple reset signal and passes it to the pass-through VIP.
- Switches Reset pass-through VIP into the runtime master mode and generates a simple reset signal.

Useful Coding Guidelines and Examples

While coding test bench for the Reset VIP, the following requirements must be met. Otherwise, the Reset VIP does not function. These codes are based on asynchronous reset. For synchronous reset, check the example design.

1. Create module test bench as all other standard SystemVerilog test benches.

```
module testbench();
      …
      endmodule
```

2. To assert reset, use `<hierarchy_path>.IF.assert_reset`.
3. To deassert reset, use `<hierarchy_path>.IF.deassert_reset`.
4. APIs used to switch pass-through VIP into runtime master and runtime pass-through modes are `set_master_mode` and `set_passthrough_mode`. The following is a simple example design code for the Reset VIP:

```
// Master RST VIP assert_reset

<=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_mst.inst.IF.assert_res
et();
    #0ps;

if( <=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_mst.inst.IF.RST !
= <=:c_rst_polarity:>) begin
      $error("reset is not as expected in master VIP assert_reset");
    end
    #(rst_hold_length);
    // Master RST VIP deassert_reset

<=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_mst.inst.IF.deassert_r
eset();
    #0ps;

if( <=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_mst.inst.IF.RST
== <=:c_rst_polarity:>) begin
      $error("reset is not as expected in master VIP deassert_reset");
    end
    #(wait_length_before_switch_mode);
    // Switch Passthrough RST VIP into Master mode

<=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_passthrough.inst.set_m
aster_mode();
    #(rst_initial_delay );
    // Passthrough RST VIP in runtime master mode assert_reset

<=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_passthrough.inst.IF.as
sert_reset();
    #0ps;

if( <=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_passthrough.inst.I
F.RST != <=:c_rst_polarity:>) begin
      $error("reset is not as expected in assert_reset of Passthrough
VIP runtime master mode");
    end
```

```
    #(rst_hold_length);
    // Passthrough RST VIP in runtime master mode deassert_reset

<=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_passthrough.inst.IF.de
assert_reset();
    #0ps;

if( <=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_passthrough.inst.I
F.RST == <=:c_rst_polarity:>) begin
      $error("reset is not as expected in deassert_reset of Passthrough
VIP runtime master mode");
    end
    #(wait_length_before_switch_mode);

<=:$ComponentName:>_exdes_tb.DUT.ex_design.rst_vip_passthrough.inst.set_p
assthrough_mode();
    #(wait_length_before_finish);
```

Related Information

Example Design

Appendix A

Upgrading

This appendix is not applicable for the first release of the core.

Reset VIP APIs

This appendix contains information about the `rst_vip_v1_0_top` APIs. These APIs can be called through the following code. The `set_passthrough_mode` and `set_master_mode` are used to switch the pass-though VIP into different runtime modes. These APIs can be called through the test bench hierarchy pointing to the top. An example would be `set_passthrough_mode()`.

```
<hierarchy_path>.set_passthrough_mode()

set_passthrough_mode
function void set_passthrough_mode()

//Sets RST VIP passthrough into run time passthrough mode

set_master_mode
function void set_master_mode()

//Sets RST VIP passthrough into run time master mode
```

Related Information

Finding the Reset VIP Hierarchy Path in IP Integrator

Appendix C

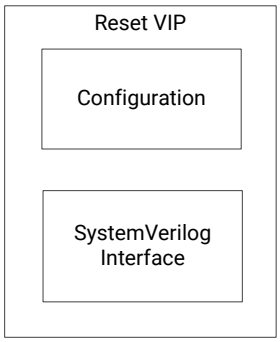
Reset VIP Generation and Flow Methodology

This appendix contains information about the Reset VIP agents and flow methodologies.

Core Architecture

Before talking about how to use Reset VIP core, the VIP architecture is described here. Different from other standard Xilinx IP, the Reset VIP core is based on the SystemVerilog interface. The Reset VIP core architecture is shown here.

Figure 12: **Reset VIP Core Architecture**



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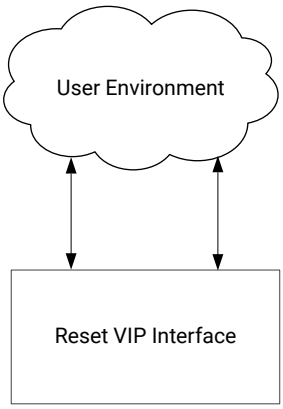
The Reset VIP core consist of two main layers:

- SystemVerilog signal interface
- Configuration

The SystemVerilog signal interface includes the typical Verilog input/output ports which are `rst_in` and `rst_out`. For more information about usage and list of APIs in the Reset VIP, see the API documentation.

Figure 13: **Reset VIP Interface**



Reset VIP Generation Flow

The following steps outline how to generate a reset using the Reset VIP core.

1. When Reset VIP is in master mode, you decide when reset should be asserted or deasserted. You control reset assert and deassert time:
   - `<hierarchy_path>.IF.assert_reset`: If RST_POLARITY of Reset VIP is High, set reset to be 1, else set reset to be 0.
   - `<hierarchy_path>.IF.deassert_reset`: If RST_POLARITY of Reset VIP is High, set reset to be 0, else set reset to be 1.
2. When Reset VIP is in pass-through mode, you have to first switch it into runtime master mode if you want to assert/deassert reset. The following is the API for reset assert and deassert:
   - `<hierarchy_path>.set_intf_master()`: Use this to set in runtime master mode.
   - `<hierarchy_path>.IF.assert_reset`: If RST_POLARITY of Reset VIP is High, set reset to be 1, else set reset to be 0.
   - `<hierarchy_path>.IF.deassert_reset`: If RST_POLARITY of Reset VIP is High, set reset to be 0, else set reset to be 1.

XILINX

Appendix D

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support. The Xilinx Community Forums are also available where members can learn, participate, share, and ask questions about Xilinx solutions.

Documentation

This product guide is the main document associated with the core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master AR for Core

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Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

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Appendix E

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this product guide:

1. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
2. *Vivado Design Suite User Guide: Designing with IP* (UG896)
3. *Vivado Design Suite User Guide: Getting Started* (UG910)
4. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
5. Reset VIP API Documentation

   Note: VIP API documentation source codes are different from the Install area implementation codes, refer to the Install area for the source codes.

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
10/30/2019 Version 1.0	
References	Updated VIP API documentation link.
05/22/2019 Version 1.0	
Features	Added Asynchronous/synchronous reset.
Chapter 2: Overview	Added sync_clk_in descriptions.
User Parameters	Added Asynchronous
Port Descriptions	Added sync_clk to table.
General Design Guidelines	Added sync_clk description.
Customize IP Window	Updated figure and added Asynchronous Reset description.
Overview	Added asynchronous description.
Useful Coding Guidelines and Examples	Added asynchronous description.
References	Added VIP API documentation link.
11/14/2018 Version 1.0	
Document updates.	Updated to latest Vivado Design Suite release.
04/04/2018 Version 1.0	
Initial release.	N/A

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