Radio over Ethernet Framer v2.0

PB056 (v2.0) May 22, 2019 **LogiCORE IP Product Brief**

IP Facts

The Xilinx® Radio over Ethernet Framer (RoE Framer) core is part of a complete eCPRI and Next Generation Fronthaul Interface (NGFI) system solution developed on the Zynq® UltraScale+™ MPSoC, relying on both hardware and software to provide a comprehensive and efficient computing platform for the required protocols and features: eCPRI, IEEE 1914.3 (NGFI), IEEE 1588, Synchronous Ethernet, and Node and Network OAM. The core enables radio data transmission through a packet-based transport network connecting Remote Radio Units (RRUs) to the centralized Baseband Unit (BBU).

Additional Documentation

A Product Guide is available for this core. Access to this material can be requested by clicking on this registration link: https://www.xilinx.com/member/ecpri/.

Features

- Supports standard IEEE 802.1 Ethernet packets, optionally including VLAN tags, as well as UDP over IPv4 or IPv6, over Ethernet.
- Fully programmable filtering rules allow the hardware to identify and manage user plane packets.
- Each Ethernet and IP/UDP header field is fully programmable.
- Alignment to an external 10 ms Start of Radio Frame pulse, enabling 1588 synchronization.
- In O-RAN (formerly xRAN) mode, the core implements *O-RAN Control, User and Synchronization Plane Specification v1.0* (O-RAN Specification v1.0). Not all features are supported; see the O-RAN Support Matrix for full details. In this mode, the core supports up to four 10 Gb/s or four 25 Gb/s Ethernet ports. Mixed rate mode is not supported.
    - Currently supports one component carrier (CC), with independent uplink and downlink timers.
    - Supports a resolution of down to one resource block (RB) per section message. This release is limited to sixteen section messages per symbol.
    - Support for up to 16 spatial streams with 2048 flow IDs.
    - Variable buffers for uplink and downlink control and downlink U-Plane messages.
    - Precoding and beam forming within the core are not yet supported in this release. The spatial stream interface does *not* include the required buffering immediately before the beam former. The implementation of an appropriate double buffer is left to the user in the present release.

- In non-O-RAN mode, the core supports up to four 10 Gb/s or two 25 Gb/s Ethernet ports.
    - Automates in hardware the encapsulation and extraction of I/Q radio samples in and from the transported packets, formed according to either the *eCPRI Specification v1.2* (eCPRI Specification V1.2), or the *IEEE 1914.3-2018 IEEE Standard for Radio Over Ethernet Encapsulations and Mappings* (IEEE 1914.3) specification.
    - Transport either time domain or frequency domain I/Q samples, the latter together with real-time control packets.
    - A programmable reception window allows you to store a convenient number of incoming packets per stream, trading off latency with resilience against packet delay variation and reordering capability.
    - Supports all eCPRI message types, including one-way delay measurement based on PCS/PMA level timestamps, relying on software API.
    - Each supported antenna-carrier flow can be associated to a programmable flow identifier, as well as to a specific packet type and Ethernet port number.
    - Two reference designs are provided: an example design and an example system.

IP Facts

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Kintex® UltraScale™, Virtex® UltraScale™, Zynq®-7000 SoC, Kintex® UltraScale+™, Virtex® UltraScale+™, Zynq® UltraScale+™ MPSoC, Zynq® UltraScale+™ RFSoC.
Supported User Interfaces	AXI4-Stream
Resources	Performance and Resource Use web page (registration required)
Provided with Core	
Design Files	Encrypted RTL
Example Design	Verilog
Test Bench	Verilog
Constraints File	Xilinx Design Constraints (XDC)
Simulation Model	Verilog
Supported S/W Driver[2]	Linux
Tested Design Flows[3]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

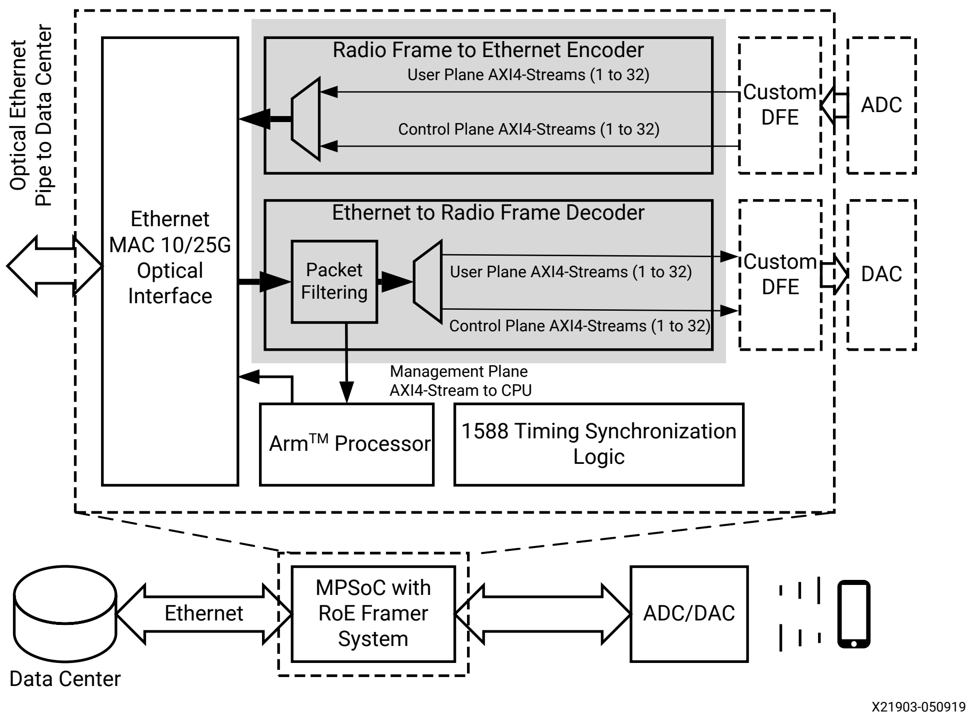
1. For a complete list of supported devices, see the Vivado IP catalog. Note that the example system is not available on Zynq-7000 devices.
2. Linux OS and driver support information is available from the Xilinx Wiki page. This is only officially supported for Zynq UltraScale+ devices.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The Radio over Ethernet Framer allows the development of a complete solution to support all the features required by an advanced fronthaul interface. In the LTE and 5G radio mobile architectures, fronthaul is the transport network interconnecting the Remote Radio Units (RRUs) to the Baseband Units (BBUs) and relies on different topologies, such as point-to-point, point-to-multipoint, and ring. To match future requirements in efficiency and flexibility, the fronthaul network is packet-based, relying either directly on the Ethernet network protocol or on a UDP/IP stack.

The RoE Framer system, shown in the following figure, built from the Radio over Ethernet Framer and other Xilinx IP, is a computing platform designed to support the management of the user, control, and synchronization planes, working as an intelligent and adaptable network interface submodule within an implementation of an RRU or BBU.

Figure 1: **RoE Framer Top Level Overview**

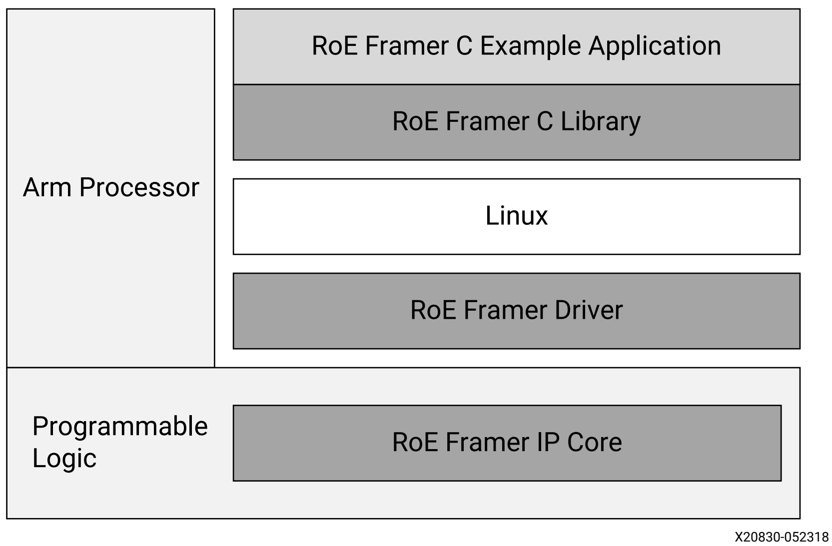


To transfer user plane information using a packet-based fronthaul, different protocols have been proposed, such as eCPRI v1.2 (*eCPRI Specification v1.2* (eCPRI Specification V1.2)) and IEEE 1914.3 (*IEEE 1914.3-2018 IEEE Standard for Radio Over Ethernet Encapsulations and Mappings* (IEEE 1914.3)).

The eCPRI protocol defines how to handle user data and real-time control packets, together with several other services used to control and monitor the remote unit. The IEEE 1914.3 standard supports both native and legacy implementations, in which existing circuit-based links, such as those relying on the CPRI protocol, are transported over an Ethernet packet network. The RoE Framer IP can be programmed to support either of the two protocols, configuring the dimensions of the supported packet formats, setting the methods used to identify each user data flow, and checking that the packet sequence is correct.

The RoE Framer supplies IP, drivers, and software APIs to implement supported protocols. The RoE Framer IP is implemented in the programmable logic (PL), and the drivers and software APIs run on Linux on the Arm® processor. In the figure below, the RoE Framer C Library, the RoE Framer Driver, and the RoE Framer IP core comprise the solution and are required for full protocol support; the RoE Framer C Example Application provides code to demonstrate the solution.

Figure 2: **RoE Framer IP Solution**



The framing and de-framing of all available antenna-carrier (user) data flows, and the corresponding real-time data control messages (when enabled), are handled in hardware. The remaining user data services can be handled by a software API library running on the embedded processor in conjunction with dedicated hardware features, such as packet timestamping at the PCS/PMA level. Because no more circuit-based interconnections are available, it is also necessary to synchronize each node through the packet network; the synchronization plane therefore relies on a PTP protocol such as *IEEE 1588 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems* (IEEE 1588), and on Synchronous Ethernet.

The RoE Framer system provides a platform to run the Linux PTP Precision Time Protocol (ptp4l) for IEEE 1588 hardware timestamping for Linux and control the hardware-based timer. The RoE Framer core can realign the user data generation to the Start of Radio Frame information transported by the synchronization plane. Control plane management relies on protocols such as SNMP and ICMP, running on an IP stack and implemented in software on the embedded processor.

The RoE Framer system deals with two different packet flows:

- A time-sensitive and high-priority flow of user plane data traffic handled by dedicated and adaptable RoE Framer hardware
- A lower-priority traffic flow, constituted by different streams and protocols, all of which can be managed by the Zynq® processor

The RoE Framer can filter each incoming downlink packet in real time, recognizing messages carrying antenna-carrier data and forwarding them to the managing hardware, while redirecting all remaining traffic to the embedded processor through a DMA interface. In the uplink direction, the RoE Framer arbitrates access to the supported Ethernet ports between the higher-priority hardware queue and the processor queue.

Unsupported Features

The RoE Framer IP core is designed to allow the implementation of fronthaul nodes relying on *eCPRI Specification v1.2* (eCPRI Specification V1.2) protocols. The table below shows the features of the standard that are not currently supported, or are only partially supported, in the IP core.

Table 1: **Unsupported and Partially Supported Features (eCPRI v1.2)**

Section in eCPRI v1.2	Comment
User Plane over IP	Partially supported. Generation of IPv4 Header Checksum and UDP_Checksum are not currently supported.
Mapping Examples	Partially supported. Only the non-concatenated case is currently supported.
Message Type #3: Generic Data Transfer	Not supported. Generic Data Transfer is not currently supported.

The following table illustrates the compliance matrix with respect to *IEEE 1914.3-2018 IEEE Standard for Radio Over Ethernet Encapsulations and Mappings* (IEEE 1914.3).

Table 2: **Unsupported and Partially Supported Features (IEEE 1914.3)**

Section in IEEE 1914.3	Comment
Sub type (subType) field	Programmable subType field supported for each antenna.
Sequence number (seqNum) field	Timestamp field not supported.
Presentation time measurement points	Supports 10 ms time intervals only.
RoE parameters	This is a higher layer function which can be added by user applications and is limited to the RoE Framer register settings.
CPRI C-plane handling	Partially supported. No specific interfaces are provided for control plane flows.
Native RoE frequency domain packet mapper	There is no specific frequency domain processing, but there is transparent Ethernet packetization for frequency domain data.
Native RoE PRACH packet	Not supported.
RoE control packet header format	Xilinx does not add the opCode byte, but this can be added as part of user data.

For the compliance matrix with respect to *O-RAN Control, User and Synchronization Plane Specification v1.0* (O-RAN Specification v1.0), see the O-RAN Support Matrix appendix.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement.The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Evaluation licenses and hardware timeout licenses are available for this core. Contact your local Xilinx sales representative for information about pricing and availability.

Note: To verify that you need a license, check the License column of the IP Catalog. Included means that a license is included with the Vivado® Design Suite; Purchase means that you have to purchase a license to use the core.

For more information about this core, visit the product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx® LogiCORE IP modules and tools, contact your local Xilinx sales representative.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

Note: IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
05/22/2019 Version 2.0	
IP Facts and Features	Updated in line with Product Guide.
12/05/2018 Version 1.0	
Initial Xilinx release.	N/A

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