PCI Express PHY

LogiCORE IP Product Guide

Vivado Design Suite

PG239 (v1.0) May 22, 2019

Table of Contents

Introduction

The Xilinx® Express PHY IP is a building block IP that allows for a PCI Express® MAC to be built as soft IP in the FPGA fabric.

The Vivado® IP catalog does not allow generation of this IP for all UltraScale™ and UltraScale+™ devices; however, if a device is selected and has the same transceiver type as the desired device (UltraScale GTH, UltraScale+ GTH or UltraScale+ GTY), the IP can then be migrated to the desired part.

Currently, the IP can be generated for the following devices:

- UltraScale+: ZU9EG (GTH), VU3P (GTY), and VU9P(GTY).
- UltraScale: KU040 (GTH), KU115 (GTH), VU440 (GTH), and VU440 ES2 (GTH).

***Note*:**

- When the IP is generated for a VU440 ES2 device, this IP should not be migrated to other devices.
- While some UltraScale devices contain GTYs, this IP does not support GTY in the UltraScale family.

Features

- Gen1 (2.5 GT/s), Gen2 (5.0 GT/s), Gen3 (8.0 GT/s), and Gen4 (16 GT/s) speeds are supported.
- UltraScale devices support 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s line rates with x1, x2, x4, x8 lane operation.
- UltraScale+ devices support 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s line rates with x1, x2, x4, x8, x16 lane operation. Additionally, they support 16.0 GT/s line rate with x1, x2, x4, x8 lane operation.
- Supports P0s low power state when configured as Gen1 or Gen2 only.
- Supports synchronous and asynchronous applications.
- Rate change between Gen1 and Gen2 is a fixed datapath implementation.
- Rate change between Gen3 is a fixed PCLK implementation.
- Low latency enabled by bypassing TX buffer.

IP Facts

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family[1]	UltraScale+™, UltraScale™
Supported User Interfaces	N/A
Resources	Performance and Resource Use web page
Provided with Core	
Design Files	Verilog
Example Design	Verilog
Test Bench	Verilog
Constraints File	Xilinx® Design Constraints (XDC)
Simulation Model	Verilog
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

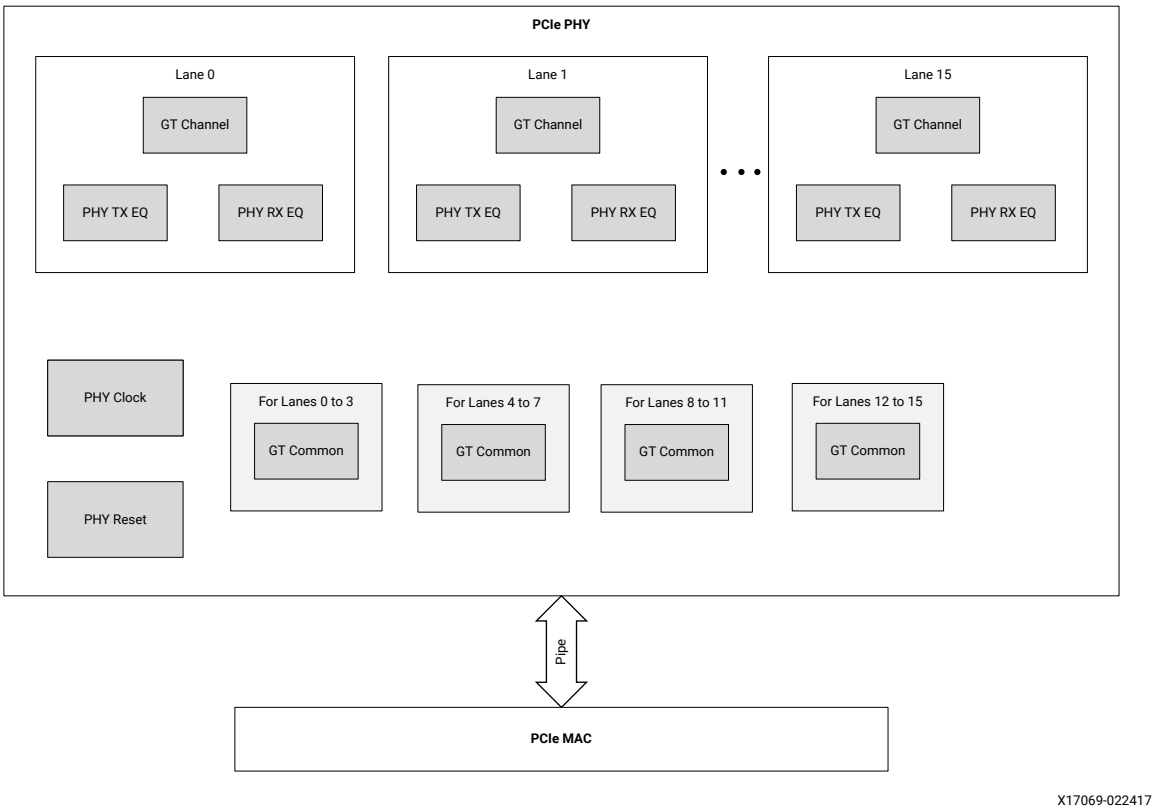
1. For a complete list of supported devices, see the Vivado® IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

This section provides a detailed description of the features, attributes, and signals associated with the PIPE interfaces of the Xilinx® PCI Express PHY IP.

The following figure is a high-level PCIe IP block diagram.

Figure 1: **High-level Block Diagram of the PCIe PHY IP**



- Lane 0 is always the master.
- One GT Common is instantiated for every quad.
- Clock and reset blocks shared by all lanes.
- The PCIe PHY IP communicates with the PCIe MAC through the PIPE interface.

Applications

The following table summarizes the recommended default features supported for different line rates.

Table 1: **Default Features Supported**

Features	Gen1	Gen2	Gen3	Gen4
Line Rate	2.5 GT/s	5 GT/s	8 GT/s	16 GT/s
PCLK Frequency	125 MHz	250 MHz	250 MHz	250MHz
2-Byte Data Width	Yes	Yes		
4-Byte Data Width			Yes	
8-Byte Data Width				Yes
CPLL	Yes			
QPLL1		Yes [1]	Yes	
QPLL0				Yes
LPM/DFE Mode	DFE [2]			
RX Elastic Buffer with Clock Correction	Yes	Yes	Yes	Yes
8b/10b Encoder and Decoder	Yes	Yes		
128b/130b Encoder and Decoder			Yes	Yes
N_FTS	255	255	255	255
UltraScale Device GT Support	GTH	GTH	GTH	N/A
UltraScale+ Device GT Support	GTH/GTY	GTH/GTY	GTH/GTY	GTH/GTY

Notes:

1. For the Gen2 speed, the default PLL option is QPLL1 in the customization GUI; you can choose either CPLL or QPLL1 also. In case of speed training down, the chosen PLL will still be active.
2. By default, DFE is enabled. You can change the value with the Form factor driven Insertion loss adjustment option in the customization GUI. For more information, see the Advanced Settings Tab.
3. A Gen4 configuration requires a -2, -2L, or -3 speed grade UltraScale+ device.

Unsupported Features

The following features are not supported in the core:

- Lane 0 (master) must not be powered down or de-activated.
- Per-lane power down is not supported.
- P0s low power state is not supported when the max speed is configured as Gen3.
- P2 low power state is not supported.
- Bypassing the RX elastic buffer is not supported.

- Gen3 equalization settings are not preserved after the rate change.
- PCIe PHY does not check or monitor for PIPE protocol errors.
- PCIe beacon transmit and receive is not supported.
- The UltraScale+™ Gen4 configuration does not support RX Lane Margining.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado® Design Suite under the terms of the Xilinx End User License.

For more information about this core, visit the PCIe PHY product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx® LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

The Xilinx® PCIe PHY IP core internally instantiates the GTY/GTH transceiver block model, which is highly configurable and tightly integrated with the programmable logic resources.

Note: UltraScale devices only support the GTH transceiver block model.

Performance and Resource Use

Resource required for the PCIe PHY IP are mentioned in the table below. These values are generated using Vivado® Design Suite for the supported devices.

Table 2: **Device Utilization – UltraScale+ Devices**

Family	Speed	Lane	Receiver Detect	XCVU3P/XCZU9EG		
				LUTs	FFs	LUT-FF Pairs
UltraScale+	Gen1	x1	Default	118	264	89
	Gen2	x1	Default	117	268	87
	Gen3	x1	Default	116	268	74
	Gen4	x1	Default	340	615	288
	Gen1	x2	Default	215	496	161
	Gen2	x2	Default	216	496	159
	Gen3	x2	Default	216	496	148
	Gen4	x2	Default	655	1195	555
	Gen1	x4	Default	406	960	304
	Gen2	x4	Default	406	952	297
	Gen3	x4	Default	408	952	296
	Gen4	x4	Default	1284	2339	1075
	Gen1	x8	Default	790	1888	579
	Gen2	x8	Default	796	1868	569
	Gen3	x8	Default	796	1868	592
	Gen4	x8	Default	2537	4633	2149
	Gen1	x16	Default	1601	3744	1158
	Gen2	x16	Default	1606	3700	1201
	Gen3	x16	Default	1606	3700	1168

Table 3: **Device Utilization – UltraScale Devices**

Family	Speed	Lane	Receiver Detect	XCVU440/XCKU040 – Production Part			XCVU440 -ES2 Part		
				LUTs	FFs	LUT-FF Pairs	LUTs	FFs	LUT-FF Pairs
UltraScale	Gen1	x1	Default	104	222	77	304	459	200
	Gen2	x1	Default	107	226	77	306	462	204
	Gen3	x1	Default	106	226	79	308	463	202
	Gen1	x2	Default	176	393	128	606	893	390
	Gen2	x2	Default	177	389	129	608	893	388
	Gen3	x2	Default	177	389	126	607	893	379
	Gen1	x4	Default	315	735	228	1,182	1,761	748
	Gen2	x4	Default	317	715	221	1,188	1,761	760
	Gen3	x4	Default	316	715	227	1,188	1,753	764
	Gen1	x8	Default	591	1419	419	2,357	3,497	1,505
	Gen2	x8	Default	593	1371	431	2,357	3,497	1,508
	Gen3	x8	Default	592	1371	422	2,343	3,476	1,488

Notes:

1. No DSP48s/36k block RAMs/18k block RAMs were used in the PCIe PHY IP.

Port Descriptions

The following tables describe the supported PIPE signals by the PCIe PHY IP. For additional details, refer to the PIPE specification. The signals described in this section are based on a single lane application. Signals can be per-lane, or per-design. If not indicated in the description, the default is per-design. Per-design indicates that one signal controls all lanes (0 to N-1 Lane).

A per-lane signal on the PCIe PHY IP is in a form of {LaneN-1[Width-1:0], ...Lane1 [Width-1:0], Lane0[Width-1:0]}.

The Gen3/Gen4 TX and RX equalization defined here is different from the PIPE specification. The custom Gen3/Gen4 equalization scheme described here must be used. For more details, refer to Equalization Sequences.

Assist signals are used to support the functionality of PCIe PHY IP according to the MAC LTSSM states.

Clock and Rest Signals Interface Ports

Table 4: **Clock and Reset Signals**

Port Name	Width	I/O	Clock	Description
phy_refclk	1	Input	refclk	Reference clock for fabric logic. This clock must be driven directly from a BUFG_GT. The recommended reference clock is 100 MHz. This clock is expected to be free running and stable. This reference clock can be either synchronous or asynchronous. In synchronous mode, the PPM is 0. In asynchronous mode, the PPM is up to ±300 or 600 PPM worst case. • 100 MHz (default) • 125 MHz • 250 MHz
phy_gtrefclk	1	Input	refclk	Reference clock for GT. This clock must be driven directly from an IBUFDS_GTE3/IBUFDS_GTE4. Same definition and frequency as phy_refclk.
phy_rst_n	1	Input	Asynchronous	When logic Low, this signal resets the PHY. This must be connected to PCIe PERST_N.
pipe_coreclk	1	Output	coreclk	Core clock options: • 250 MHz (default) • 500 MHz
pipe_userclk	1	Output	userclk	User clock options: • 62.5 MHz • 125 MHz • 250 MHz (default) • 500 MHz pipe_userclk is edge-aligned and phase-aligned to pipe_coreclk.
pipe_mcapclk	1	Output	mcapclk	Additional clock options: • 62.5 MHz • 125 MHz (default) pipe_mcapclk is edge-aligned and phase-aligned to pipe_coreclk.
phy_pclk	1	Output	pclk	PIPE interface clock options: • 125 MHz: Gen1 operating speed • 250 MHz: Gen2, Gen3, Gen4 operating speed phy_pclk is edge-aligned, but not phase-aligned to pipe_coreclk and pipe_userclk.

TX Data Signals for UltraScale+ Devices Interface Ports

Table 5: **TX Data Signals for Ultrascale+ Devices Interface Ports**

Port Name	Width	I/O	Clock Domain	Description
phy_txdata[63:0]	64	Input	pclk	Parallel data input. Bits [63:32] are used for Gen4 only and must be ignored in Gen1, Gen2, and Gen3. Bits[31:16] are used for Gen3 only and must be ignored in Gen1 and Gen2. Per-lane.
phy_txdatak[1:0]	2	Input	pclk	Indicates whether TXDATA is control or data for Gen1 and Gen2 only. Per-lane. • 0b: Data • 1b: Control
phy_txdata_valid	1	Input	pclk	This signal allows the MAC to instruct the PHY to ignore TXDATA for one PCLK cycle. When logic High, this indicates the PHY will use TXDATA. When logic Low, this indicates the PHY will not use TXDATA for one PCLK cycle. Gen3 and Gen4 only. Per-lane.
phy_txstart_block	1	Input	pclk	This signal allows the MAC to tell the PHY the starting byte for a 128b block. The starting byte for a 128b block must always start at bit [0] of TXDATA. Gen3 and Gen4 only. Per-lane.
phy_txsync_header[1:0]	2	Input	pclk	Provide the sync header for the PHY to use the next 130b block. The PHY reads this value when the txsync_block is asserted. Gen3 and Gen4 only. Per-lane.
phy_tx[p/n]	1	Output	Serial	The differential transmitter outputs. Per-lane.

TX Data Signals for UltraScale Devices Interface Ports

Table 6: **TX Data Signals for UltraScale Devices**

Port Name	Width	I/O	Clock domain	Description
phy_txdata[31:0]	32	Input	pclk	Parallel data input. Bits [31:16] are used for Gen3 only and must be ignored in Gen1 and Gen2. Per-lane.
phy_txdatak[1:0]	2	Input	pclk	Indicates whether TXDATA is control or data for Gen1 and Gen2 only. Per-lane. • 0b: Data • 1b: Control
phy_txdata_valid	1	Input	pclk	This signal allows the MAC to instruct the PHY to ignore TXDATA for one PCLK cycle. When logic High, this indicates the PHY will use TXDATA. When logic Low, this indicates the PHY will not use TXDATA for one PCLK cycle. Gen3 only. Per-lane.

Table 6: **TX Data Signals for UltraScale Devices** *(cont'd)*

Port Name	Width	I/O	Clock domain	Description
phy_txstart_block	1	Input	pclk	This signal allows the MAC to tell the PHY the starting byte for a 128b block. The starting byte for a 128b block must always start at bit [0] of TXDATA. Gen3 only. Per-lane.
phy_txsync_header[1:0]	2	Input	pclk	Provide the sync header for the PHY to use the next 130b block. The PHY reads this value when the txsync_block is asserted. Gen3 only. Per-lane.
phy_tx[p/n]	1	Output	Serial	The differential transmitter outputs. Per-lane.

RX Data Signals for Ultrascale+ Devices Interface Ports

Table 7: **RX Data Signals for UltraScale+ Devices**

Port Name	Width	I/O	Clock Domain	Description
phy_rx[p/n]	1	Input	Serial	The differential receiver inputs to the PHY. Per-lane.
phy_rxdata[63:0]	64	Output	pclk	PIPE data output from receiver. Bits[63:32] are used for Gen4 only and must be ignored in Gen1, Gen2, and Gen3. Bits[31:16] are used for Gen3 only and must be ignored in Gen1 and Gen2. Per-lane.
phy_rxdatak[1:0]	2	Output	pclk	Indicates whether RXDATA is control or data. Gen1 and Gen2 only. Per-lane. • 0b: Data • 1b: Control
phy_rxdata_valid	1	Output	pclk	This signal allows the PHY to instruct the MAC to ignore RXDATA for one pclk cycle. When logic High, this indicates to use RXDATA. When logic Low, this indicates to ignore RXDATA for one pclk cycle. Gen3 and Gen4 only. Per-lane.
phy_rxstart_block[1:0]	2	Output	pclk	This signal allows the PHY to tell the MAC the starting byte for a 128b block. • 00b: Data with no start • 01b: A block starts at lower 32 bits • 10b: A block starts at upper 32 bits, inactive when operating at Gen3 speed. • 11b: Lower 32 bits has valid data and upper 32 bits are invalid, inactive when operating at Gen3 speed. Gen3 and Gen4 only. Per-lane.

Table 7: **RX Data Signals for UltraScale+ Devices** *(cont'd)*

Port Name	Width	I/O	Clock Domain	Description
phy_rxsync_header[1:0]	2	Output	pclk	Provide the sync header for the MAC to use the next 128b block. The MAC reads this value when the RXSYNC_BLOCK is asserted. Gen3 and Gen4 only. Per-lane.

RX Data Signals for Ultrascale Devices Interface Ports

Table 8: **RX Data Signals for UltraScale Devices**

Port Name	Width	I/O	Clock Domain	Description
phy_rx[p/n]	1	Input	Serial	The differential receiver inputs to the PHY. Per-lane.
phy_rxdata[31:0]	32	Output	pclk	PIPE data output from receiver. Bits[31:16] are used for Gen3 only and must be ignored in Gen1 and Gen2. Per-lane.
phy_rxdatak[1:0]	2	Output	pclk	Indicates whether RXDATA is control or data. Gen1 and Gen2 only. Per-lane. • 0b: Data • 1b: Control
phy_rxdata_valid	1	Output	pclk	This signal allows the PHY to instruct the MAC to ignore RXDATA for one pclk cycle. When logic High, this indicates to use RXDATA. When logic Low, this indicates to ignore RXDATA for one pclk cycle. Gen3 only. Per-lane.
phy_rxstart_block	1	Output	pclk	This signal allows the PHY to tell the MAC the starting byte for a 128b block. The starting byte for a 128b block must always start at bit [0] of RXDATA. Gen3 only. Per-lane.
phy_rxsync_header[1:0]	2	Output	pclk	Provide the sync header for the MAC to use the next 128b block. The MAC reads this value when the RXSYNC_BLOCK is asserted. Gen3 only. Per-lane.

Command Signals Interface Ports

Table 9: **Command Signals**

Port Name	Width	I/O	Clock Domain	Description
phy_txdetectrx	1	Input	pclk	Tells the PHY to perform receiver detection when this signal is logic High and POWERDOWN is in P1 low power state. Receiver detection is complete when phystatus asserts for one pclk cycle. The status of receiver detection is indicated in rxstatus when phystatus is logic High for one pclk cycle. • rxstatus = 000b: Receiver not Present • rxstatus = 001b: Receiver Present
phy_txelecidle	1	Input	pclk	Forces the tx[p/n] to electrical idle when this signal is logic High. During electrical idle, tx[p/n] are driven to the DC common mode voltage. Per-lane.
phy_txcompliance	1	Input	pclk	Sets the running disparity to negative when this signal is logic High. Used when transmitting the PCIe compliance pattern. Per-lane.
phy_rxpolarity	1	Input	pclk	Requests the PHY to perform polarity inversion on the received data when this signal is logic High. Per-lane.
phy_powerdown[1:0]	2	Input	pclk	Request PHY to enter power saving state or return to normal power state. Power management is complete when PHYSTATUS asserts for one PCLK cycle. • 00b: P0, normal operation. • 01b: P0s, power saving state with low recovery time latency. • 10b: P1, power saving state with longer recovery time latency. • 11b: P2, lowest power state. P2 not supported.
phy_rate[1:0]	2	Input	pclk	Request the PHY to perform a dynamic rate change. Rate change is complete when PHYSTATUS asserts for one PCLK cycle. rxvalid, rxdata, and rxstatus must be ignored while the PHY is in rate change. • 00b: Gen1 • 01b: Gen2 • 10b: Gen3 In the simulation mode (PHY_SIM_EN = TRUE), PHY status assertion takes about 45 us for Gen3 speed change.

Status Signals Interface Ports

Table 10: **Status Signals**

Name	Width	Direction	Clock Domain	Description
phy_rxvalid	1	Output	pclk	Indicates symbol lock and valid data on rxdata when logic High. This signal must be ignored during reset and rate change Gen1 and Gen2 only. Per-lane.
phy_phystatus	1	Output	pclk /Asynchronous	Used to communicate completion of several PIPE operations including reset, receiver detection, power management, and rate change. Except for reset, this signal indicates done when asserted for one pclk cycle. This signal is held High and asynchronous during reset. In error situations, such as PHY not responding with PHYSTATUS, the MAC should perform the necessary error recovery. Per-lane.
phy_phystatus_rst	1	Output	pclk /Asynchronous	Similar to phystatus, except this port is used to communicate completion of reset only. This signal is HIGH immediately upon reset. After the PHY and GT resets are complete,this signal transitions from High to Low.
phy_rxelecidle	1	Output	Asynchronous	RXELECIDLE = High indicates RX electrical idle detected. Gen1 and Gen2 only. Per-lane.
phy_rxstatus[2:0]	3	Output	pclk	Encodes RX status and error codes for the RX data. Per-lane. • 000b: Received data OK • 001b: 1 SKP added • 010b: 1 SKP removed • 011b: Receiver detected • 100b: 8b/10b (Gen1/Gen2) or 128b/130b (Gen3) decode error • 101b: Elastic buffer overflow • 110b: Elastic buffer underflow • 111b: Receive disparity error (Gen1/Gen2)

TX Driver Signal Interface Ports

Table 11: **TX Driver Signals for Gen1 and Gen2**

Name	Width	Direction	Clock Domain	Description
phy_txmargin[2:0]	3	Input	pclk	Selects TX voltage levels. The recommendation is to set this port to 000b for the normal operating voltage range. • 000b: Programmable (default) • 001b: Programmable • 010b: Programmable • 011b: Programmable • 100b: Programmable • 101b: Programmable • 110b: Programmable • 111b: Programmable
phy_txswing	1	Input	pclk	Controls TX voltage swing level. Gen1 and Gen2 only. • 0b: Full swing (default) • 1b: Low swing
phy_txdeemph	1	Input	pclk	Selects TX de-emphasis. Gen1 and Gen2 only. • 0b: -6.0 dB de-emphasis • 1b: -3.5 dB de-emphasis (default)

TX Equalization Interface Ports

The Gen3/Gen4 TX and RX equalization defined here is different from the PIPE specification. The custom Gen3/Gen4 equalization scheme described here must be used. For more details, refer to Equalization Sequences.

Table 12: **TX Equalization Signals for Gen3 and Gen4**

Name	Width	I/O	Clock Domain	Description
phy_txeq_ctrl[1:0]	2	Input	pclk	TX equalization control. Must set back to 00b when txeq_done = 1b is detected. Gen3 only for UltraScale™ devices. Gen3 and Gen4 only for UltraScale+ devices. Per-lane. • 00b: Idle • 01b: TX preset • 10b: TX coefficient • 11b: TX query

Table 12: **TX Equalization Signals for Gen3 and Gen4** *(cont'd)*

Name	Width	I/O	Clock Domain	Description
phy_txeq_preset[3:0]	4	Input	pclk	Set the TX equalization to one of the defined preset when txeq_ctrl = 01b. Must use txeq_ctrl to change the preset, otherwise the default preset 0100b is used. Gen3 only for UltraScale devices. Gen3 and Gen4 only for UltraScale+ devices. Per-lane.
phy_txeq_coeff[5:0]	6	Input	pclk	Set the TX equalization to a custom coefficient when txeq_control = 10b. Three consecutive pclk cycles are required to register the new 18-bit TX coefficient. • The first pclk cycle is used to register pre-cursor. • The second pclk cycle is used to register main-cursor. • The third pclk cycle is used to register post-cursor. Gen3 only for UltraScale devices. Gen3 and Gen4 only for UltraScale+ devices. Per-lane.
phy_txeq_fs[5:0]	6	Output	pclk	Indicates the full swing of the TX driver. Static value based on characteristics of TX driver. Gen3 only for UltraScale devices. Gen3 and Gen4 only for UltraScale+ devices.
phy_txeq_lf[5:0]	6	Output	pclk	Indicates the low frequency of the TX driver. Static value based on characteristics of TX driver. Gen3 only for UltraScale devices. Gen3 and Gen4 only for UltraScale+ devices.

Table 12: **TX Equalization Signals for Gen3 and Gen4**

Preset	Pre-shoot (dB)	De-emphasis (dB)
0000b	0	6
0001b	0	3.5
0010b	0	4.5
0011b	0	2.5
0100b	0	0
0101b	2	0
0110b	2.5	0
0111b	3.5	6
1000b	3.5	3.5
1001b	3.5	0
1010b	0	9.5
Others	Reserved	

Table 12: **TX Equalization Signals for Gen3 and Gen4** *(cont'd)*

Name	Width	I/O	Clock Domain	Description
phy_txeq_new_coeff[17:0]	18	Output	pclk	Shows the status of the current TX equalization coefficient. Gen3 only. Per-lane. • [17:12]: Pre-cursor. • [11:6]: Main-cursor. • [5:0]: Post-cursor.
phy_txeq_done	1	Output	pclk	This port is High when TXEQ is equalization done. Single cycle done indicator for `txeq_control`. Gen3 only for UltraScale devices. Gen3 and Gen4 only for UltraScale+ devices. Per-lane.

RX Equalization Signals Interface Ports

Table 13: **RX Equalization Signals for Gen3 and Gen4**

Name	Width	I/O	Clock Domain	Description
phy_rxeq_ctrl[1:0]	2	Input	pclk	RX equalization control. Must set back to 00b when rxeq_done = 1b detected. Gen3 only for UltraScaleUltraScale™ devices. Gen3 and Gen4 only for UltraScale+ devices. Per-lane. • 00b: Idle • 01b: Reserved • 10b: RX EQ • 11b: RX EQ Bypass
phy_rxeq_txpreset[3:0]	4	Input	pclk	Link partner status for TX preset. Gen3 only for UltraScale devices. Gen3 and Gen4 only for UltraScale+ devices. Per-lane.
phy_rxeq_preset_sel	1	Output	pclk	This output port serves indications as Coefficient or preset when rxeq_done = 1b. Gen3 only for UltraScale devices. Gen3 and Gen4 only for UltraScale+ devices. Per-lane. • 0b: Coefficient • 1b: Preset
phy_rxeq_new_txcoeff[17:0]	18	Output	pclk	This is presented to the link partner to request new TX coefficient or preset. Valid only when RXEQ_DONE is High. When indicating preset, only the lower four bits are valid. Gen3 only for UltraScale devices. Gen3 and Gen4 only for UltraScale+ devices. Per-lane.
phy_rxeq_adapt_done	1	Output	pclk	RX equalization adaptation done. Single PCLK cycle done indicator for rxeq_control = 10b and 11b. If both rxeq_adapt_done and rxeq_done are High, then RX equalization is successfully done. If rxeq_adapt_done is Low and rxeq_done is High, then RX equalization must be requested again. Gen3 only for UltraScale devices. Gen3 and Gen4 only forUltraScale+ devices. Per-lane.

Table 13: **RX Equalization Signals for Gen3 and Gen4** *(cont'd)*

Name	Width	I/O	Clock Domain	Description
phy_rxeq_done	1	Output	pclk	RX equalization done. Single pclk cycle done indicator for rxeq_control. Must set pipe_rxeq_control back to 00b when pipe_rxeq_done = High is detected. RX equalization must be re-initiated if rxeq_adapt_done is not High. Gen3 only for UltraScale devices. Gen3 and Gen4 only for UltraScale+ devices. Per-lane.

Assist Signal Interface Ports

Assist signals are used to support the functionality of PCIe PHY IP according to the MAC LTSSM states.

Table 14: **Assist Signal**

Name	Width	Direction	Clock Domain	Description
as_mac_in_detect	1	Input	pclk	Tell the PHY to switch the Receiver Termination between VTT and GND. Set to 1 when MAC is in: • Detect.Quiet • Detect.Active Set to 0 when in other states.
as_cdr_hold_req	1	Input	pclk	Tell the PHY when to hold CDR. Set to 1 when MAC is in: • Recovery.Speed • L1.Entry • L1.Idle • Loopback.Speed • Loopback.Entry Set to 0 when in other states.

Notes:

1. The LTSSM states and substates mentioned in the description above are indicative. Your configured MAC implementation might not have the same substates as indicated. Generate the above mentioned assist signals as per states implemented in your configured MAC.

ASPM Assist Signal Interface Ports

Table 15: **ASPM Assist Signal**

Name	Width	I/O	Clock Domain	Description
as_mac_in_L0	1	Input	pclk	Tells the PHY when MAC is in L0 state. • Set to 1 when ltssm state is L0. • Set to 0 when in other states. This input is valid only when ASPM Optionality is selected as L0s_supported in UltraScale+™ devices

Table 15: **ASPM Assist Signal** *(cont'd)*

Name	Width	I/O	Clock Domain	Description
cfg_rx_pm_state	2	Input	pclk	Current RX Active State Power Management L0s State. Encoding is listed below and valid when ltssm_state is indicating L0: • RX_NOT_IN_L0s =0, • RX_L0s_ENTRY =1, • RX_L0s_IDLE =2, • RX_L0s_FTS =3 This input is only valid when ASPM Optionality is selected as L0s_supported in UltraScale+ devices.

Notes:

1. The states and substates mentioned in this table are indicative. Your configured MAC implementation might not have the same substates as indicated. Generate the above mentioned assist signals as per states implemented in your configured MAC.

GT Specific Interface Ports

Table 16: **GT Specific Ports For UltraScale+ Devices Only**

Name	Width	I/O	Clock Domain	Description
gt_gtpowergood	1	Output	async	GT power good indicator, connects to GTPOWERGOOD on transceiver channel primitives. Per Lane. This signal must be connected to the CE pin of the BUFG_GT that is driven by IBUFDS_GTE4(ref clock). (Make sure that all BUFG_GTs driven by the IBUFGS_GTE4 have the same CE/CLR pins)
gt_drpaddr	10	Input	refclk	GT Wizard DRP address. Per-lane
gt_drpen	1	Input	refclk	GT Wizard DRP Enable. Per-lane
g_drpwe	1	Input	refclk	GT Wizard DRP write/read. Per-lane
gt_drpdi	16	Input	refclk	GT Wizard DRP data in. Per-lane
gt_drprdy	1	Output	refclk	GT Wizard DRP ready. Per-lane
gt_drpdo	16	Output	refclk	GT Wizard DRP data out. Per-lane

Designing with the Core

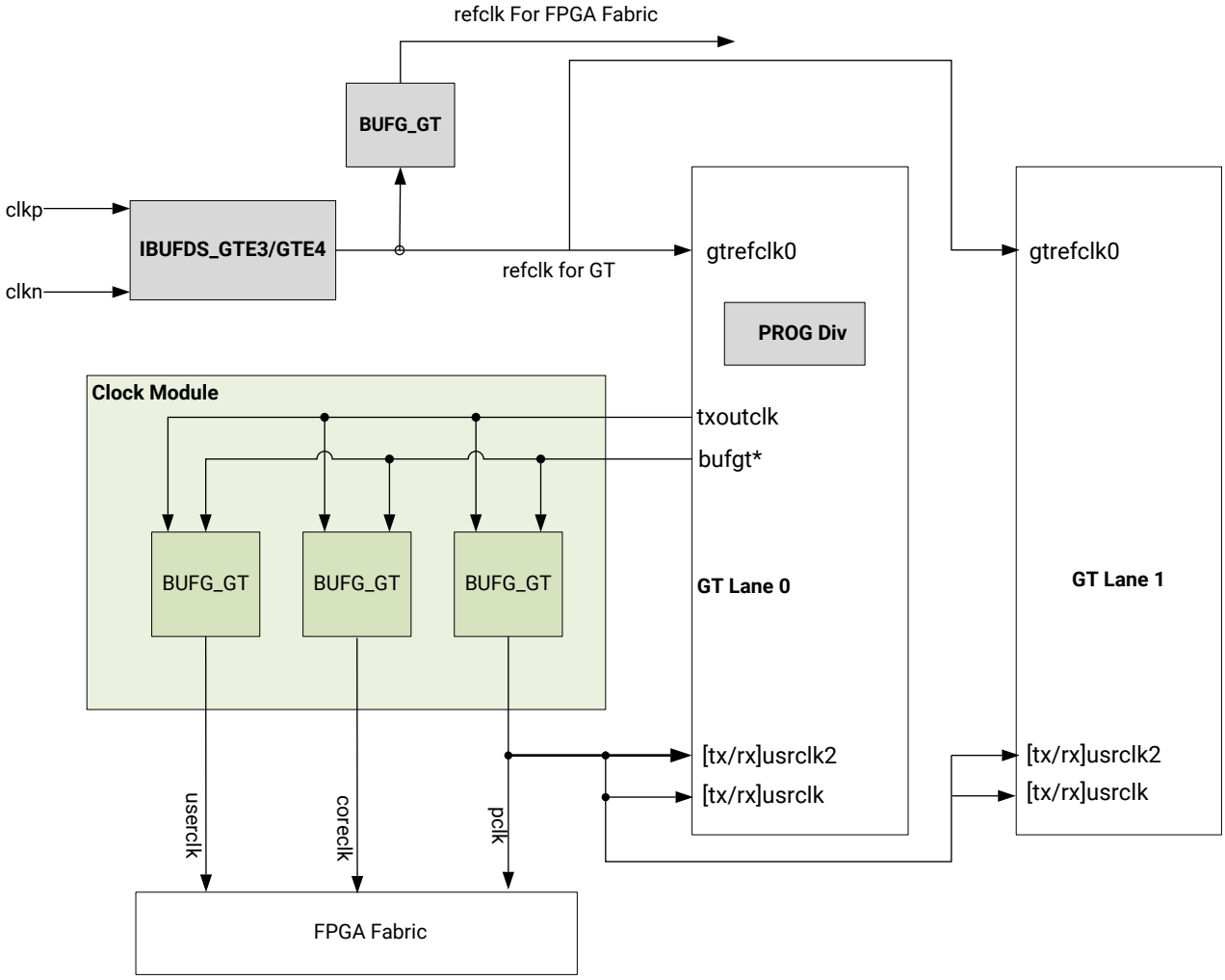
This section includes guidelines and additional information to facilitate designing with the core.

Clocking

- PCI Express® PHY IP GTH/GTY can be configured to support PCIe® applications with 100 MHz, 125 MHz, or 250 MHz reference clock.
- The reference clock can be synchronous or asynchronous.
- The `phy_pclk` is the primary clock for the PIPE interface, FPGA fabric, and GTH/GTY [TX/RX] `usrclk` and [TX/RX] `usrclk2`.
- In addition to `phy_pclk`, two other clocks (`phy_coreclk` and `phy_userclk`) are available to support the PCIe MAC
- `BUFG_GTs` are used to generate these clocks, so MMCM will not be required.
- The source of the GTH/GTY reference clock must come directly from IBUFDS_GTE4 for UltraScale+ devices and from IBUDS_GTE3 for UltraScale devices.
- To use the reference clock for FPGA fabric, another `BUFG_GT` must be used.
- The `gt_gtpowergood` output port of the PCIe PHY IP must drive the CE pin of BUFG_GT.

The following figure shows an x2 PCIe architecture example.

Figure 2: **Clock Architecture**



X16370-040717

For more information on PHY IP Clocking, refer to the *Clocking* section in the *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213).

Resets

To successfully reset UltraScale GTH for PCIe® applications, the recommended PCIe reset scheme should be used.

- It is recommended that the MAC or upper layer reset the PHY after power-on and fatal error conditions.

- The reference clock must be stable during reset.
- Once system reset is detected and synchronized, the PHY must assert `phystatus`.

The following is an example of a x1 PCIe reset procedure:

1. Stay in IDLE state until system reset is released.
2. Assert [CPLL/QPLL] `reset`, [TX/RX] `progdivreset` and GT[TX/RX] `reset` until GT `powergood` is active-High.
3. Release [CPLL/QPLL] `reset` and wait for [CPLL/QPLL] `lock` to go active-High.
4. Release [TX/RX] `progdivreset` and wait for [TX/RX] `progdivresetdone` to go active-High.
5. Release GT[TX/RX] `reset`, assert [TX/RX] `userrdy` and wait for [TX/RX] `resetdone` to go active-High.
6. Start TX SYNC alignment. Extend `txsync_start` to four `refclk` cycles.
7. Wait for TXSYNC alignment to be done.
8. Wait for `phystatus` to get deasserted.
9. Connect the `phystatus_rst` output (communicates the completion of reset sequence) from the PHY to the PCIe MAC.
10. PCIe MAC reset is complete.

MAC Requirements

For the MAC to function properly with the PCIe PHY IP, it is necessary that the MAC satisfies these requirements:

- RX lane-to-lane `deskew` must be handled by the PCIe MAC.
- PCIe MAC should not depend on `rxelecidle` low-to-high transition.
- RX electrical idle entry must be inferred by the PCIe MAC.
- TX SKP OS must be 16 symbols for Gen3.

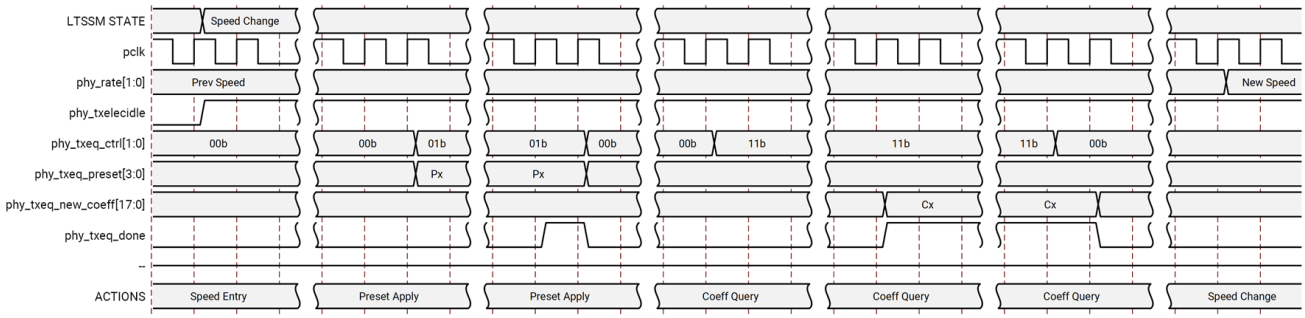
Equalization Sequences

This section describes the equalization sequences of the PCIe PHY IP.

Preset Apply During Speed Change

The following figure shows the TX Equalization interface signals during the speed change. It includes Preset Apply (`phy_txeq_ctrl = 2'b01`) and Coefficient Query (`phy_txeq_ctrl = 2'b11`). The speed change is performed in LTSSM Recovery.Speed and LTSSM Polling.Compliance states. Preset Apply step must be performed after asserting `phy_txelecidle` and before driving `phy_rate` to the new speed.

Figure 3: **TX Equalization Interface Signals during Speed Change (Preset Apply)**

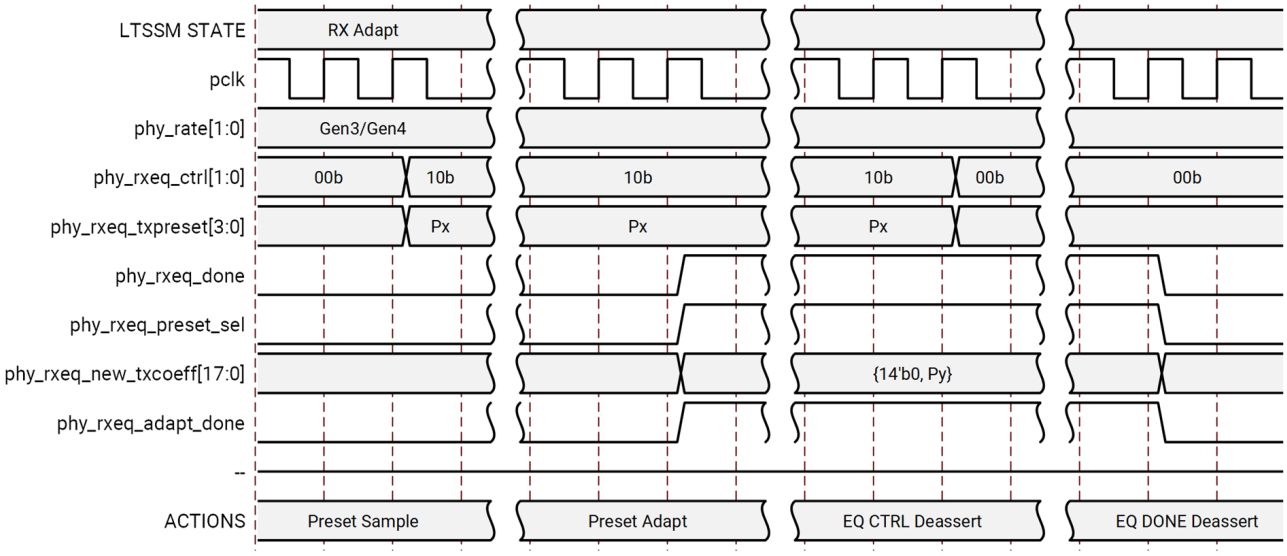


RX Adapt

The following figures describe the RX Equalization interface signals during the RX adapt. RX Adapt is performed in Phase 2 of the LTSSM Recovery.Equalization state for the Upstream Port and Phase 3 of the LTSSM Recovery.Equalization state for the Downstream Port. It is composed of two steps: a) New Proposal, and b) Adaptation, in that order.

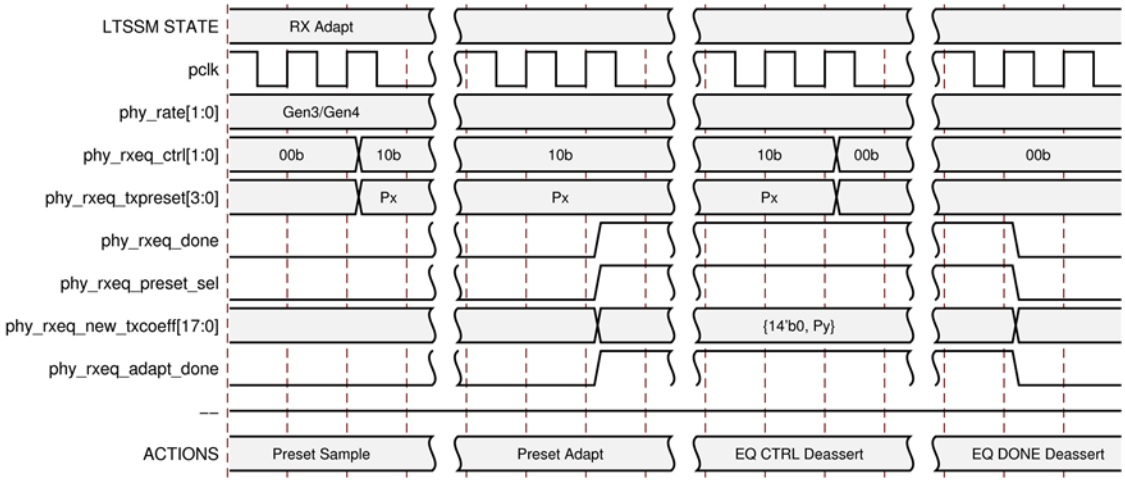
The following figure shows the New Proposal step where RX purposes a new preset (`phy_rxeq_done = 1'b1` and `phy_rxeq_adapt_done = 1'b0`) upon a TX preset request (`phy_rxeq_txpreset` with `phy_rxeq_ctrl= 2'b10`).

Figure 4: **RX Equalization Interface Signals during RX Adapt (New Proposal)**



The following figure shows the Adaptation step where RX adapts the preset (`phy_rxeq_done` = `1'b1` and `phy_rxeq_adapt_done` = `1'b1`) which TX requests (`phy_rxeq_txpreset` with `phy_rxeq_ctrl`= `2'b10`).

Figure 5: **RX Equalization Interface Signals during RX Adapt (Adapted)**

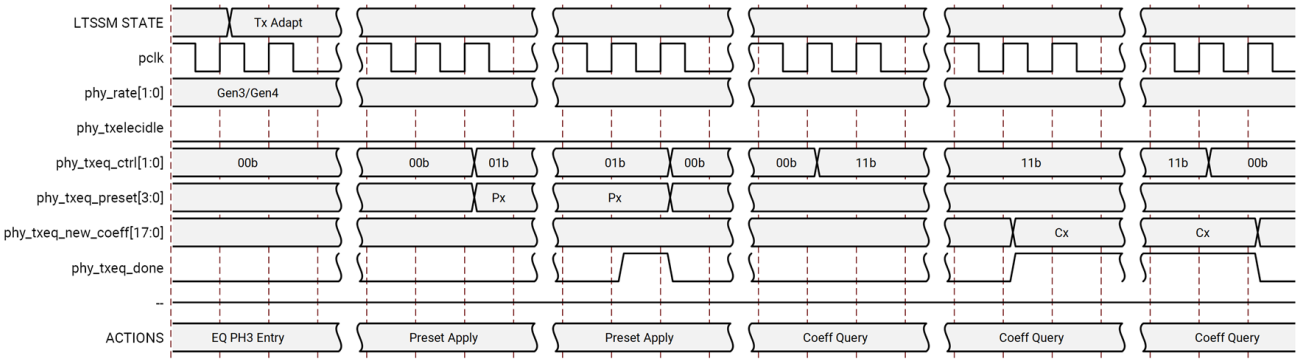


TX Adapt

The following figures describe the TX Adapt steps. TX Adapt is performed in Phase 3 of the LTSSM Recovery. Equalization state for the Upstream Port and Phase 2 of the LTSSM Recovery. Equalization state for the Downstream Port.

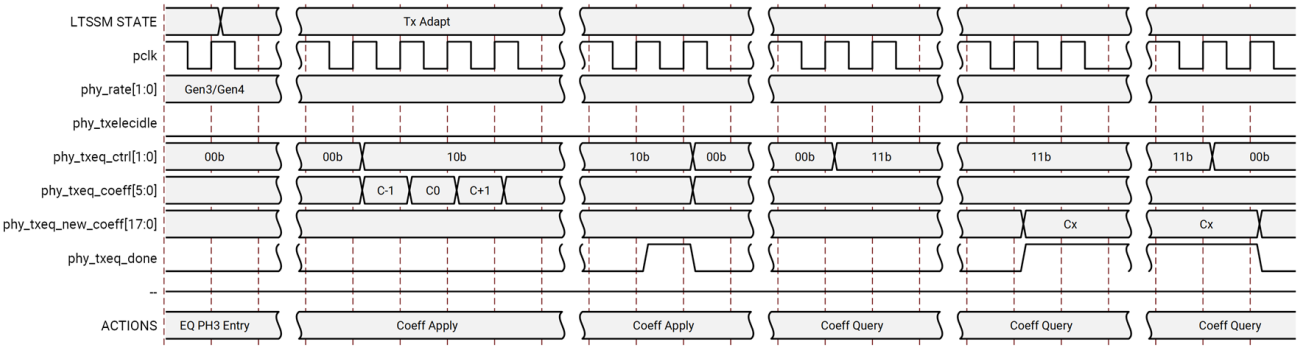
The following figure shows the New Proposal step where RX purposes a new preset (`phy_rxeq_done` = `1'b1` and `phy_rxeq_adapt_done` = `1'b0`) upon a TX preset request (`phy_rxeq_txpreset` with `phy_rxeq_ctrl` = `2'b10`).

Figure 6: **TX Equalization Interface Signals during TX Adapt (Preset)**



The following figure shows the TX Adapt step when receiving Coefficients. It includes Coefficient Apply (`phy_txeq_ctrl` =`2'b10`) and Coefficient Query (`phy_txeq_ctrl` = `2'b11`).

Figure 7: **TX Equalization Interface Signals during TX Adapt (Coefficients)**



Design Flow Steps

This section describes customizing and generating the core, constraining the core, and the simulation, synthesis, and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
- *Vivado Design Suite User Guide: Designing with IP* (UG896)
- *Vivado Design Suite User Guide: Getting Started* (UG910)
- *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado® Design Suite.

Targeted Supported Devices

The main purpose of this IP is to enable you to generate the PHY wrappers, which can be used with any UltraScale™ or UltraScale+™ devices.

- UltraScale+ device family supports both GTH and GTY transceivers.
  - The UltraScale+ GTH PHY wrapper can be generated using the ZU9EG device.
  - The UltraScale+ GTY PHY wrapper can be generated using the VU3P or VU9P device.
- Similarly, UltraScale device family supports only GTH transceivers.
  - The UltraScale GTH PHY wrapper can be generated using the KU040/KU115 device.
  - The VU440 device from UltraScale family is also supported in PHY IP; it requires a different set of wrapper files.

In summary, though a limited number of devices are supported by this IP, the generated IP targeting the supported device can be migrated easily to other devices.

Customizing the Core

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

- Select the IP from the Vivado® IP catalog.
- Double-click the selected IP or select the **Customize IP** command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the *Vivado Design Suite User Guide: Getting Started* (UG910).

***Note*:** Figures in this chapter are illustrations of the Vivado Integrated Design Environment (IDE). The layout depicted here might vary from the current version.

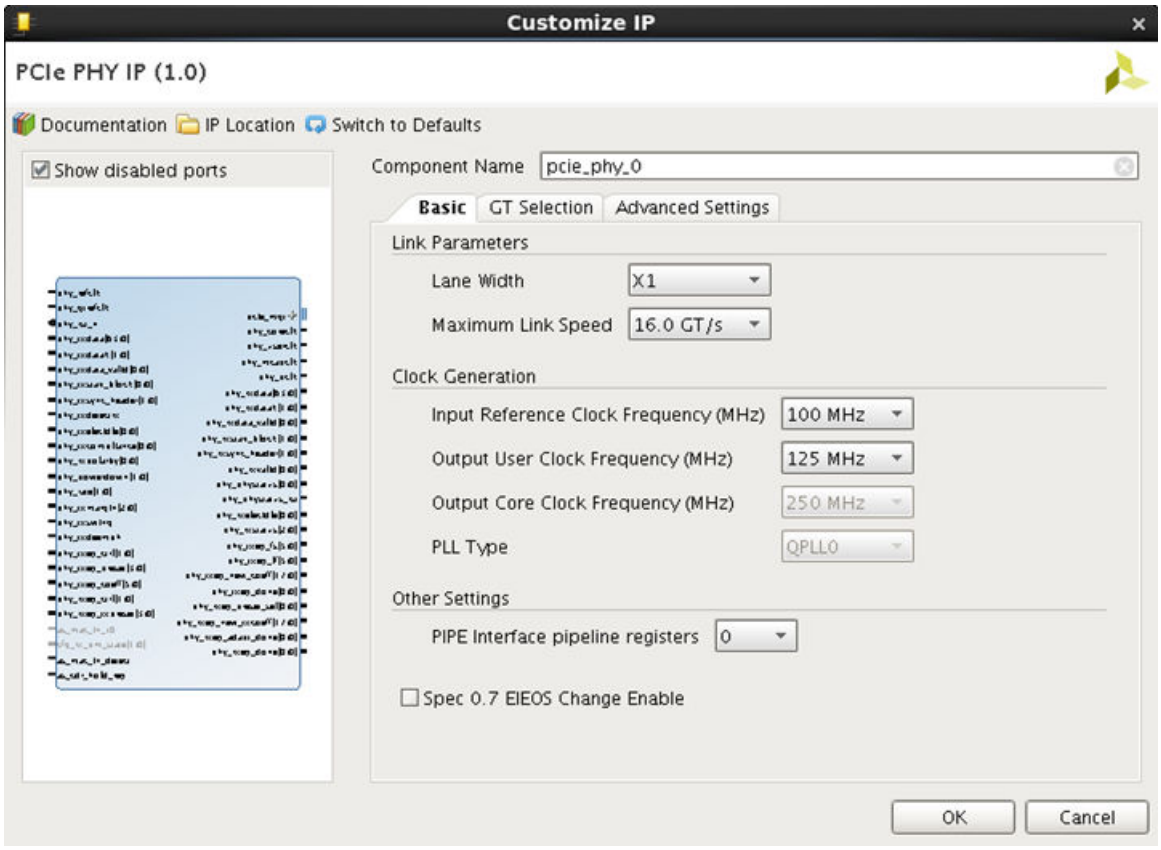
The Customize IP dialog box for the PCIe® PHY IP for UltraScale+™ devices consists of the following tabs:

1. Basic Tab
2. GT Selection Tab
3. Advanced Settings Tab

Basic Tab

The initial customization screen is used to define the basic parameters for the core, including the component name, reference clock frequency, lane width, and speed.

Figure 8: **Basic Tab**



- **Component Name:** It is the base name of the output files generated for the core. The name must begin with a letter and can be composed of these characters: a to z, 0 to 9, and "_."
- **Lane Width:** The core requires the selection of the initial lane width. Supported lane widths are x1, x2, x4, x8, and x16 (UltraScale+™devices only).
- **Maximum Link Speed:** The core allows you to select the Maximum Link Speed supported by the device. Supported link speeds are:
  - 2.5 Gb/s, 5.0 Gb/s, and 8.0 Gb/s for UltraScale devices.
  - 2.5 Gb/s, 5.0 Gb/s, 8.0 Gb/s and 16.0 Gb/s for UltraScale+ devices.
- **Input Reference Clock Frequency:** Selects the input frequency of the reference clock provided on `sys_clk`. It is the GT REFCLK frequency for the IP. Supported values are 100 MHz, 125 MHz, and 250 MHz. For important information about clocking, see Clocking.
- **Output User Clock Frequency:** Selects the frequency of the output USERCLK that can be used by the PCIe MAC.

Table 17: **User Clock Options**

Speed	Lane	UltraScale+ User Clock (in MHz)	UltraScale User Clock (in MHz)
Gen1	x1	62.5, 125, 250	62.5, 125, 250
	x2	62.5, 125, 250	62.5, 125, 250
	x4	62.5, 125, 250	125, 250
	x8	62.5, 125, 250	125, 250
	x16	62.5, 125, 250	N/A
Gen2	x1	62.5, 125, 250	62.5, 125, 250
	x2	62.5, 125, 250	125, 250
	x4	62.5, 125, 250	125, 250
	x8	62.5, 125, 250	125, 250
	x16	62.5, 125, 250	N/A
Gen3	x1	62.5, 125, 250	125, 250
	x2	62.5, 125, 250	125, 250
	x4	62.5, 125, 250	125, 250
	x8	62.5, 125, 250	250
	x16	62.5, 125, 250, 500	N/A
Gen4	x1	125, 250	N/A
	x2	125, 250	N/A
	x4	125, 250	N/A
	x8	125, 250, 500	N/A

For important information about clocking the core, see Clocking.

- **Output Core Clock Frequency:** Selects the frequency of the output `coreclk` that can be used by the PCIe MAC. 250 MHz is supported for all configurations. In UltraScale+ devices, there is support for 500 MHz for x16 Gen3 (8.0 Gb/s) and for x8 Gen4 (16.0 Gb/s) configurations. For important information about clocking the core, see Clocking.
- **PLL Type:** Selects the PLL type for GTs used. For Gen2 speed, select between CPLL and QPLL1. For Gen1 speed, PLL type is fixed to CPLL and for Gen3 speed it is fixed to QPLL1.

Table 18: **PLL Type**

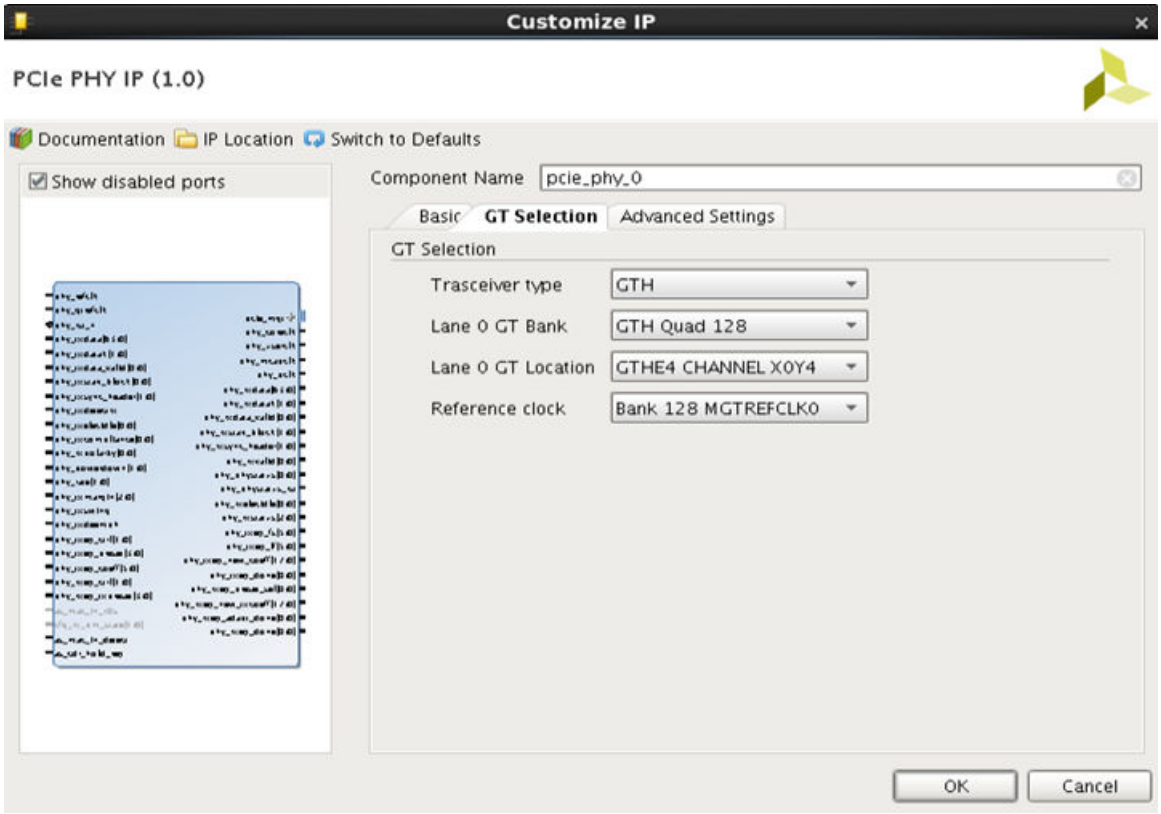
Link Speed	PLL Type	Description
2.5 GT/s	CPLL	The default is CPLL and not available for selection.
5.0 GT/s	QPLL1, CPLL	The default is QPLL1 and not available for selection.
8.0 GT/s	QPLL1	The default is QPLL1 and not available for selection.
16.0 GT/s	QPLL0	The default is QPLL0 and not available for selection.

- **PIPE Interface pipeline registers:** Selects the number of pipeline stages in the PIPE interface. Supported values are 0, 1, 2, and 3.
- **Spec 0.7 EIEOS Change Enable:** Enables the EIEOS support feature from the v0.7 Spec for PCIe Gen4. This option is only available for UltraScale+ devices (except Zynq® UltraScale+ ES1 Silicon parts).

GT Selection Tab

The GT Selection tab contains the GT selection information. Once the Lane 0 GT Quad and Lane 0 GT Location is selected, then the rest of the GT locations are derived from those two selections. The reference clock selection is also narrowed by the Lane 0 GT Quad and Channel locations. For more information on the GT quad selections, see the *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213).

Figure 10: **GT Selection Tab for the Core**



- **Transceiver Type:** Transceiver type allows you to select the type of the transceiver based on the FPGA selection. Following table shows the transceiver selection available for the IP core.

Table 19: **Transceiver Type Selection**

Device	Transceiver Type
VU3P/VU9P	GTY

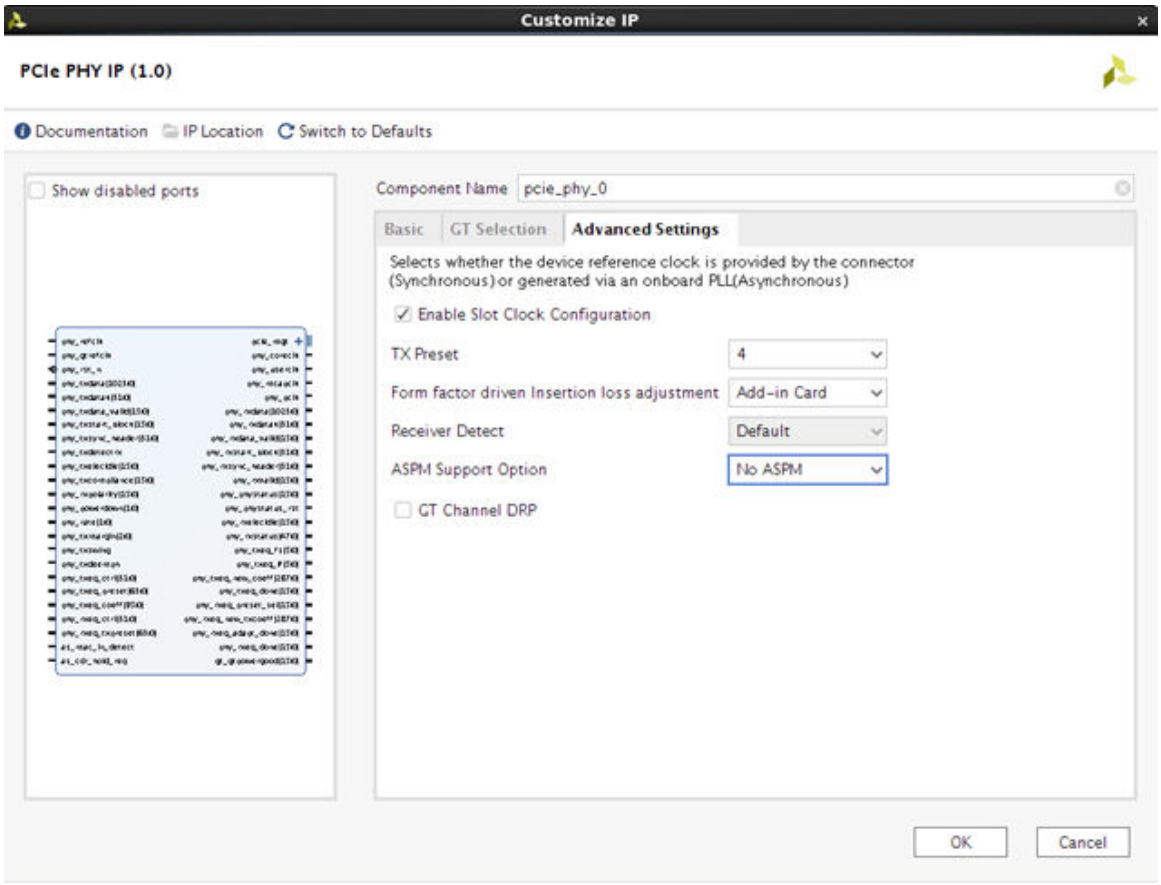
Table 19: **Transceiver Type Selection** *(cont'd)*

Device	Transceiver Type
ZU9EG	GTH
KU040	GTH
VU440	GTH
KU115	GTH

- **Lane 0 GT Bank:** Selects the GT Quad for lane 0 (Master lane) in the design.
- **Lane 0 GT Location:** Once the Lane 0 GT bank is selected, select the Lane 0 GT location under this option. The remainder of the GT locations will be assigned from this location.
- **Reference Clock:** Specifies the PCIe reference clock pin for the PCIe MAC GT Selection.

Advanced Settings Tab

Figure 11: **Advanced Settings Tab**



- **Enable Slot Clock Configuration:** When this option is selected, the link is synchronously clocked, that is, whether the device reference clock would be provided synchronously by the connector or asynchronously through an onboard PLL. For more information on clocking options, refer to the *Clocking* section in the *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213).
- **TX Preset:** It is not advisable to change the default value of 4. Preset value of 5 might work better on some systems.
- **Form factor driven Insertion loss adjustment:** Indicates the transmitter to receiver insertion loss at the Nyquist frequency depending on the form factor selection. There are three available options: Chip to Chip, Add-in Card, and Backplane in the menu, corresponds to 5 dB, 15 dB, and 20 dB insertion loss, respectively. Also, this parameter internally sets LPM mode for the Chip to Chip option, and DFE mode for all others in the GTs.
- **Receiver Detect:** Indicates the type of Receiver Detect Default or Falling Edge. This parameter is only available for UltraScale devices. For more information about this option, see the *UltraScale Architecture GTH Transceivers User Guide* (UG576).
- **ASPM Support Option:** This parameter is only available for UltraScale+™ devices. The available options are No_ASPM, L0s Supported and L1 Supported. Select the option that is the same as that supported in the MAC.
- **GT Channel DRP:** This parameter is only available for UltraScale+ devices. It enables GT DRP ports.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Constraining the Core

This section contains information about constraining the core in the Vivado®.

Required Constraints

The PCIe PHY IP solution requires the specification of timing and other physical implementation constraints to meet specified performance requirements. These constraints are provided in a Xilinx Design Constraints (XDC) file. Pinouts and hierarchy names in the generated XDC correspond to the provided example design.

IMPORTANT! *If the example design top file is not used, copy the IBUFDS_GTE3/IBUFDS_GTE4 instance for the reference clock, IBUF Instance for* `sys_rst`*, and also the timing constraints associated with them into your local design top.*

You should provide the location constraint for `sys_rst` and `sys_rst_override` pins based on the development board in use.

Constraints provided with the integrated block solution have been tested in hardware and provide consistent results. Constraints can be modified, but modifications should only be made with a thorough understanding of the effect of each constraint. Additionally, support is not provided for designs that deviate from the provided constraints.

Device, Package, and Speed Grade Selections

The device selection portion of the XDC informs the implementation tools which part, package, and speed grade to target for the design.

The device selection section always contains a part selection line, but can also contain part or package-specific options. An example part selection line follows:

```
CONFIG PART = XVU3P-ffvc1517-1-i-es1
```

***Note*:** A Gen4 configuration requires -2, -2L, or -3 speed grade UltraScale+ device.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900).

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

XILINX

Chapter 6

Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

The example design is a design assistant to validate the functionality of the PCIe PHY IP core. It ensures the connectivity, clock connections, reset sequence, and enablement of rate change based on your selection.

Overview

The example design operation is explained below:

- The example design expects the system reset to be received from the link partner.
- You have an additional option to override the system reset using `sys_rst_override` provided in the example design. This can be connected to any I/O on the board, such as a switch pin.
- The TX and RX electrical idle is High at this point.
- The design waits for the reset sequence to finish. For more information on the reset sequence, see Resets.
- The transceiver provides the `phystatus_rst` which indicates that the PHY is ready. Make sure the PCIe MAC is connected to this output from the PHY.
- The design now waits for `phystatus` on all lanes.
- Based on your selection of `phyrate` (either Gen1, Gen2, or Gen3), the design changes to the desired speed.

Simulating the Example Design

The example design provides a quick method to simulate and observe the behavior of the core generated using the Vivado® Design Suite.

The currently supported simulators are:

- Vivado simulator (default)
- Mentor Graphics QuestaSim
- Cadence Incisive Enterprise Simulator (IES)
- Synopsys Verilog Compiler Simulator (VCS)

The simulator uses the example design test bench and test cases provided along with the example design for the design configuration.

For any project (PCIe PHY IP core) generated out of the box, the simulations using the default Vivado simulator can be run as follows:

1. In the Sources Window, right-click the example project file (`.xci`), and select **Open IP Example Design**.

   The example project is created.

2. In the Flow Navigator (left-hand pane), under Simulation, right-click **Run Simulation** and select **Run Behavioral Simulation**.

IMPORTANT! *The post-synthesis and post-implementation simulation options are not supported for the PCIe PHY.*

   After the Run Behavioral Simulation Option is running, you can observe the compilation and elaboration phase through the activity in the Tcl Console, and in the Simulation tab of the Log Window.

3. In Tcl Console, type the run all command and press Enter. This runs the complete simulation as per the test case provided in example design test bench.

   After the simulation is complete, the result can be viewed in the Tcl Console.

In Vivado IDE, change the simulation settings as follows:

1. In the Flow Navigator, under Simulation, select **Simulation Settings**.
2. Set the Target simulator to QuestaSim/ModelSim Simulator, Incisive EnterpriseSimulator (IES), or Verilog Compiler Simulator.
3. In the simulator tab, select **Run Simulation > Run behavioral simulation**.
4. When prompted, click **Yes** to change and then run the simulator.

The simulation environment provided with the PCIe PHY IP core performs rate change operation in the same sequence as described in the Overview. The simulation environment has the target speed set to Gen3.

Appendix A

Upgrading

This appendix is not applicable for the first release of the core.

Appendix B

Debugging

This appendix includes details about resources available on the Xilinx® Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support. The Xilinx Community Forums are also available where members can learn, participate, share, and ask questions about Xilinx solutions.

Documentation

This product guide is the main document associated with the core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the PCI Express PHY

Xilinx Answer 66988.

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Debug Tools

There are many tools available to address PCIe PHY design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx® devices.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

XILINX

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
2. *Vivado Design Suite User Guide: Designing with IP* (UG896)
3. *Vivado Design Suite User Guide: Getting Started* (UG910)
4. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
5. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
6. *Vivado Design Suite User Guide: Implementation* (UG904)
7. *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213)
8. *UltraScale Architecture GTH Transceivers User Guide* (UG576)

Revision History

Section	Revision Summary
05/22/2019 Version 1.0	
Unsupported Features	Updated section.
04/04/2018 Version 1.0	
General Updates	Updated to reflect the Gen4 supports -2L speed grade.
10/04/2017 Version 1.0	
Port Descriptions	• Added GT Specific Ports for Ultrascale+ Devices only figure. • Updated the ASPM Support Option and added GT Channel DRP option to the Advanced Setting Tab in the IP Customization Dialog Box.
IP Facts	Minor editorial changes.
04/05/2017 Version 1.0	
General Updates	Updated Device Utilization – Ultrascale+ Devices table.
10/05/2016 Version 1.0	
General Updates	• Updated for support of Gen 1, Gen 2, and Gen3 speeds in UltraScale devices, and Gen1, Gen2, Gen3, and Gen4 speeds in UltraScale+ devices. • Updated to include the supported KU115 UltraScale devices. • Updated to reflect the UltraScale devices also support 16.0 GT/s link speeds.
Performance and Resource Use	Updated section.
Chapter 3: Product Specification	Added new Assist Signals table.
Chapter 5: Design Flow Steps	• Added that the limited supported target devices can be migrated easily to other devices. • Added the Spec 0.7 EIEOS Change Enable parameter, and update the Basic Tab figure. • Added the ASPM Support Option parameter, and updated the Advanced Settings Tab figure.

Section	Revision Summary
06/08/2016 Version 1.0	
General Updates	Added UltraScale architecture.
IP Facts	Updated Features section.
Chapter 2: Overview	Updated description.
Applications	Updated table.
Port Descriptions	Added TX, RX Data Signals for UltraScale, and Assist Signal tables
Clocking	Updated section.
Customizing and Generating the Core	Updated section.
Constraining the Core	Added note to Required Constraints section.
04/15/2016 Version 1.0	
IP FactsChapter 3: Product Specification	Minor editorial changes.
04/06/2016 Version 1.0	
Initial Xilinx release.	N/A

Please Read: Important Legal Notices

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

Copyright