Local Memory Bus (LMB) v3.0

LogiCORE IP Product Guide

Vivado Design Suite

PG113 April 6, 2016

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Appendix C: Additional Resources and Legal Notices

Introduction

The LogiCORE™ IP Local Memory Bus (LMB) core is used as the LMB interconnect for Xilinx device embedded processor systems. The LMB is a fast, local bus for connecting the MicroBlaze™ processor instruction and data ports to high-speed peripherals, primarily on-chip block RAM (BRAM).

Features

- Efficient, single master bus (requires no arbiter)
- Separate read and write data buses
- Low FPGA resource utilization
- Support for extended address up to 64 bits

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	UltraScale+™ Families UltraScale™ Architecture Zynq®-7000 All Programmable SoC 7 Series
Supported User Interfaces	LMB
Resources	N/A
Provided with Core	
Design Files	Vivado: RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	VHDL Behavioral
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP Catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

A MicroBlaze™ processor system using two LMB IP cores is shown in Figure 1-1. This system shows the use of both Instruction (I) and Data (D) side LMB buses connecting to a dual-ported BRAM block through separate LMB BRAM interface controllers. For information on the LMB BRAM Interface Controller see the *LMB BRAM Interface Controller LogiCORE IP Product Guide* (PG112) [Ref 1].

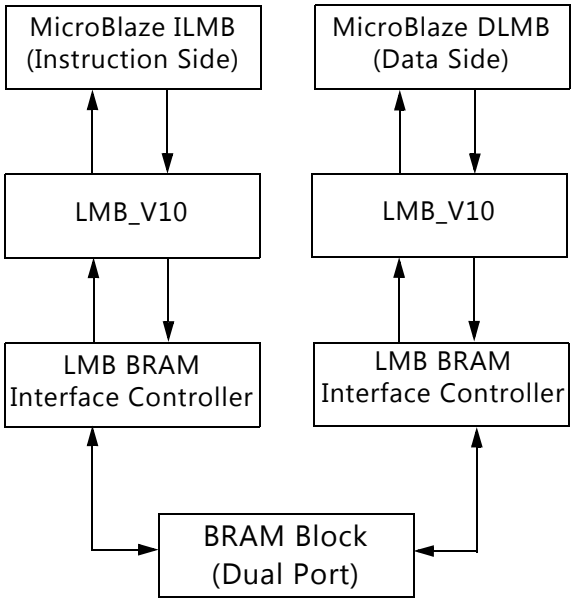

Figure 1-1: **MicroBlaze Processor System Using Two LMB IP Cores**

Feature Summary

The LMB core is used as the local memory bus interconnect for embedded processor systems. The LMB is a fast, local bus for connecting the MicroBlaze processor instruction and data ports to high-speed peripherals, primarily on-chip block RAM (BRAM).

The LMB supports an extended address of up to 64 bits.

Licensing and Ordering Information

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado® Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Standards

The LogiCORE™ IP Local Memory Bus (LMB) core implements the Processor Local Bus. The LMB is a synchronous bus used primarily to access on-chip block RAM. It uses a minimum number of control signals and a simple protocol to ensure that local block RAM are accessed in a single clock cycle. All LMB signals are active-High. See the *MicroBlaze Processor Reference Guide* (UG984) [Ref 2], Local Memory Bus (LMB) Interface Description, for a detailed definition of the bus.

Performance

The frequency and latency of the Local Memory Bus core are optimized for use with MicroBlaze™. This means that the frequency targets are aligned to MicroBlaze targets as well as the 1 cycle latency optimized for MicroBlaze instruction and data access.

Maximum Frequencies

For details about performance, visit Performance and Resource Utilization.

Latency

Data read from block RAM is available the clock cycle after the address strobe is asserted. Data write is performed the clock cycle after the address strobe is asserted.

Throughput

The nominal throughput is one read or write access every clock cycle.

Port Descriptions

The I/O ports for the LMB core are listed in Table 2-1.

Table 2-1: **LMB Core I/O Ports**

Port Name	MSB:LSB	I/O	Description
LMB_CLK		I	LMB Clock
SYS_Rst		I	External System Reset
LMB_Rst		O	LMB Reset
M_ABus	0:C_LMB_AWIDTH-1	I	Master Address Bus
M_ReadStrobe		I	Master Read Strobe
M_WriteStrobe		I	Master Write Strobe
M_AddrStrobe		I	Master Address Strobe
M_DBus	0:C_LMB_DWIDTH-1	I	Master Data Bus
M_BE	0:C_LMB_DWIDTH/8-1	I	Master Byte Enables
Sl_DBus	0:C_LMB_DWIDTH*C_LMB_NUM_SLAVES-1	I	Slave Data Bus
Sl_Ready	0:C_LMB_NUM_SLAVES-1	I	Slave Data Ready
Sl_Wait	0:C_LMB_NUM_SLAVES-1	I	Slave Data Wait
Sl_UE	0:C_LMB_NUM_SLAVES-1	I	Slave Uncorrectable Data Error
Sl_CE	0:C_LMB_NUM_SLAVES-1	I	Slave Correctable Data Error
LMB_ABus	0:C_LMB_AWIDTH-1	O	LMB Address Bus
LMB_ReadStrobe		O	LMB Read Strobe
LMB_WriteStrobe		O	LMB Write Strobe
LMB_AddrStrobe		O	LMB Address Strobe
LMB_ReadDBus	0:C_LMB_DWIDTH-1	O	LMB Read Data Bus
LMB_WriteDBus	0:C_LMB_DWIDTH-1	O	LMB Write Data Bus
LMB_Ready		O	LMB Data Ready
LMB_Wait		O	LMB Data Wait
LMB_UE		O	LMB Uncorrectable Data Error
LMB_CE		O	LMB Correctable Data Error
LMB_BE	0:C_LMB_DWIDTH/8-1	O	LMB Byte Enables

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

In a typical MicroBlaze™ system the LMB core is typically connected as in Figure 3-1.

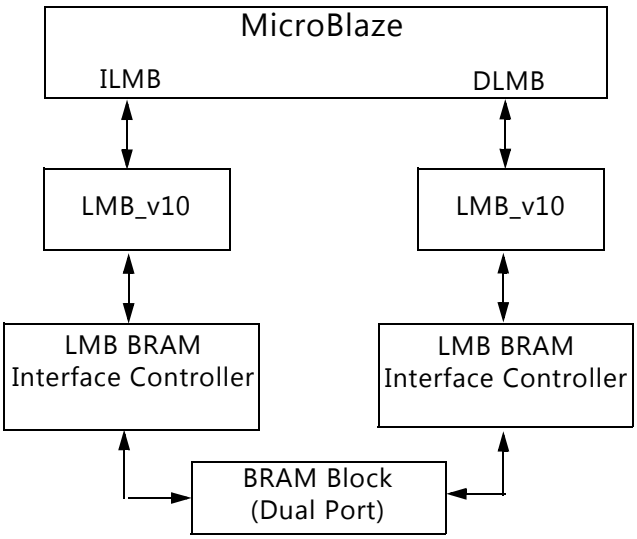

Figure 3-1: **Typical MicroBlaze System**

For additional examples, and a description of how Error Correcting Codes (ECC) are used with the Local Memory Bus, see the *LMB BRAM Interface Controller LogiCORE IP Product Guide* (PG112) [Ref 1].

Clocking

The LMB core is fully synchronous with all clocked elements clocked with the `LMB_Clk`.

Resets

The `LMB_Rst` is the master reset input signal for the LMB core.

Protocol Description

See the LMB Interface Description timing diagrams in the *MicroBlaze Processor Reference Guide* (UG984) [Ref 2].

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 3]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 5]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 3] for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the Vivado IP catalog.
2. Double-click the selected IP or select the **Customize IP** command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 5].

Note: Figures in this chapter are illustrations of the Vivado Integrated Design Environment (IDE). The layout depicted here might vary from the current version.

The LMB core parameters are included on a single configuration page, shown in Figure 4-1.

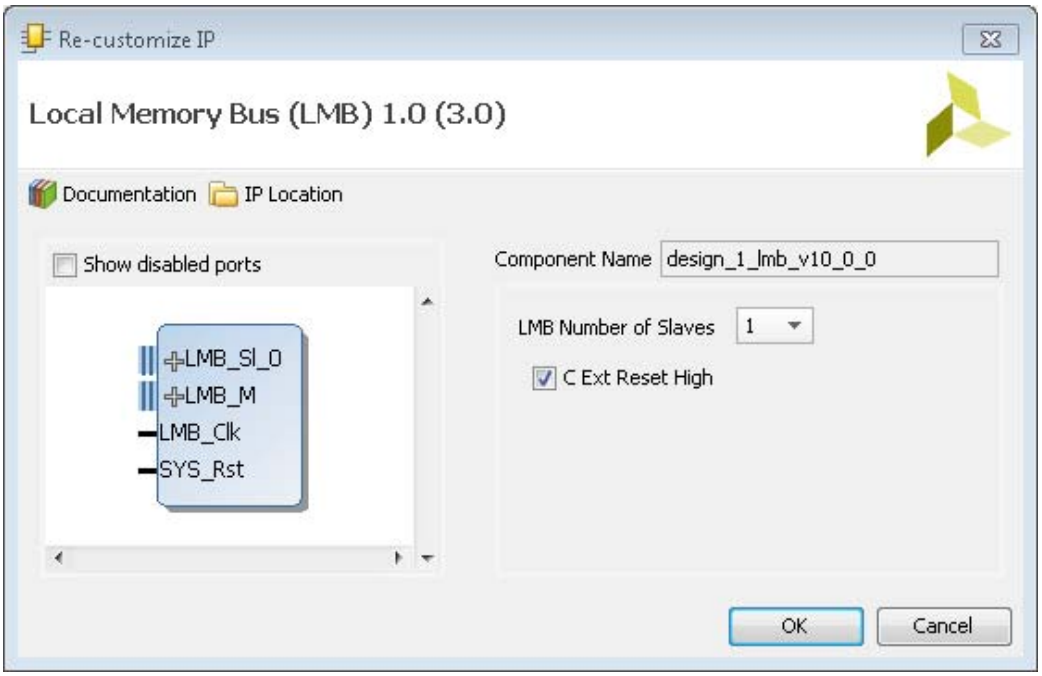

Figure 4-1: **LMB Core Parameter Page**

- **LMB Number of Slaves** - Sets the number of ports available to connect to MicroBlaze™.
- **C Ext Reset High** - Defines that `LMB_Rst` is active-High.

LMB Memory Bus Parameters

Table 4-1: **LMB Core Design Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_LMB_NUM_SLAVES	Number of LMB Slaves	1–16	4	integer
C_LMB_AWIDTH	LMB Address Bus Width	32–64	32	integer
C_LMB_DWIDTH	LMB Data Bus Width	32	32	integer
C_EXT_RESET_HIGH	Level of external reset	0 = Active-Low reset 1 = Active-High reset	1	integer

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

Parameter - Port Dependencies

The LMB core parameter-port dependencies are listed in Table 4-2.

Table 4-2: **Parameter-Port Dependencies**

Parameter Name	Ports (Port width depends on parameter)
C_LMB_NUM_SLAVES	SI_DBus, SI_Ready. SI_Wait, SI_UE, SI_CE
C_LMB_AWIDTH	M_ABus, LMB_ABus
C_LMB_DWIDTH	M_DBus, M_BE, SI_DWIDTH, LMB_ReadDBus, LMB_WriteDBus, LMB_BE
C_EXT_RESET_HIGH	none

User Parameters

Table 4-3 shows the relationship between the fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl console).

Table 4-3: **Vivado IDE Parameter to User Parameter Relationship**

Vivado IDE Parameter	User Parameter	Default Value
LMB Number of Slaves	C_LMB_NUM_SLAVES	1
C Ext Reset High	C_EXT_RESET_HIGH	1

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

The LMB core is fully synchronous with all clocked elements clocked by the `LMB_Clk` input.

To operate properly when connected to MicroBlaze™, the `LMB_Clk` must be the same as MicroBlaze clock.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6].

IMPORTANT: *For cores targeting 7 series or Zynq-7000 devices, UNIFAST libraries are not supported. Xilinx IP is tested and qualified with UNISIM libraries only.*

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4].

Migrating

This appendix contains information about upgrading to a more recent version of the IP core.

Migrating to the Vivado Design Suite

For information on migrating to the Vivado® Design Suite, see the *ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 7].

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the LMB core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the LMB core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator.

Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Answer Records for the LMB Core

- AR54431

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Debug Tools

The main tool available to address LMB design issues is the Vivado® Design Suite debug feature.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used to interact with the logic debug IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 8].

Reference Boards

All 7 series Xilinx development boards support the LMB core. These boards can be used to prototype designs and establish that the core can communicate with the system.

Simulation Debug

The simulation debug flow for Mentor Graphics Questa Simulator (QuestaSim) is described below. A similar approach can be used with other simulators.

- Check for the latest supported versions of QuestaSim in the Xilinx Design Tools: Release Notes Guide. Is this version being used? If not, update to this version.
- If using Verilog, do you have a mixed mode simulation license? If not, obtain a mixed-mode license.
- Ensure that the proper libraries are compiled and mapped. In the Vivado Design Suite this can be done using **Flow > Simulation Settings.**
- Have you associated the intended software program for the MicroBlaze™ processor with the simulation? Use the command **Tools > Associate ELF Files** in Vivado Design Suite.
- When observing the traffic on the LMB interface connected to the LMB core, see the *MicroBlaze Processor Reference Guide* (UG984) [Ref 2] for the LMB timing.

Hardware Debug

This section provides debug steps for common issues. The Vivado Design Suite debug feature is a valuable resource to use in hardware debug. The signal names mentioned in the following sections can be probed using the debug feature to debug specific problems. Many of these common issues can also be applied to debugging design simulations.

General Checks

Ensure that all the timing constraints were met during implementation.

- Does it work in post-place and route timing simulation? If problems are seen in hardware but not in timing simulation, this could indicate a PCB issue. Ensure that all clock sources are active and clean.
- If using MMCMs in the design, ensure that all MMCMs have obtained lock by monitoring the `LOCKED` port.

LMB Checks

To monitor the LMB interface, the signals `LMB_ABus`, `LMB_WriteDBus`, `LMB_ReadStrobe`, `LMB_AddrStrobe`, `LMB_WriteStrobe`, `LMB_BE`, `Sl_DBus`, and `Sl_Ready` can be connected to the Vivado debug feature. When Error Correction Codes are used, the signals `Sl_Wait`, `Sl_CE`, and `Sl_UE` can also be added. To sample the interface signals, the Vivado debug feature should use the `LMB_Clk` clock signal.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

References

1. *LogiCORE IP LMB BRAM Interface Controller Product Guide* (PG112)
2. *MicroBlaze Processor Reference Guide* (UG984)
3. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
4. *Vivado Design Suite User Guide: Designing with IP* (UG896)
5. *Vivado Design Suite User Guide: Getting Started* (UG910)
6. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
7. *ISE to Vivado Design Suite Migration Guide* (UG911)
8. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/06/2016	3.0	Updated with description of extended addressing.
11/18/2015	3.0	Added support for UltraScale+ families.
06/24/2015	3.0	Moved performance and resource utilization data to the web.
03/20/2013	1.0	This Product Guide replaces PG087. There are no documentation changes for this release.

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