Card Management Solution Subsystem v1.0

Product Guide

Vivado Design Suite

PG348 (v1.0) May 22, 2019

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Introduction

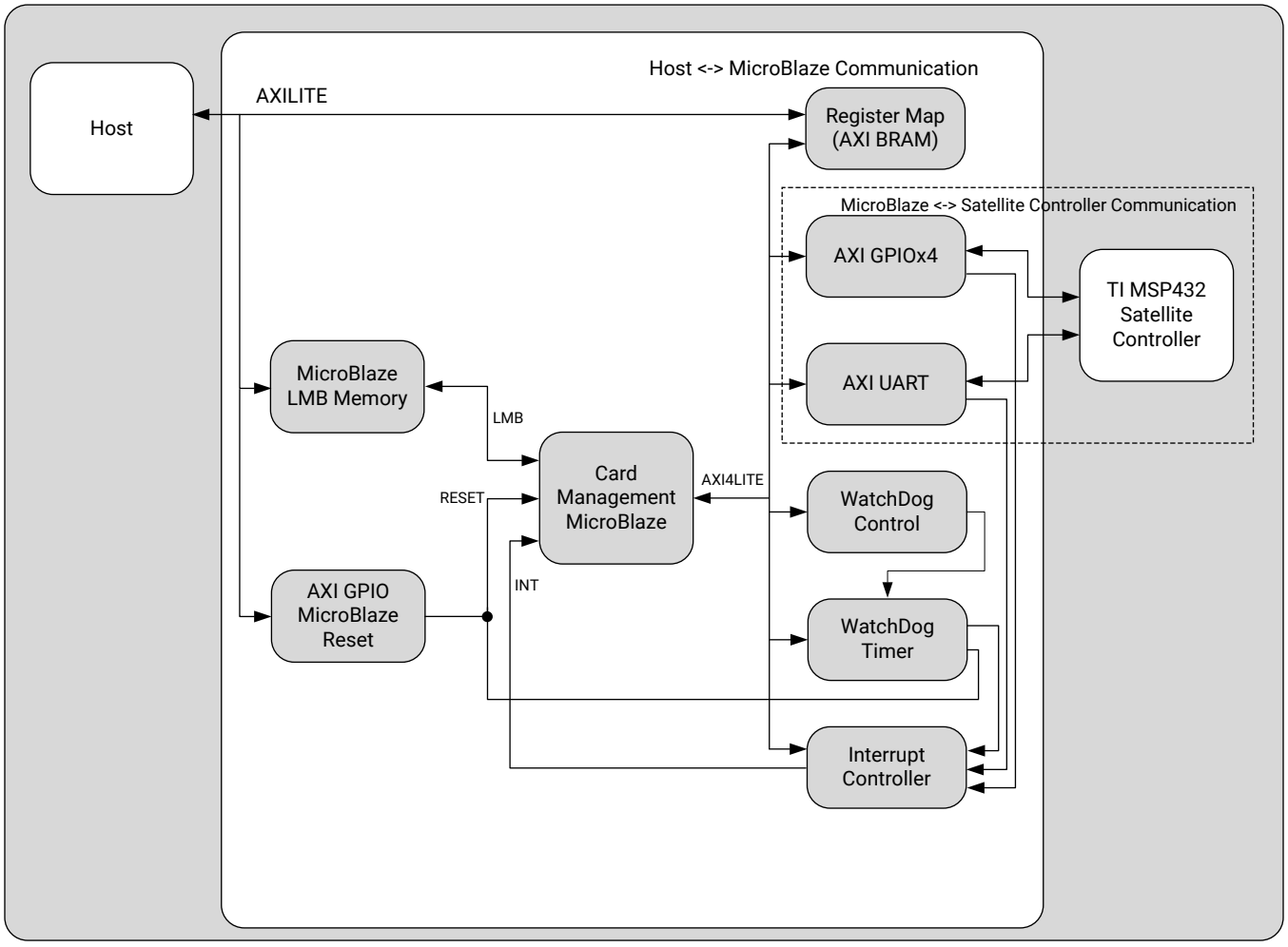
The Card Management Solution Subsystem (CMS Subsystem) is a MicroBlaze™ based design compatible with U200 and U250 Alveo™ Acceleration Boards. CMS Firmware autonomously reads sensor information from the TI MSP432 satellite controller over UART and write instantaneous, maximum and average values to a shared memory for collection by host software. Sensor information is monitored and gathered for:

- Voltages
- Currents
- Temperatures
- Fan Speed

The CMS solution includes the following functions:

- A MicroBlaze™ microprocessor and firmware solution. Software configuration of the CMS subsystem is not required (the CMS is fixed function).
- CMS firmware polls for sensor information (100ms poll) from the satellite controller (TI MSP432) over a UART interface with GPIO handshake lines.
- CMS firmware processes sensor information and writes instantaneous, maximum and average values to a shared memory (memory mapped) for collection by host software.
- Host software polls shared memory for updated sensor information. (CMS does not interrupt the host.)

Figure 1: **Card Management Solution Subsystem Block Diagram**



Features

- **Voltage Monitoring:** Reports key voltage rails from Satellite Controller.
- **Current Monitoring:** Reports key current values from Satellite Controller.
- **Temperature Monitoring:** Reports key temperatures from Satellite Controller.
- **Fan Speed Monitoring:** Reports fan speed from local fan via Satellite Controller.

***Note*:** Fan speed is reported only for active cards with local fans - Passive cards do not contain fans.

IP Facts

LogiCORE™ IP Facts Table	
Subsystem Specifics	
Supported Device Family[1]	UltraScale+™ ***Note*:** This solution is targeted to the U200 and U250 boards.
Supported User Interfaces	AXI4-Lite
Resources	Performance and Resource Use web page
Provided with Subsystem	
Design Files	IP integrator HIP Subsystem
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Xilinx Constraints File
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado® IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

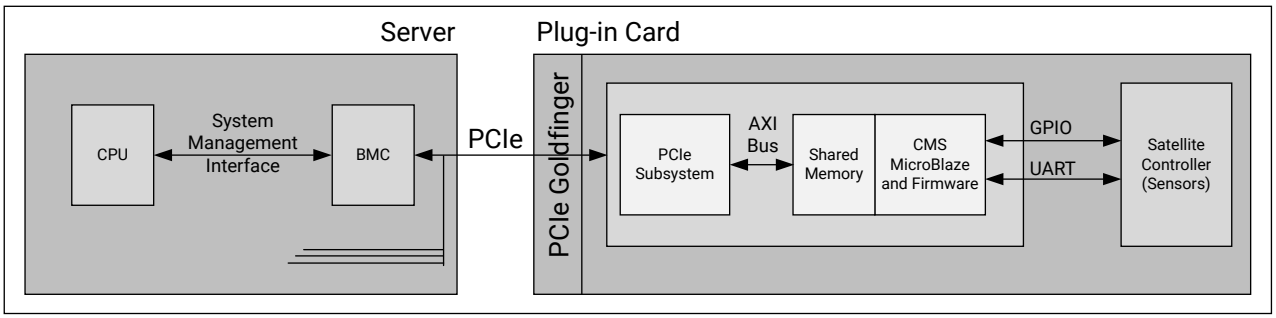
Overview

Applications

The CMS Subsystem subsystem is designed for in-band card management systems for plug-in PCIe® cards for servers typically deployed in data centers.

A typical configuration deployment configuration is shown in the following figure.

Figure 2: **CMS Subsystem Typical Configuration**



X22661-050219

Unsupported Features

The following features of the standard are not supported in the subsystem:

- Firmware upgrade.
- Watchdog.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado® Design Suite under the terms of the Xilinx End User License.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx® LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Performance

For full details about performance and resource use, visit the Performance and Resource Use web page.

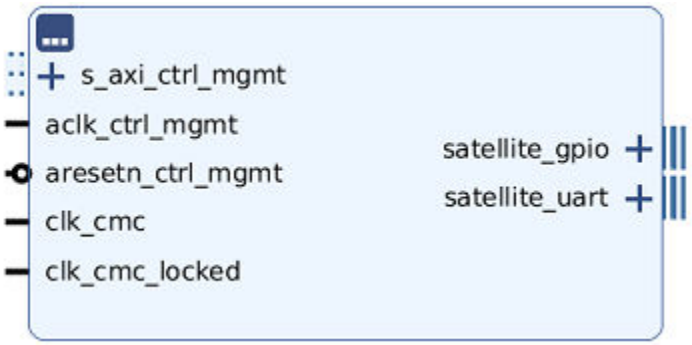
Resource Utilization

For full details about performance and resource use, visit the Performance and Resource Use web page.

Port Descriptions

The CMS Subsystem ports are shown in the following figure.

Figure 3: **CMS Subsystem IP Symbol**



I/O Signal Description

Table 1: **CMS Subsystem I/O Descriptions**

Port Name	I/O	Clock	Description
s_axi_ctrl_mgmt	I/O	aclk_ctrl_mgmt	AXI4-Lite Control Management Slave interface
aclk_ctrl_mgmt	I	N/A	AXI4-Lite Control Management Clock Pin (50MHz)
aresetn_ctrl_mgmt	I	aclk_ctrl_mgmt	AXI4-Lite Control Management Reset Pin. Active-Low reset.
clk_cmc	I	clk_cmc	Card Management Controller Clock (50MHz). This port should be connected to a free running clock available in the design
clk_cmc_locked	I	N/A	Card Management Controller Clock MMCM 'Locked' Signal
satellite_gpio	O	clk_cmc	GPIO signals to/from MSP432 Satellite Controller
satellite_uart	O	clk_cmc	UART interface to MSP432 Satellite Controller

Register Space

Table 2: **CMS Subsystem Register Address Space**

Address (hex)	Name	Access Type	Description
0x000000-0x3FFFC	Reserved	N/A	Reserved
0x040000-0x04FFFC	REG_MAP	See REG_MAP Register Definitions	Host/CMS shared memory map
0x050000-0x07FFFC	Reserved	N/A	Reserved

Table 2: **CMS Subsystem Register Address Space** *(cont'd)*

Address (hex)	Name	Access Type	Description
0x080000	MB_RESETN_REG	RW	Microblaze reset register. Active low.

Table 3: **REG_MAP Register Definitions (0x040000)**

Address (hex)	Name	Access Type	Description
0x0000	REG_MAP_ID_REG	RO	Register Map ID. (0x74736574)
0x0004	FW_VERSION_REG	RO	Firmware Version (0x001ECF1C)
0x0008	STATUS_REG	RO	CMS Status Register 31:28 MSP432 Mode (Normal = 1) 27:0 Reserved
0x000C	ERROR_REG	RO	CMS Error Register 31:28 Reserved 27 MSP432 Communication Error (1=Error, use CONTROL_REG to clear) 26:0 Reserved
0x0010-0x0014	Reserved	N/A	N/A
0x0018	CONTROL_REG	RW	CMS Control Register 31:7 Reserved 6 Set to reboot Microblaze 5:2 Reserved 1 Set to Reset ERROR_REG self clearing 0 Set to reset MAX and AVG sensor values, self clearing
0x001C	Reserved	N/A	N/A
0x0020	12V_PEX_MAX_REG	RO	12V_PEX Max Voltage. Unsigned 32b int (mV)
0x0024	12V_PEX_AVG_REG	RO	12V_PEX Average Voltage. Unsigned 32b int (mV)
0x0028	12V_PEX_INS_REG	RO	12V_PEX Instantaneous Voltage. Unsigned 32b int (mV)
0x002C	3V3_PEX_MAX_REG	RO	3V3_PEX Max Voltage. Unsigned 32b int (mV)
0x0030	3V3_PEX_AVG_REG	RO	3V3_PEX Average Voltage. Unsigned 32b int (mV)
0x0034	3V3_PEX_INS_REG	RO	3V3_PEX Instantaneous Voltage. Unsigned 32b int (mV)
0x0038	3V3_AUX_MAX_REG	RO	3V3_AUX Max Voltage. Unsigned 32b int (mV)
0x003C	3V3_AUX_AVG_REG	RO	3V3_AUX Average Voltage. Unsigned 32b int (mV)
0x0040	3V3_AUX_INS_REG	RO	3V3_AUX Instantaneous Voltage. Unsigned 32b int (mV)

Table 3: **REG_MAP Register Definitions (0x040000)** *(cont'd)*

Address (hex)	Name	Access Type	Description
0x0044	12V_AUX_MAX_REG	RO	12V_AUX Max Voltage. Unsigned 32b int (mV)
0x0048	12V_AUX_AVG_REG	RO	12V_AUX Average Voltage. Unsigned 32b int (mV)
0x004C	12V_AUX_INS_REG	RO	12V_AUX Instantaneous Voltage. Unsigned 32b int (mV)
0x0050	DDR4_VPP_BTM_MAX_REG	RO	DDR4 VPP BTM Max Voltage. Unsigned 32b int (mV)
0x0054	DDR4_VPP_BTM_AVG_REG	RO	DDR4 VPP BTM Average Voltage. Unsigned 32b int (mV)
0x0058	DDR4_VPP_BTM_INS_REG	RO	DDR4 VPP BTM Instantaneous Voltage. Unsigned 32b int (mV)
0x005C	SYS_5V5_MAX_REG	RO	SYS_5V5 Max Voltage. Unsigned 32b int (mV)
0x0060	SYS_5V5_AVG_REG	RO	SYS_5V5 Average Voltage. Unsigned 32b int (mV)
0x0064	SYS_5V5_INS_REG	RO	SYS_5V5 Instantaneous Voltage. Unsigned 32b int (mV)
0x0068	VCC1V2_TOP_MAX_REG	RO	VCC1V2_TOP Max Voltage. Unsigned 32b int (mV)
0x006C	VCC1V2_TOP_AVG_REG	RO	VCC1V2_TOP Average Voltage. Unsigned 32b int (mV)
0x0070	VCC1V2_TOP_INS_REG	RO	VCC1V2_TOP Instantaneous Voltage. Unsigned 32b int (mV)
0x0074	VCC1V8_MAX_REG	RO	VCC1V8 Max Voltage. Unsigned 32b int (mV)
0x0078	VCC1V8_AVG_REG	RO	VCC1V8 Average Voltage. Unsigned 32b int (mV)
0x007C	VCC1V8_INS_REG	RO	VCC1V8 Instantaneous Voltage. Unsigned 32b int (mV)
0x0080	VCC0V85_MAX_REG	RO	VCC0V85 Max Voltage. Unsigned 32b int (mV)
0x0084	VCC0V85_AVG_REG	RO	VCC0V85 Average Voltage. Unsigned 32b int (mV)
0x0088	VCC0V85_INS_REG	RO	VCC0V85 Instantaneous Voltage. Unsigned 32b int (mV)
0x008C	DDR4_VPP_TOP_MAX_REG	RO	DDR4_VPP_TOP Max Voltage. Unsigned 32b int (mV)
0x0090	DDR4_VPP_TOP_AVG_REG	RO	DDR4_VPP_TOP Average Voltage. Unsigned 32b int (mV)
0x0094	DDR4_VPP_TOP_INS_REG	RO	DDR4_VPP_TOP Instantaneous Voltage. Unsigned 32b int (mV)

Table 3: **REG_MAP Register Definitions (0x040000)** *(cont'd)*

Address (hex)	Name	Access Type	Description
0x0098	MGT0V9AVCC_MAX_REG	RO	MGT0V9AVCC Max Voltage. Unsigned 32b int (mV)
0x009C	MGT0V9AVCC_AVG_REG	RO	MGT0V9AVCC Average Voltage. Unsigned 32b int (mV)
0x00A0	MGT0V9AVCC_INS_REG	RO	MGT0V9AVCC Instantaneous Voltage. Unsigned 32b int (mV)
0x00A4	12V_SW_MAX_REG	RO	12V_SW Max Voltage. Unsigned 32b int (mV)
0x00A8	12V_SW_AVG_REG	RO	12V_SW Average Voltage. Unsigned 32b int (mV)
0x00AC	12V_SW_INS_REG	RO	12V_SW Instantaneous Voltage. Unsigned 32b int (mV)
0x00B0	MGTAVTT_MAX_REG	RO	MGTAVTT Max Voltage. Unsigned 32b int (mV)
0x00B4	MGTAVTT_AVG_REG	RO	MGTAVTT Average Voltage. Unsigned 32b int (mV)e
0x00B8	MGTAVTT_INS_REG	RO	MGTAVTT Instantaneous Voltage. Unsigned 32b int (mV)
0x00BC	VCC1V2_BTM_MAX_REG	RO	VCC1V2_BTM Max Voltage. Unsigned 32b int (mV)
0x00C0	VCC1V2_BTM_AVG_REG	RO	VCC1V2_BTM Average Voltage. Unsigned 32b int (mV)
0x00C4	VCC1V2_BTM_INS_REG	RO	VCC1V2_BTM Instantaneous Voltage. Unsigned 32b int (mV)
0x00C8	12VPEX_I_IN_MAX_REG	RO	12VPEX_I_IN Max Current. Unsigned 32b int (mA)
0x00CC	12VPEX_I_IN_AVG_REG	RO	12VPEX_I_IN Average Current. Unsigned 32b int (mA)
0x00D0	12VPEX_I_IN_INS_REG	RO	12VPEX_I_IN Instantaneous Current. Unsigned 32b int (mA)
0x00D4	12V_AUX_I_IN_MAX_REG	RO	12V_AUX_I_IN Max Current. Unsigned 32b int (mA)
0x00D8	12V_AUX_I_IN_AVG_REG	RO	12V_AUX_I_IN Average Current. Unsigned 32b int (mA)
0x00DC	12V_AUX_I_IN_INS_REG	RO	12V_AUX_I_IN Instantaneous Current. Unsigned 32b int (mA)
0x00E0	VCCINT_MAX_REG	RO	VCCINT Max Voltage. Unsigned 32b int (mV)
0x00E4	VCCINT_AVG_REG	RO	VCCINT Average Voltage. Unsigned 32b int (mV)
0x00E8	VCCINT_INS_REG	RO	VCCINT Instantaneous Voltage. Unsigned 32b int (mV)

Table 3: **REG_MAP Register Definitions (0x040000)** *(cont'd)*

Address (hex)	Name	Access Type	Description
0x00EC	VCCINT_I_MAX_REG	RO	VCCINT_I Max Current. Unsigned 32b int (mA)
0x00F0	VCCINT_I_AVG_REG	RO	VCCINT_I Average Current. Unsigned 32b int (mA)
0x00F4	VCCINT_I_INS_REG	RO	VCCINT_I Instantaneous Current. Unsigned 32b int (mA)
0x00F8	FPGA_TEMP_MAX_REG	RO	FPGA_TEMP Max Temperature. Unsigned 32b int (C)
0x00FC	FPGA_TEMP_AVG_REG	RO	FPGA_TEMP Average Temperature. Unsigned 32b int (C)
0x0100	FPGA_TEMP_INS_REG	RO	FPGA_TEMP Instantaneous Temperature. Unsigned 32b int (C).
0x0104	FAN_TEMP_MAX_REG	RO	FAN_TEMP Max Temperature. Unsigned 32b int (C)
0x0108	FAN_TEMP_AVG_REG	RO	FAN_TEMP Average Temperature. Unsigned 32b int (C)
0x010C	FAN_TEMP_INS_REG	RO	FAN_TEMP Instantaneous Temperature. Unsigned 32b int (C).
0x0110	DIMM_TEMP0_MAX_REG	RO	DIMM_TEMP0 Max Temperature. Unsigned 32b int (C)
0x0114	DIMM_TEMP0_AVG_REG	RO	DIMM_TEMP0 Average Temperature. Unsigned 32b int (C)
0x0118	DIMM_TEMP0_INS_REG	RO	DIMM_TEMP0 Instantaneous Temperature. Unsigned 32b int (C).
0x011C	DIMM_TEMP1_MAX_REG	RO	DIMM_TEMP1 Max Temperature. Unsigned 32b int (C)
0x0120	DIMM_TEMP1_AVG_REG	RO	DIMM_TEMP1 Average Temperature. Unsigned 32b int (C)
0x0124	DIMM_TEMP1_INS_REG	RO	DIMM_TEMP1 Instantaneous Temperature. Unsigned 32b int (C).
0x0128	DIMM_TEMP2_MAX_REG	RO	DIMM_TEMP2 Max Temperature. Unsigned 32b int (C)
0x012C	DIMM_TEMP2_AVG_REG	RO	DIMM_TEMP2 Average Temperature. Unsigned 32b int (C)
0x0130	DIMM_TEMP2_INS_REG	RO	DIMM_TEMP2 Instantaneous Temperature. Unsigned 32b int (C).
0x0134	DIMM_TEMP3_MAX_REG	RO	DIMM_TEMP3 Max Temperature. Unsigned 32b int (C)
0x0138	DIMM_TEMP3_AVG_REG	RO	DIMM_TEMP3 Average Temperature. Unsigned 32b int (C)
0x013C	DIMM_TEMP3_INS_REG	RO	DIMM_TEMP3 Instantaneous Temperature. Unsigned 32b int (C).

Table 3: **REG_MAP Register Definitions (0x040000)** *(cont'd)*

Address (hex)	Name	Access Type	Description
0x0140	SE98_TEMP0_MAX_REG	RO	SE98_TEMP0 Max Temperature. Unsigned 32b int (C)
0x0144	SE98_TEMP0_AVG_REG	RO	SE98_TEMP0 Average temperature. Unsigned 32b int (C)
0x0148	SE98_TEMP0_INS_REG	RO	SE98_TEMP0 Instantaneous temperature. Unsigned 32b int (C).
0x014C	SE98_TEMP1_MAX_REG	RO	SE98_TEMP1 Max Temperature. Unsigned 32b int (C)
0x0150	SE98_TEMP1_AVG_REG	RO	SE98_TEMP1 Average Temperature. Unsigned 32b int (C)
0x0154	SE98_TEMP1_INS_REG	RO	SE98_TEMP1 Instantaneous Temperature. Unsigned 32b int (C).
0x0158	SE98_TEMP2_MAX_REG	RO	SE98_TEMP2 Max Temperature. Unsigned 32b int (C)
0x015C	SE98_TEMP2_AVG_REG	RO	SE98_TEMP2 Average Temperature. Unsigned 32b int (C)
0x0160	SE98_TEMP2_INS_REG	RO	SE98_TEMP2 Instantaneous Temperature. Unsigned 32b int (C).
0x0164	FAN_SPEED_MAX_REG	RO	FAN_SPEED Max Speed. Unsigned 32b int (RPM)
0x0168	FAN_SPEED_AVG_REG	RO	FAN_SPEED Average Speed. Unsigned 32b int (RPM)
0x016C	FAN_SPEED_INS_REG	RO	FAN_SPEED Instantaneous Speed. Unsigned 32b int (RPM).
0x0170	CAGE_TEMP0_MAX_REG	RO	CAGE_TEMP0 Max Temperature. Unsigned 32b int (C)
0x0174	CAGE_TEMP0_AVG_REG	RO	CAGE_TEMP0 Average Temperature. Unsigned 32b int (C)
0x0178	CAGE_TEMP0_INS_REG	RO	CAGE_TEMP0 Instantaneous Temperature. Unsigned 32b int (C).
0x017C	CAGE_TEMP1_MAX_REG	RO	CAGE_TEMP1 Max Temperature. Unsigned 32b int (C)
0x0180	CAGE_TEMP1_AVG_REG	RO	CAGE_TEMP1 Average Temperature. Unsigned 32b int (C)
0x0184	CAGE_TEMP1_INS_REG	RO	CAGE_TEMP1 Instantaneous Temperature. Unsigned 32b int (C).
0x0188	CAGE_TEMP2_MAX_REG	RO	CAGE_TEMP2 Max Temperature. Unsigned 32b int (C)
0x018C	CAGE_TEMP2_AVG_REG	RO	CAGE_TEMP2 Average Temperature. Unsigned 32b int (C)
0x0190	CAGE_TEMP2_INS_REG	RO	CAGE_TEMP2 Instantaneous Temperature. Unsigned 32b int (C).

Table 3: **REG_MAP Register Definitions (0x040000)** *(cont'd)*

Address (hex)	Name	Access Type	Description
0x0194	CAGE_TEMP3_MAX_REG	RO	CAGE_TEMP3 Max Temperature. Unsigned 32b int (C)
0x0198	CAGE_TEMP3_AVG_REG	RO	CAGE_TEMP3 Average Temperature. Unsigned 32b int (C)
0x019C	CAGE_TEMP3_INS_REG	RO	CAGE_TEMP3 Instantaneous Temperature. Unsigned 32b int (C).
0x01A0-0x025C	Reserved	N/A	N/A
0x0260	HBM_TEMP_MAX_REG	RO	HBM_TEMP Max Temperature. Unsigned 32b int (C)
0x0264	HBM_TEMP_AVG_REG	RO	HBM_TEMP Average Temperature. Unsigned 32b int (C)
0x0268	HBM_TEMP_INS_REG	RO	HBM_TEMP Instantaneous Temperature. Unsigned 32b int (C).

Designing with the Subsystem

This section includes guidelines and additional information to facilitate designing with the subsystem.

Clocking

Table 5: **Clocks**

Clock	Description
clk_cmc	This clock pin should be connected to a free-running clock available in the design. The clock drives the CMS Subsystem MicroBlaze and associated peripherals.
aclk_ctrl_mgmt	This clock pin should be connected to the AXI clock used in the design.

Resets

The CMS Subsystem uses a single active-low reset pin, `aresetn_ctrl_mgmt`. This reset should be synchronous to `aclk_ctrl_mgmt`.

Addressing

The CMS Subsystem requires 1M of Address space (`0x10_000`). The selected address segment offset must be in the range `0x00000000-0x01F00000` at a 1M boundary (`0x00_000`, `0x10_000`, `0x20_000` ...).

Design Flow Steps

This section describes customizing and generating the subsystem, constraining the subsystem, and the simulation, synthesis, and implementation steps that are specific to this IP subsystem. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
- *Vivado Design Suite User Guide: Designing with IP* (UG896)
- *Vivado Design Suite User Guide: Getting Started* (UG910)
- *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Customizing and Generating the Subsystem

This section includes information about using Xilinx® tools to customize and generate the subsystem in the Vivado® Design Suite.

If you are customizing and generating the subsystem in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP subsystem using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the *Vivado Design Suite User Guide: Getting Started* (UG910).

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Constraining the Subsystem

Required Constraints

The following constraints are required for this subsystem

Alveo U200/U250 IO Constraints

- **Satellite UART:**

```
set_property PACKAGE_PIN BA19 [get_ports satellite_uart_rxd]
set_property -dict {IOSTANDARD LVCMOS12} [get_ports satellite_uart_rxd]
set_property PACKAGE_PIN BB19 [get_ports satellite_uart_txd]
set_property -dict {IOSTANDARD LVCMOS12 DRIVE 4} [get_ports
satellite_uart_txd]
```

- **Satellite GPIO:**

```
set_property PACKAGE_PIN AR20 [get_ports satellite_gpio_tri_io[0]]
set_property -dict {IOSTANDARD LVCMOS12 DRIVE 4} [get_ports
satellite_gpio_tri_io[0]]
set_property PACKAGE_PIN AM20 [get_ports satellite_gpio_tri_io[1]]
set_property -dict {IOSTANDARD LVCMOS12 DRIVE 4} [get_ports
satellite_gpio_tri_io[1]]
set_property PACKAGE_PIN AM21 [get_ports satellite_gpio_tri_io[2]]
set_property -dict {IOSTANDARD LVCMOS12 DRIVE 4} [get_ports
satellite_gpio_tri_io[2]]
set_property PACKAGE_PIN AN21 [get_ports satellite_gpio_tri_io[3]]
set_property -dict {IOSTANDARD LVCMOS12 DRIVE 4} [get_ports
satellite_gpio_tri_io[3]]
```

Device, Package, and Speed Grade Selections

This section is not applicable for this IP subsystem.

Clock Frequencies

This section is not applicable for this IP subsystem.

Clock Management

This section is not applicable for this IP subsystem.

Clock Placement

This section is not applicable for this IP subsystem.

Banking

This section is not applicable for this IP subsystem.

Transceiver Placement

This section is not applicable for this IP subsystem.

I/O Standard and Placement

This section is not applicable for this IP subsystem.

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900).

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

XILINX

Appendix A

Upgrading

This appendix is not applicable for the first release of the subsystem.

Appendix B

Debugging

This appendix includes details about resources available on the Xilinx® Support website and debugging tools.

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

Note: IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.

Finding Help on Xilinx.com

To help in the design and debug process when using the subsystem, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support. The Xilinx Community Forums are also available where members can learn, participate, share, and ask questions about Xilinx solutions.

Documentation

This product guide is the main document associated with the subsystem. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this subsystem can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Debug Tools

There are many tools available to address CMS Subsystem design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx® devices.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado® debug feature is a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the debug feature for debugging the specific problems.

General Checks

Ensure that all the timing constraints for the core were properly incorporated from the example design and that all constraints were met during implementation.

- Does it work in post-place and route timing simulation? If problems are seen in hardware but not in timing simulation, this could indicate a PCB issue. Ensure that all clock sources are active and clean.
- If using MMCMs in the design, ensure that all MMCMs have obtained lock by monitoring the locked port.
- If your outputs go to 0, check your licensing.

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
2. *Vivado Design Suite User Guide: Designing with IP* (UG896)
3. *Vivado Design Suite User Guide: Getting Started* (UG910)
4. *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
05/22/2019 Version 1.0	
Initial Xilinx release.	N/A

Please Read: Important Legal Notices

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