Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics

DS926 (v1.8) April 6, 2021 **Product Specification**

Summary

The Xilinx® Zynq® UltraScale+™ RFSoCs are available in -2 and -1 speed grades, with -2E or -2I devices having the highest performance. The -2LE, -2LI, and -1LI devices are screened for lower maximum static power. The XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR devices in the -2LE and -1LI speed grades and the XQZU21DR, XQZU28DR, and XQZU29DR devices in the -1LI speed grade can operate at a V_{CCINT} voltage at 0.85V or 0.72V. The XCZU39DR device in the -2LI speed grade and the XCZU43DR, XCZU46DR, XCZU47DR, XCZU48DR, XCZU49DR, XQZU48DR, and XQZU49DR devices in the -2LI and -1LI speed grades operate at a V_{CCINT} voltage at 0.72V. When operated at V_{CCINT} = 0.85V, using -2LE and -1LI devices, the speed specification for the L devices is the same as the -2I or -1I speed grades. When operated at V_{CCINT} = 0.72V, the -2LE, -2LI, and -1LI performance and static and dynamic power is reduced.

DC and AC characteristics are specified in extended (E), industrial (I), and military (M) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade extended device are the same as for a -1 speed grade industrial device). However, only selected speed grades and/or devices are available in each temperature range.

The XQ references in this data sheet are specific to the devices available in XQ Ruggedized packages. See the *Defense-Grade UltraScale Architecture Data Sheet: Overview* (DS895) for further information on XQ Defense-grade part numbers, packages, and ordering information.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the Zynq UltraScale+ RFSoCs, is available on the Xilinx website at www.xilinx.com/documentation.

DC Characteristics

Absolute Maximum Ratings

Table 1: **Absolute Maximum Ratings**

Symbol	Description[1]	Min	Max	Units
Processor System (PS)				
$V_{CC\_PSINTFP}$	PS primary logic full-power domain supply voltage	–0.500	1.000	V
$V_{CC\_PSINTLP}$	PS primary logic low-power domain supply voltage	–0.500	1.000	V
V_{CC_PSAUX}	PS auxiliary supply voltage	–0.500	2.000	V
$V_{CC\_PSINTFP\_DDR}$	PS DDR controller and PHY supply voltage	–0.500	1.000	V
V_{CC_PSADC}	PS SYSMON ADC supply voltage relative to GND_PSADC	–0.500	2.000	V
V_{CC_PSPLL}	PS PLL supply voltage	–0.500	1.320	V
$V_{PS\_MGTRAVCC}$	PS-GTR supply voltage	–0.500	1.000	V
$V_{PS\_MGTRAVTT}$	PS-GTR termination voltage	–0.500	2.000	V
$V_{PS\_MGTREFCLK}$	PS-GTR reference clock input voltage	–0.500	1.100	V
V_{PS_MGTRIN}	PS-GTR receiver input voltage	–0.500	1.100	V
V_{CCO_PSDDR}	PS DDR I/O supply voltage	–0.500	1.650	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage	–0.500	2.000	V
V_{CCO_PSIO}	PS I/O supply	–0.500	3.630	V
V_{PSIN}[2]	PS I/O input voltage	–0.500	V_{CCO_PSIO} + 0.550	V
	PS DDR I/O input voltage	–0.500	V_{CCO_PSDDR} + 0.550	V
V_{CC_PSBATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage	–0.500	2.000	V
Programmable Logic (PL)				
V_{CCINT}	Internal supply voltage	–0.500	1.000	V
V_{CCINT_IO}[3]	Internal supply voltage for the I/O banks	–0.500	1.000	V
V_{CCAUX}	Auxiliary supply voltage	–0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.500	1.000	V
V_{CCO}	Output drivers supply voltage for HD I/O banks	–0.500	3.400	V
	Output drivers supply voltage for HP I/O banks	–0.500	2.000	V
V_{CCAUX_IO}[4]	Auxiliary supply voltage for the I/O banks	–0.500	2.000	V
V_{REF}	Input reference voltage	–0.500	2.000	V
V_{IN}[2, 5, 6]	I/O input voltage for HD I/O banks	–0.550	V_{CCO} + 0.550	V
	I/O input voltage for HP I/O banks	–0.550	V_{CCO} + 0.550	V
I_{DC}	Available output current at the pad	–20	20	mA
I_{RMS}	Available RMS output current at the pad	–20	20	mA
GTY Transceiver[7]				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers	–0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column	–0.500	1.300	V

Table 1: **Absolute Maximum Ratings** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating[8]	–	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND[9]	–	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable[10]	–	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	6	mA
RF-ADC, RF-DAC, and SD-FEC				
V_{ADC_AVCC}	ADC and PLL supply voltage	–0.500	1.000	V
$V_{ADC\_AVCCAUX}$	Input buffer and PLL supply voltage	–0.500	2.000	V
V_{DAC_AVCC}	DAC and PLL supply voltage	–0.500	1.000	V
$V_{DAC\_AVCCAUX}$	Output buffer and PLL supply voltage	–0.500	2.000	V
V_{DAC_AVTT}	DAC on-die 50Ω termination supply voltage	–0.500	3.200	V
V_{CCINT_AMS}	Digital down converter supply voltage	–0.500	1.000	V
$V_{CCSDFEC}$	SD-FEC supply voltage	–0.500	1.000	V
$V_{RFDC\_CLK\_IN}$	ADC_CLK, DAC_CLK, and SYSREF input voltage	–0.500	2.000	V
V_{ADC_VIN}	ADC_VIN input voltage for ZU2xDR and ZU39DR devices	–0.300	2.100	V
	ADC_VIN input voltage for ZU4xDR devices	–0.500	2.100	V
PL System Monitor				
V_{CCADC}	PL System Monitor supply relative to GNDADC	–0.500	2.000	V
V_{REFP}	PL System Monitor reference input relative to GNDADC	–0.500	2.000	V
Temperature[11]				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum dry rework soldering temperature	–	260	°C
	Maximum reflow soldering temperature for FFVD1156, FFVE1156, FSVE1156, FFVG1517, FSVG1517, FFVF1760, FSVF1760, FFVH1760, and FSVH1760 packages	–	245	°C
	Maximum reflow soldering temperature for FFRD1156, FFRE1156, FFRG1517, and FFRF1760 packages	–	225	°C

Table 1: **Absolute Maximum Ratings** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
T_j	Maximum junction temperature	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When operating outside of the recommended operating conditions, refer to Table 6, Table 7, and Table 8 for maximum overshoot and undershoot specifications.
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. V_{CCAUX_IO} must be connected to V_{CCAUX}.
5. The lower absolute voltage specification always applies.
6. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
7. For more information on supported GTY transceiver terminations see the *UltraScale Architecture GTY Transceivers User Guide* (UG578).
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ Device Packaging and Pinouts Product Specification User Guide* (UG1075).

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions**

Symbol	Description[1, 2]	Min	Typ	Max	Units
Processor System					
$V_{CC\_PSINTFP}$[3]	PS full-power domain supply voltage	0.808	0.850	0.892	V
	For -1LI, -2LI, and -2LE (V_{CCINT} = 0.72V) devices: PS full-power domain supply voltage	0.808	0.850	0.892	V
$V_{CC\_PSINTLP}$	PS low-power domain supply voltage	0.808	0.850	0.892	V
	For -1LI, -2LI, and -2LE (V_{CCINT} = 0.72V) devices: PS low-power domain supply voltage	0.808	0.850	0.892	V
V_{CC_PSAUX}	PS auxiliary supply voltage	1.710	1.800	1.890	V
$V_{CC\_PSINTFP\_DDR}$[3]	PS DDR controller and PHY supply voltage	0.808	0.850	0.892	V
	For -1LI, -2LI, and -2LE (V_{CCINT} = 0.72V) devices: PS DDR controller and PHY supply voltage	0.808	0.850	0.892	V
V_{CC_PSADC}	PS SYSMON ADC supply voltage relative to GND_PSADC	1.710	1.800	1.890	V
V_{CC_PSPLL}	PS PLL supply voltage	1.164	1.200	1.236	V
$V_{PS\_MGTRAVCC}$[4]	PS-GTR supply voltage	0.825	0.850	0.875	V
$V_{PS\_MGTRAVTT}$[4]	PS-GTR termination voltage	1.746	1.800	1.854	V
V_{CCO_PSDDR}[5]	PS DDR I/O supply voltage	1.06	–	1.575	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage	1.710	1.800	1.890	V
V_{CCO_PSIO}[6]	PS I/O supply	1.710	–	3.465	V
V_{PSIN}	PS I/O input voltage	–0.200	–	V_{CCO_PSIO} + 0.200	V
	PS DDR I/O input voltage	–0.200	–	V_{CCO_PSDDR} + 0.200	V
V_{CC_PSBATT}[7]	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage	1.200	–	1.500	V

Table 2: **Recommended Operating Conditions** *(cont'd)*

Symbol	Description[1, 2]	Min	Typ	Max	Units
Programmable Logic					
V_{CCINT}	PL internal supply voltage	0.825	0.850	0.876	V
	For -1LI, -2LI, and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage	0.698	0.720	0.742	V
V_{CCINT_IO}[8]	PL internal supply voltage for the I/O banks	0.825	0.850	0.876	V
	For -1LI, -2LI, and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage for the I/O banks	0.825	0.850	0.876	V
V_{CCBRAM}	Block RAM supply voltage	0.825	0.850	0.876	V
V_{CCAUX}	Auxiliary supply voltage	1.746	1.800	1.854	V
V_{CCO}[9]	Supply voltage for HD I/O banks	1.140	–	3.400	V
	Supply voltage for HP I/O banks	0.950	–	1.900	V
V_{CCAUX_IO}[10]	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V_{IN}[11]	I/O input voltage	–0.200	–	V_{CCO} + 0.200	V
I_{IN}[12]	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
GTY Transceiver					
$V_{MGTAVCC}$[13]	Analog supply voltage for the GTY transceiver	0.873	0.900	0.927	V
$V_{MGTAVTT}$[13]	Analog supply voltage for the GTY transmitter and receiver termination circuits	1.164	1.200	1.236	V
$V_{MGTVCCAUX}$[13]	Auxiliary analog QPLL voltage supply for the transceivers	1.746	1.800	1.854	V
$V_{MGTAVTTRCAL}$[13]	Analog supply voltage for the resistor calibration circuit of the GTY transceiver column	1.164	1.200	1.236	V
RF-ADC, RF-DAC, and SD-FEC					
V_{ADC_AVCC}	ADC and PLL supply voltage	0.897	0.925	0.953	V
$V_{ADC\_AVCCAUX}$	Input buffer and PLL supply voltage	1.746	1.800	1.854	V
V_{DAC_AVCC}	DAC and PLL supply voltage	0.897	0.925	0.953	V
$V_{DAC\_AVCCAUX}$	Output buffer and PLL supply voltage	1.746	1.800	1.854	V
V_{DAC_AVTT}[14]	Termination voltage, on-die 50Ω termination resistors: 20 mA	2.425	2.500	2.575	V
	Termination voltage, on-die 50Ω termination resistors: 32 mA	2.910	3.000	3.090	V
	Termination voltage, on-die 50Ω termination resistors variable output power (VOP) disabled[15]	2.425	2.500	2.575	V
	Termination voltage, on-die 50Ω termination resistors VOP enabled[15]	2.910	3.000	3.090	V
V_{CCINT_AMS}[16]	Digital down converter supply voltage	0.825	0.850	0.876	V
$V_{CCSDFEC}$[17]	SD-FEC supply voltage	0.825	0.850	0.876	V
PL System Monitor					
V_{CCADC}	PL System Monitor supply relative to GNDADC	1.746	1.800	1.854	V
V_{REFP}	PL System Monitor externally supplied reference voltage relative to GNDADC	1.200	1.250	1.300	V

Table 2: **Recommended Operating Conditions** *(cont'd)*

Symbol	Description[1, 2]	Min	Typ	Max	Units
Temperature					
T_j[18]	Junction temperature operating range for extended (E) temperature devices[19]	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices[20]	–40	–	100	°C
	Junction temperature operating range for military (M) temperature devices	–55	–	125	°C
	Junction temperature operating range for eFUSE programming	–40	–	125	°C

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult the *UltraScale Architecture PCB Design User Guide* (UG583).
3. $V_{CC\_PSINTFP\_DDR}$ must be tied to $V_{CC\_PSINTFP}$.
4. Each voltage listed requires filtering as described in the *UltraScale Architecture PCB Design User Guide* (UG583).
5. Includes V_{CCO_PSDDR} of 1.2V, 1.35V, 1.5V at ±5% and 1.1V +0.07V/–0.04V depending upon the tolerances required by specific memory standards.
6. Applies to all PS I/O supply banks. Includes V_{CCO_PSIO} of 1.8V, 2.5V, and 3.3V at ±5%.
7. Up to 1.89V is acceptable on V_{CC_PSBATT}. If the battery-backed RAM or RTC is not used, connect V_{CC_PSBATT} to GND or V_{CC_PSAUX}.
8. V_{CCINT_IO} must be connected to V_{CCBRAM}.
9. Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at ±5%, and 3.3V (HD I/O only) at +3/–5%.
10. V_{CCAUX_IO} must be connected to V_{CCAUX}.
11. The lower absolute voltage specification always applies.
12. A total of 200 mA per bank should not be exceeded.
13. Each voltage listed requires filtering as described in the *UltraScale Architecture GTY Transceivers User Guide* (UG578).
14. RF-DAC output current swing must be set to 32 mA for 3V termination when using ZU2xDR or ZU39DR devices.
15. When using the VOP feature, only AC coupling mode is supported.
16. Xilinx recommends connecting V_{CCINT_AMS} to V_{CCBRAM}.
17. $V_{CCSDFEC}$ must be connected to V_{CCBRAM}.
18. Xilinx recommends measuring the T_j of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The SYSMON temperature measurement errors (that are described in Table 69 and Table 139) must be accounted for in your design. For example, when using the PL system monitor with an external reference of 1.25V, and when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted T_j (100°C – 3°C = 97°C).
19. Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature between 100°C and 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation up to T_j = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
20. Devices labeled with the speed/temperature grade of -2LI can operate for a limited time at a junction temperature between 100°C and 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C. Operation up to T_j = 110°C is limited to 5% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 5% of the device lifetime.

Available Speed Grades and Operating Voltages

Table 3 describes the speed grades per device and the V_{CCINT} operating supply voltages for the full-power, low-power, and DDR domains. For more information on selecting devices and speed grades, see the *UltraScale Architecture and Product Data Sheet: Overview* (DS890).

Table 3: **Available Speed Grades and Operating Voltages**

Speed Grade	V_{CCINT}	$V_{CC\_PSINTLP}$	$V_{CC\_PSINTFP}$	$V_{CC\_PSINTFP\_DDR}$	Units
-2E	0.85	0.85	0.85	0.85	V
-2I	0.85	0.85	0.85	0.85	V
-2LE	0.85	0.85	0.85	0.85	V
-1E	0.85	0.85	0.85	0.85	V
-1I	0.85	0.85	0.85	0.85	V
-1M	0.85	0.85	0.85	0.85	V
-1LI	0.85	0.85	0.85	0.85	V
-2LE	0.72	0.85	0.85	0.85	V
-2LI	0.72	0.85	0.85	0.85	V
-1LI	0.72	0.85	0.85	0.85	V

DC Characteristics Over Recommended Operating Conditions

Table 4: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.68	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (HD I/O and HP I/O[2]) (sample-tested)	–	–	15	µA
	Input or output leakage current per pin (PS DDR I/O) (sample-tested)	–	–	113	µA
C_{IN}[3]	Die input capacitance at the pad (HP I/O)	–	–	3.1	pF
	Die input capacitance at the pad (HD I/O)	–	–	4.75	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V	75	–	190	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V	50	–	169	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V	60	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V	30	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V	10	–	100	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V	60	–	200	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V	29	–	120	µA
$I_{CCADCONPL}$	Analog supply current for the PL SYSMON circuits in the power-up state	–	–	8	mA
$I_{CCADCONPS}$	Analog supply current for the PS SYSMON circuits in the power-up state	–	–	10	mA
$I_{CCADCOFFPL}$	Analog supply current for the PL SYSMON circuits in the power-down state	–	–	1.5	mA
$I_{CCADCOFFPS}$	Analog supply current for the PS SYSMON circuits in the power-down state	–	–	1.8	mA

Table 4: **DC Characteristics Over Recommended Operating Conditions** *(cont'd)*

Symbol	Description	Min	Typ[1]	Max	Units
I_{CC_PSBATT}[4, 5]	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC enabled	–	–	3650	nA
	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC disabled	–	–	650	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC enabled	–	–	3150	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC disabled	–	–	150	nA
I_{PSFS}[6]	PS V_{CC_PSAUX} additional supply current during eFUSE programming	–	–	115	mA
Calibrated programmable on-die termination (DCI) in HP I/O banks[7] (measured per JEDEC specification)					
R[9]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40	–10%[8]	40	+10%[8]	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–10%[8]	48	+10%[8]	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60	–10%[8]	60	+10%[8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–10%[8]	40	+10%[8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–10%[8]	48	+10%[8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–10%[8]	60	+10%[8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–10%[8]	120	+10%[8]	Ω
	Programmable input termination to $V_{CCO}$where ODT = RTT_240	–10%[8]	240	+10%[8]	Ω
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
R[9]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240	–50%	240	+50%	Ω
Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)					
R[9]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–50%	48	+50%	Ω
ADC_R_{EXT}	ADC external resistor reference	–1%	2490	+1%	Ω
DAC_R_{EXT}	DAC external resistor reference	–1%	2490	+1%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks	–35%	100	+35%	Ω
n	Temperature diode ideality factor	–	1.026	–	–

Table 4: **DC Characteristics Over Recommended Operating Conditions** *(cont'd)*

Symbol	Description	Min	Typ[1]	Max	Units
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For the HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{CC_PSBATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. VRP resistor tolerance is (240Ω ±1%).
8. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 5: **PS MIO Pull-up and Pull-down Current**

Symbol	Description	Min	Max	Units
I_{RPU}[1]	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSIO} = 3.3V	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSIO} = 2.5V	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSIO} = 1.8V	15	65	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 2.5V	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V	15	65	µA

Notes:

1. After power-on, the reset values of the MIO pin configuration registers enable and select the PS MIO pull-ups.

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks**

AC Voltage Overshoot[1]	% of UI[2] at –40°C to 100°C	AC Voltage Undershoot[1]	% of UI[2] at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	90%
V_{CCO} + 0.40	100%	–0.40	78%
V_{CCO} + 0.45	100%	–0.45	40%
V_{CCO} + 0.50	100%	–0.50	24%
V_{CCO} + 0.55	100%	–0.55	18.0%
V_{CCO} + 0.60	100%	–0.60	13.0%
V_{CCO} + 0.65	100%	–0.65	10.8%
V_{CCO} + 0.70	92%	–0.70	9.0%
V_{CCO} + 0.75	92%	–0.75	7.0%
V_{CCO} + 0.80	92%	–0.80	6.0%
V_{CCO} + 0.85	92%	–0.85	5.0%
V_{CCO} + 0.90	92%	–0.90	4.0%
V_{CCO} + 0.95	92%	–0.95	2.5%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.
3. For the -1M devices, the temperature limits are –55°C to 125°C.

Table 7: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks**

AC Voltage Overshoot[1]	% of UI[2] at –40°C to 100°C	AC Voltage Undershoot[1]	% of UI[2] at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	100%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.
3. For the -1M devices, the temperature limits are –55°C to 125°C.

Table 8: **V_{PSIN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O Banks**

AC Voltage Overshoot[1]	% of UI[2] at –40°C to 100°C[3]	AC Voltage Undershoot[1]	% of UI[2] at –40°C to 100°C[3]
V_{CCO_PSIO} + 0.30	100%	–0.30	100%
V_{CCO_PSIO} + 0.35	100%	–0.35	75%
V_{CCO_PSIO} + 0.40	100%	–0.40	45%
V_{CCO_PSIO} + 0.45	100%	–0.45	40%
V_{CCO_PSIO} + 0.50	75%	–0.50	10%
V_{CCO_PSIO} + 0.55	75%	–0.55	6%
V_{CCO_PSIO} + 0.60	60%	–0.60	2%
V_{CCO_PSIO} + 0.65	30%	–0.65	0%
V_{CCO_PSIO} + 0.70	20%	–0.70	0%
V_{CCO_PSIO} + 0.75	10%	–0.75	0%
V_{CCO_PSIO} + 0.80	10%	–0.80	0%
V_{CCO_PSIO} + 0.85	8%	–0.85	0%
V_{CCO_PSIO} + 0.90	6%	–0.90	0%
V_{CCO_PSIO} + 0.95	6%	–0.95	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.
3. For the -1M devices, the temperature limits are –55°C to 125°C.

Quiescent Supply Current

Table 9: **Typical Quiescent Supply Current**

Symbol	Description[1, 2, 3, 4]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.85V		0.72V		
			-2	-1	-2	-1	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XCZU21DR	2423	2423	2125	2125	mA
		XCZU25DR	2423	2423	2125	2125	mA
		XCZU27DR	2423	2423	2125	2125	mA
		XCZU28DR	2423	2423	2125	2125	mA
		XCZU29DR	2423	2423	2125	2125	mA
		XCZU39DR	2423	N/A	2125	N/A	mA
		XQZU21DR	2423	2423	N/A	2125	mA
		XQZU28DR	2423	2423	N/A	2125	mA
		XQZU29DR	2423	2423	N/A	2125	mA
		XCZU43DR	2338	2338	2125	2125	mA
		XCZU46DR	2338	2338	2125	2125	mA
		XCZU47DR	2338	2338	2125	2125	mA
		XCZU48DR	2338	2338	2125	2125	mA
		XCZU49DR	2338	2338	2125	2125	mA
		XQZU48DR	2338	2338	2125	2125	mA
		XQZU49DR	2338	2338	2125	2125	mA
I_{CCINT_IOQ}	Quiescent V_{CCINT_IO} supply current	XCZU21DR	115	115	115	115	mA
		XCZU25DR	115	115	115	115	mA
		XCZU27DR	115	115	115	115	mA
		XCZU28DR	115	115	115	115	mA
		XCZU29DR	115	115	115	115	mA
		XCZU39DR	115	N/A	115	N/A	mA
		XQZU21DR	115	115	N/A	115	mA
		XQZU28DR	115	115	N/A	115	mA
		XQZU29DR	115	115	N/A	115	mA
		XCZU43DR	114	114	114	114	mA
		XCZU46DR	114	114	114	114	mA
		XCZU47DR	114	114	114	114	mA
		XCZU48DR	114	114	114	114	mA
		XCZU49DR	114	114	114	114	mA
		XQZU48DR	114	114	114	114	mA
		XQZU49DR	114	114	114	114	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	All devices	1	1	1	1	mA

Table 9: **Typical Quiescent Supply Current** *(cont'd)*

Symbol	Description[1, 2, 3, 4]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.85V		0.72V		
			-2	-1	-2	-1	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XCZU21DR	334	334	334	334	mA
		XCZU25DR	334	334	334	334	mA
		XCZU27DR	334	334	334	334	mA
		XCZU28DR	334	334	334	334	mA
		XCZU29DR	334	334	334	334	mA
		XCZU39DR	334	N/A	334	N/A	mA
		XQZU21DR	334	334	N/A	334	mA
		XQZU28DR	334	334	N/A	334	mA
		XQZU29DR	334	334	N/A	334	mA
		XCZU43DR	334	334	334	334	mA
		XCZU46DR	334	334	334	334	mA
		XCZU47DR	334	334	334	334	mA
		XCZU48DR	334	334	334	334	mA
		XCZU49DR	334	334	334	334	mA
		XQZU48DR	334	334	334	334	mA
		XQZU49DR	334	334	334	334	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XCZU21DR	58	58	58	58	mA
		XCZU25DR	58	58	58	58	mA
		XCZU27DR	58	58	58	58	mA
		XCZU28DR	58	58	58	58	mA
		XCZU29DR	58	58	58	58	mA
		XCZU39DR	58	N/A	58	N/A	mA
		XQZU21DR	58	58	N/A	58	mA
		XQZU28DR	58	58	N/A	58	mA
		XQZU29DR	58	58	N/A	58	mA
		XCZU43DR	58	58	58	58	mA
		XCZU46DR	58	58	58	58	mA
		XCZU47DR	58	58	58	58	mA
		XCZU48DR	58	58	58	58	mA
		XCZU49DR	58	58	58	58	mA
		XQZU48DR	58	58	58	58	mA
		XQZU49DR	58	58	58	58	mA

Table 9: **Typical Quiescent Supply Current** *(cont'd)*

Symbol	Description[1, 2, 3, 4]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.85V		0.72V		
			-2	-1	-2	-1	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XCZU21DR	34	34	34	34	mA
		XCZU25DR	34	34	34	34	mA
		XCZU27DR	34	34	34	34	mA
		XCZU28DR	34	34	34	34	mA
		XCZU29DR	278	278	278	278	mA
		XCZU39DR	278	N/A	278	N/A	mA
		XQZU21DR	34	34	N/A	34	mA
		XQZU28DR	34	34	N/A	34	mA
		XQZU29DR	34	34	N/A	34	mA
		XCZU43DR	34	34	34	34	mA
		XCZU46DR	34	34	34	34	mA
		XCZU47DR	34	34	34	34	mA
		XCZU48DR	34	34	34	34	mA
		XCZU49DR	277	277	277	277	mA
		XQZU48DR	34	34	34	34	mA
		XQZU49DR	277	277	277	277	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, and all I/O pins are 3-state and floating.
3. Use the Xilinx® Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions or supplies other than those specified.
4. Typical values depend upon your configuration. To accurately estimate all PS supply currents, use the interactive XPE spreadsheet tool.

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power domain (LPD) must operate before the full-power domain (FPD) can function. The low-power and full-power domains can be powered simultaneously. The PS_POR_B input must be asserted to GND during the power-on sequence (see Table 37). The FPD (when used) must be powered before PS_POR_B is released.

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC\_PSINTLP}$
2. V_{CC_PSAUX}, V_{CC_PSADC}, and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC\_PSINTFP}$ and $V_{CC\_PSINTFP\_DDR}$ driven from the same supply source.
2. $V_{PS\_MGTRAVCC}$ and $V_{CC\_PSDDR\_PLL}$ in any order or simultaneously.
3. $V_{PS\_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

For ZU2xDR and ZU39DR devices, V_{ADC_AVCC}, $V_{ADC\_AVCCAUX}$, V_{DAC_AVCC}, $V_{DAC\_AVCCAUX}$, and V_{DAC_AVTT} can be powered at any time and have no power-up sequencing requirements. For ZU4xDR devices, V_{DAC_AVCC}, $V_{DAC\_AVCCAUX}$, and V_{DAC_AVTT} can be powered at any time and have no power-up sequencing requirements. V_{ADC_AVCC} and $V_{ADC\_AVCCAUX}$ have a required power-up sequence: $V_{ADC\_AVCCAUX}$ followed by V_{ADC_AVCC}. The required power-off sequence is the reverse of the power-on sequence: V_{ADC_AVCC} followed by $V_{ADC\_AVCCAUX}$.

The recommended power-on sequence to achieve minimum current draw for the GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

PS-PL Power Sequencing

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 10 shows the minimum current, in addition to I_{CCQ} maximum, required by each Zynq UltraScale+ RFSoC for proper power-on and configuration. If these current minimums are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies. The XPE spreadsheet tool (download at https://www.xilinx.com/power) is also used to estimate power-on current for all supplies.

Table 10: **Power-on Current by Device**

I_{CC} Min =	$I_{CCINTMIN}$	I_{CCINT_IOMIN} + $I_{CCBRAMMIN}$	I_{CCOMIN}	$I_{CCAUXMIN}$ + I_{CCAUX_IOMIN}	$I_{CCSDFECMIN}$	Units
I_{CCQ} +	I_{CCINTQ} +	$I_{CCBRAMQ}$ + I_{CCINT_IOQ} +	I_{CCOQ} +	I_{CCAUXQ} + I_{CCAUX_IOQ} +	$I_{CCSDFECQ}$ +	
XCZU21DR XQZU21DR	4500	770	50	320	250	mA
XCZU25DR	4500	770	50	320	250	mA
XCZU27DR	4500	770	50	320	250	mA
XCZU28DR XQZU28DR	4500	770	50	320	250	mA
XCZU29DR XQZU29DR	4500	1020	50	320	N/A	mA
XCZU39DR	4500	1020	50	320	N/A	mA
XCZU43DR	4500	1020	50	320	N/A	mA
XCZU46DR	4500	1020	50	320	250	mA
XCZU47DR	4500	1020	50	320	N/A	mA
XCZU48DR XQZU48DR	4500	1020	50	320	250	mA
XCZU49DR XQZU49DR	4500	1020	50	320	N/A	mA

Table 11: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$	0.2	40	ms
$T_{VCC\_PSINTFP}$	Ramp time from GND to 95% of $V_{CC\_PSINTFP}$	0.2	40	ms
$T_{VCC\_PSINTLP}$	Ramp time from GND to 95% of $V_{CC\_PSINTLP}$	0.2	40	ms
T_{VCC_PSAUX}	Ramp time from GND to 95% of V_{CC_PSAUX}	0.2	40	ms
$T_{VCC\_PSINTFP\_DDR}$	Ramp time from GND to 95% of $V_{CC\_PSINTFP\_DDR}$	0.2	40	ms
T_{VCC_PSADC}	Ramp time from GND to 95% of V_{CC_PSADC}	0.2	40	ms
T_{VCC_PSPLL}	Ramp time from GND to 95% of V_{CC_PSPLL}	0.2	40	ms
$T_{PS\_MGTRAVCC}$	Ramp time from GND to 95% of $V_{CC\_MGTRAVCC}$	0.2	40	ms
$T_{PS\_MGTRAVTT}$	Ramp time from GND to 95% of $V_{CC\_MGTRAVTT}$	0.2	40	ms
T_{VCCO_PSDDR}	Ramp time from GND to 95% of V_{CCO_PSDDR}	0.2	40	ms
$T_{VCC\_PSDDR\_PLL}$	Ramp time from GND to 95% of $V_{CC\_PSDDR\_PLL}$	0.2	40	ms
T_{VCCO_PSIO}	Ramp time from GND to 95% of V_{CCO_PSIO}	0.2	40	ms
T_{VADC_AVCC}	Ramp time from GND to 95% of V_{ADC_AVCC}	0.2	40	ms
$T_{VADC\_AVCCAUX}$	Ramp time from GND to 95% of $V_{ADC\_AVCCAUX}$	0.2	40	ms
T_{VDAC_AVCC}	Ramp time from GND to 95% of V_{DAC_AVCC}	0.2	40	ms
$T_{VDAC\_AVCCAUX}$	Ramp time from GND to 95% of $V_{DAC\_AVCCAUX}$	0.2	40	ms
T_{VDAC_AVTT}	Ramp time from GND to 95% of V_{DAC_AVTT}	0.2	40	ms
$T_{VCCSDFEC}$	Ramp time from GND to 95% of $V_{CCSDFEC}$	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: **PS MIO and CONFIG DC Input and Output Levels**

I/O Standard[1]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS33	–0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	–12
LVCMOS25	–0.300	0.700	1.700	V_{CCO_PSIO} + 0.30	0.70	1.70	12	–12
LVCMOS18	–0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	V_{CCO_PSIO} + 0.30	0.45	V_{CCO_PSIO} – 0.45	12	–12

Notes:

1. Tested according to relevant specifications.

Table 13: **PS DDR DC Input and Output Levels**

DDR Standard[1]	V_{IL}		V_{IH}		V_{OL}[2]	V_{OH}[2]	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.8 x V_{CCO_PSDDR} – 0.150	0.8 x V_{CCO_PSDDR} + 0.150	10	–0.1
LPDDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.3 x V_{CCO_PSDDR} – 0.150	0.3 x V_{CCO_PSDDR} + 0.150	0.1	–10
DDR3	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.175	0.5 x V_{CCO_PSDDR} + 0.175	8	–8
LPDDR3	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8
DDR3L	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

PL I/O Levels

Table 14: **SelectIO DC Input and Output Levels For HD I/O Banks**

I/O Standard[1, 2]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 4	Note 4
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 4	Note 4
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.300	0.800	2.000	3.400	0.400	2.400	Note 4	Note 4
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.9	–8.9
SSTL135_II	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	13.0	–13.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	8.9	–8.9
SSTL15_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	13.0	–13.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	8.0	–8.0
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.600	$V_{CCO}/2$ + 0.600	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.

Table 15: **SelectIO DC Input and Output Levels for HP I/O Banks**

I/O Standard[1, 2, 3]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	7.0	–7.0
MIPI_DPHY_ DCI_LP[6]	–0.300	0.550	0.880[7]	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 21, and Table 22.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.
7. When operating at data rates of 1.5 Gb/s to 2.5 Gb/s, the minimum V_{IH} is 0.790V. These data rates, outlined in Table 72 are supported for XC devices only.

Table 16: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards**

I/O Standard[1, 2]	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 17: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]			V_{ILHS}[3]	V_{IHHS}[3]	V_{OCM} (V)[4]			V_{OD} (V)[5]		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS[8]	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_ DCI_HS[9, 10]	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS_25 is specified in Table 23.
7. LVDS is specified in Table 24.
8. Only the SUB_LVDS receiver is supported in HD I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.
10. When operating at data rates of 1.5 Gb/s to 2.5 Gb/s, the minimum V_{ID} is 0.040V. These data rates, outlined in Table 72 are supported for XC devices only.

Table 18: **Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]		V_{OL} (V)[3]	V_{OH} (V)[4]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL135_II	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL15_II	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.0	–8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 19: **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks**

I/O Standard[1]	V_{ICM} (V)[2]			V_{ID} (V)[3]		V_{OL} (V)[4]	V_{OH} (V)[5]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} - 0.400$	6.2	–6.2
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0
DIFF_SSTL18_I	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 20, Table 21, Table 22.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 20: **DC Input Levels for Differential POD10 and POD12 I/O Standards**

I/O Standard[1, 2]	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 21: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards**

Symbol	Description[1, 2]	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 22)	36	40	44	Ω
R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 22)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 22: **Definitions for DC Output Levels for Single-ended and Differential POD10 and POD12 Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity)	$0.8 \times V_{CCO}$	V

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 23: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{CCO}[1]	Supply voltage	2.375	2.500	2.625	V
V_{IDIFF}	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	100	350	600[2]	mV
V_{ICM}	Input common-mode voltage	0.300	1.200	1.425	V

Notes:

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 24: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}[1]	Supply voltage		1.710	1.800	1.890	V
V_{ODIFF}[2]	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}[2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}[3]	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600[3]	mV
V_{ICM_DC}[4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.425	V
V_{ICM_AC}[5]	Input common-mode voltage (AC coupling)		0.600	–	1.100	V

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the Recommended Operating Condition (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in the following table.

Table 25: **Speed Specification Version By Device**

2020.2.2	Device
1.29	XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, XCZU29DR, XCZU39DR XQZU21DR, XQZU28DR, XQZU29DR
1.32	XCZU43DR, XCZU46DR, XCZU47DR, XCZU48DR, XCZU49DR, XQZU48DR, XQZU49DR

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

- **Advance Product Specification:** These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.
- **Preliminary Product Specification:** These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.
- **Product Specification:** These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ RFSoCs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 26 correlates the current status of the Zynq UltraScale+ RFSoC on a per speed grade basis. See Table 3 for operating voltages listed by speed grade.

Table 26: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU21DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V)[1], -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V)[1], -2LE (V_{CCINT} = 0.72V)[2], -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XCZU25DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V)[1], -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V)[1], -2LE (V_{CCINT} = 0.72V)[2], -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XCZU27DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V)[1], -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V)[1], -2LE (V_{CCINT} = 0.72V)[2], -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XCZU28DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V)[1], -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V)[1], -2LE (V_{CCINT} = 0.72V)[2], -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XCZU29DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V)[1], -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V)[1], -2LE (V_{CCINT} = 0.72V)[2], -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XCZU39DR			-2I (V_{CCINT} = 0.85V) -2LI (V_{CCINT} = 0.72V)[2]
XQZU21DR			-2I (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V)[1], -1M (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.72V)[2]
XQZU28DR			-2I (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V)[1], -1M (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.72V)[2]
XQZU29DR			-2I (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.85V)[1], -1M (V_{CCINT} = 0.85V), -1LI (V_{CCINT} = 0.72V)[2]
XCZU43DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XCZU46DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XCZU47DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XCZU48DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XCZU49DR			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V), -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]
XQZU48DR			-2I (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1M (V_{CCINT} = 0.85V), -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]

Table 26: **Speed Grade Designations by Device** *(cont'd)*

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XQZU49DR			-2I (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -1M (V_{CCINT} = 0.85V), -2LI (V_{CCINT} = 0.72V)[2], -1LI (V_{CCINT} = 0.72V)[2]

Notes:

1. The low power -1LI and -2LE devices, where V_{CCINT} = 0.85V, are listed in the Vivado Design Suite as -1L and -2L respectively.
2. The lowest power -1LI, -2LE, and -2LI devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -1LV, -2LV, and -2LVI, respectively.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 27 lists the production released Zynq UltraScale+ RFSoC, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: **Zynq UltraScale+ RFSoC Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages[1, 2]							
	0.85V					0.72V		
	-2	-1	-1M	-2LE	-1LI	-2LE	-2LI	-1LI
XCZU21DR	Vivado tools 2018.2 v1.20		N/A	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2.1 v1.21
XCZU25DR	Vivado tools 2018.2 v1.20		N/A	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2.1 v1.21
XCZU27DR	Vivado tools 2018.2 v1.20		N/A	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2.1 v1.21
XCZU28DR	Vivado tools 2018.2 v1.20		N/A	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2.1 v1.21
XCZU29DR	Vivado tools 2018.2 v1.20		N/A	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2 v1.20	Vivado tools 2018.2.1 v1.21	Vivado tools 2018.2.1 v1.21
XCZU39DR	Vivado tools 2019.1 v1.23	N/A	N/A	N/A	N/A	N/A	Vivado tools 2019.1 v1.23	N/A
XQZU21DR	Vivado tools 2018.3 v1.23		Vivado tools 2018.3 v1.23	N/A	Vivado tools 2018.3 v1.23	N/A	N/A	Vivado tools 2018.3 v1.23
XQZU28DR	Vivado tools 2018.3 v1.23		Vivado tools 2018.3 v1.23	N/A	Vivado tools 2018.3 v1.23	N/A	N/A	Vivado tools 2018.3 v1.23
XQZU29DR	Vivado tools 2018.3.1 v1.23		Vivado tools 2018.3.1 v1.23	N/A	Vivado tools 2018.3.1 v1.23	N/A	N/A	Vivado tools 2018.3.1 v1.23
XCZU43DR	Vivado tools 2020.2 v1.30		N/A	N/A	N/A	N/A	Vivado tools 2020.2 v1.30	
XCZU46DR	Vivado tools 2020.2 v1.30		N/A	N/A	N/A	N/A	Vivado tools 2020.2 v1.30	
XCZU47DR	Vivado tools 2020.2 v1.30		N/A	N/A	N/A	N/A	Vivado tools 2020.2 v1.30	
XCZU48DR	Vivado tools 2020.2 v1.30		N/A	N/A	N/A	N/A	Vivado tools 2020.2 v1.30	
XCZU49DR	Vivado tools 2020.2 v1.30		N/A	N/A	N/A	N/A	Vivado tools 2020.2 v1.30	
XQZU48DR	Vivado tools 2020.2.2 v1.32			N/A	N/A	N/A	Vivado tools 2020.2.2 v1.32	
XQZU49DR	Vivado tools 2020.2.2 v1.32			N/A	N/A	N/A	Vivado tools 2020.2.2 v1.32	

Notes:

1. See Table 3 for the complete list of operating voltages by speed grade.
2. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

Processor System (PS) Performance Characteristics

Table 28: **Processor Performance**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{APUMAX}	Maximum APU clock frequency	1333	1200	MHz
F_{RPUMAX}	Maximum RPU clock frequency	533	500	MHz
F_{GPUMAX}	Maximum GPU clock frequency	600	600	MHz

Table 29: **Configuration and Security Unit Performance**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{CSUCIBMAX}$	Maximum CSU crypto interface block frequency	400	400	MHz

Table 30: **PS DDR Performance**

Memory Standard	DRAM Type	Speed Grade				Units
		-2E/-2LE -1E		-2I/-2LI -1I/-1M/-1LI		
		Min	Max	Min	Max	
DDR4[4]	Single rank component	664	2400	1000	2400	Mb/s
	1 rank DIMM[1, 2]	664	2133	1000	2133	Mb/s
	2 rank DIMM[1, 3]	664	1866	1000	1866	Mb/s
LPDDR4[5]	Single die package[6, 7]	664	2400	1000	2400	Mb/s
	Dual die package[6, 7]	664	2133	1000	2133	Mb/s
DDR3	Single rank component	664	2133	1000	2133	Mb/s
	1 rank DIMM[1, 2]	664	1866	1000	1866	Mb/s
	2 rank DIMM[1, 3]	664	1600	1000	1600	Mb/s
DDR3L	Single rank component	664	1866	1000	1866	Mb/s
	1 rank DIMM[1, 2]	664	1600	1000	1600	Mb/s
	2 rank DIMM[1, 3]	664	1333	1000	1333	Mb/s
LPDDR3	Single die package[8]	664	1600	1000	1600	Mb/s
	Dual die package[8]	664	1333	1000	1333	Mb/s

Notes:

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, and UDIMM.
2. Includes: 1 rank 1 slot, dual-die package 2 rank.
3. Includes: 2 rank 1 slot.
4. The JEDEC JESD79-4B standard for DDR4 SDRAM limits the maximum t_{CK} to 1.6 ns. Because of this limitation, Xilinx recommends working with your DRAM vendor to verify support for data rates at or less than 1066 Mb/s.
5. Byte-mode LPDDR4 devices are not supported.
6. LPDDR4 single die package with ECC is limited to the performance specified for the LPDDR4 dual die package.
7. LPDDR4 support is only available as a 32-bit interface.
8. 64-bit LPDDR3 interface performance values are defined without ECC support.

Table 31: **PS NAND NV-DDR Synchronous Performance**

Memory Standard	Mode	Speed Grade		Units
		-2	-1	
		Max	Max	
NV-DDR[1]	5	200	200	Mb/s
	4	166.6	166.6	Mb/s
	3	133.3	133.3	Mb/s
	2	100	100	Mb/s
	1	66.6	66.6	Mb/s
	0	40	40	Mb/s

Notes:
1. The PS NAND memory controller interface for NV-DDR switching characteristics meets the requirements of the ONFI 3.1 specification.

Table 32: **PS NAND SDR Asynchronous Performance**

Memory Standard	Mode	Speed Grade		Units
		-2	-1	
		Max	Max	
SDR[1, 2]	5	50	50	Mb/s
	4	40	40	Mb/s
	3	33.3	33.3	Mb/s
	2	28.5	28.5	Mb/s
	1	20	20	Mb/s
	0	10	10	Mb/s

Notes:
1. The PS NAND memory controller interface for SDR switching characteristics meets the requirements of the ONFI 3.1 specification.
2. The NAND controller reference clock frequency maximum is 83 MHz.

Table 33: **PS-PL Interface Performance**

Symbol	Description	Min	Max	Units
$F_{EMIOGEMCLK}$	EMIO gigabit Ethernet controller maximum frequency	–	125	MHz
$F_{EMIOSDCLK}$	EMIO SD controller maximum frequency	–	25	MHz
$F_{EMIOSPICLK}$	EMIO SPI controller maximum frequency	–	25	MHz
$F_{EMIOTRACECLK}$	EMIO trace controller maximum frequency	–	125	MHz
$F_{FCIDMACLK}$	Flow control interface DMA maximum frequency	–	333	MHz
F_{AXICLK}	Maximum AXI interface performance	–	333	MHz
$F_{DPLIVEVIDEO}$	DisplayPort controller live video interface maximum frequency	–	300	MHz

PS Switching Characteristics

PS Clocks

Table 34: **PS Reference Clock Requirements**

Symbol	Description[1]	Min	Typ	Max	Units
$T_{RMSJPSCLK}$	PS_REF_CLK input RMS clock jitter	–	–	3	ps
$T_{PJPSCLK}$	PS_REF_CLK input period jitter (peak-to-peak) Number of clock cycles = 10,000	–	–	50	ps
$T_{DCPSCLK}$	PS_REF_CLK duty cycle	45	–	55	%
$T_{RFPSCLK}$	PS_REF_CLK rise time (20%–80%) and fall time (80%–20%)	–	–	2.22	ns
F_{PSCLK}	PS_REF_CLK frequency	27	–	60	MHz

Notes:

1. The values in this table are applicable to alternative PS reference clock inputs ALT_REF_CLK, AUX_REF_CLK, and VIDEO_CLK.

Table 35: **PS RTC Crystal Requirements**

Symbol	Description[1]	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency	–	32.8	–	KHz
T_{FTXTAL}	Frequency tolerance	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz)	–	70	–	KΩ
C_{SHUNT}	Crystal shunt capacitance	–	1.4	–	pF

Notes:

1. See the crystal circuit example in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

Table 36: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
$T_{LOCKPSPLL}$	PLL maximum lock time	100	100	µs
$F_{PSPLLMAX}$	PLL maximum output frequency	1600	1600	MHz
$F_{PSPLLMIN}$	PLL minimum output frequency	750	750	MHz
$F_{PSPLLVCOMAX}$	PLL maximum VCO frequency	3000	3000	MHz
$F_{PSPLLVCOMIN}$	PLL minimum VCO frequency	1500	1500	MHz

Table 37: **PS Reset Assertion Timing Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time[1]	10	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time	3	–	–	PS_REF_CLK Clock Cycles

Notes:

1. PS_POR_B must be asserted Low at power-up and continue to be asserted for a duration of T_{PSPOR} after all the PS supply voltages reach minimum levels. PS_POR_B must be asserted Low for the duration of T_{POR} when the PS and PL power-up at the same time and the application uses both the PS and PL after power-up.

Table 38: **PS Clocks Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{TOPSW\_MAINMAX}$	FPD AXI interconnect clock maximum frequency	533	533	MHz
$F_{TOPSW\_LSBUSMAX}$	FPD APB bus clock maximum frequency	100	100	MHz
$F_{GDMAMAX}$	FPD-DMA controller clock maximum frequency	600	600	MHz
$F_{DPDMAMAX}$	DisplayPort controller clock maximum frequency	600	600	MHz
$F_{LPD\_SWITCH\_CTRLMAX}$	LPD AXI interconnect clock maximum frequency	500	500	MHz
$F_{LPD\_LSBUS\_CTRLMAX}$	LPD APB bus clock maximum frequency	100	100	MHz
$F_{ADMAMAX}$	LPD-DMA maximum frequency	500	500	MHz
$F_{APLL\_TO\_LPDMAX}$	APLL_TO_LPD maximum frequency	533	533	MHz
$F_{DPLL\_TO\_LPDMAX}$	DPLL_TO_LPD maximum frequency	533	533	MHz
$F_{VPLL\_TO\_LPDMAX}$	VPLL_TO_LPD maximum frequency	533	533	MHz
$F_{IOPLL\_TO\_FPDMAX}$	IOPLL_TO_FPD maximum frequency	533	533	MHz
$F_{RPLL\_TO\_FPDMAX}$	RPLL_TO_FPD maximum frequency	533	533	MHz

PS Configuration

Table 39: **Processor Configuration Access Port Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
F_{PCAPCK}	Maximum processor configuration access port (PCAP) frequency	200	200	150	150	MHz

Table 40: **Boundary-Scan Port Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
F_{TCK}	JTAG clock maximum frequency	25	25	15	15	MHz
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup and hold	4.0/2.0	4.0/2.0	5.0/2.0	5.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	16.1	16.1	24	24	ns, Max

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength.

PS Interface Specifications

PS Quad-SPI Controller Interface

Table 41: **Generic Quad-SPI Interface**

Symbol	Description[1]	Load Conditions[2]	Min	Max	Units
Quad-SPI device clock frequency operating at 150 MHz. Loopback enabled. LVCMOS 1.8V or LVCMOS 3.3V I/O standard.					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	15 pF	45	55	%
$T_{QSPISSSCLK1}$	Slave select asserted to next clock edge	15 pF	5.0	–	ns
$T_{QSPISCLKSS1}$	Clock edge to slave select deasserted	15 pF	5.0	–	ns
$T_{QSPICKO1}$	Clock to output delay, all outputs	15 pF	2.9	4.5	ns
$T_{QSPIDCK1}$	Setup time, all inputs	15 pF	0.9	–	ns
$T_{QSPICKD1}$	Hold time, all inputs	15 pF	1.0	–	ns
$F_{QSPICLK1}$	Quad-SPI device clock frequency	15 pF	–	150	MHz
$F_{QSPIREFCLK1}$	Quad-SPI reference clock frequency	15 pF	–	300	MHz
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V or LVCMOS 3.3V I/O standard.					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK2}$	Slave select asserted to next clock edge	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPISCLKSS2}$	Clock edge to slave select deasserted	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPICKO2}$	Clock to output delay, all outputs	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
$T_{QSPIDCK2}$	Setup time, all inputs	15 pF	2.3	–	ns
		30 pF	2.3	–	ns
$T_{QSPICKD2}$	Hold time, all inputs	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPICLK2}$	Quad-SPI device clock frequency	15 pF	–	100	MHz
		30 pF	–	100	MHz
$F_{QSPIREFCLK2}$	Quad-SPI reference clock frequency	15 pF	–	200	MHz
		30 pF	–	200	MHz
Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 1.8V I/O standard.					
$T_{DCQSPICLK3}$	Quad-SPI clock duty cycle	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK3}$	Slave select asserted to next clock edge[3]	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPISCLKSS3}$	Clock edge to slave select deasserted	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPICKO3}$	Clock to output delay, all outputs	15 pF	5.2	14.8	ns
		30 pF	5.2	14.8	ns
$T_{QSPIDCK3}$	Setup time, all inputs	15 pF	13.4	–	ns
		30 pF	14.1	–	ns

Table 41: **Generic Quad-SPI Interface** *(cont'd)*

Symbol	Description[1]	Load Conditions[2]	Min	Max	Units
$T_{QSPICKD3}$	Hold time, all inputs	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK3}$	Quad-SPI reference clock frequency	15 pF	–	160	MHz
		30 pF	–	160	MHz
$F_{QSPICLK3}$	Quad-SPI clock frequency	15 pF	–	40	MHz
		30 pF	–	40	MHz
Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 3.3V I/O standard.					
$T_{DCQSPICLK4}$	Quad-SPI clock duty cycle	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK4}$	Slave select asserted to next clock edge[3]	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPISCLKSS4}$	Clock edge to slave select deasserted	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPICKO4}$	Clock to output delay, all outputs	15 pF	5.2	14.8	ns
		30 pF	5.2	14.8	ns
$T_{QSPIDCK4}$	Setup time, all inputs	15 pF	13.9	–	ns
		30 pF	14.9	–	ns
$T_{QSPICKD4}$	Hold time, all inputs	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK4}$	Quad-SPI reference clock frequency	15 pF	–	160	MHz
		30 pF	–	160	MHz
$F_{QSPICLK4}$	Quad-SPI clock frequency	15 pF	–	40	MHz
		30 pF	–	40	MHz

Notes:

1. The test conditions are configured for the generic Quad-SPI interface at 150/100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for dual-parallel stacked or stacked modes.
3. $T_{QSPISSSCLK3}$ and $T_{QSPISSSCLK4}$ are only valid when two reference clock cycles are programmed between the chip select and clock.

Table 42: **Linear Quad-SPI Interface**

Symbol	Description[1]	Load Conditions[2]	Min	Max	Units
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V or LVCMOS 3.3V I/O standard.					
$T_{DCQSPICLK5}$	Quad-SPI clock duty cycle	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK5}$	Slave select asserted to next clock edge[3]	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPISCLKSS5}$	Clock edge to slave select deasserted	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPICKO5}$	Clock to output delay, all outputs	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
$T_{QSPIDCK5}$	Setup time, all inputs	15 pF	2.4	–	ns
		30 pF	2.4	–	ns

Table 42: **Linear Quad-SPI Interface** *(cont'd)*

Symbol	Description[1]	Load Conditions[2]	Min	Max	Units
$T_{QSPICKD5}$	Hold time, all inputs	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK5}$	Quad-SPI reference clock frequency	15 pF	–	200	MHz
		30 pF	–	200	MHz
$F_{QSPICLK5}$	Quad-SPI device clock frequency	15 pF	–	100	MHz
		30 pF	–	100	MHz
Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 1.8V I/O standard.					
$T_{DCQSPICLK6}$	Quad-SPI clock duty cycle	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK6}$	Slave select asserted to next clock edge	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPISCLKSS6}$	Clock edge to slave select deasserted	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPICKO6}$	Clock to output delay, all outputs	15 pF	5.2	14.8	ns
		30 pF	5.2	14.8	ns
$T_{QSPIDCK6}$	Setup time, all inputs	15 pF	13.4	–	ns
		30 pF	13.4	–	ns
$T_{QSPICKD6}$	Hold time, all inputs	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK6}$	Quad-SPI reference clock frequency	15 pF	–	160	MHz
		30 pF	–	160	MHz
$F_{QSPICLK6}$	Quad-SPI device clock frequency	15 pF	–	40	MHz
		30 pF	–	40	MHz
Quad-SPI device clock frequency operating at 40 MHz. Loopback disabled. LVCMOS 3.3V I/O standard.					
$T_{DCQSPICLK7}$	Quad-SPI clock duty cycle	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK7}$	Slave select asserted to next clock edge	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPISCLKSS7}$	Clock edge to slave select deasserted	15 pF	7.0	–	ns
		30 pF	7.0	–	ns
$T_{QSPICKO7}$	Clock to output delay, all outputs	15 pF	5.2	14.8	ns
		30 pF	5.2	14.8	ns
$T_{QSPIDCK7}$	Setup time, all inputs	15 pF	14.0	–	ns
		30 pF	14.0	–	ns
$T_{QSPICKD7}$	Hold time, all inputs	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK7}$	Quad-SPI reference clock frequency	15 pF	–	160	MHz
		30 pF	–	160	MHz

Table 42: **Linear Quad-SPI Interface** *(cont'd)*

Symbol	Description[1]	Load Conditions[2]	Min	Max	Units
$F_{QSPICLK7}$	Quad-SPI device clock frequency	15 pF	–	40	MHz
		30 pF	–	40	MHz

Notes:

1. The test conditions are configured for the linear Quad-SPI interface at 100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for stacked modes.
3. $T_{QSPISSSCLK5}$ is only valid when two reference clock cycles are programmed between chip select and clock.

PS USB Interface

Table 43: **ULPI Interface**

Symbol	Description[1]	Min	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs	4.5	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs	0	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs	2.0	8.86	ns
$F_{ULPICLK}$	ULPI reference clock frequency	–	60	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Gigabit Ethernet Controller Interface

Table 44: **RGMII Interface**

Symbol	Description[1]	Min	Max	Units
$T_{DCGEMTXCLK}$	Transmit clock duty cycle	45	55	%
$T_{GEMTXCKO}$	TXD output clock to out time	–0.5	0.5	ns
$T_{GEMRXDCK}$	RXD input setup time	0.8	–	ns
$T_{GEMRXCKD}$	RXD input hold time	0.8	–	ns
$T_{MDIOCLK}$	MDC output clock period	400	–	ns
$T_{MDIOCKL}$	MDC low time	160	–	ns
$T_{MDIOCKH}$	MDC high time	160	–	ns
$T_{MDIODCK}$	MDIO input data setup time	80	–	ns
$T_{MDIOCKD}$	MDIO input data hold time	0.0	–	ns
$T_{MDIOCKO}$	MDIO output data delay time	–1.0	15	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency	–	125	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency	–	125	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 2.5V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SD/SDIO Controller Interface

Table 45: **SD/SDIO Interface**

Symbol	Description[1]	Min	Max	Units
SD/SDIO Interface DDR50 Mode				
$T_{DCDDRCLK}$	SD device clock duty cycle	45	55	%
$T_{SDDDRCKO1}$	Clock to output delay, data[2]	1.0	6.8	ns
$T_{SDDDRIVW}$	Input valid data window[3]	3.5	–	ns
$T_{SDDDRDCK2}$	Input setup time, command	4.7	–	ns
$T_{SDDDRCKD2}$	Input hold time, command	1.5	–	ns
$T_{SDDDRCKO2}$	Clock to output delay, command	1.0	13.8	ns
$F_{SDDDRCLK}$	High-speed mode SD device clock frequency	–	50	MHz
SD/SDIO Interface SDR104				
$T_{DCSDHSCLK1}$	SD device clock duty cycle	40	60	%
$T_{SDSDRCKO1}$	Clock to output delay, all output[2]	1.0	3.2	ns
$T_{SDSDR1IVW}$	Input valid data window[3]	0.5	–	UI
$F_{SDSDRCLK1}$	SDR104 mode device clock frequency	–	200	MHz
SD/SDIO Interface SDR50/25				
$T_{DCSDHSCLK2}$	SD device clock duty cycle	40	60	%
$T_{SDSDRCKO2}$	Clock to output delay, all outputs[2]	1.0	6.8	ns
$T_{SDSDR2IVW}$	Input valid data window[3]	0.3	–	UI
$F_{SDSDRCLK2}$	SDR50 mode device clock frequency	–	100	MHz
	SDR25 mode device clock frequency	–	50	MHz
SD/SDIO Interface SDR12				
$T_{DCSDHSCLK3}$	SD device clock duty cycle	40	60	%
$T_{SDSDRCKO3}$	Clock to output delay, all outputs	1.0	36.8	ns
$T_{SDSDRDCK3}$	Input setup time, all inputs	10.0	–	ns
$T_{SDSDRCKD3}$	Input hold time, all inputs	1.5	–	ns
$F_{SDSDRCLK3}$	SDR12 mode device clock frequency	–	25	MHz
SD/SDIO Interface High-Speed Mode				
$T_{DCSDHSCLK}$	SD device clock duty cycle	47	53	%
$T_{SDHSCKO}$	Clock to output delay, all outputs[2]	2.2	13.8	ns
$T_{SDHSDIVW}$	Input valid data window[3]	0.35	–	UI
$F_{SDHSCLK}$	High-speed mode SD device clock frequency	–	50	MHz
SD/SDIO Interface Standard Mode				
$T_{DCSDSCLK}$	SD device clock duty cycle	45	55	%
T_{SDSCKO}	Clock to output delay, all outputs	–2.0	4.5	ns
T_{SDSDCK}	Input setup time, all inputs	2.0	–	ns
T_{SDSCKD}	Input hold time, all inputs	2.0	–	ns
$F_{SDIDCLK}$	Clock frequency in identification mode	–	400	KHz

Table 45: **SD/SDIO Interface** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
F_{SDSCLK}	Standard SD device clock frequency	–	19	MHz

Notes:

1. The test conditions SD/SDIO standard mode (default speed mode) use an 8 mA drive strength, fast slew rate, and a 30 pF load. For SD/SDIO high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other SD/SDIO modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS eMMC Standard Interface

Table 46: **eMMC Standard Interface**

Symbol	Description[1]	Min	Max	Units
eMMC Standard Interface				
$T_{DCEMMCHSCLK}$	eMMC clock duty cycle	45	55	%
$T_{EMMCHSCKO}$	Clock to output delay, all outputs	–2.0	4.5	ns
$T_{EMMCHSDCK}$	Input setup time, all inputs	2.0	–	ns
$T_{EMMCHSCKD}$	Input hold time, all inputs	2.0	–	ns
$F_{EMMCHSCLK}$	eMMC clock frequency	–	25	MHz
eMMC High-Speed SDR Interface				
$T_{DCEMMCHSCLK}$	eMMC high-speed SDR clock duty cycle	45	55	%
$T_{EMMCHSCKO}$	Clock to output delay, all outputs[2]	3.2	16.8	ns
$T_{EMMCHSDIVW}$	Input valid data window[3]	0.4	–	UI
$F_{EMMCHSCLK}$	eMMC high speed SDR clock frequency	–	50	MHz
eMMC High-Speed DDR Interface				
$T_{DCEMMCDDRCLK}$	eMMC high-speed DDR clock duty cycle	45	55	%
$T_{EMMCDDRSCKO1}$	Data clock to output delay[2]	2.7	7.3	ns
$T_{EMMCDDRIVW}$	Input valid data window[3]	3.5	–	ns
$T_{EMMCDDRSCKO2}$	Command clock to output delay	3.2	16	ns
$T_{EMMCDDRDCK2}$	Command input setup time	3.9	–	ns
$T_{EMMCDDRCKD2}$	Command input hold time	2.5	–	ns
$F_{EMMCDDRCLK}$	eMMC high-speed DDR clock frequency	–	50	MHz
eMMC HS200 Interface				
$T_{DCEMMCHS200CLK}$	eMMC HS200 clock duty cycle	40	60	%
$T_{EMMCHS200CKO}$	Clock to output delay, all outputs[2]	1.0	3.4	ns
$T_{EMMCSDR1IVW}$	Input valid data window[3]	0.4	–	UI
$F_{EMMCHS200CLK}$	eMMC HS200 clock frequency	–	200	MHz

Notes:

1. The test conditions for eMMC standard mode use an 8 mA drive strength, fast slew rate, and a 30 pF load. For eMMC high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other eMMC modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS I2C Controller Interface

Table 47: **I2C Interface**

Symbol	Description[1]	Min	Max	Units
I2C Fast-mode Interface				
$T_{I2CFCKL}$	SCL Low time	1.3	–	µs
$T_{I2CFCKH}$	SCL High time	0.6	–	µs
$T_{I2CFCKO}$	SDA clock to out delay	–	900	ns
$T_{I2CFDCK}$	SDA input setup time	100	–	ns
$F_{I2CFCLK}$	SCL clock frequency	–	400	KHz
I2C Standard-mode Interface				
$T_{I2CSCKL}$	SCL Low time	4.7	–	µs
$T_{I2CSCKH}$	SCL High time	4.0	–	µs
$T_{I2CSCKO}$	SDA clock to out delay	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time	250	–	ns
$F_{I2CSCLK}$	SCL clock frequency	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SPI Controller Interface

Table 48: **SPI Interfaces**

Symbol	Description[1]	Min	Max	Units
SPI Master Interface				
$T_{DCMSPICLK}$	SPI master mode clock duty cycle	45	55	%
$T_{MSPISSSCLK}$	Slave select asserted to first active clock edge	1[2]	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted	1[2]	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPIDCK}$	Input setup time for MISO	–2.0	–	ns
$T_{MSPICKD}$	Input hold time for MISO	0.3	–	$F_{MSPICLK}$ cycles
$T_{MSPICKO}$	MOSI and slave select clock to out delay	–2.0	5.0	ns
$F_{MSPICLK}$	SPI master device clock frequency	–	50	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	200	MHz
SPI Slave Interface				
$T_{SSPISSSCLK}$	Slave select asserted to first active clock edge	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISCLKSS}$	Last active clock edge to slave select deasserted	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPIDCK}$	Input setup time for MOSI	5.0	–	ns
$T_{SSPICKD}$	Input hold time for MOSI	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	MISO clock to out delay	0.0	13.0	ns
$F_{SSPICLK}$	SPI slave mode device clock frequency	–	25	MHz

Table 48: **SPI Interfaces** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency	–	200	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
2. Valid when two SPI_REF_CLK delays are programmed between CS and CLK for $T_{MSPISSSCLK}$, and between CLK and CS for $T_{MSPISCLKSS}$ in the SPI delay_reg0 register.

PS CAN Controller Interface

Table 49: **CAN Interface**

Symbol	Description[1]	Min	Max	Units
$T_{PWCANRX}$	Receive pulse width	1.0	–	µs
$T_{PWCANTX}$	Transmit pulse width	1.0	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency	–	100	MHz
	Externally sourced CAN reference clock frequency	–	40	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS DAP Interface

Table 50: **DAP Interface**

Symbol	Description[1, 2]	Min	Max	Units
$T_{PDAPDCK}$	PS DAP input setup time	3.0	–	ns
$T_{PDAPCKD}$	PS DAP input hold time	2.0	–	ns
$T_{PDAPCKO}$	PS DAP clock to out delay	–	10.86	ns
$F_{PDAPCLK}$	PS DAP clock frequency	–	44	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. PS DAP interface signals connect to MIO pins.

PS UART Interface

Table 51: **UART Interface**

Symbol	Description[1]	Min	Max	Units
$BAUD_{TXMAX}$	Transmit baud rate	–	6.25	Mb/s
$BAUD_{RXMAX}$	Receive baud rate	–	6.25	Mb/s
$F_{UART\_REF\_CLK}$	UART reference clock frequency	–	100	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS General Purpose I/O Interface

Table 52: **General Purpose I/O (GPIO) Interface**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input High pulse width	10 x 1/$F_{LPD\_LSBUS\_CTRLMAX}$	–	µs
$T_{PWGPIOL}$	Input Low pulse width	10 x 1/$F_{LPD\_LSBUS\_CTRLMAX}$	–	µs

PS Trace Interface

Table 53: **Trace Interface**

Symbol	Description[1]	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs	–0.5	0.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle	45	55	%
F_{TCECLK}	Trace clock frequency	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Triple-timer Counter Interface

Table 54: **Triple-timer Counter Interface**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width	60.4	–	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency	–	16.5	MHz
$T_{TTCICLKL}$	Triple-timer counter input clock high pulse width	1.5 x 1/$F_{LPD\_LSBUS\_CTRLMAX}$	–	ns
$T_{TTCICLKH}$	Triple-timer counter input clock low pulse width	1.5 x 1/$F_{LPD\_LSBUS\_CTRLMAX}$	–	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency	–	$F_{LPD\_LSBUS\_CTRLMAX}$/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: **Watchdog Timer Interface**

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency	–	100	MHz

PS-GTR Transceiver

Table 56: **PS-GTR Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)		100	–	1200	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND		75	–	$V_{PS\_MGTRAVCC}$	mV
V_{CMIN}	Common mode input voltage		–	0	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to maximum value	800	–	–	mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based)		$V_{PS\_MGTRAVCC} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
$R_{MGTRREF}$	Resistor value between calibration resistor pin to GND		497.5	500	502.5	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (All packages)		–	–	20	ps
C_{EXT}	Recommended external AC coupling capacitor[2]		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 57: **PS-GTR Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 58: **PS-GTR Transceiver Performance**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{GTRMAX}	PS-GTR maximum line rate	6.0	6.0	Gb/s
F_{GTRMIN}	PS-GTR minimum line rate	1.25	1.25	Gb/s

Table 59: **PS-GTR Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Min	Typ	Max	Units
T_{LOCK}	Initial PLL lock	–	–	0.11	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time	–	–	24×10^6	UI

Table 60: **PS-GTR Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequencies supported	PCI Express®[1]	100 MHz			
		SATA	125 MHz or 150 MHz			
		USB 3.0	26 MHz, 52 MHz, or 100 MHz			
		DisplayPort	27 MHz, 108 MHz, or 135 MHz			
		SGMII	125 MHz			
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%
		USB 3.0 with reference clock <40 MHz	47.5	–	52.5	%

Notes:

1. Only the common clock architecture is supported.

Table 61: **PS-GTR Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description[1]	Offset Frequency	Min	Typ	Max	Units
$PLL_{REFCLKMASK}$	PLL reference clock select phase noise mask at REFCLK frequency = 25 MHz	100	–	–	–102	dBc/Hz
		1 KHz	–	–	–124	
		10 KHz	–	–	–132	
		100 KHz	–	–	–139	
		1 MHz	–	–	–152	
		10 MHz	–	–	–154	
	PLL reference clock select phase noise mask at REFCLK frequency = 50 MHz	100	–	–	–96	dBc/Hz
		1 KHz	–	–	–118	
		10 KHz	–	–	–126	
		100 KHz	–	–	–133	
		1 MHz	–	–	–146	
		10 MHz	–	–	–148	
	PLL reference clock select phase noise mask at REFCLK frequency = 100 MHz	100	–	–	–90	dBc/Hz
		1 KHz	–	–	–112	
		10 KHz	–	–	–120	
		100 KHz	–	–	–127	
		1 MHz	–	–	–140	
		10 MHz	–	–	–142	
	PLL reference clock select phase noise mask at REFCLK frequency = 125 MHz	100	–	–	–88	dBc/Hz
		1 KHz	–	–	–110	
		10 KHz	–	–	–118	
		100 KHz	–	–	–125	
		1 MHz	–	–	–138	
		10 MHz	–	–	–140	
	PLL reference clock select phase noise mask at REFCLK frequency = 150 MHz	100	–	–	–86	dBc/Hz
		1 KHz	–	–	–108	
		10 KHz	–	–	–116	
		100 KHz	–	–	–123	
		1 MHz	–	–	–136	
		10 MHz	–	–	–138	

Notes:

1. For reference clock frequencies not in this table, use the phase noise mask for the nearest reference clock frequency.

Table 62: **PS-GTR Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRTX}	Serial data rate range		1.25	–	6.0	Gb/s
T_{RTX}	TX rise time	20%–80%	–	65	–	ps
T_{FTX}	TX fall time	80%–20%	–	65	–	ps

Table 63: **PS-GTR Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRRX}	Serial data rate		1.25	–	6	Gb/s
RX_{SST}	Receiver spread-spectrum tracking	Modulated at 33 KHz	–5000	–	0	ppm
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	All data rates	–350	–	350	ppm

Table 64: **PCI Express Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description[1]	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2[2]	Receiver inherent timing error	5000	0.4	–	UI
	Receiver inherent deterministic timing error	5000	0.3	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 65: **Serial ATA (SATA) Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial ATA Transmitter Jitter Generation					
SATA Gen 1	Total transmitter jitter	1500	–	0.37	UI
SATA Gen 2	Total transmitter jitter	3000	–	0.37	UI
SATA Gen 3	Total transmitter jitter	6000	–	0.52	UI
Serial ATA Receiver High Frequency Jitter Tolerance					
SATA Gen 1	Total receiver jitter tolerance	1500	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance	3000	0.27	–	UI
SATA Gen 3	Total receiver jitter tolerance	6000	0.16	–	UI

Table 66: **DisplayPort Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description[1]	Line Rate (Mb/s)	Min	Max	Units
DisplayPort Transmitter Jitter Generation					
RBR	Total transmitter jitter	1620	–	0.42	UI
HBR	Total transmitter jitter	2700	–	0.42	UI
HBR2 D10.2	Total transmitter jitter	5400	–	0.40	UI
HBR2 CPAT	Total transmitter jitter	5400	–	0.58	UI

Notes:

1. Only the transmitter is supported.

Table 67: **USB 3.0 Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance	5000	0.2	–	UI

Table 68: **Serial-GMII Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter	1250	–	0.25	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance	1250	0.25	–	UI

PS System Monitor Specifications

Table 69: **PS SYSMON Specifications**

Parameter	Comments	Conditions	Min	Typ	Max	Units
V_{CC_PSADC} = 1.8V ±3%, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy (T_j = –55°C to 125°C) [1]						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		T_j = –55°C to 110°C	–	–	±3.5	°C
		T_j = 110°C to 125°C	–	–	±5	°C
Supply sensor error[2]	Supply voltages less than or electrically connected to V_{CC_PSADC}	T_j = –55°C to 125°C	–	–	±1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC}	T_j = –55°C to 125°C	–	–	±1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range	T_j = –55°C to 125°C	–	–	±2.5	%
Conversion Rate[3]						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	AMS REFCLK frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	26	MHz

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
3. See the Adjusting the Acquisition Settling Time section in the *UltraScale Architecture System Monitor User Guide* (UG580).

Programmable Logic (PL) Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the Zynq UltraScale+ RFSoCs. These values are subject to the same guidelines as the AC Switching Characteristics section.

In each of the following LVDS performance tables, the I/O bank type is either high performance (HP) or high density (HD).

In LVDS component mode:

- For the input/output registers in HP I/O banks, the Vivado tools limit clock frequencies to 312.9 MHz for all speed grades.
- For IDDR in HP I/O banks, Vivado tools limit clock frequencies to 625.0 MHz for all speed grades.

- For ODDR in HP I/O banks, Vivado tools limit clock frequencies to 625.0 MHz for all speed grades.

Table 70: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.85V				0.72V				
		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)[1]	HP	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)[1]	HP	0	625	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	0	125	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 71: **LVDS Native Mode Performance**

Description[1, 2]	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.85V				0.72V						
			-2E/-2I/-2LE		-1E/-1I/ -1M/-1LI		-2LE		-2LI		-1LI		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1400	375	1260	375	1260	Mb/s
	8		375	1600	375	1600	375	1600	375	1600	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	700	187.5	630	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	800	187.5	800	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE)[3]	4	HP	375	1600[4]	375	1600[4]	375	1400[4]	375	1260[4]	375	1260[4]	Mb/s
	8		375	1600[4]	375	1600[4]	375	1600[4]	375	1600[4]	375	1600[4]	Mb/s
LVDS RX SDR (RX_BITSLICE)[3]	4	HP	187.5	800	187.5	800	187.5	700	187.5	630	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	800	187.5	800	187.5	800	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_F_{VCOMIN}/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.
4. Asynchronous receiver performance is limited to 1300 Mb/s for the -2E, -2I, and -2LE speed grades and to 1250 Mb/s for the -2LI, -1E, -1I, -1M, and -1LI speed grades.

Table 72: **MIPI D-PHY Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
MIPI D-PHY transmitter or receiver	HP	1500[1]	1260[2]	1260[2]	1260	Mb/s

Notes:

1. The Zynq UltraScale+ RFSoCs performance is specified at 1500 Mb/s when designing with Vivado Design Suite v2019.1 or earlier. For XC devices, the performance is specified at 2500 Mb/s when designing with Vivado Design Suite v2019.1.1 or later. XQ devices are specified at 1500 Mb/s specification.
2. The Zynq UltraScale+ RFSoCs performance is specified at 1260 Mb/s when designing with Vivado Design Suite v2019.1 or earlier. For XC devices, the performance is specified at 2500 Mb/s when designing with Vivado Design Suite v2019.1.1 or later. XQ devices are specified at 1260 Mb/s.

Table 73: **LVDS Native-Mode 1000BASE-X Support**

Description[1]	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages			
		0.85V		0.72V	
		-2	-1	-2	-1
1000BASE-X	HP	Yes			

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

The following table provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ RFSoC memory PHY. Refer to Memory Interfaces for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design User Guide* (UG583), electrical analysis, and characterization of the system.

Table 74: **Maximum Physical Interface (PHY) Rate for Memory Interfaces**

Memory Standard	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.85V		0.72V			
		-2E/-2I/-2LE	-1E/-1I/-1M/-1LI	-2LE	-2LI	-1LI	
DDR4	Single rank component	2666	2400	2400	2400	2133	Mb/s
	1 rank DIMM[1, 2, 3]	2400	2133	2133	2133	1866	Mb/s
	2 rank DIMM[1, 4]	2133	1866	1866	1866	1600	Mb/s
	4 rank DIMM[1, 5]	1600	1333	1333	1333	N/A	Mb/s
DDR3	Single rank component	2133	2133	2133	1866	1866	Mb/s
	1 rank DIMM[1, 2]	1866	1866	1866	1600	1600	Mb/s
	2 rank DIMM[1, 4]	1600	1600	1600	1333	1333	Mb/s
	4 rank DIMM[1, 5]	1066	1066	1066	800	800	Mb/s

Table 74: **Maximum Physical Interface (PHY) Rate for Memory Interfaces** *(cont'd)*

Memory Standard	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.85V		0.72V			
		-2E/-2I/-2LE	-1E/-1I/-1M/-1LI	-2LE	-2LI	-1LI	
DDR3L	Single rank component	1866	1866	1866	1600	1600	Mb/s
	1 rank DIMM[1, 2]	1600	1600	1600	1333	1333	Mb/s
	2 rank DIMM[1, 4]	1333	1333	1333	1066	1066	Mb/s
	4 rank DIMM[1, 5]	800	800	800	606	606	Mb/s
QDR II+	Single rank component[6]	633	600	600	550	550	MHz
RLDRAM 3	Single rank component	1200	1066	1066	933	933	MHz
QDR IV XP	Single rank component	1066	1066	933	933	933	MHz
LPDDR3	Single rank component	1600	1600	1600	1600	1600	Mb/s

Notes:

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
2. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
3. For the DDR4 DDP components at -2 (V_{CCINT} = 0.85V) speed grade, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -2 (V_{CCINT} = 0.85V) speed grade.
4. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
5. Includes: 2 rank 2 slot, 4 rank 1 slot.
6. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

Programmable Logic (PL) Switching Characteristics

The following IOB high-density (HD) and IOB high-performance (HP) tables summarize the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF\_DELAY\_PAD\_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF\_DELAY\_O\_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF\_DELAY\_TD\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table 75: **IOB High Density (HD) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.978	1.058	0.978	1.058	1.574	1.718	1.966	2.101	1.160	1.271	1.515	1.544	ns
DIFF_HSTL_I_18_S	0.978	1.058	0.978	1.058	1.805	1.950	2.197	2.333	1.748	1.867	2.103	2.104	ns

Table 75: **IOB High Density (HD) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
DIFF_HSTL_I_F	0.978	1.058	0.978	1.058	1.611	1.762	2.003	2.145	1.313	1.417	1.668	1.668	ns
DIFF_HSTL_I_S	0.978	1.058	0.978	1.058	1.798	1.913	2.190	2.296	1.630	1.780	1.985	1.986	ns
DIFF_HSUL_12_F	0.911	0.977	0.911	0.977	1.573	1.703	1.965	2.086	1.222	1.335	1.577	1.578	ns
DIFF_HSUL_12_S	0.911	0.977	0.911	0.977	1.711	1.864	2.103	2.247	1.536	1.665	1.891	1.891	ns
DIFF_SSTL12_F	0.906	0.977	0.906	0.977	1.643	1.792	2.035	2.175	1.285	1.423	1.640	1.640	ns
DIFF_SSTL12_S	0.906	0.977	0.906	0.977	1.784	1.948	2.176	2.331	1.567	1.706	1.922	1.922	ns
DIFF_SSTL135_F	0.927	0.995	0.927	0.995	1.625	1.765	2.017	2.148	1.341	1.458	1.696	1.696	ns
DIFF_SSTL135_II_F	0.927	0.995	0.927	0.995	1.623	1.770	2.015	2.153	1.325	1.470	1.680	1.689	ns
DIFF_SSTL135_II_S	0.927	0.995	0.927	0.995	1.768	1.916	2.160	2.299	1.722	1.911	2.077	2.078	ns
DIFF_SSTL135_S	0.927	0.995	0.927	0.995	1.869	2.025	2.261	2.408	1.814	1.976	2.169	2.169	ns
DIFF_SSTL15_F	0.928	1.020	0.928	1.020	1.628	1.771	2.020	2.154	1.374	1.483	1.729	1.729	ns
DIFF_SSTL15_II_F	0.928	1.020	0.928	1.020	1.622	1.778	2.014	2.161	1.356	1.442	1.711	1.712	ns
DIFF_SSTL15_II_S	0.928	1.020	0.928	1.020	1.821	1.987	2.213	2.370	1.895	2.047	2.250	2.250	ns
DIFF_SSTL15_S	0.928	1.020	0.928	1.020	1.824	1.977	2.216	2.360	1.743	1.907	2.098	2.098	ns
DIFF_SSTL18_II_F	0.961	1.038	0.961	1.038	1.729	1.880	2.121	2.263	1.377	1.492	1.732	1.732	ns
DIFF_SSTL18_II_S	0.961	1.038	0.961	1.038	1.796	1.965	2.188	2.348	1.616	1.800	1.971	1.972	ns
DIFF_SSTL18_I_F	0.961	1.038	0.961	1.038	1.609	1.755	2.001	2.138	1.220	1.313	1.575	1.575	ns
DIFF_SSTL18_I_S	0.961	1.038	0.961	1.038	1.786	1.942	2.178	2.325	1.677	1.836	2.032	2.033	ns
HSTL_I_18_F	0.947	1.021	0.947	1.021	1.574	1.718	1.966	2.101	1.160	1.271	1.515	1.544	ns
HSTL_I_18_S	0.947	1.021	0.947	1.021	1.805	1.950	2.197	2.333	1.748	1.867	2.103	2.104	ns
HSTL_I_F	0.856	0.900	0.856	0.900	1.611	1.762	2.003	2.145	1.313	1.417	1.668	1.668	ns
HSTL_I_S	0.856	0.900	0.856	0.900	1.798	1.913	2.190	2.296	1.630	1.780	1.985	1.986	ns
HSUL_12_F	0.780	0.867	0.780	0.867	1.573	1.703	1.965	2.086	1.222	1.335	1.577	1.578	ns
HSUL_12_S	0.780	0.867	0.780	0.867	1.711	1.864	2.103	2.247	1.536	1.665	1.891	1.891	ns
LVCMOS12_F_12	0.918	0.976	0.918	0.976	1.689	1.856	2.081	2.239	1.202	1.317	1.557	1.557	ns
LVCMOS12_F_4	0.918	0.976	0.918	0.976	1.742	1.922	2.134	2.305	1.353	1.478	1.708	1.708	ns
LVCMOS12_F_8	0.918	0.976	0.918	0.976	1.714	1.879	2.106	2.262	1.292	1.432	1.647	1.647	ns
LVCMOS12_S_12	0.918	0.976	0.918	0.976	2.073	2.247	2.465	2.630	1.581	1.717	1.936	1.937	ns
LVCMOS12_S_4	0.918	0.976	0.918	0.976	1.979	2.182	2.371	2.565	1.633	1.772	1.988	1.989	ns
LVCMOS12_S_8	0.918	0.976	0.918	0.976	2.205	2.406	2.597	2.789	1.767	1.928	2.122	2.123	ns
LVCMOS15_F_12	0.905	0.958	0.905	0.958	1.713	1.892	2.105	2.275	1.275	1.428	1.630	1.630	ns
LVCMOS15_F_16	0.905	0.958	0.905	0.958	1.722	1.881	2.114	2.264	1.260	1.407	1.615	1.615	ns
LVCMOS15_F_4	0.905	0.958	0.905	0.958	1.825	1.959	2.217	2.342	1.453	1.557	1.808	1.809	ns
LVCMOS15_F_8	0.905	0.958	0.905	0.958	1.778	1.930	2.170	2.313	1.378	1.458	1.733	1.733	ns
LVCMOS15_S_12	0.905	0.958	0.905	0.958	1.991	2.139	2.383	2.522	1.516	1.648	1.871	1.871	ns
LVCMOS15_S_16	0.905	0.958	0.905	0.958	2.172	2.389	2.564	2.772	1.707	1.888	2.062	2.062	ns
LVCMOS15_S_4	0.905	0.958	0.905	0.958	2.313	2.483	2.705	2.866	1.952	2.123	2.307	2.307	ns
LVCMOS15_S_8	0.905	0.958	0.905	0.958	2.170	2.400	2.562	2.783	1.817	1.984	2.172	2.173	ns
LVCMOS18_F_12	0.915	0.958	0.915	0.958	1.805	1.962	2.197	2.345	1.383	1.471	1.738	1.738	ns

Table 75: **IOB High Density (HD) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
LVCMOS18_F_16	0.915	0.958	0.915	0.958	1.785	1.917	2.177	2.300	1.338	1.446	1.693	1.693	ns
LVCMOS18_F_4	0.915	0.958	0.915	0.958	1.868	2.013	2.260	2.396	1.472	1.599	1.827	1.832	ns
LVCMOS18_F_8	0.915	0.958	0.915	0.958	1.797	1.979	2.189	2.362	1.384	1.487	1.739	1.739	ns
LVCMOS18_S_12	0.915	0.958	0.915	0.958	2.201	2.408	2.593	2.791	1.762	1.894	2.117	2.118	ns
LVCMOS18_S_16	0.915	0.958	0.915	0.958	2.173	2.362	2.565	2.745	1.702	1.834	2.057	2.057	ns
LVCMOS18_S_4	0.915	0.958	0.915	0.958	2.346	2.567	2.738	2.950	1.951	2.092	2.306	2.306	ns
LVCMOS18_S_8	0.915	0.958	0.915	0.958	2.292	2.511	2.684	2.894	1.848	2.008	2.203	2.204	ns
LVCMOS25_F_12	0.988	1.042	0.988	1.042	2.153	2.453	2.545	2.836	1.692	1.856	2.047	2.047	ns
LVCMOS25_F_16	0.988	1.042	0.988	1.042	2.105	2.406	2.497	2.789	1.623	1.786	1.978	1.979	ns
LVCMOS25_F_4	0.988	1.042	0.988	1.042	2.344	2.554	2.736	2.937	1.842	2.039	2.197	2.197	ns
LVCMOS25_F_8	0.988	1.042	0.988	1.042	2.184	2.516	2.576	2.899	1.726	1.910	2.081	2.081	ns
LVCMOS25_S_12	0.988	1.042	0.988	1.042	2.558	2.840	2.950	3.223	1.971	2.194	2.326	2.327	ns
LVCMOS25_S_16	0.988	1.042	0.988	1.042	2.449	2.740	2.841	3.123	1.852	2.063	2.207	2.207	ns
LVCMOS25_S_4	0.988	1.042	0.988	1.042	2.770	3.066	3.162	3.449	2.224	2.458	2.579	2.579	ns
LVCMOS25_S_8	0.988	1.042	0.988	1.042	2.663	2.963	3.055	3.346	2.091	2.373	2.446	2.446	ns
LVCMOS33_F_12	1.154	1.213	1.154	1.213	2.415	2.651	2.807	3.034	1.754	1.915	2.109	2.109	ns
LVCMOS33_F_16	1.154	1.213	1.154	1.213	2.383	2.603	2.775	2.986	1.734	1.869	2.089	2.089	ns
LVCMOS33_F_4	1.154	1.213	1.154	1.213	2.541	2.765	2.933	3.148	1.932	2.135	2.287	2.287	ns
LVCMOS33_F_8	1.154	1.213	1.154	1.213	2.603	2.822	2.995	3.205	1.937	2.130	2.292	2.294	ns
LVCMOS33_S_12	1.154	1.213	1.154	1.213	2.705	3.047	3.097	3.430	2.049	2.318	2.404	2.404	ns
LVCMOS33_S_16	1.154	1.213	1.154	1.213	2.714	3.024	3.106	3.407	2.028	2.232	2.383	2.383	ns
LVCMOS33_S_4	1.154	1.213	1.154	1.213	2.999	3.340	3.391	3.723	2.320	2.610	2.675	2.675	ns
LVCMOS33_S_8	1.154	1.213	1.154	1.213	2.929	3.260	3.321	3.643	2.260	2.532	2.615	2.616	ns
LVDS_25	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	1.164	1.223	1.164	1.223	2.415	2.651	2.807	3.034	1.754	1.915	2.109	2.109	ns
LVTTL_F_16	1.164	1.223	1.164	1.223	2.464	2.732	2.856	3.115	1.750	1.986	2.105	2.117	ns
LVTTL_F_4	1.164	1.223	1.164	1.223	2.541	2.765	2.933	3.148	1.932	2.135	2.287	2.287	ns
LVTTL_F_8	1.164	1.223	1.164	1.223	2.582	2.787	2.974	3.170	1.910	2.063	2.265	2.265	ns
LVTTL_S_12	1.164	1.223	1.164	1.223	2.731	3.075	3.123	3.458	2.072	2.343	2.427	2.427	ns
LVTTL_S_16	1.164	1.223	1.164	1.223	2.714	3.024	3.106	3.407	2.028	2.232	2.383	2.383	ns
LVTTL_S_4	1.164	1.223	1.164	1.223	2.999	3.340	3.391	3.723	2.320	2.610	2.675	2.675	ns
LVTTL_S_8	1.164	1.223	1.164	1.223	2.929	3.260	3.321	3.643	2.260	2.532	2.615	2.616	ns
SLVS_400_25	1.020	1.136	1.020	1.136	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.780	0.867	0.780	0.867	1.643	1.792	2.035	2.175	1.285	1.423	1.640	1.640	ns
SSTL12_S	0.780	0.867	0.780	0.867	1.784	1.948	2.176	2.331	1.567	1.706	1.922	1.922	ns
SSTL135_F	0.798	0.881	0.798	0.881	1.625	1.765	2.017	2.148	1.341	1.458	1.696	1.696	ns
SSTL135_II_F	0.798	0.881	0.798	0.881	1.623	1.770	2.015	2.153	1.325	1.470	1.680	1.689	ns
SSTL135_II_S	0.798	0.881	0.798	0.881	1.768	1.916	2.160	2.299	1.722	1.911	2.077	2.078	ns

Table 75: **IOB High Density (HD) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
SSTL135_S	0.798	0.881	0.798	0.881	1.869	2.025	2.261	2.408	1.814	1.976	2.169	2.169	ns
SSTL15_F	0.838	0.880	0.838	0.880	1.612	1.754	2.004	2.137	1.357	1.464	1.712	1.713	ns
SSTL15_II_F	0.838	0.880	0.838	0.880	1.622	1.778	2.014	2.161	1.356	1.442	1.711	1.712	ns
SSTL15_II_S	0.838	0.880	0.838	0.880	1.821	1.987	2.213	2.370	1.895	2.047	2.250	2.250	ns
SSTL15_S	0.838	0.880	0.838	0.880	1.824	1.977	2.216	2.360	1.743	1.907	2.098	2.098	ns
SSTL18_II_F	0.947	1.021	0.947	1.021	1.729	1.880	2.121	2.263	1.377	1.492	1.732	1.732	ns
SSTL18_II_S	0.947	1.021	0.947	1.021	1.796	1.965	2.188	2.348	1.616	1.800	1.971	1.972	ns
SSTL18_I_F	0.947	1.021	0.947	1.021	1.609	1.755	2.001	2.138	1.220	1.313	1.575	1.575	ns
SSTL18_I_S	0.947	1.021	0.947	1.021	1.786	1.942	2.178	2.325	1.677	1.836	2.032	2.033	ns
SUB_LVDS	1.002	1.036	1.002	1.036	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

IOB High Performance (HP) Switching Characteristics

Table 76: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
DIFF_HSTL_I_12_F	0.394	0.402	0.394	0.402	0.423	0.443	0.423	0.443	0.553	0.582	0.553	0.582	ns
DIFF_HSTL_I_12_M	0.394	0.402	0.394	0.402	0.552	0.583	0.552	0.583	0.641	0.679	0.641	0.679	ns
DIFF_HSTL_I_12_S	0.394	0.402	0.394	0.402	0.752	0.800	0.752	0.800	0.813	0.868	0.813	0.868	ns
DIFF_HSTL_I_18_F	0.319	0.339	0.319	0.339	0.456	0.474	0.456	0.474	0.576	0.606	0.576	0.606	ns
DIFF_HSTL_I_18_M	0.319	0.339	0.319	0.339	0.570	0.603	0.570	0.603	0.653	0.692	0.653	0.692	ns
DIFF_HSTL_I_18_S	0.319	0.339	0.319	0.339	0.782	0.834	0.782	0.834	0.816	0.871	0.816	0.871	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.402	0.394	0.402	0.406	0.429	0.406	0.429	0.534	0.564	0.534	0.564	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.402	0.394	0.402	0.557	0.587	0.557	0.587	0.653	0.694	0.653	0.694	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.402	0.394	0.402	0.755	0.806	0.755	0.806	0.842	0.907	0.842	0.907	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.339	0.323	0.339	0.445	0.461	0.445	0.461	0.566	0.595	0.566	0.595	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.339	0.323	0.339	0.555	0.586	0.555	0.586	0.643	0.684	0.643	0.684	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.339	0.323	0.339	0.762	0.818	0.762	0.818	0.836	0.900	0.836	0.900	ns
DIFF_HSTL_I_DCI_F	0.397	0.417	0.397	0.417	0.431	0.445	0.431	0.445	0.555	0.575	0.555	0.575	ns
DIFF_HSTL_I_DCI_M	0.397	0.417	0.397	0.417	0.553	0.583	0.553	0.583	0.644	0.684	0.644	0.684	ns
DIFF_HSTL_I_DCI_S	0.397	0.417	0.397	0.417	0.767	0.823	0.767	0.823	0.848	0.912	0.848	0.912	ns
DIFF_HSTL_I_F	0.404	0.417	0.404	0.417	0.423	0.443	0.423	0.443	0.549	0.581	0.549	0.581	ns
DIFF_HSTL_I_M	0.404	0.417	0.404	0.417	0.555	0.586	0.555	0.586	0.640	0.677	0.640	0.677	ns
DIFF_HSTL_I_S	0.404	0.417	0.404	0.417	0.767	0.818	0.767	0.818	0.811	0.866	0.811	0.866	ns
DIFF_HSUL_12_DCI_F	0.381	0.400	0.381	0.400	0.425	0.443	0.425	0.443	0.558	0.586	0.558	0.586	ns
DIFF_HSUL_12_DCI_M	0.381	0.400	0.381	0.400	0.557	0.587	0.557	0.587	0.653	0.694	0.653	0.694	ns
DIFF_HSUL_12_DCI_S	0.381	0.400	0.381	0.400	0.737	0.787	0.737	0.787	0.822	0.885	0.822	0.885	ns

Table 76: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
DIFF_HSUL_12_F	0.394	0.402	0.394	0.402	0.412	0.430	0.412	0.430	0.538	0.566	0.538	0.566	ns
DIFF_HSUL_12_M	0.394	0.402	0.394	0.402	0.552	0.583	0.552	0.583	0.641	0.679	0.641	0.679	ns
DIFF_HSUL_12_S	0.394	0.402	0.394	0.402	0.752	0.800	0.752	0.800	0.813	0.868	0.813	0.868	ns
DIFF_POD10_DCI_F	0.411	0.430	0.411	0.430	0.425	0.444	0.425	0.444	0.555	0.584	0.555	0.584	ns
DIFF_POD10_DCI_M	0.411	0.430	0.411	0.430	0.542	0.571	0.542	0.571	0.640	0.681	0.640	0.681	ns
DIFF_POD10_DCI_S	0.411	0.430	0.411	0.430	0.754	0.815	0.754	0.815	0.850	0.917	0.850	0.917	ns
DIFF_POD10_F	0.411	0.433	0.411	0.433	0.438	0.459	0.438	0.459	0.569	0.601	0.569	0.601	ns
DIFF_POD10_M	0.411	0.433	0.411	0.433	0.538	0.568	0.538	0.568	0.630	0.667	0.630	0.667	ns
DIFF_POD10_S	0.411	0.433	0.411	0.433	0.766	0.821	0.766	0.821	0.836	0.894	0.836	0.894	ns
DIFF_POD12_DCI_F	0.407	0.432	0.407	0.432	0.425	0.443	0.425	0.443	0.558	0.586	0.558	0.586	ns
DIFF_POD12_DCI_M	0.407	0.432	0.407	0.432	0.543	0.572	0.543	0.572	0.638	0.678	0.638	0.678	ns
DIFF_POD12_DCI_S	0.407	0.432	0.407	0.432	0.772	0.822	0.772	0.822	0.862	0.929	0.862	0.929	ns
DIFF_POD12_F	0.409	0.430	0.409	0.430	0.455	0.476	0.455	0.476	0.595	0.626	0.595	0.626	ns
DIFF_POD12_M	0.409	0.430	0.409	0.430	0.551	0.582	0.551	0.582	0.641	0.679	0.641	0.679	ns
DIFF_POD12_S	0.409	0.430	0.409	0.430	0.767	0.817	0.767	0.817	0.832	0.889	0.832	0.889	ns
DIFF_SSTL12_DCI_F	0.381	0.400	0.381	0.400	0.425	0.443	0.425	0.443	0.558	0.586	0.558	0.586	ns
DIFF_SSTL12_DCI_M	0.381	0.400	0.381	0.400	0.557	0.587	0.557	0.587	0.654	0.694	0.654	0.694	ns
DIFF_SSTL12_DCI_S	0.381	0.400	0.381	0.400	0.754	0.803	0.754	0.803	0.842	0.908	0.842	0.908	ns
DIFF_SSTL12_F	0.394	0.402	0.394	0.402	0.412	0.430	0.412	0.430	0.538	0.566	0.538	0.566	ns
DIFF_SSTL12_M	0.394	0.402	0.394	0.402	0.553	0.584	0.553	0.584	0.641	0.676	0.641	0.676	ns
DIFF_SSTL12_S	0.394	0.402	0.394	0.402	0.758	0.808	0.758	0.808	0.823	0.879	0.823	0.879	ns
DIFF_SSTL135_DCI_F	0.371	0.402	0.371	0.402	0.411	0.428	0.411	0.428	0.537	0.565	0.537	0.565	ns
DIFF_SSTL135_DCI_M	0.371	0.402	0.371	0.402	0.551	0.582	0.551	0.582	0.645	0.685	0.645	0.685	ns
DIFF_SSTL135_DCI_S	0.371	0.402	0.371	0.402	0.746	0.799	0.746	0.799	0.829	0.893	0.829	0.893	ns
DIFF_SSTL135_F	0.375	0.402	0.375	0.402	0.408	0.428	0.408	0.428	0.528	0.561	0.528	0.561	ns
DIFF_SSTL135_M	0.375	0.402	0.375	0.402	0.555	0.585	0.555	0.585	0.641	0.679	0.641	0.679	ns
DIFF_SSTL135_S	0.375	0.402	0.375	0.402	0.772	0.823	0.772	0.823	0.827	0.878	0.827	0.878	ns
DIFF_SSTL15_DCI_F	0.397	0.417	0.397	0.417	0.412	0.429	0.412	0.429	0.531	0.563	0.531	0.563	ns
DIFF_SSTL15_DCI_M	0.397	0.417	0.397	0.417	0.553	0.583	0.553	0.583	0.645	0.685	0.645	0.685	ns
DIFF_SSTL15_DCI_S	0.397	0.417	0.397	0.417	0.768	0.822	0.768	0.822	0.847	0.912	0.847	0.912	ns
DIFF_SSTL15_F	0.404	0.417	0.404	0.417	0.424	0.445	0.424	0.445	0.551	0.577	0.551	0.577	ns
DIFF_SSTL15_M	0.404	0.417	0.404	0.417	0.554	0.585	0.554	0.585	0.639	0.677	0.639	0.677	ns
DIFF_SSTL15_S	0.404	0.417	0.404	0.417	0.767	0.817	0.767	0.817	0.813	0.867	0.813	0.867	ns
DIFF_SSTL18_I_DCI_F	0.320	0.336	0.320	0.336	0.445	0.461	0.445	0.461	0.566	0.595	0.566	0.595	ns
DIFF_SSTL18_I_DCI_M	0.320	0.336	0.320	0.336	0.554	0.585	0.554	0.585	0.644	0.683	0.644	0.683	ns
DIFF_SSTL18_I_DCI_S	0.320	0.336	0.320	0.336	0.762	0.818	0.762	0.818	0.837	0.899	0.837	0.899	ns
DIFF_SSTL18_I_F	0.316	0.336	0.316	0.336	0.454	0.476	0.454	0.476	0.578	0.608	0.578	0.608	ns
DIFF_SSTL18_I_M	0.316	0.336	0.316	0.336	0.571	0.603	0.571	0.603	0.652	0.692	0.652	0.692	ns
DIFF_SSTL18_I_S	0.316	0.336	0.316	0.336	0.782	0.835	0.782	0.835	0.816	0.870	0.816	0.870	ns

Table 76: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
HSLVDCI_15_F	0.393	0.415	0.393	0.415	0.425	0.443	0.425	0.443	0.548	0.579	0.548	0.579	ns
HSLVDCI_15_M	0.393	0.415	0.393	0.415	0.552	0.581	0.552	0.581	0.644	0.684	0.644	0.684	ns
HSLVDCI_15_S	0.393	0.415	0.393	0.415	0.748	0.802	0.748	0.802	0.827	0.890	0.827	0.890	ns
HSLVDCI_18_F	0.424	0.447	0.424	0.447	0.445	0.461	0.445	0.461	0.566	0.595	0.566	0.595	ns
HSLVDCI_18_M	0.424	0.447	0.424	0.447	0.567	0.598	0.567	0.598	0.658	0.699	0.658	0.699	ns
HSLVDCI_18_S	0.424	0.447	0.424	0.447	0.761	0.817	0.761	0.817	0.836	0.900	0.836	0.900	ns
HSTL_I_12_F	0.378	0.399	0.378	0.399	0.423	0.443	0.423	0.443	0.553	0.582	0.553	0.582	ns
HSTL_I_12_M	0.378	0.399	0.378	0.399	0.551	0.582	0.551	0.582	0.642	0.679	0.642	0.679	ns
HSTL_I_12_S	0.378	0.399	0.378	0.399	0.750	0.799	0.750	0.799	0.813	0.868	0.813	0.868	ns
HSTL_I_18_F	0.322	0.339	0.322	0.339	0.456	0.474	0.456	0.474	0.576	0.606	0.576	0.606	ns
HSTL_I_18_M	0.322	0.339	0.322	0.339	0.569	0.602	0.569	0.602	0.653	0.692	0.653	0.692	ns
HSTL_I_18_S	0.322	0.339	0.322	0.339	0.781	0.833	0.781	0.833	0.816	0.871	0.816	0.871	ns
HSTL_I_DCI_12_F	0.378	0.399	0.378	0.399	0.406	0.429	0.406	0.429	0.534	0.564	0.534	0.564	ns
HSTL_I_DCI_12_M	0.378	0.399	0.378	0.399	0.556	0.586	0.556	0.586	0.654	0.694	0.654	0.694	ns
HSTL_I_DCI_12_S	0.378	0.399	0.378	0.399	0.754	0.803	0.754	0.803	0.842	0.907	0.842	0.907	ns
HSTL_I_DCI_18_F	0.321	0.339	0.321	0.339	0.445	0.461	0.445	0.461	0.566	0.595	0.566	0.595	ns
HSTL_I_DCI_18_M	0.321	0.339	0.321	0.339	0.554	0.585	0.554	0.585	0.643	0.684	0.643	0.684	ns
HSTL_I_DCI_18_S	0.321	0.339	0.321	0.339	0.761	0.817	0.761	0.817	0.836	0.900	0.836	0.900	ns
HSTL_I_DCI_F	0.393	0.415	0.393	0.415	0.431	0.445	0.431	0.445	0.555	0.575	0.555	0.575	ns
HSTL_I_DCI_M	0.393	0.415	0.393	0.415	0.552	0.581	0.552	0.581	0.644	0.684	0.644	0.684	ns
HSTL_I_DCI_S	0.393	0.415	0.393	0.415	0.766	0.821	0.766	0.821	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.399	0.378	0.399	0.423	0.443	0.423	0.443	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.399	0.378	0.399	0.554	0.585	0.554	0.585	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.399	0.378	0.399	0.766	0.816	0.766	0.816	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.399	0.378	0.399	0.425	0.443	0.425	0.443	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.399	0.378	0.399	0.556	0.586	0.556	0.586	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.399	0.378	0.399	0.736	0.784	0.736	0.784	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.399	0.378	0.399	0.412	0.430	0.412	0.430	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.399	0.378	0.399	0.551	0.582	0.551	0.582	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.399	0.378	0.399	0.750	0.799	0.750	0.799	0.813	0.868	0.813	0.868	ns
LVCMOS12_F_2	0.512	0.555	0.512	0.555	0.672	0.692	0.672	0.692	0.898	0.922	0.898	0.922	ns
LVCMOS12_F_4	0.512	0.555	0.512	0.555	0.504	0.521	0.504	0.521	0.664	0.693	0.664	0.693	ns
LVCMOS12_F_6	0.512	0.555	0.512	0.555	0.485	0.507	0.485	0.507	0.634	0.669	0.634	0.669	ns
LVCMOS12_F_8	0.512	0.555	0.512	0.555	0.465	0.489	0.465	0.489	0.611	0.666	0.611	0.666	ns
LVCMOS12_M_2	0.512	0.555	0.512	0.555	0.708	0.727	0.708	0.727	0.916	0.945	0.916	0.945	ns
LVCMOS12_M_4	0.512	0.555	0.512	0.555	0.550	0.573	0.550	0.573	0.664	0.690	0.664	0.690	ns
LVCMOS12_M_6	0.512	0.555	0.512	0.555	0.527	0.554	0.527	0.554	0.622	0.652	0.622	0.652	ns
LVCMOS12_M_8	0.512	0.555	0.512	0.555	0.540	0.571	0.540	0.571	0.614	0.649	0.614	0.649	ns
LVCMOS12_S_2	0.512	0.555	0.512	0.555	0.767	0.803	0.767	0.803	0.990	1.024	0.990	1.024	ns

Table 76: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
LVCMOS12_S_4	0.512	0.555	0.512	0.555	0.666	0.704	0.666	0.704	0.803	0.848	0.803	0.848	ns
LVCMOS12_S_6	0.512	0.555	0.512	0.555	0.657	0.695	0.657	0.695	0.732	0.774	0.732	0.774	ns
LVCMOS12_S_8	0.512	0.555	0.512	0.555	0.708	0.761	0.708	0.761	0.745	0.790	0.745	0.790	ns
LVCMOS15_F_12	0.414	0.445	0.414	0.445	0.500	0.522	0.500	0.522	0.647	0.682	0.647	0.682	ns
LVCMOS15_F_2	0.414	0.445	0.414	0.445	0.702	0.722	0.702	0.722	0.919	0.940	0.919	0.940	ns
LVCMOS15_F_4	0.414	0.445	0.414	0.445	0.579	0.601	0.579	0.601	0.755	0.781	0.755	0.781	ns
LVCMOS15_F_6	0.414	0.445	0.414	0.445	0.547	0.569	0.547	0.569	0.711	0.742	0.711	0.742	ns
LVCMOS15_F_8	0.414	0.445	0.414	0.445	0.518	0.538	0.518	0.538	0.686	0.703	0.686	0.703	ns
LVCMOS15_M_12	0.414	0.445	0.414	0.445	0.607	0.644	0.607	0.644	0.637	0.676	0.637	0.676	ns
LVCMOS15_M_2	0.414	0.445	0.414	0.445	0.741	0.770	0.741	0.770	0.938	0.962	0.938	0.962	ns
LVCMOS15_M_4	0.414	0.445	0.414	0.445	0.625	0.651	0.625	0.651	0.754	0.786	0.754	0.786	ns
LVCMOS15_M_6	0.414	0.445	0.414	0.445	0.576	0.604	0.576	0.604	0.674	0.710	0.674	0.710	ns
LVCMOS15_M_8	0.414	0.445	0.414	0.445	0.568	0.601	0.568	0.601	0.639	0.681	0.639	0.681	ns
LVCMOS15_S_12	0.414	0.445	0.414	0.445	0.788	0.855	0.788	0.855	0.695	0.733	0.695	0.733	ns
LVCMOS15_S_2	0.414	0.445	0.414	0.445	0.829	0.864	0.829	0.864	1.039	1.079	1.039	1.079	ns
LVCMOS15_S_4	0.414	0.445	0.414	0.445	0.687	0.725	0.687	0.725	0.813	0.851	0.813	0.851	ns
LVCMOS15_S_6	0.414	0.445	0.414	0.445	0.671	0.710	0.671	0.710	0.726	0.763	0.726	0.763	ns
LVCMOS15_S_8	0.414	0.445	0.414	0.445	0.704	0.755	0.704	0.755	0.721	0.758	0.721	0.758	ns
LVCMOS18_F_12	0.418	0.445	0.418	0.445	0.573	0.601	0.573	0.601	0.731	0.769	0.731	0.769	ns
LVCMOS18_F_2	0.418	0.445	0.418	0.445	0.739	0.760	0.739	0.760	0.945	0.971	0.945	0.971	ns
LVCMOS18_F_4	0.418	0.445	0.418	0.445	0.609	0.630	0.609	0.630	0.778	0.802	0.778	0.802	ns
LVCMOS18_F_6	0.418	0.445	0.418	0.445	0.603	0.633	0.603	0.633	0.781	0.808	0.781	0.808	ns
LVCMOS18_F_8	0.418	0.445	0.418	0.445	0.573	0.600	0.573	0.600	0.733	0.767	0.733	0.767	ns
LVCMOS18_M_12	0.418	0.445	0.418	0.445	0.640	0.678	0.640	0.678	0.670	0.709	0.670	0.709	ns
LVCMOS18_M_2	0.418	0.445	0.418	0.445	0.798	0.822	0.798	0.822	0.991	1.016	0.991	1.016	ns
LVCMOS18_M_4	0.418	0.445	0.418	0.445	0.664	0.693	0.664	0.693	0.798	0.836	0.798	0.836	ns
LVCMOS18_M_6	0.418	0.445	0.418	0.445	0.629	0.663	0.629	0.663	0.735	0.775	0.735	0.775	ns
LVCMOS18_M_8	0.418	0.445	0.418	0.445	0.626	0.661	0.626	0.661	0.705	0.746	0.705	0.746	ns
LVCMOS18_S_12	0.418	0.445	0.418	0.445	0.795	0.861	0.795	0.861	0.683	0.721	0.683	0.721	ns
LVCMOS18_S_2	0.418	0.445	0.418	0.445	0.862	0.897	0.862	0.897	1.076	1.098	1.076	1.098	ns
LVCMOS18_S_4	0.418	0.445	0.418	0.445	0.716	0.758	0.716	0.758	0.829	0.872	0.829	0.872	ns
LVCMOS18_S_6	0.418	0.445	0.418	0.445	0.682	0.724	0.682	0.724	0.724	0.762	0.724	0.762	ns
LVCMOS18_S_8	0.418	0.445	0.418	0.445	0.707	0.760	0.707	0.760	0.709	0.745	0.709	0.745	ns
LVDCI_15_F	0.425	0.462	0.425	0.462	0.426	0.443	0.426	0.443	0.548	0.581	0.548	0.581	ns
LVDCI_15_M	0.425	0.462	0.425	0.462	0.553	0.582	0.553	0.582	0.645	0.685	0.645	0.685	ns
LVDCI_15_S	0.425	0.462	0.425	0.462	0.749	0.803	0.749	0.803	0.821	0.890	0.821	0.890	ns
LVDCI_18_F	0.414	0.447	0.414	0.447	0.441	0.459	0.441	0.459	0.560	0.589	0.560	0.589	ns
LVDCI_18_M	0.414	0.447	0.414	0.447	0.554	0.585	0.554	0.585	0.644	0.683	0.644	0.683	ns
LVDCI_18_S	0.414	0.447	0.414	0.447	0.760	0.818	0.760	0.818	0.837	0.899	0.837	0.899	ns

Table 76: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
LVDS	0.539	0.620	0.539	0.620	0.626	0.662	0.626	0.662	960.447				ns
MIPI_DPHY_DCI_HS	0.386	0.415	0.386	0.415	0.502	0.522	0.502	0.522	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.792	8.438	8.792	0.914	0.937	0.914	0.937	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.408	0.430	0.408	0.430	0.425	0.444	0.425	0.444	0.555	0.584	0.555	0.584	ns
POD10_DCI_M	0.408	0.430	0.408	0.430	0.542	0.571	0.542	0.571	0.640	0.681	0.640	0.681	ns
POD10_DCI_S	0.408	0.430	0.408	0.430	0.754	0.815	0.754	0.815	0.850	0.917	0.850	0.917	ns
POD10_F	0.407	0.430	0.407	0.430	0.438	0.459	0.438	0.459	0.569	0.601	0.569	0.601	ns
POD10_M	0.407	0.430	0.407	0.430	0.538	0.568	0.538	0.568	0.630	0.667	0.630	0.667	ns
POD10_S	0.407	0.430	0.407	0.430	0.766	0.821	0.766	0.821	0.836	0.894	0.836	0.894	ns
POD12_DCI_F	0.409	0.431	0.409	0.431	0.425	0.443	0.425	0.443	0.558	0.586	0.558	0.586	ns
POD12_DCI_M	0.409	0.431	0.409	0.431	0.543	0.572	0.543	0.572	0.638	0.678	0.638	0.678	ns
POD12_DCI_S	0.409	0.431	0.409	0.431	0.772	0.822	0.772	0.822	0.862	0.929	0.862	0.929	ns
POD12_F	0.409	0.431	0.409	0.431	0.455	0.476	0.455	0.476	0.595	0.626	0.595	0.626	ns
POD12_M	0.409	0.431	0.409	0.431	0.551	0.582	0.551	0.582	0.641	0.679	0.641	0.679	ns
POD12_S	0.409	0.431	0.409	0.431	0.767	0.817	0.767	0.817	0.832	0.889	0.832	0.889	ns
SLVS_400_18	0.539	0.620	0.539	0.620	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.399	0.381	0.399	0.425	0.443	0.425	0.443	0.558	0.586	0.558	0.586	ns
SSTL12_DCI_M	0.381	0.399	0.381	0.399	0.557	0.587	0.557	0.587	0.654	0.694	0.654	0.694	ns
SSTL12_DCI_S	0.381	0.399	0.381	0.399	0.754	0.803	0.754	0.803	0.842	0.908	0.842	0.908	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.412	0.430	0.412	0.430	0.538	0.566	0.538	0.566	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.553	0.584	0.553	0.584	0.641	0.676	0.641	0.676	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.758	0.808	0.758	0.808	0.823	0.879	0.823	0.879	ns
SSTL135_DCI_F	0.366	0.399	0.366	0.399	0.411	0.428	0.411	0.428	0.537	0.565	0.537	0.565	ns
SSTL135_DCI_M	0.366	0.399	0.366	0.399	0.551	0.582	0.551	0.582	0.645	0.685	0.645	0.685	ns
SSTL135_DCI_S	0.366	0.399	0.366	0.399	0.746	0.799	0.746	0.799	0.829	0.893	0.829	0.893	ns
SSTL135_F	0.378	0.399	0.378	0.399	0.408	0.428	0.408	0.428	0.528	0.561	0.528	0.561	ns
SSTL135_M	0.378	0.399	0.378	0.399	0.555	0.585	0.555	0.585	0.641	0.679	0.641	0.679	ns
SSTL135_S	0.378	0.399	0.378	0.399	0.772	0.823	0.772	0.823	0.827	0.878	0.827	0.878	ns
SSTL15_DCI_F	0.402	0.417	0.402	0.417	0.412	0.429	0.412	0.429	0.531	0.563	0.531	0.563	ns
SSTL15_DCI_M	0.402	0.417	0.402	0.417	0.553	0.583	0.553	0.583	0.645	0.685	0.645	0.685	ns
SSTL15_DCI_S	0.402	0.417	0.402	0.417	0.768	0.822	0.768	0.822	0.847	0.912	0.847	0.912	ns
SSTL15_F	0.371	0.400	0.371	0.400	0.408	0.428	0.408	0.428	0.530	0.556	0.530	0.556	ns
SSTL15_M	0.371	0.400	0.371	0.400	0.554	0.585	0.554	0.585	0.639	0.677	0.639	0.677	ns
SSTL15_S	0.371	0.400	0.371	0.400	0.767	0.817	0.767	0.817	0.813	0.867	0.813	0.867	ns
SSTL18_I_DCI_F	0.329	0.336	0.329	0.336	0.445	0.461	0.445	0.461	0.566	0.595	0.566	0.595	ns
SSTL18_I_DCI_M	0.329	0.336	0.329	0.336	0.554	0.585	0.554	0.585	0.644	0.683	0.644	0.683	ns
SSTL18_I_DCI_S	0.329	0.336	0.329	0.336	0.762	0.818	0.762	0.818	0.837	0.899	0.837	0.899	ns
SSTL18_I_F	0.316	0.337	0.316	0.337	0.454	0.476	0.454	0.476	0.578	0.608	0.578	0.608	ns
SSTL18_I_M	0.316	0.337	0.316	0.337	0.571	0.603	0.571	0.603	0.652	0.692	0.652	0.692	ns

Table 76: **IOB High Performance (HP) Switching Characteristics** *(cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.85V		0.72V		0.85V		0.72V		0.85V		0.72V		
	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	-2	-1	
SSTL18_I_S	0.316	0.337	0.316	0.337	0.782	0.835	0.782	0.835	0.816	0.870	0.816	0.870	ns
SUB_LVDS	0.539	0.620	0.539	0.620	0.660	0.692	0.660	0.692	969.863				ns

IOB 3-state Output Switching Characteristics

Table 77 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$.

- $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).
- $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output.
- In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used.
- In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the INTERMDISABLE pin is used.

Table 77: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
$T_{OUTBUF\_DELAY\_TE\_PAD}$	T input to pad high-impedance for HD I/O banks	6.318	6.369	6.699	6.752	ns
	T input to pad high-impedance for HP I/O banks	5.330	5.341	5.330	5.341	ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks	2.266	2.430	2.266	2.430	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	0.936	1.037	0.936	1.037	ns

Input Delay Measurement Methodology

The following table shows the test setup parameters used for measuring input delay.

Table 78: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L [1, 2]	V_H [1, 2]	V_{MEAS} [1, 4]	V_{REF} [1, 3, 5]
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–

Table 78: **Input Delay Measurement Methodology** *(cont'd)*

Description	I/O Standard Attribute	V_L [1, 2]	V_H [1, 2]	V_{MEAS} [1, 4]	V_{REF} [1, 3, 5]
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	V_{REF} – 0.2875	V_{REF} + 0.2875	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
POD10, 1.0V	POD10	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.7
POD12, 1.2V	POD12	V_{REF} – 0.24	V_{REF} + 0.24	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.25	0.6 + 0.25	0[6]	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	0.75 – 0.325	0.75 + 0.325	0[6]	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	0.9 – 0.4	0.9 + 0.4	0[6]	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.25	0.6 + 0.25	0[6]	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.25	0.6 + 0.25	0[6]	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	0.675 – 0.2875	0.675 + 0.2875	0[6]	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	0.75 – 0.325	0.75 + 0.325	0[6]	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.4	0.9 + 0.4	0[6]	–
DIFF_POD10, 1.0V	DIFF_POD10	0.5 – 0.2	0.5 + 0.2	0[6]	–
DIFF_POD12, 1.2V	DIFF_POD12	0.6 – 0.25	0.6 + 0.25	0[6]	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0[6]	–
LVDS_25, 2.5V	LVDS_25	1.25 – 0.125	1.25 + 0.125	0[6]	–
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0[6]	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0[6]	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0[6]	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0[6]	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0[6]	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0[6]	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

Figure 1: **Single-Ended Test Setup**

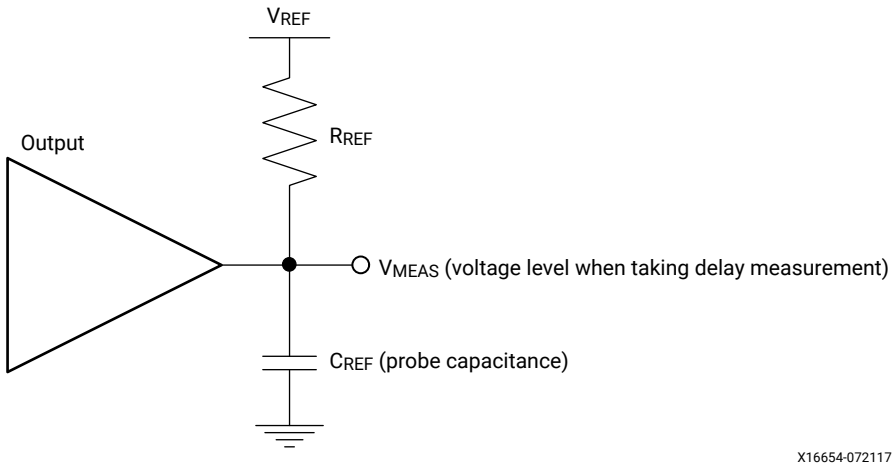
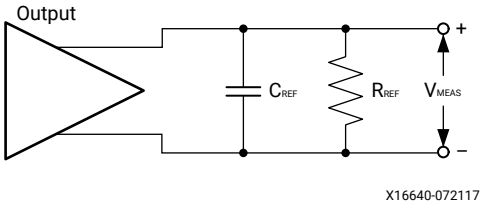


Figure 2: **Differential Test Setup**



Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 79.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 79: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0

Table 79: **Output Delay Measurement Methodology** *(cont'd)*

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V_{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V_{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V_{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0[2]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0[2]	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table 80: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.85V		0.72V			
		-2E/-2I/ -2LE	-1E/-1I/ -1M/-1LI	-2LE	-2LI	-1LI	
Maximum Frequency							
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes)	738	645	585	516	516	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode)	637	575	510	495	460	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	738	645	585	516	516	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE	637	575	510	460	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode	738	645	585	516	516	MHz
T_{PW}[1]	Minimum pulse width	542	543	577	578	578	ps
Block RAM and FIFO Clock-to-Out Delays							
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)	1.02	1.11	1.46	1.46	1.53	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)	0.29	0.30	0.42	0.42	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists the Zynq UltraScale+ RFSoCs that include this memory.

Table 81: **UltraRAM Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.85V		0.72V			
		-2E/-2I/ -2LE	-1E/-1I/ -1M/-1LI	-2LE	-2LI	-1LI	
Maximum Frequency							
F_{MAX}	UltraRAM maximum frequency with OREG_B = True	600	575	500	495	481	MHz
$F_{MAX\_ECC\_NOPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = True	400	386	312	303	303	MHz
$F_{MAX\_NOPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False	500	478	404	389	389	MHz
T_{PW}[1]	Minimum pulse width	700	730	800	832	832	ps
T_{RSTPW}	Asynchronous reset minimum pulse width. One cycle required	1 clock cycle					

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table 82: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
F_{REFCLK}	Reference clock frequency for IDELAYCTRL (component mode)	300 to 800				MHz
	Reference clock frequency when using BITSLICE_CONTROL with REFCLK (in native mode (for RX_BITSLICE only))	300 to 800				MHz
	Reference clock frequency for BITSLICE_CONTROL with PLL_CLK (in native mode)[1]	300 to 2666.67	300 to 2400	300 to 2400	300 to 2133	MHz
T_{MINPER_CLK}	Minimum period for IODELAY clock	3.195	3.195	3.195	3.195	ns
T_{MINPER_RST}	Minimum reset pulse width	52.00				ns
$T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$	IDELAY/ODELAY chain resolution	2.1 to 12				ps

Notes:

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_F_{VCOMIN}/2.

DSP48 Slice Switching Characteristics

Table 83: **DSP48 Slice Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.85V		0.72V			
		-2E/-2I/ -2LE	-1E/-1I/ -1M/-1LI	-2LE	-2LI	-1LI	
Maximum Frequency							
F_{MAX}	With all registers used	775	645	644	600	600	MHz
F_{MAX_PATDET}	With pattern detector	687	571	562	524	524	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	544	456	440	413	413	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	492	410	395	371	371	MHz
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG	565	468	453	423	423	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	410	338	323	304	304	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	379	314	299	280	280	MHz

Clock Buffers and Networks

Table 84: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)						
F_{MAX}	Maximum frequency of a global clock tree (BUFG)	775	667	725	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)						
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV)	775	667	725	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)						
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE)	775	667	725	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)						
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF)	775	667	725	667	MHz
GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)						
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	512	512	512	512	MHz

MMCM Switching Characteristics

Table 85: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
MMCM_F_{INMAX}	Maximum input clock frequency	933	800	933	800	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz	25–75				%
	Input duty cycle range: 50–199 MHz	30–70				%
	Input duty cycle range: 200–399 MHz	35–65				%
	Input duty cycle range: 400–499 MHz	40–60				%
	Input duty cycle range: >500 MHz	45–55				%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	500	450	500	450	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	800	800	800	800	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1600	1600	1600	1600	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical[1]	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical[1]	4.00	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs[2]	0.12	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3				
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision[4]	0.20	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN}	100	100	100	100	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency	775	667	725	667	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency[4, 5]	6.25	6.25	6.25	6.25	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector	500	450	500	450	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector	10	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path	5 ns Max or one clock cycle				
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 86: **PLL Specification**

Symbol	Description[1]	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
PLL_F_{INMAX}	Maximum input clock frequency	933	800	933	800	MHz
PLL_F_{INMIN}	Minimum input clock frequency	70	70	70	70	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Input duty cycle range: 70–399 MHz	35–65				%
	Input duty cycle range: 400–499 MHz	40–60				%
	Input duty cycle range: >500 MHz	45–55				%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	750	750	750	750	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	1500	1500	1500	1500	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs[2]	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 3				
PLL_$T_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision[4]	0.20	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time	100				µs
PLL_F_{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B	775	667	725	667	MHz
	PLL maximum output frequency at CLKOUTPHY	2667	2400	2400	2133	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B[5]	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY	2 x VCO mode: 1500, 1 x VCO mode: 750, 0.5 x VCO mode: 375				MHz
PLL_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	667.5	667.5	667.5	667.5	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	70	70	70	70	MHz
PLL_$F_{BANDWIDTH}$	PLL bandwidth at typical	14	14	14	14	MHz
PLL_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

RF-ADC/RF-DAC to PL Interface Switching Characteristics

The following table outlines the performance of the AXI4 interface.

Table 87: **RF-ADC/RF-DAC to PL Interface Performance**

Symbol	Description	Min	Max	Units
$F_{AXI\_LITE\_CLK}$	AXI4-Lite clock frequency	10	250	MHz
$F_{ADC\_GEARBOX\_FIFO}$	Maximum RF-ADC tile interface clock frequency for ZU25DR, ZU27DR, ZU28DR, ZU29DR, and ZU39DR	–	520	MHz
	Maximum RF-ADC tile interface clock frequency for ZU43DR, ZU46DR, ZU47DR, ZU48DR, and ZU49DR	–	614	MHz
$F_{DAC\_GEARBOX\_FIFO}$	Maximum RF-DAC tile interface clock frequency for ZU25DR, ZU27DR, ZU28DR, ZU29DR, and ZU39DR	–	500	MHz
	Maximum RF-DAC tile interface clock frequency for ZU43DR, ZU46DR, ZU47DR, ZU48DR, and ZU49DR with digital up converter (DUC) enabled	–	614	MHz
	Maximum RF-DAC tile interface clock frequency for ZU43DR, ZU46DR, ZU47DR, ZU48DR, and ZU49DR with DUC bypassed	–	625	MHz

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 88: **Global Clock Input to Output Delay Without MMCM (Near Clock Region)**

Symbol	Description[1]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.85V		0.72V		
			-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM							
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM (near clock region)	XCZU21DR	6.26	6.73	7.80	8.36	ns
		XCZU25DR	6.05	6.50	7.55	8.09	ns
		XCZU27DR	6.26	6.73	7.80	8.36	ns
		XCZU28DR	6.26	6.73	7.80	8.36	ns
		XCZU29DR	6.26	6.73	7.80	8.36	ns
		XCZU39DR	6.26	N/A	7.80	N/A	ns
		XQZU21DR	6.26	6.73	N/A	8.36	ns
		XQZU28DR	6.26	6.73	N/A	8.36	ns
		XQZU29DR	6.26	6.73	N/A	8.36	ns
		XCZU43DR	6.26	6.73	7.80	8.36	ns
		XCZU46DR	6.26	6.73	7.80	8.36	ns
		XCZU47DR	6.26	6.73	7.80	8.36	ns
		XCZU48DR	6.26	6.73	7.80	8.36	ns
		XCZU49DR	6.26	6.73	7.80	8.36	ns
		XQZU48DR	6.26	6.73	7.80	8.36	ns
		XQZU49DR	6.26	6.73	7.80	8.36	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 89: **Global Clock Input to Output Delay Without MMCM (Far Clock Region)**

Symbol	Description[1]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.85V		0.72V		
			-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM							
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM (far clock region)	XCZU21DR	6.89	7.39	8.64	9.27	ns
		XCZU25DR	6.48	6.96	8.11	8.71	ns
		XCZU27DR	6.89	7.39	8.64	9.27	ns
		XCZU28DR	6.89	7.39	8.64	9.27	ns
		XCZU29DR	6.89	7.39	8.64	9.27	ns
		XCZU39DR	6.89	N/A	8.64	N/A	ns
		XQZU21DR	6.89	7.39	N/A	9.27	ns
		XQZU28DR	6.89	7.39	N/A	9.27	ns
		XQZU29DR	6.89	7.39	N/A	9.27	ns
		XCZU43DR	6.89	7.39	8.64	9.27	ns
		XCZU46DR	6.89	7.39	8.64	9.27	ns
		XCZU47DR	6.89	7.39	8.64	9.27	ns
		XCZU48DR	6.89	7.39	8.64	9.27	ns
		XCZU49DR	6.89	7.39	8.64	9.27	ns
		XQZU48DR	6.89	7.39	8.64	9.27	ns
		XQZU49DR	6.89	7.39	8.64	9.27	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 90: **Global Clock Input to Output Delay With MMCM**

Symbol	Description[1, 2]	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.85V		0.72V		
			-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM							
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM	XCZU21DR	2.31	2.53	2.97	3.13	ns
		XCZU25DR	2.28	2.49	2.96	3.12	ns
		XCZU27DR	2.31	2.53	2.97	3.13	ns
		XCZU28DR	2.31	2.53	2.97	3.13	ns
		XCZU29DR	2.31	2.53	2.97	3.13	ns
		XCZU39DR	2.31	N/A	2.97	N/A	ns
		XQZU21DR	2.31	2.53	N/A	3.13	ns
		XQZU28DR	2.31	2.53	N/A	3.13	ns
		XQZU29DR	2.31	2.53	N/A	3.13	ns
		XCZU43DR	2.31	2.53	2.97	3.13	ns
		XCZU46DR	2.31	2.53	2.97	3.13	ns
		XCZU47DR	2.31	2.53	2.97	3.13	ns
		XCZU48DR	2.31	2.53	2.97	3.13	ns
		XCZU49DR	2.31	2.53	2.97	3.13	ns
		XQZU48DR	2.31	2.53	2.97	3.13	ns
		XQZU49DR	2.31	2.53	2.97	3.13	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 91: **Source Synchronous Output Characteristics (Component Mode)**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.85V		0.72V		
	-2	-1	-2	-1	
$T_{OUTPUT\_LOGIC\_DELAY\_VARIATION}$[1]	80				ps

Notes:

1. Delay mismatch across a transmit bus when using component mode output logic (ODDRE1, OSERDESE3) within a bank.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 92: **Global Clock Input Setup and Hold With 3.3V HD I/O Without MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages				Units
				0.85V		0.72V		
				-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1, 2, 3]								
T_{PSFD_ZU21}	Global clock input and input flip-flop (or latch) *without* MMCM	Setup	XCZU21	0.81	0.83	1.68	1.83	ns
T_{PHFD_ZU21}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_ZU25}		Setup	XCZU25	0.57	0.57	1.39	1.52	ns
T_{PHFD_ZU25}		Hold		0.79	0.88	0.39	0.39	ns
T_{PSFD_ZU27}		Setup	XCZU27	0.81	0.83	1.68	1.83	ns
T_{PHFD_ZU27}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_ZU28}		Setup	XCZU28	0.81	0.83	1.68	1.83	ns
T_{PHFD_ZU28}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_ZU29}		Setup	XCZU29	0.81	0.83	1.68	1.83	ns
T_{PHFD_ZU29}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_ZU39}		Setup	XCZU39	0.81	N/A	1.68	N/A	ns
T_{PHFD_ZU39}		Hold		0.64	N/A	0.22	N/A	ns
T_{PSFD_XQZU21}		Setup	XQZU21	0.81	0.83	N/A	1.83	ns
T_{PHFD_XQZU21}		Hold		0.64	0.69	N/A	0.22	ns
T_{PSFD_XQZU28}		Setup	XQZU28	0.81	0.83	N/A	1.83	ns
T_{PHFD_XQZU28}		Hold		0.64	0.69	N/A	0.22	ns
T_{PSFD_XQZU29}		Setup	XQZU29	0.81	0.83	N/A	1.83	ns
T_{PHFD_XQZU29}		Hold		0.64	0.69	N/A	0.22	ns
T_{PSFD_ZU43}		Setup	XCZU43	0.81	0.83	1.69	1.83	ns
T_{PHFD_ZU43}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_ZU46}		Setup	XCZU46	0.81	0.83	1.69	1.83	ns
T_{PHFD_ZU46}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_ZU47}		Setup	XCZU47	0.81	0.83	1.69	1.83	ns
T_{PHFD_ZU47}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_ZU48}		Setup	XCZU48	0.81	0.83	1.69	1.83	ns
T_{PHFD_ZU48}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_ZU49}		Setup	XCZU49	0.81	0.83	1.69	1.83	ns
T_{PHFD_ZU49}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_XQZU48}		Setup	XQZU48	0.81	0.83	1.69	1.83	ns
T_{PHFD_XQZU48}		Hold		0.64	0.69	0.22	0.22	ns
T_{PSFD_XQZU49}		Setup	XQZU49	0.81	0.83	1.69	1.83	ns
T_{PHFD_XQZU49}		Hold		0.64	0.69	0.22	0.22	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 93: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages				Units
				0.85V		0.72V		
				-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1, 2, 3]								
$T_{PSMMCMCC\_ZU21}$	Global clock input and input flip-flop (or latch) with MMCM	Setup	XCZU21	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU21}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_ZU25}$		Setup	XCZU25	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU25}$		Hold		–0.11	–0.11	–0.20	–0.20	ns
$T_{PSMMCMCC\_ZU27}$		Setup	XCZU27	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU27}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_ZU28}$		Setup	XCZU28	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU28}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_ZU29}$		Setup	XCZU29	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU29}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_ZU39}$		Setup	XCZU39	1.95	N/A	1.95	N/A	ns
$T_{PHMMCMCC\_ZU39}$		Hold		–0.09	N/A	–0.18	N/A	ns
$T_{PSMMCMCC\_XQZU21}$		Setup	XQZU21	1.95	2.09	N/A	2.09	ns
$T_{PHMMCMCC\_XQZU21}$		Hold		–0.09	–0.09	N/A	–0.18	ns
$T_{PSMMCMCC\_XQZU28}$		Setup	XQZU28	1.95	2.09	N/A	2.09	ns
$T_{PHMMCMCC\_XQZU28}$		Hold		–0.09	–0.09	N/A	–0.18	ns
$T_{PSMMCMCC\_XQZU29}$		Setup	XQZU29	1.95	2.09	N/A	2.09	ns
$T_{PHMMCMCC\_XQZU29}$		Hold		–0.09	–0.09	N/A	–0.18	ns
$T_{PSMMCMCC\_ZU43}$		Setup	XCZU43	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU43}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_ZU46}$		Setup	XCZU46	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU46}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_ZU47}$		Setup	XCZU47	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU47}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_ZU48}$		Setup	XCZU48	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU48}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_ZU49}$		Setup	XCZU49	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_ZU49}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_XQZU48}$		Setup	XQZU48	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_XQZU48}$		Hold		–0.09	–0.09	–0.18	–0.18	ns
$T_{PSMMCMCC\_XQZU49}$		Setup	XQZU49	1.95	2.09	1.95	2.09	ns
$T_{PHMMCMCC\_XQZU49}$		Hold		–0.09	–0.09	–0.18	–0.18	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 94: **Sampling Window**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.85V		0.72V		
	-2	-1	-2	-1	
T_{SAMP_BUFG}[1]	610	610	610	610	ps
$T_{SAMP\_NATIVE\_DPA}$[2]	100	125	125	150	ps
$T_{SAMP\_NATIVE\_BISC}$[3]	60	85	85	110	ps

Notes:

1. This parameter indicates the total sampling error of the Zynq UltraScale+ RFSoC DDR input registers, measured across voltage, temperature, and process. The measurement methodology uses the MMCM to capture the edges of operation of the DDR input registers. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.
2. This parameter is the receive sampling error for RX_BITSLICE when using dynamic phase alignment.
3. This parameter is the receive sampling error for RX_BITSLICE when using built-in self-calibration (BISC).

Table 95: **Input Logic Characteristics for Dynamic Phase Aligned Applications (Component Mode)**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.85V		0.72V		
	-2	-1	-2	-1	
$T_{INPUT\_LOGIC\_UNCERTAINTY}$[1]	40				ps
T_{CAL_ERROR}[2]	24				ps

Notes:

1. Input_logic_uncertainty accounts for the setup/hold and any pattern dependent jitter for the input logic (input register, IDDRE1, or ISERDESE3).
2. Calibration error associated with quantization effects based on the IDELAY resolution. Calibration must be performed for each input pin to ensure optimal performance.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 96: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew[1, 2]	XCZU21DR	FFVD1156	156	ps
		XCZU25DR	FFVE1156	145	ps
			FSVE1156	145	ps
			FFVG1517	165	ps
			FSVG1517	165	ps
		XCZU27DR	FFVE1156	145	ps
			FSVE1156	145	ps
			FFVG1517	165	ps
			FSVG1517	165	ps
		XCZU28DR	FFVE1156	145	ps
			FSVE1156	145	ps
			FFVG1517	165	ps
			FSVG1517	165	ps
		XCZU29DR	FFVF1760	160	ps
			FSVF1760	160	ps
		XCZU39DR	FFVF1760	160	ps
			FSVF1760	160	ps
		XQZU21DR	FFRD1156	168	ps
		XQZU28DR	FFRE1156	145	ps
			FFRG1517	164	ps
		XQZU29DR	FFRF1760	160	ps
		XCZU43DR	FFVE1156	145	ps
			FSVE1156	145	ps
			FFVG1517	148	ps
			FSVG1517	148	ps
		XCZU46DR	FFVH1760	131	ps
			FSVH1760	131	ps
		XCZU47DR	FFVE1156	145	ps
			FSVE1156	145	ps
			FFVG1517	148	ps
			FSVG1517	148	ps
		XCZU48DR	FFVE1156	145	ps
			FSVE1156	145	ps
			FFVG1517	148	ps
			FSVG1517	148	ps
		XCZU49DR	FFVF1760	158	ps
			FSVF1760	158	ps
		XQZU48DR	FFRE1156	143	ps
			FSRG1517	149	ps
		XQZU49DR	FSRF1760	157	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists the Zynq UltraScale+ RFSoCs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 97 summarizes the DC specifications of the GTY transceivers in Zynq UltraScale+ RFSoCs. Consult the *UltraScale Architecture GTY Transceivers User Guide* (UG578) for further details.

Table 97: **GTY Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to `11111`	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}[2]	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor[3]		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceivers User Guide* (UG578) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Figure 3: **Single-Ended Peak-to-Peak Voltage**

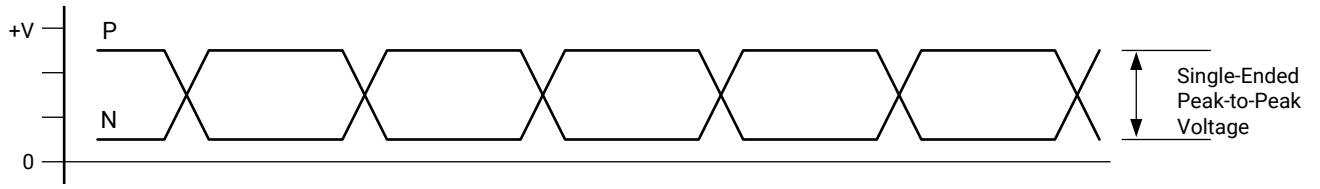
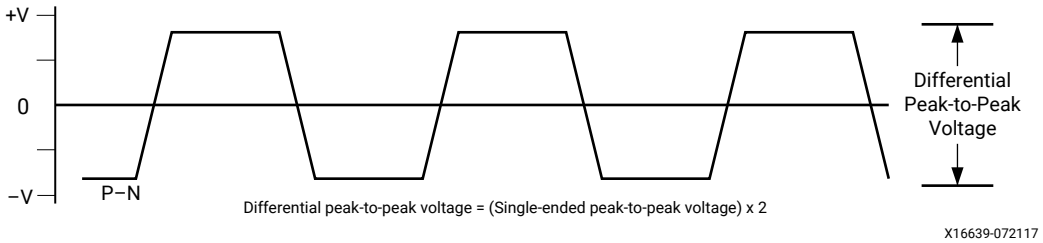


Figure 4: **Differential Peak-to-Peak Voltage**



The following tables summarize the DC specifications of the clock input/output levels of the GTY transceivers in Zynq UltraScale+ RFSoCs. Consult the *UltraScale Architecture GTY Transceivers User Guide* (UG578) for further details.

Table 98: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 99: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceivers User Guide* (UG578) for further information.

Table 100: **GTY Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.85V		0.72V		
			-2	-1	-2	-1	
F_{GTYMAX}	GTY maximum line rate		28.21	25.785	28.21	12.5	Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5	0.5	0.5	0.5	Gb/s

Table 100: **GTY Transceiver Performance** *(cont'd)*

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages								Units
			0.85V				0.72V				
			-2		-1		-2		-1		
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range[1]	1	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A								Gb/s
		32	N/A								Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range[2]	1	19.6	28.21	19.6	25.785	19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range[3]	1	16.0	26.0	16.0	25.785	16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. The values listed are the rounded results of the calculated equation (2 × CPLL_Frequency)/Output_Divider.
2. The values listed are the rounded results of the calculated equation (QPLL0_Frequency × RATE)/Output_Divider where RATE is 1 when QPLL0_CLKOUT_RATE is set to HALF and 2 if QPLL0_CLKOUT_RATE is set to FULL.
3. The values listed are the rounded results of the calculated equation (QPLL1_Frequency × RATE)/Output_Divider where RATE is 1 when QPLL1_CLKOUT_RATE is set to HALF and 2 if QPLL1_CLKOUT_RATE is set to FULL.

Table 101: **GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency	250	MHz

Table 102: **GTY Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

Table 103: **GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description[1, 2]	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 104: **GTY Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE)	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled		–	50,000	2.3×10^6	UI

Table 105: **GTY Transceiver User Clock Switching Characteristics**

Symbol	Description[1]	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages				Units
				0.85V		0.72V		
		Internal Logic	Interconnect Logic	-2[2, 3]	-1[5, 6, 7]	-2[3, 4]	-1[6]	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	402.891	402.832	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	402.891	402.832	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[8] maximum frequency	16	16, 32	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	390.625	390.625	322.266	MHz
		64	64, 128	440.781	402.891	402.832	195.313	MHz
		20	20, 40	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	312.500	350.000	257.813	MHz
		80	80, 160	352.625	322.313	352.625	156.250	MHz
F_{RXIN}	RXUSRCLK[8] maximum frequency	16	16, 32	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	390.625	390.625	322.266	MHz
		64	64, 128	440.781	402.891	402.832	195.313	MHz
		20	20, 40	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	312.500	350.000	257.813	MHz
		80	80, 160	352.625	322.313	352.625	156.250	MHz

Table 105: **GTY Transceiver User Clock Switching Characteristics** *(cont'd)*

Symbol	Description[1]	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages				Units
				0.85V		0.72V		
		Internal Logic	Interconnect Logic	-2[2, 3]	-1[5, 6, 7]	-2[3, 4]	-1[6]	
F_{TXIN2}	TXUSRCLK2[8] maximum frequency	16	16	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	195.313	195.313	161.133	MHz
		64	64	440.781	402.891	402.832	195.313	MHz
		64	128	220.391	201.445	201.416	97.656	MHz
		20	20	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	312.500	350.000	257.813	MHz
		40	80	204.688	156.250	175.000	128.906	MHz
		80	80	352.625	322.313	352.625	156.250	MHz
		80	160	176.313	161.156	176.313	78.125	MHz
F_{RXIN2}	RXUSRCLK2[8] maximum frequency	16	16	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	195.313	195.313	161.133	MHz
		64	64	440.781	402.891	402.832	195.313	MHz
		64	128	220.391	201.445	201.416	97.656	MHz
		20	20	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	312.500	350.000	257.813	MHz
		40	80	204.688	156.250	175.000	128.906	MHz
		80	80	352.625	322.313	352.625	156.250	MHz
		80	160	176.313	161.156	176.313	78.125	MHz

Notes:

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceivers User Guide* (UG578).
2. For speed grades -2E and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grade -2LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.72V.
5. For speed grades -1E,-1I, and -1M, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
6. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
7. For the speed grades -1E,-1I, and -1M, only a 64- or 80-bit internal data path can be used for line rates above 12.5 Gb/s.
8. When the gearbox is used, these maximums refer to the XCLK. For more information, see the Valid Data Width Combinations for TX Asynchronous Gearbox table in the *UltraScale Architecture GTY Transceivers User Guide* (UG578).

Table 106: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew[1]		–	–	500.00	ps
$T_{J28.21}$	Total jitter[2, 4]	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J16.375}$	Total jitter[2, 4]	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J15.0}$	Total jitter[2, 4]	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2, 4]	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2, 4]	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J13.1}$	Total jitter[2, 4]	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter[2, 4]	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter[3, 4]	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter[2, 4]	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter[2, 4]	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter[3, 4]	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter[2, 4]	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter[3, 4]	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J8.0}$	Total jitter[3, 4]	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J6.6}$	Total jitter[3, 4]	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J5.0}$	Total jitter[3, 4]	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J4.25}$	Total jitter[3, 4]	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J3.20}$	Total jitter[3, 4]	3.20 Gb/s[5]	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter[3, 4]		–	–	0.10	UI
$T_{J2.5}$	Total jitter[3, 4]	2.5 Gb/s[6]	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter[3, 4]		–	–	0.10	UI

Table 106: **GTY Transceiver Transmitter Switching Characteristics** *(cont'd)*

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J1.25}$	Total jitter[3, 4]	1.25 Gb/s[7]	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter[3, 4]		–	–	0.06	UI
T_{J500}	Total jitter[3, 4]	500 Mb/s[8]	–	–	0.10	UI
D_{J500}	Deterministic jitter[3, 4]		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 107: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking[1]	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance[2]						
$J_{T\_SJ28.21}$	Sinusoidal jitter (QPLL)[3]	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)[3]	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)[3]	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)[3]	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)[3]	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)[3]	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)[3]	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)[3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)[3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)[3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)[3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL)[3]	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL)[3]	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)[3]	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)[3]	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)[3]	3.2 Gb/s[4]	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)[3]	2.5 Gb/s[5]	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)[3]	1.25 Gb/s[6]	0.30	–	–	UI

Table 107: **GTY Transceiver Receiver Switching Characteristics** *(cont'd)*

Symbol	Description	Condition	Min	Typ	Max	Units
J_{T_SJ500}	Sinusoidal jitter (CPLL)[3]	500 Mb/s[7]	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye[2]						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye[8]	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye[8]	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:
1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceivers User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 108: **GTY Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant[1]
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant[1]
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–28.21	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR[2]	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant

Table 108: **GTY Transceiver Protocol List** *(cont'd)*

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI[3]	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI[3]	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant[3]
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale+ Interlaken. The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ RFSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 109).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 110).
- 12 x 25.78125 Gb/s lane logic only mode (Table 111).

Table 109: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.85V				0.72V				
		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		MHz
		Min[1]	Max	Min[1]	Max	Min[1]	Max	Min[1]	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 110: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.85V				0.72V				
		-2E/-2I/-2LE[1]		-1E/-1I/-1M/-1LI		-2LE		-2LI/-1LI		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		N/A		250.00		N/A		MHz
		Min[2]	Max	Min	Max	Min[2]	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50[3]	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00[4]	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT} = 0.85V) speed grade.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 111: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	N/A	N/A	N/A	MHz

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale+ Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ RFSoC.

Table 112: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
CAUI-10 Mode						
F_{TX_CLK}	Transmit clock	390.625	322.266	322.266	322.266	MHz
F_{RX_CLK}	Receive clock	390.625	322.266	322.266	322.266	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	322.266	322.266	322.266	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	MHz
CAUI-4, CAUI-4 + RS-FEC, and RS-FEC Transcode Bypass Modes						
F_{TX_CLK}	Transmit clock	322.266	322.266	322.266	N/A	MHz
F_{RX_CLK}	Receive clock	322.266	322.266	322.266	N/A	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	322.266	322.266	322.266	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	N/A	MHz

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express® designs can be found at PCI Express. The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ RFSoC.

Table 113: **Maximum Performance for PCIE4-based PCI Express Designs for ZU2xDR and ZU39DR Devices**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency	500.00	500.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency	125.00	125.00	125.00	125.00	MHz

The PCIE4C blocks for ZU4xDR devices have support for the CCIX protocol and timing enhancements allowing the PCIE4C blocks to run Gen3 x16 except with -1 speed grade when V_{CCINT} = 0.72V.

Table 114: **Maximum Performance for PCIE4C-based PCI Express and CCIX Designs for ZU4xDR Devices**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency	500.00	500.00	500.00	250.00	MHz
$F_{CORECLKCCIX}$	CCIX TL interface clock maximum frequency	500.00	500.00	N/A	N/A	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency	125.00	125.00	125.00	125.00	MHz

Integrated RF-ADC Block

RF-ADC Electrical Characteristics

Table 115: **RF-ADC Electrical Characteristics for ZU2xDR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog Inputs					
Resolution		12	–	–	Bits
Sample Rate	Devices using quad ADC tile channel	0.5	–	2.058	GS/s
	Devices using dual ADC tile channel	1	–	4.096	GS/s
Full-scale Input	Input 100Ω on-die termination[3]	–	1	–	V_{PPD}
		–	1	–	dBm
Analog Input Bandwidth	Full-power bandwidth (–3 dB)[3]	–	4	–	GHz
Common mode voltage[4]	AC coupling mode with internal bias	–	1.25	–	V
Crosstalk isolation between channels[5]	F_{IN} = 240 MHz	–	–70	–	dBc
	F_{IN} = 1.9 GHz	–	–70	–	dBc
	F_{IN} = 2.4 GHz	–	–70	–	dBc
	F_{IN} = 3.5 GHz	–	–70	–	dBc

Notes:

1. Analog inputs at –1 dBFS, unless otherwise noted in the test conditions.
2. Typical values are specified at nominal voltage, T_j = 25°C.
3. Consult S parameter I/O files for further details on input characteristics.
4. When using DC coupling mode, use the VCM output pin to bias the input to the RF-ADC.
5. Values represent two channel crosstalk worst-case values for any combination of channel selections.

Table 116: **RF-ADC Electrical Characteristics for ZU39DR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog Inputs					
Resolution		12	–	–	Bits
Sample Rate	Devices using quad ADC tile channel	0.5	–	2.220	GS/s
Full-scale Input	Input 100Ω on-die termination	–	1	–	V_{PPD}
		–	1	–	dBm
Analog Input Bandwidth	Full-power bandwidth (–3 dB)	–	5	–	GHz
Return Loss (R_L)[3]	Up to 4 GHz	–	–10	–	dB
	Up to 5 GHz	–	–8	–	dB
Common mode voltage[4]	AC coupling mode with internal bias	–	1.25	–	V
Crosstalk isolation between channels[5]	F_{IN} = 240 MHz	–	–70	–	dBc
	F_{IN} = 1.9 GHz	–	–70	–	dBc
	F_{IN} = 2.4 GHz	–	–70	–	dBc
	F_{IN} = 3.5 GHz	–	–70	–	dBc
	F_{IN} = 4.2 GHz	–	–69	–	dBc
	F_{IN} = 4.9 GHz	–	–67	–	dBc

Notes:

1. Analog inputs at –1 dBFS, unless otherwise noted in the test conditions.
2. Typical values are specified at nominal voltage, T_j = 25°C.
3. This is the return loss of the worst case channel quoted from DC to a specified frequency point. Consult the S parameter I/O files for further details as input characteristics depend on differential I/O selection. The RL reference plan is closed to the BGA footprint, keeping two times the BGA pitch distance from ball contact to avoid micro-probing electromagnetic disturbance.
4. When using DC coupling mode, use the VCM output pin to bias the input to the RF-ADC.
5. Values represent two channel crosstalk worst-case values for any combination of channel selections.

Table 117: **RF-ADC Electrical Characteristics for ZU4xDR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog inputs					
Resolution		14	–	–	Bits
Sample Rate	Devices using quad ADC tile channel	0.5	–	2.5	GS/s
	Devices using dual ADC tile channel	1	–	5	GS/s
Full-scale input	Input 100Ω on-die termination when DSA attenuation = 0 dB	–	1	–	V_{PPD}
		–	1	–	dBm
Maximum allowed input power	Input 100Ω on-die termination when DSA attenuation ≥ 15 dB	–	4.8	–	V_{PPD}
		–	14.6	–	dBm
Digital Attenuation Range		0	–	27	dB
Attenuator step size		–	1	–	dB
Auto attenuation	Automatically set when amplitude over-voltage is asserted	–	15	–	dB
Analog input bandwidth	Full-power bandwidth (–3 dB)	–	6	–	GHz
Return loss (R_L)[3]	Up to 4 GHz	–	–12	–	dB
	Up to 6 GHz	–	–10	–	dB
Optimized common mode voltage range	Performance optimized range. AC and DC coupling modes[4]	0.68	0.7	0.72	V
Maximum common mode voltage range	Available range before triggering over-voltage protection. AC and DC coupling modes[4]	0.4	0.7	1	V
Crosstalk isolation between channels[5]	F_{IN} = 0–4 GHz	–	–75	–	dBc
	F_{IN} = 0–6 GHz	–	–70	–	dBc

Notes:

1. Analog inputs at –1 dBFS, unless otherwise noted in the test conditions.
2. Typical values are specified at nominal voltage, T_j = 40°C.
3. This is the return loss of the worst case channel quoted from DC to a specified frequency point. Consult the S parameter I/O files for further details because input characteristics depend on channel and package selection. The RL reference plan is close to the BGA footprint, keeping two times the BGA pitch distance from ball contact to avoid micro-probing electromagnetic disturbance.
4. When using DC coupling mode, use the VCM output pin to bias the input to the RF-ADC.
5. Values represent two channel crosstalk worst-case values for any combination of channel selections. This specification is only characterized on the XCZU46DR-H1760.

RF-ADC Performance Characteristics

Table 118: **RF-ADC Quad ADC Tile Performance Characteristics for ZU2xDR Devices**

Symbol	Parameter	Comments/Conditions		Min	Typ[1, 2]	Max	Units
ACLR	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB	F_{IN} = 3.5 GHz at full-scale Bandwidth = 18 MHz		–	–63	–	dBc
		F_{IN} = 3.5 GHz, carrier at –10 dBFS, Bandwidth = 18 MHz		–	–60	–58	dBc
	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB, using internal PLL to sample RF-ADC with F_{REF} = 250 MHz	F_{IN} = 3.5 GHz at full-scale Bandwidth = 18 MHz		–	–62	–	dBc
		F_{IN} = 3.5 GHz, carrier at –10 dBFS Bandwidth = 18 MHz		–	–60	–	dBc
NSD	Noise spectral density averaged across the first Nyquist zone	Input at –35 dBFS (noise floor)		–	–151.5	–	dBFS/Hz
		F_{IN} = 240 MHz		–	–150	–147	dBFS/Hz
		F_{IN} = 1.9 GHz		–	–148	–	dBFS/Hz
		F_{IN} = 2.4 GHz		–	–146	–144	dBFS/Hz
		F_{IN} = 3.5 GHz (by temperature range)	E and I	–	–144	–142	dBFS/Hz
			M	–	–144	–141	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS		–	–149.5	–146	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –20 dBFS		–	–151.5	–	dBFS/Hz
	Noise spectral density averaged across the first Nyquist zone using internal PLL to sample RF-ADC with F_{REF} = 250 MHz	Input at –35 dBFS (noise floor)		–	–152	–	dBFS/Hz
		F_{IN} = 240 MHz		–	–150	–	dBFS/Hz
		F_{IN} = 1.9 GHz		–	–147	–	dBFS/Hz
		F_{IN} = 2.4 GHz		–	–145	–	dBFS/Hz
		F_{IN} = 3.5 GHz		–	–143	–	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS		–	–149	–	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –20 dBFS		–	–152	–	dBFS/Hz
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion.	F_{IN} = 240 MHz		77	85	–	dBc
		F_{IN} = 1.9 GHz		–	83	–	dBc
		F_{IN} = 2.4 GHz		–	82	–	dBc
		F_{IN} = 3.5 GHz		71	80	–	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS		69	77	–	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS		–	70	–	dBc
HD2	Second-order harmonic distortion	F_{IN} = 240 MHz		–	–85	–	dBc
		F_{IN} = 1.9 GHz		–	–68	–	dBc
		F_{IN} = 2.4 GHz		–	–67	–	dBc
		F_{IN} = 3.5 GHz		–	–65	–	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS		–	–70	–	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS		–	–79	–	dBc

Table 118: **RF-ADC Quad ADC Tile Performance Characteristics for ZU2xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions		Min	Typ[1, 2]	Max	Units
HD3	Third-order harmonic distortion	F_{IN} = 240 MHz		–	–78	–68	dBc
		F_{IN} = 1.9 GHz		–	–66	–	dBc
		F_{IN} = 1.9 GHz at –2 dBFS		–	–71	–	dBc
		F_{IN} = 1.9 GHz at –3 dBFS		–	–74	–	dBc
		F_{IN} = 2.4 GHz	E and I	–	–64	–60	dBc
			M	–	–64	–58	dBc
		F_{IN} = 2.4 GHz at –2 dBFS		–	–67	–	dBc
		F_{IN} = 2.4 GHz at –3 dBFS		–	–69	–	dBc
		F_{IN} = 3.5 GHz		–	–64	–	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS		–	–79	–67	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS		–	–82	–	dBc
IM3	Two–tone (F_1,F_2) third-order intermodulation distortion	F_{IN} = 240 MHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta		–	–78	–68	dBc
		F_{IN} = 1.9 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta		–	–72	–	dBc
		F_{IN} = 2.4 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta		–	–67	–	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	E and I	–	–62	–60	dBc
			M	–	–62	–58	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –8 dBFS and 20 MHz delta		–	–65	–	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –9 dBFS and 20 MHz delta		–	–67	–	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –16 dBFS and 20 MHz delta		–	–77	–68	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –26 dBFS and 20 MHz delta		–	–76	–	dBc
GTIS	Gain/time interleaving spur at K * $F_S/N \pm F_{IN}$, where N = 4 and K = 0, 1, 2, ... N	F_{IN} = 240 MHz		–	–88	–80	dBc
		F_{IN} = 1.9 GHz		–	–85	–	dBc
		F_{IN} = 2.4 GHz		–	–83	–	dBc
		F_{IN} = 3.5 GHz		–	–80	–70	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS		–	–79	–70	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS		–	–76	–	dBc
OIS	Offset interleaving spur at K * F_S/N, where N = 4 and K = 0, 1, 2, ... N	F_{IN} = 240 MHz		–	–92	–83	dBFS
		F_{IN} = 1.9 GHz		–	–92	–	dBFS
		F_{IN} = 2.4 GHz		–	–92	–	dBFS
		F_{IN} = 3.5 GHz		–	–92	–	dBFS
		F_{IN} = 3.5 GHz, CW at –10 dBFS		–	–92	–82	dBFS
		F_{IN} = 3.5 GHz, CW at –20 dBFS		–	–92	–	dBFS

Notes:

1. RF-ADC sampling rate is 2 GS/s using external sampling clock and ADC analog inputs at –1 dBFS, unless otherwise noted in the test conditions. ADC calibration mode is set using the guidance in the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).
2. Typical values are specified at nominal voltage, T_j = 40°C.

Table 119: **RF-ADC Quad ADC Tile Performance Characteristics for ZU39DR Devices**

Symbol	Parameter	Comments/Conditions	Min	Typ[1, 2]	Max	Units
ACLR	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB	F_{IN} = 3.5 GHz at full-scale Bandwidth = 18 MHz	–	–63	–	dBc
		F_{IN} = 3.5 GHz, carrier at –10 dBFS, Bandwidth = 18 MHz	–	–60	–58	dBc
	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB, using internal PLL to sample RF-ADC with F_{REF} = 250 MHz	F_{IN} = 3.5 GHz at full-scale Bandwidth = 18 MHz	–	–62	–	dBc
		F_{IN} = 3.5 GHz, carrier at –10 dBFS Bandwidth = 18 MHz	–	–60	–	dBc
	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB	F_{IN} = 4.9 GHz at full-scale Bandwidth = 18 MHz	–	–62	–	dBc
		F_{IN} = 4.9 GHz, carrier at –10 dBFS, Bandwidth = 18 MHz	–	–58	–	dBc
	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB, using internal PLL to sample RF-ADC with F_{REF} = 250 MHz	F_{IN} = 4.9 GHz at full-scale Bandwidth = 18 MHz	–	–59	–	dBc
		F_{IN} = 4.9 GHz, carrier at –10 dBFS, Bandwidth = 18 MHz	–	–57	–	dBc
NSD	Noise spectral density averaged across the first Nyquist zone	Input at –35 dBFS (noise floor)	–	–151.5	–	dBFS/Hz
		F_{IN} = 240 MHz	–	–150	–147	dBFS/Hz
		F_{IN} = 1.9 GHz	–	–148	–	dBFS/Hz
		F_{IN} = 2.4 GHz	–	–146	–144	dBFS/Hz
		F_{IN} = 3.5 GHz	–	–144	–142	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–149.5	–146	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–151.5	–	dBFS/Hz
		F_{IN} = 4.2 GHz	–	–144	–	dBFS/Hz
		F_{IN} = 4.9 GHz	–	–142	–139	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–149	–	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–151	–	dBFS/Hz
	Noise spectral density averaged across the first Nyquist zone using internal PLL to sample RF-ADC with F_{REF} = 250 MHz	Input at –35 dBFS (noise floor)	–	–152	–	dBFS/Hz
		F_{IN} = 240 MHz	–	–150	–	dBFS/Hz
		F_{IN} = 1.9 GHz	–	–147	–	dBFS/Hz
		F_{IN} = 2.4 GHz	–	–145	–	dBFS/Hz
		F_{IN} = 3.5 GHz	–	–143	–	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–149	–	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–152	–	dBFS/Hz
		F_{IN} = 4.2 GHz	–	–142	–	dBFS/Hz
		F_{IN} = 4.9 GHz	–	–140	–	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–147	–	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–151	–	dBFS/Hz

Table 119: **RF-ADC Quad ADC Tile Performance Characteristics for ZU39DR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	Min	Typ[1, 2]	Max	Units
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion	F_{IN} = 240 MHz	77	85	–	dBc
		F_{IN} = 1.9 GHz	–	83	–	dBc
		F_{IN} = 2.4 GHz	–	82	–	dBc
		F_{IN} = 3.5 GHz	71	80	–	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	69	77	–	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	70	–	dBc
		F_{IN} = 4.2 GHz	–	77.5	–	dBc
		F_{IN} = 4.9 GHz	–	72.5	–	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	76	–	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	67	–	dBc
HD2	Second-order harmonic distortion	F_{IN} = 1.9 GHz	–	–68	–	dBc
		F_{IN} = 2.4 GHz	–	–67	–	dBc
		F_{IN} = 3.5 GHz	–	–65	–	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–70	–	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–79	–	dBc
		F_{IN} = 4.2 GHz	–	–60	–	dBc
		F_{IN} = 4.9 GHz	–	–50	–	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–63	–	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–73	–	dBc
HD3	Third-order harmonic distortion	F_{IN} = 240 MHz	–	–78	–68	dBc
		F_{IN} = 1.9 GHz	–	–66	–	dBc
		F_{IN} = 1.9 GHz at –2 dBFS	–	–71	–	dBc
		F_{IN} = 1.9 GHz at –3 dBFS	–	–74	–	dBc
		F_{IN} = 2.4 GHz	–	–64	–	dBc
		F_{IN} = 2.4 GHz at –2 dBFS	–	–67	–	dBc
		F_{IN} = 2.4 GHz at –3 dBFS	–	–69	–	dBc
		F_{IN} = 3.5 GHz	–	–64	–	dBc
		F_{IN} = 3.5 GHz at –2 dBFS	–	–64	–	dBc
		F_{IN} = 3.5 GHz at –3 dBFS	–	–66	–	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–79	–67	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–82	–	dBc
		F_{IN} = 4.2 GHz	–	–53	–	dBc
		F_{IN} = 4.9 GHz	–	–47	–	dBc
		F_{IN} = 4.9 GHz at –2 dBFS	–	–49	–	dBc
		F_{IN} = 4.9 GHz at –3 dBFS	–	–51	–	dBc
		F_{IN} = 4.9 GHz at –10 dBFS	–	–65	–	dBc
		F_{IN} = 4.9 GHz at –20 dBFS	–	–80	–	dBc

Table 119: **RF-ADC Quad ADC Tile Performance Characteristics for ZU39DR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	Min	Typ[1, 2]	Max	Units
IM3	Two–tone (F_1,F_2) third-order intermodulation distortion	F_{IN} = 240 MHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–78	–68	dBc
		F_{IN} = 1.9 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–72	–	dBc
		F_{IN} = 2.4 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–67	–	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–62	–60	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –8 dBFS and 20 MHz delta	–	–65	–	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –9 dBFS and 20 MHz delta	–	–67	–	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –16 dBFS and 20 MHz delta	–	–77	–68	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –26 dBFS and 20 MHz delta	–	–76	–	dBc
		F_{IN} = 4.2 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–62	–	dBc
		F_{IN} = 4.9 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–54	–	dBc
		F_{IN} = 4.9 GHz center frequency F_1, F_2 at –8 dBFS and 20 MHz delta	–	–56	–	dBc
		F_{IN} = 4.9 GHz center frequency F_1, F_2 at –9 dBFS and 20 MHz delta	–	–59	–	dBc
		F_{IN} = 4.9 GHz center frequency F_1, F_2 at –16 dBFS and 20 MHz delta	–	–73	–	dBc
		F_{IN} = 4.9 GHz center frequency F_1, F_2 at –26 dBFS and 20 MHz delta	–	–76	–	dBc
GTIS	Gain/time interleaving spur at K * $F_S/N \pm F_{IN}$, where N = 4 and K = 0, 1, 2, … N	F_{IN} = 240 MHz	–	–88	–80	dBc
		F_{IN} = 1.9 GHz	–	–85	–	dBc
		F_{IN} = 2.4 GHz	–	–83	–	dBc
		F_{IN} = 3.5 GHz	–	–80	–70	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–79	–70	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–76	–	dBc
		F_{IN} = 4.2 GHz	–	–79	–	dBc
		F_{IN} = 4.9 GHz	–	–77	–	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–76	–	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–76	–	dBc

Table 119: **RF-ADC Quad ADC Tile Performance Characteristics for ZU39DR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	Min	Typ[1, 2]	Max	Units
OIS	Offset interleaving spur at K * F_S/N, where N = 4 and K = 0, 1, 2, ... N	F_{IN} = 240 MHz	–	–92	–83	dBFS
		F_{IN} = 1.9 GHz	–	–92	–	dBFS
		F_{IN} = 2.4 GHz	–	–92	–	dBFS
		F_{IN} = 3.5 GHz	–	–92	–	dBFS
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–92	–82	dBFS
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–92	–	dBFS
		F_{IN} = 4.2 GHz	–	–92	–	dBFS
		F_{IN} = 4.9 GHz	–	–92	–	dBFS
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–92	–	dBFS
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–92	–	dBFS

Notes:

1. RF-ADC sampling rate is 2 GS/s using external sampling clock and ADC analog inputs at –1 dBFS, unless otherwise noted in the test conditions. ADC calibration mode is set using the guidance in the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).
2. Typical values are specified at nominal voltage, T_j = 40°C.

Table 120: **RF-ADC Quad ADC Tile Performance Characteristics for ZU4xDR Devices (ACLR Only)**

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			5 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
ACLR	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB, measured with external sampling clock forwarded between tiles.	F_{IN} = 3.5 GHz at full-scale Bandwidth = 18 MHz	–	–63.0	–	–60.0	dBc
		F_{IN} = 3.5 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–60.0	–56.4	–60.0	dBc
		F_{IN} = 4.9 GHz at full-scale Bandwidth = 18 MHz	–	–62.0	–	–58.0	dBc
		F_{IN} = 4.9 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–60.0	–56.4	–60.0	dBc
		F_{IN} = 5.9 GHz at full-scale Bandwidth = 18 MHz	–	–58.0	–	–56.0	dBc
		F_{IN} = 5.9 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–59.0	–55.9	–59.0	dBc
	Adjacent channel leakage ratio with F_{REF} = 500 MHz[3] measured with sampling clock generated from internal RF PLL and forwarded between tiles.	F_{IN} = 3.5 GHz at full-scale Bandwidth = 18 MHz	–	–62.0	–	–60.0	dBc
		F_{IN} = 3.5 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–60.0	–55.4	–59.0	dBc
		F_{IN} = 4.9 GHz at full-scale Bandwidth = 18 MHz	–	–61.0	–	–58.0	dBc
		F_{IN} = 4.9 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–59.0	–55.4	–59.0	dBc
		F_{IN} = 5.9 GHz at full-scale Bandwidth = 18 MHz	–	–58.0	–	–55.0	dBc
		F_{IN} = 5.9 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–58.0	–54.9	–58.0	dBc

Notes:

1. RF-ADC sampling rate is 2.5 GS/s using external sampling clock and ADC analog inputs at –1 dBFS, unless otherwise noted in the test conditions. ADC calibration mode is set to AutoCal mode. The ADC tiles are characterized using the on-chip clock forwarding configuration from tile 1 (bank 225), except when mentioned in the parameter condition column.
2. Typical values are specified at nominal voltage, T_j = 40°C.
3. See *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for internal PLL information.

Table 121: **RF-ADC Quad ADC Tile Performance Characteristics for ZU4xDR Devices**

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			10 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
NSD	Noise spectral density averaged across the first Nyquist zone, measured with external sampling clock forwarded between tiles.	Input at –35 dBFS (noise floor)	–	–150.5	–	–151.0	dBFS/Hz
		F_{IN} = 240 MHz	–	–150.0	–147.0	–150.0	dBFS/Hz
		F_{IN} = 1.9 GHz	–	–149.0	–	–149.0	dBFS/Hz
		F_{IN} = 2.4 GHz	–	–148.0	–146.0	–148.0	dBFS/Hz
		F_{IN} = 3.5 GHz	–	–146.0	–144.0	–146.0	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–150.0	–147.5	–150.0	dBFS/Hz
		F_{IN} = 4.9 GHz	–	–145.0	–143.0	–145.0	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–149.0	–147.8	–149.0	dBFS/Hz
		F_{IN} = 5.9 GHz	–	–144.0	–141.0	–144.0	dBFS/Hz
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–149.0	–147.1	–149.0	dBFS/Hz
	Noise spectral density with F_{REF} = 500 MHz,[3] measured with sampling clock generated from internal RF PLL and forwarded between tiles.	Input at –35 dBFS (noise floor)	–	–150.5	–	–151.0	dBFS/Hz
		F_{IN} = 240 MHz	–	–150.0	–145.0	–150.0	dBFS/Hz
		F_{IN} = 1.9 GHz	–	–147.0	–	–147.0	dBFS/Hz
		F_{IN} = 2.4 GHz	–	–145.0	–	–145.0	dBFS/Hz
		F_{IN} = 3.5 GHz	–	–143.0	–142.0	–143.0	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–149.0	–147.0	–149.0	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–150.0	–	–150.0	dBFS/Hz
		F_{IN} = 4.9 GHz	–	–142.0	–140.0	–142.0	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–148.0	–146.0	–148.0	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–151.0	–	–151.0	dBFS/Hz
		F_{IN} = 5.9 GHz	–	–140.0	–	–140.0	dBFS/Hz
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–147.0	–	–147.0	dBFS/Hz
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–150.0	–	–150.0	dBFS/Hz
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion, and including OIS and GTIS spurs.	F_{IN} = 240 MHz	72.0	84.0	–	82.0	dBc
		F_{IN} = 1.9 GHz	–	83.0	–	81.0	dBc
		F_{IN} = 2.4 GHz	–	82.0	–	80.0	dBc
		F_{IN} = 3.5 GHz	72.0	80.0	–	79.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	64.0	77.0	–	74.0	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	66.0	–	65.0	dBc
		F_{IN} = 4.9 GHz	67.0	77.0	–	76.0	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	66.0	75.0	–	74.0	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	66.0	–	65.0	dBc
		F_{IN} = 5.9 GHz	66.0	75.0	–	75.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS	65.0	74.0	–	73.0	dBc
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	66.0	–	65.0	dBc

Table 121: **RF-ADC Quad ADC Tile Performance Characteristics for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			10 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
HD2	Second-order harmonic distortion	F_{IN} = 240 MHz	–	–81.0	–	–82.0	dBc
		F_{IN} = 1.9 GHz	–	–67.0	–	–64.0	dBc
		F_{IN} = 2.4 GHz	–	–62.0	–	–60.0	dBc
		F_{IN} = 3.5 GHz	–	–56.0	–	–54.0	dBc
		F_{IN} = 3.5 GHz, CW at –2 dBFS	–	–57.0	–	–55.0	dBc
		F_{IN} = 3.5 GHz, CW at –3 dBFS	–	–58.0	–	–56.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–65.0	–	–63.0	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–75.0	–	–74.0	dBc
		F_{IN} = 4.9 GHz	–	–51.0	–	–48.0	dBc
		F_{IN} = 4.9 GHz, CW at –2 dBFS	–	–52.0	–	–49.0	dBc
		F_{IN} = 4.9 GHz, CW at –3 dBFS	–	–53.0	–	–50.0	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–60.0	–	–57.0	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–69.0	–	–67.0	dBc
		F_{IN} = 5.9 GHz	–	–49.0	–	–47.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–58.0	–	–56.0	dBc
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–68.0	–	–66.0	dBc
HD3	Third-order harmonic distortion	F_{IN} = 240 MHz	–	–76.0	–65.0	–73.0	dBc
		F_{IN} = 1.9 GHz	–	–69.0	–	–65.0	dBc
		F_{IN} = 2.4 GHz	–	–68.0	–	–66.0	dBc
		F_{IN} = 3.5 GHz	–	–67.0	–	–69.0	dBc
		F_{IN} = 3.5 GHz, CW at –2 dBFS	–	–68.0	–	–71.0	dBc
		F_{IN} = 3.5 GHz, CW at –3 dBFS	–	–70.0	–	–72.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–80.0	–67.0	–81.0	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–82.0	–	–82.0	dBc
		F_{IN} = 4.9 GHz	–	–56.0	–	–56.0	dBc
		F_{IN} = 4.9 GHz, CW at –2 dBFS	–	–58.0	–	–58.0	dBc
		F_{IN} = 4.9 GHz, CW at –3 dBFS	–	–60.0	–	–60.0	dBc
		F_{IN} = 4.9 GHz at –10 dBFS	–	–75.0	–64.0	–75.0	dBc
		F_{IN} = 4.9 GHz at –20 dBFS	–	–81.0	–	–81.0	dBc
		F_{IN} = 5.9 GHz	–	–50.0	–	–50.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–68.0	–61.0	–68.0	dBc
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–80.0	–	–80.0	dBc

Table 121: **RF-ADC Quad ADC Tile Performance Characteristics for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			10 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
IM3	Two–tone (F_1, F_2) third-order inter-modulation distortion	F_{IN} = 240 MHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–81.0	–74.0	–75.0	dBc
		F_{IN} = 1.9 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–75.0	–	–71.0	dBc
		F_{IN} = 2.4 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–74.0	–	–70.0	dBc
		F_{IN} = 3.5 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–69.0	–61.0	–70.0	dBc
		F_{IN} = 3.5 GHz center frequency, F_1, F_2 at –9 dBFS and 20 MHz delta	–	–74.0	–	–74.0	dBc
		F_{IN} = 3.5 GHz center frequency, F_1, F_2 at –16 dBFS and 20 MHz delta	–	–80.0	–68.0	–80.0	dBc
		F_{IN} = 3.5 GHz center frequency, F_1, F_2 at –26 dBFS and 20 MHz delta	–	–75.0	–	–75.0	dBc
		F_{IN} = 4.9 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–59.0	–53.0	–56.0	dBc
		F_{IN} = 4.9 GHz center frequency, F_1, F_2 at –16 dBFS and 20 MHz delta	–	–75.0	–68.0	–75.0	dBc
		F_{IN} = 4.9 GHz center frequency, F_1, F_2 at –26 dBFS and 20 MHz delta	–	–74.0	–	–74.0	dBc
		F_{IN} = 5.9 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–53.0	–	–53.0	dBc
		F_{IN} = 5.9 GHz center frequency, F_1, F_2 at –16 dBFS and 20 MHz delta	–	–71.0	–65.0	–71.0	dBc
		F_{IN} = 5.9 GHz center frequency, F_1, F_2 at –26 dBFS and 20 MHz delta	–	–74.0	–	–74.0	dBc
GTIS	Gain/time interleaving spur at K * F_S/N ± F_{IN}, where N = 4 and K = 0, 1, 2, ... N	F_{IN} = 240 MHz	–	–97.0	–80.0	–97.0	dBc
		F_{IN} = 1.9 GHz	–	–90.0	–	–90.0	dBc
		F_{IN} = 2.4 GHz	–	–88.0	–	–88.0	dBc
		F_{IN} = 3.5 GHz	–	–85.0	–75.0	–85.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–83.0	–75.0	–83.0	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–78.0	–	–78.0	dBc
		F_{IN} = 4.9 GHz	–	–82.0	–	–82.0	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–81.0	–73.0	–81.0	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–76.0	–	–76.0	dBc
		F_{IN} = 5.9 GHz	–	–80.0	–	–80.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–80.0	–70.0	–80.0	dBc
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–76.0	–	–76.0	dBc

Table 121: **RF-ADC Quad ADC Tile Performance Characteristics for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			10 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
OIS	Offset interleaving spur at K * F_S/N, where N = 4 and K = 0, 1, 2, ... N	F_{IN} = 240 MHz	–	–88.0	–77.0	–85.0	dBFS
		F_{IN} = 1.9 GHz	–	–86.0	–	–83.0	dBFS
		F_{IN} = 2.4 GHz	–	–86.0	–	–81.0	dBFS
		F_{IN} = 3.5 GHz	–	–87.0	–76.0	–82.0	dBFS
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–87.0	–76.0	–85.0	dBFS
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–87.0	–	–85.0	dBFS
		F_{IN} = 4.9 GHz	–	–82.0	–71.0	–81.0	dBFS
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–87.0	–76.0	–84.0	dBFS
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–88.0	–	–86.0	dBFS
		F_{IN} = 5.9 GHz	–	–81.0	–70.0	–79.0	dBFS
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–87.0	–76.0	–85.0	dBFS
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–88.0	–	–86.0	dBFS

Notes:

1. RF-ADC sampling rate is 2.5 GS/s using external sampling clock and ADC analog inputs at –1 dBFS, unless otherwise noted in the test conditions. ADC calibration mode is set to AutoCal mode. The ADC tiles are characterized using the on-chip clock forwarding configuration from tile 1 (bank 225), except when mentioned in the parameter condition column.
2. Typical values are specified at nominal voltage, T_j = 40°C.
3. See *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for internal PLL information.

Table 122: **RF-ADC Dual ADC Tile Performance Characteristics for ZU2xDR Devices**

Symbol	Parameter	Comments/Conditions	Min	Typ[1, 2]	Max	Units
ACLR	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB	F_{IN} = 3.5 GHz at full scale. Bandwidth = 18 MHz	–	–67	–	dBc
		F_{IN} = 3.5 GHz at –10 dBFS. Bandwidth = 18 MHz	–	–62	–61	dBc
	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB, using internal PLL to sample RF-ADC with F_{REF} = 250 MHz	F_{IN} = 3.5 GHz at full scale. Bandwidth = 18 MHz	–	–63	–	dBc
		F_{IN} = 3.5 GHz at –10 dBFS. Bandwidth = 18 MHz	–	–60	–	dBc
NSD	Noise spectral density averaged across the first Nyquist zone	Input at –35 dBFS (noise floor)	–	–153	–151	dBFS/Hz
		F_{IN} = 240 MHz	–	–152	–151	dBFS/Hz
		F_{IN} = 1.9 GHz	–	–151	–	dBFS/Hz
		F_{IN} = 2.4 GHz	–	–150	–	dBFS/Hz
		F_{IN} = 3.5 GHz	–	–148	–146	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–153	–150	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–153	–	dBFS/Hz
	Noise spectral density averaged across the first Nyquist zone using internal PLL to sample RF-ADC with F_{REF} = 250 MHz	Input at –35 dBFS (noise floor)	–	–153	–	dBFS/Hz
		F_{IN} = 240 MHz	–	–153	–	dBFS/Hz
		F_{IN} = 1.9 GHz	–	–151	–	dBFS/Hz
		F_{IN} = 2.4 GHz	–	–150	–	dBFS/Hz
		F_{IN} = 3.5 GHz	–	–148	–	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–153	–	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–153	–	dBFS/Hz

Table 122: **RF-ADC Dual ADC Tile Performance Characteristics for ZU2xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	Min	Typ[1, 2]	Max	Units
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion.	F_{IN} = 240 MHz	78	86	–	dBc
		F_{IN} = 1.9 GHz	–	83	–	dBc
		F_{IN} = 2.4 GHz	–	78	–	dBc
		F_{IN} = 3.5 GHz	64	72	–	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	70	78	–	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	70	–	dBc
HD2	Second-order harmonic distortion	F_{IN} = 240 MHz	–	–70	–	dBc
		F_{IN} = 1.9 GHz	–	–66	–	dBc
		F_{IN} = 2.4 GHz	–	–65	–	dBc
		F_{IN} = 3.5 GHz	–	–63	–	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–70	–	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–78	–	dBc
HD3	Third-order harmonic distortion	F_{IN} = 240 MHz	–	–72	–63	dBc
		F_{IN} = 1.9 GHz	–	–61	–	dBc
		F_{IN} = 2.4 GHz	–	–62	–	dBc
		F_{IN} = 2.4 GHz at –2 dBFS	–	–65	–	dBc
		F_{IN} = 2.4 GHz at –3 dBFS	–	–67	–	dBc
		F_{IN} = 3.5 GHz	–	–63	–58	dBc
		F_{IN} = 3.5 GHz at –2 dBFS	–	–64	–	dBc
		F_{IN} = 3.5 GHz at –3 dBFS	–	–65	–	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–77	–67	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–81	–	dBc
IM3	Two–tone, third-order intermodulation distortion	F_{IN} = 240 MHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–70	–66	dBc
		F_{IN} = 1.9 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–67	–	dBc
		F_{IN} = 2.4 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–63	–	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –7 dBFS and 20 MHz delta	–	–58	–55	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –8 dBFS and 20 MHz delta	–	–62	–	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –9 dBFS and 20 MHz delta	–	–65	–	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –16 dBFS and 20 MHz delta	–	–74	–67	dBc
		F_{IN} = 3.5 GHz center frequency F_1, F_2 at –26 dBFS and 20 MHz delta	–	–76	–	dBc
GTIS	Gain/time interleaving spur at K * $F_S/N \pm F_{IN}$, where N = 8 and K = 0, 1, 2, ... N	F_{IN} = 240 MHz	–	–81	–73	dBc
		F_{IN} = 1.9 GHz	–	–80	–	dBc
		F_{IN} = 2.4 GHz	–	–80	–	dBc
		F_{IN} = 3.5 GHz	–	–79	–70	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–78	–70	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–74	–	dBc

Table 122: **RF-ADC Dual ADC Tile Performance Characteristics for ZU2xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	Min	Typ[1, 2]	Max	Units
OIS	Offset interleaving spur at K * F_S/N, where N = 8 and K = 0, 1, 2, ... N	F_{IN} = 240 MHz	–	–91	–86	dBFS
		F_{IN} = 1.9 GHz	–	–91	–	dBFS
		F_{IN} = 2.4 GHz	–	–91	–	dBFS
		F_{IN} = 3.5 GHz	–	–91	–86	dBFS
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–91	–86	dBFS
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–91	–	dBFS

Notes:

1. RF-ADC sampling rate is 4 GS/s using external sampling clock and ADC analog inputs at –1 dBFS, unless otherwise noted in the test conditions. ADC calibration mode is set using the guidance in the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).
2. Typical values are specified at nominal voltage, T_j = 40°C.

Table 123: **RF-ADC Dual ADC Tile Performance Characteristics for ZU4xDR Devices (ACLR Only)**

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			5 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
ACLR	Adjacent channel leakage ratio using 64QAM modulation, PAR = 6.5 dB, measured with external sampling clock forwarded between tiles	F_{IN} = 3.5 GHz at full-scale Bandwidth = 18 MHz	–	–65.0	–	–63.0	dBc
		F_{IN} = 3.5 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–63.0	–59.4	–63.0	dBc
		F_{IN} = 4.9 GHz at full-scale Bandwidth = 18 MHz	–	–63.0	–	–58.0	dBc
		F_{IN} = 4.9 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–63.0	–59.1	–63.0	dBc
		F_{IN} = 5.9 GHz at full-scale Bandwidth = 18 MHz	–	–60.0	–	–56.0	dBc
		F_{IN} = 5.9 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–62.0	–58.8	–61.0	dBc
	Adjacent channel leakage ratio with F_{REF} = 500 MHz[3] measured with sampling clock generated from internal RF PLL and forwarded between tiles	F_{IN} = 3.5 GHz at full-scale Bandwidth = 18 MHz	–	–63.0	–	–63.0	dBc
		F_{IN} = 3.5 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–62.5	–58.5	–62.5	dBc
		F_{IN} = 4.9 GHz at full-scale Bandwidth = 18 MHz	–	–61.0	–	–58.0	dBc
		F_{IN} = 4.9 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–61.5	–57.9	–61.5	dBc
		F_{IN} = 5.9 GHz at full-scale Bandwidth = 18 MHz	–	–59.0	–	–56.0	dBc
		F_{IN} = 5.9 GHz, Carrier at –10 dBFS, Bandwidth = 18 MHz	–	–60.0	–57.4	–60.0	dBc

Notes:

1. RF-ADC sampling rate is 5.0 GS/s using external sampling clock and ADC analog inputs at –1 dBFS, unless otherwise noted in the test conditions. ADC calibration mode is set to AutoCal mode. The ADC tiles are characterized using the on-chip clock forwarding configuration from tile 2 (bank 226), except when mentioned in the parameter condition column.
2. Typical values are specified at nominal voltage, T_j = 40°C.
3. See *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for internal PLL information.

Table 124: **RF-ADC Dual ADC Tile Performance Characteristics for ZU4xDR Devices**

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			10 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
NSD	Noise spectral density averaged across the first Nyquist zone, measured with external sampling clock forwarded between tiles	Input at –35 dBFS (noise floor)	–	–154.0	–	–154.0	dBFS/Hz
		F_{IN} = 240 MHz	–	–154.0	–150.4	–154.0	dBFS/Hz
		F_{IN} = 1.9 GHz	–	–152.5	–	–152.5	dBFS/Hz
		F_{IN} = 2.4 GHz	–	–152.0	–150.1	–152.0	dBFS/Hz
		F_{IN} = 3.5 GHz	–	–151.0	–148.3	–151.0	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–153.0	–151.5	–153.0	dBFS/Hz
		F_{IN} = 4.9 GHz	–	–149.0	–146.9	–148.5	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–153.0	–151.3	–153.0	dBFS/Hz
		F_{IN} = 5.9 GHz	–	–147.0	–144.9	–147.0	dBFS/Hz
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–152.0	–150.5	–152.0	dBFS/Hz
	Noise spectral density with F_{REF} = 500 MHz,[3] measured with sampling clock generated from internal RF PLL and forwarded between tiles.	Input at –35 dBFS (noise floor)	–	–154.0	–	–154.0	dBFS/Hz
		F_{IN} = 240 MHz	–	–154.0	–151.0	–154.0	dBFS/Hz
		F_{IN} = 1.9 GHz	–	–151.0	–	–151.0	dBFS/Hz
		F_{IN} = 2.4 GHz	–	–150.0	–148.0	–150.0	dBFS/Hz
		F_{IN} = 3.5 GHz	–	–149.0	–146.0	–149.0	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–153.5	–150.0	–153.5	dBFS/Hz
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–155.0	–	–155.0	dBFS/Hz
		F_{IN} = 4.9 GHz	–	–147.0	–144.0	–147.0	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–153.0	–150.0	–153.0	dBFS/Hz
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–155.0	–	–155.0	dBFS/Hz
		F_{IN} = 5.9 GHz	–	–145.0	–142.0	–145.0	dBFS/Hz
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–152.0	–149.0	–152.0	dBFS/Hz
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–154.0	–	–155.0	dBFS/Hz
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion, and including OIS and GTIS spurs	F_{IN} = 240 MHz	70.0	84.0	–	84.0	dBc
		F_{IN} = 1.9 GHz	–	84.0	–	84.0	dBc
		F_{IN} = 2.4 GHz	–	83.5	–	83.5	dBc
		F_{IN} = 3.5 GHz	74.0	82.0	–	82.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	67.0	75.0	–	75.0	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	66.0	–	66.0	dBc
		F_{IN} = 4.9 GHz	71.0	80.0	–	72.0	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	67.0	75.0	–	75.0	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	65.0	–	65.0	dBc
		F_{IN} = 5.9 GHz	68.0	77.0	–	67.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS	68.0	75.0	–	74.5	dBc
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	65.0	–	65.0	dBc

Table 124: **RF-ADC Dual ADC Tile Performance Characteristics for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			10 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
HD2	Second-order harmonic distortion	F_{IN} = 240 MHz	–	–87.0	–	–85.0	dBc
		F_{IN} = 1.9 GHz	–	–71.0	–	–70.0	dBc
		F_{IN} = 2.4 GHz	–	–67.0	–	–65.0	dBc
		F_{IN} = 3.5 GHz	–	–59.0	–	–57.0	dBc
		F_{IN} = 3.5 GHz, CW at –2 dBFS	–	–60.0	–	–58.0	dBc
		F_{IN} = 3.5 GHz, CW at –3 dBFS	–	–62.0	–	–59.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–68.0	–	–66.0	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–77.0	–	–74.0	dBc
		F_{IN} = 4.9 GHz	–	–56.0	–	–52.0	dBc
		F_{IN} = 4.9 GHz, CW at –2 dBFS	–	–57.0	–	–53.0	dBc
		F_{IN} = 4.9 GHz, CW at –3 dBFS	–	–57.0	–	–54.0	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–65.0	–	–61.0	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–74.0	–	–71.0	dBc
		F_{IN} = 5.9 GHz	–	–52.0	–	–47.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–61.0	–	–56.0	dBc
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–71.0	–	–66.0	dBc
HD3	Third-order harmonic distortion	F_{IN} = 240 MHz	–	–77.0	–67.0	–76.0	dBc
		F_{IN} = 1.9 GHz	–	–65.0	–	–62.0	dBc
		F_{IN} = 2.4 GHz	–	–65.0	–	–62.0	dBc
		F_{IN} = 3.5 GHz	–	–71.0	–	–67.0	dBc
		F_{IN} = 3.5 GHz, CW at –2 dBFS	–	–73.0	–	–69.0	dBc
		F_{IN} = 3.5 GHz, CW at –3 dBFS	–	–76.0	–	–72.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS (E/I speed grade)	–	–85.0	–70.0	–84.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS (M speed grade)	–	–85.0	–60.0	–84.0	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–82.0	–	–81.0	dBc
		F_{IN} = 4.9 GHz	–	–69.0	–	–72.0	dBc
		F_{IN} = 4.9 GHz, CW at –2 dBFS	–	–70.0	–	–73.0	dBc
		F_{IN} = 4.9 GHz, CW at –3 dBFS	–	–72.0	–	–75.0	dBc
		F_{IN} = 4.9 GHz at –10 dBFS (E/I speed grade)	–	–83.0	–67.0	–82.0	dBc
		F_{IN} = 4.9 GHz at –10 dBFS (M speed grade)	–	–83.0	–60.0	–82.0	dBc
		F_{IN} = 4.9 GHz at –20 dBFS	–	–82.0	–	–83.0	dBc
		F_{IN} = 5.9 GHz	–	–58.0	–	–58.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS (E/I speed grade)	–	–75.0	–66.0	–75.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS (M speed grade)	–	–75.0	–60.0	–75.0	dBc
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–81.0	–	–81.0	dBc

Table 124: **RF-ADC Dual ADC Tile Performance Characteristics for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			10 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
IM3	Two–tone (F_1, F_2) third-order inter-modulation distortion	F_{IN} = 240 MHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–80.0	–72.0	–72.0	dBc
		F_{IN} = 1.9 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–75.0	–	–72.0	dBc
		F_{IN} = 2.4 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–75.0	–	–69.0	dBc
		F_{IN} = 3.5 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–72.0	–64.0	–71.0	dBc
		F_{IN} = 3.5 GHz center frequency, F_1, F_2 at –9 dBFS and 20 MHz delta	–	–76.0	–	–76.0	dBc
		F_{IN} = 3.5 GHz center frequency, F_1, F_2 at –16 dBFS and 20 MHz delta (E/I speed grade)	–	–81.0	–68.0	–80.0	dBc
		F_{IN} = 3.5 GHz center frequency, F_1, F_2 at –16 dBFS and 20 MHz delta (M speed grade)	–	–81.0	–62.0	–80.0	dBc
		F_{IN} = 3.5 GHz center frequency, F_1, F_2 at –26 dBFS and 20 MHz delta	–	–75.0	–	–75.0	dBc
		F_{IN} = 4.9 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–66.0	–59.0	–60.0	dBc
		F_{IN} = 4.9 GHz center frequency, F_1, F_2 at –16 dBFS and 20 MHz delta (E/I speed grade)	–	–79.0	–68.0	–79.0	dBc
		F_{IN} = 4.9 GHz center frequency, F_1, F_2 at –16 dBFS and 20 MHz delta (M speed grade)	–	–79.0	–62.0	–79.0	dBc
		F_{IN} = 4.9 GHz center frequency, F_1, F_2 at –26 dBFS and 20 MHz delta	–	–74.0	–	–75.0	dBc
		F_{IN} = 5.9 GHz center frequency, F_1, F_2 at –7 dBFS and 20 MHz delta	–	–62.0	–	–60.0	dBc
		F_{IN} = 5.9 GHz center frequency, F_1, F_2 at –16 dBFS and 20 MHz delta (E/I speed grade)	–	–78.0	–70.0	–78.0	dBc
		F_{IN} = 5.9 GHz center frequency, F_1, F_2 at –16 dBFS and 20 MHz delta (M speed grade)	–	–78.0	–65.0	–78.0	dBc
		F_{IN} = 5.9 GHz center frequency, F_1, F_2 at –26 dBFS and 20 MHz delta	–	–75.0	–	–75.0	dBc

Table 124: **RF-ADC Dual ADC Tile Performance Characteristics for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions	RF-DSA Attenuation				Units
			0 dB			10 dB	
			Min	Typ[1, 2]	Max	Typ[1, 2]	
GTIS	Gain/time interleaving spur at K * $F_S/N \pm F_{IN}$, where N = 8 and K = 0, 1, 2, ... N	F_{IN} = 240 MHz	–	–92.0	–80.0	–92.0	dBc
		F_{IN} = 1.9 GHz	–	–88.0	–	–88.0	dBc
		F_{IN} = 2.4 GHz	–	–87.0	–	–87.0	dBc
		F_{IN} = 3.5 GHz	–	–84.0	–75.0	–84.0	dBc
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–83.0	–75.0	–83.0	dBc
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–76.0	–	–76.0	dBc
		F_{IN} = 4.9 GHz	–	–81.0	–	–79.0	dBc
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–79.0	–72.0	–79.0	dBc
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–76.0	–	–76.0	dBc
		F_{IN} = 5.9 GHz	–	–78.0	–	–78.0	dBc
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–78.0	–70.0	–78.0	dBc
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–75.0	–	–75.0	dBc
OIS	Offset interleaving spur at K * F_S/N, where N = 8 and K = 0, 1, 2, ... N	F_{IN} = 240 MHz	–	–86.0	–77.0	–86.0	dBFS
		F_{IN} = 1.9 GHz	–	–86.0	–	–86.0	dBFS
		F_{IN} = 2.4 GHz	–	–86.0	–	–86.0	dBFS
		F_{IN} = 3.5 GHz	–	–85.0	–76.0	–85.0	dBFS
		F_{IN} = 3.5 GHz, CW at –10 dBFS	–	–86.0	–76.0	–86.0	dBFS
		F_{IN} = 3.5 GHz, CW at –20 dBFS	–	–86.0	–	–86.0	dBFS
		F_{IN} = 4.9 GHz	–	–84.0	–75.0	–84.0	dBFS
		F_{IN} = 4.9 GHz, CW at –10 dBFS	–	–86.0	–76.0	–86.0	dBFS
		F_{IN} = 4.9 GHz, CW at –20 dBFS	–	–86.0	–	–86.0	dBFS
		F_{IN} = 5.9 GHz	–	–82.0	–72.0	–82.0	dBFS
		F_{IN} = 5.9 GHz, CW at –10 dBFS	–	–86.0	–76.0	–86.0	dBFS
		F_{IN} = 5.9 GHz, CW at –20 dBFS	–	–86.0	–	–86.0	dBFS

Notes:

1. RF-ADC sampling rate is 5.0 GS/s using external sampling clock and ADC analog inputs at –1 dBFS, unless otherwise noted in the test conditions. ADC calibration mode is set to AutoCal mode. The ADC tiles are characterized using the on-chip clock forwarding configuration from tile 2 (bank 226), except when mentioned in the parameter condition column.
2. Typical values are specified at nominal voltage, T_j = 40°C.
3. See *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for internal PLL information.

Integrated RF-DAC Block

RF-DAC Electrical Characteristics

Table 125: **RF-DAC Electrical Characteristics for ZU2xDR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog Outputs					
Resolution		14	–	–	Bits
Sample Rate		0.5	–	6.554	GS/s
Maximum Output Power	20 mA mode, V_{DAC_AVTT} = 2.5V, 100Ω termination	–	+1	–	dBm
	32 mA mode, V_{DAC_AVTT} = 3.0V, 100Ω termination	–	+5	–	dBm
Analog Bandwidth	Full power bandwidth (–3 dB)	–	4	–	GHz
On-die Termination	Single-ended on-die termination to external 2.5V/3V V_{DAC_AVTT}[3]	–	50	–	Ω
Crosstalk isolation between channels[4]	F_{OUT} = 240 MHz	–	–70	–	dBc
	F_{OUT} = 1.9 GHz	–	–70	–	dBc
	F_{OUT} = 2.4 GHz	–	–70	–	dBc
	F_{OUT} = 3.5 GHz	–	–70	–	dBc

Notes:

1. RF-DAC sampling rate is 6.554 GS/s using external sampling clock.
2. Typical values are specified at nominal voltage, T_j = 25°C.
3. Consult S parameter I/O files for further details on input characteristics.
4. Values represent two channel crosstalk worst-case values for any combination of channel selections.

Table 126: **RF-DAC Electrical Characteristics for ZU39DR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog Outputs					
Resolution		14	–	–	Bits
Sample Rate		0.5	–	6.554	GS/s
Maximum Output Power	20 mA mode, V_{DAC_AVTT} = 2.5V, 100Ω termination	–	+1	–	dBm
	32 mA mode, V_{DAC_AVTT} = 3.0V, 100Ω termination	–	4.5	–	dBm
Analog Bandwidth	Full power bandwidth (–3 dB)	–	5	–	GHz
Return Loss (R_L)[3]	Up to 4 GHz	–	–10	–	dB
	Up to 5 GHz	–	–8	–	dB
On-die Termination	Single-ended on-die termination to external 2.5V/3V V_{DAC_AVTT}	–	50	–	Ω
Crosstalk isolation between channels[4]	F_{OUT} = 240 MHz	–	–70	–	dBc
	F_{OUT} = 1.9 GHz	–	–70	–	dBc
	F_{OUT} = 2.4 GHz	–	–70	–	dBc
	F_{OUT} = 3.5 GHz	–	–70	–	dBc
	F_{OUT} = 4.2 GHz	–	–69	–	dBc
	F_{OUT} = 4.9 GHz	–	–67	–	dBc

Notes:

1. RF-DAC sampling rate is 6.554 GS/s using external sampling clock.
2. Typical values are specified at nominal voltage, T_j = 25°C.
3. This is the return loss of the worst case channel quoted from DC to a specified frequency point. Consult the S parameter I/O files for further details as input characteristics depend on differential I/O selection. The RL reference plan is closed to the BGA footprint, keeping two times the BGA pitch distance from ball contact to avoid micro-probing electromagnetic disturbance.
4. Values represent two channel crosstalk worst-case values for any combination of channel selections.

Table 127: **RF-DAC Electrical Characteristics for ZU4xDR Devices**

Parameter	Comments/Conditions[1]	Min	Typ[2]	Max	Units
Analog Outputs					
Resolution		14	–	–	Bits
Sample rate[3]	-2E, -2I, -2LI speed grade without clock forwarding	0.5	–	9.85	GS/s
	-2E, -2I, -2LI speed grade with clock forwarding	0.5	–	9.70	GS/s
	-1E, -1I, -1LI, -1M speed grade	0.5	–	8.92	GS/s
Maximum output power	V_{DAC_AVTT} = 3.0V, 100Ω termination, signal frequency <200 MHz	–18.5	–	6.5	dBm
Output current range	V_{DAC_AVTT} = 3.0V, 100Ω termination, signal frequency <200 MHz	2.25	–	40.5	mA
Variable output current step size		–	43.75	–	µA
Variable output power range Equivalent dynamic range from output current range[4]	At 240 MHz	24	–	–	dB
	At 3500 MHz	20	–	–	dB
	At 4900 MHz	18	–	–	dB
	At 5900 MHz	17	–	–	dB
Analog bandwidth	Full power bandwidth (–3 dB)[5]	–	6	–	GHz
Return loss (R_L)[5]	Up to 4 GHz	–	–12	–	dB
	Up to 6 GHz	–	–10	–	dB
On-die termination	Single-ended on-die termination to external 3V V_{DAC_AVTT}[5]	–	50	–	Ω
Crosstalk isolation between channels[6]	F_{OUT} = 0–4 GHz	–	–75	–	dBc
	F_{OUT} = 0–6 GHz	–	–70	–	dBc

Notes:

1. RF-DAC sampling rate is the highest rate using external sampling clock.
2. Typical values are specified at nominal voltage, T_j = 40°C.
3. Measured with DAC data-path mode equal to *DUC bypass*.
4. The variable output power effective dynamic range depends on the signal frequency that is shown in the equivalent dynamic range.
5. This is the return loss of the worst case channel quoted from DC to a specified frequency point. Consult the S parameter I/O files for further details as input characteristics depend on channel and package selection. The RL reference plan is closed to the BGA footprint, keeping two times the BGA pitch distance from ball contact to avoid micro-probing electromagnetic disturbance.
6. Values represent two channel crosstalk worst-case values for any combination of channel selections. This specification is only characterized on XCZU46DR-H1760.

RF-DAC Performance Characteristics

Table 128: **RF-DAC Performance Characteristics for ZU2xDR Devices–High Linearity Mode**

Symbol	Parameter	Comments/Conditions[1]		20 mA Mode			32 mA Mode			Units
				Min	Typ[2]	Max	Min	Typ[2]	Max	
ACLR	Adjacent channel leakage ratio	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–82	–78	–	–81	–76	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–80	–	–	–79	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–78	–	–	–76	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM PAR = 8.6 dB (by temperature range)	E or I	–	–72	–67	–	–68	–63.5	dBc
			M	–	–72	–66	–	–68	–62	dBc
	Adjacent channel leakage ratio using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–81	–	–	–79	–	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–69	–	–	–69	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–67	–	–	–67	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB		–	–66.5	–	–	–65	–	dBc
OOB[3]	Spurious out-of-band emissions	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–85	–	–	–79	–	dBm/MHz
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–84	–	–	–79	–	dBm/MHz
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–83	–	–	–79	–	dBm/MHz
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB		–	–81	–	–	–77	–	dBm/MHz

Table 128: **RF-DAC Performance Characteristics for ZU2xDR Devices–High Linearity Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
NSD	Noise spectral density averaged across the 1st Nyquist zone	F_{OUT} = 240 MHz CW at 0 dBFS	–	–158	–151	–	–149	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–157	–	–	–150	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–157	–	–	–149	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–163	–160	–	–158	–153	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–158	–	–	–150	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–157	–	–	–148	–	dBm/Hz
	Noise spectral density averaged across the 1st Nyquist zone using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_{OUT} = 240 MHz CW at 0 dBFS	–	–158	–	–	–148	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–157	–	–	–149	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–156	–	–	–149	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–162	–	–	–158	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–158	–	–	–149	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–157	–	–	–148	–	dBm/Hz
	Noise spectral density averaged across the 2nd Nyquist zone	F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–156	–150	–	–151	–	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–157	–154.6	–	–153	–	dBm/Hz
	Noise spectral density averaged across the 2nd Nyquist zone using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–155	–	–	–151	–	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–157	–	–	–152	–	dBm/Hz
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion and Fs/2	F_{OUT} = 240 MHz CW at 0 dBFS	80	84	–	83.5	88	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	84	–	–	83	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	82	–	–	78	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	63	72	–	65	74	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	71.5	77	–	72	79	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	78	–	–	79	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	76	–	–	77	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	63	69	–	64	72	–	dBc
		F_{OUT} = 2.4 GHz CW at –15 dBFS	–	68	–	–	70	–	dBc
		F_{OUT} = 3.5 GHz CW at –15 dBFS	–	63	–	–	70	–	dBc
HD2	Second-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–85	–	–	–81	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–77	–	–	–77	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–76	–	–	–74	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–59	–	–	–65	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–81	–	–	–85	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–75	–	–	–75	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–75	–	–	–74	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–59	–	–	–62	–	dBc

Table 128: **RF-DAC Performance Characteristics for ZU2xDR Devices–High Linearity Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
HD3	Third-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–86	–78	–	–79	–70	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–76	–	–	–73	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–71	–	–	–68	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–64	–57	–	–59	–53	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–84	–79	–	–86	–81	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–82	–	–	–73	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–75	–	–	–70	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–78	–72	–	–68	–68	dBc
		F_{OUT} = 2.4 GHz CW at –15 dBFS	–	–73	–	–	–67	–	dBc
		F_{OUT} = 3.5 GHz CW at –15 dBFS	–	–71	–	–	–67	–	dBc
IM3	Two-tone, third-order intermodulation distortion	F_{OUT} = 240 MHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–90	–86	–	–92	–80	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–78.5	–	–	–78	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–71	–	–	–69.5	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–68.5	–61	–	–62	–56	dBc
		F_{OUT} = 240 MHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–85	–80	–	–86	–77	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–82	–	–	–84	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–78.5	–	–	–80	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–78	–73	–	–82	–78	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–73	–	–	–77	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–73	–	–	–77	–	dBc

Notes:

1. RF-DAC sampling rate is 6.4 GS/s using external sampling clock, DAC in mixed-mode for F_{OUT} > 3.2 GHz.
2. Typical values are specified at nominal voltage, T_j = 25°C.
3. Excludes HD2, HD3.

Table 129: **RF-DAC Performance Characteristics for ZU39DR Devices–High Linearity Mode**

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
ACLR	Adjacent channel leakage ratio	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–82	–78	–	–81	–76	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–80	–	–	–79	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–78	–	–	–76	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM PAR = 8.6 dB	–	–72	–67	–	–68	–63.5	dBc
		F_C = 4.2 GHz, single 18 MHz 16QAM PAR = 8.6 dB	–	–70.3	–	–	–71	–	dBc
		F_C = 4.9 GHz, single 18 MHz 16QAM PAR = 8.6 dB	–	–69.5	–	–	–70.2	–	dBc
	Adjacent channel leakage ratio using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–81	–	–	–79	–	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–69	–	–	–69	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–67	–	–	–67	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–66.5	–	–	–65	–	dBc
		F_C = 4.2 GHz, single 18 MHz 16QAM PAR = 8.6 dB	–	–65.8	–	–	–65.5	–	dBc
		F_C = 4.9 GHz, single 18 MHz 16QAM PAR = 8.6 dB	–	–64.4	–	–	–64.3	–	dBc
OOB[3]	Spurious out-of-band emissions	F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–84	–	–	–79	–	dBm/MHz
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–83	–	–	–79	–	dBm/MHz
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–81	–	–	–77	–	dBm/MHz
		F_C = 4.2 GHz, single 18 MHz 16QAM PAR = 8.6 dB	–	–81	–	–	–77	–	dBm/MHz
		F_C = 4.9 GHz, single 18 MHz 16QAM PAR = 8.6 dB	–	–81	–	–	–76.4	–	dBm/MHz

Table 129: **RF-DAC Performance Characteristics for ZU39DR Devices–High Linearity Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
NSD	Noise spectral density averaged across the 1st Nyquist zone	F_{OUT} = 240 MHz CW at 0 dBFS	–	–158	–151	–	–149	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–157	–	–	–150	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–157	–	–	–149	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–163	–160	–	–158	–153	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–158	–	–	–150	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–157	–	–	–148	–	dBm/Hz
	Noise spectral density averaged across the 1st Nyquist zone using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_{OUT} = 240 MHz CW at 0 dBFS	–	–158	–	–	–148	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–157	–	–	–149	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–156	–	–	–149	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–162	–	–	–158	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–158	–	–	–149	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–157	–	–	–148	–	dBm/Hz
	Noise spectral density averaged across the 2nd Nyquist zone	F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–156	–150	–	–151	–	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–157	–154.6	–	–153	–	dBm/Hz
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	–156	–	–	–151	–	dBm/Hz
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	–157	–	–	–153		dBm/Hz
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	–156	–	–	–151	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	–157	–	–	–153	–	dBm/Hz
	Noise spectral density averaged across the 2nd Nyquist zone using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–155	–	–	–151	–	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–157	–	–	–152	–	dBm/Hz
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	–155	–	–	–151	–	dBm/Hz
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	–157	–	–	–152	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	–155	–	–	–151	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	–157	–	–	–152	–	dBm/Hz
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion and Fs/2	F_{OUT} = 240 MHz CW at 0 dBFS	80	84	–	83.5	88	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	84	–	–	83	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	82	–	–	78	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	63	72	–	65	74	–	dBc
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	76.4	–	–	79.2	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	74.6	–	–	78	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	71.5	77	–	72	79	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	78	–	–	79	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	76	–	–	77	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	63	69	–	64	72	–	dBc
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	69.4	–	–	73.4	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	69.3	–	–	71.5	–	dBc
		F_{OUT} = 2.4 GHz CW at –15 dBFS	–	68	–	–	70	–	dBc
		F_{OUT} = 3.5 GHz CW at –15 dBFS	–	63	–	–	70	–	dBc
		F_{OUT} = 4.2 GHz CW at –15 dBFS	–	63.9	–	–	68.1	–	dBc
		F_{OUT} = 4.9 GHz CW at –15 dBFS	–	60.6	–	–	64.6	–	dBc

Table 129: **RF-DAC Performance Characteristics for ZU39DR Devices–High Linearity Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
HD2	Second-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–85	–	–	–81	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–76	–	–	–74	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–59	–	–	–65	–	dBc
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	–64.3	–	–	–64.3	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	–67.5	–	–	–66	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–81	–	–	–85	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–75	–	–	–75	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–75	–	–	–74	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–59	–	–	–62	–	dBc
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	–66.6	–	–	–68.4	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	–71.3	–	–	–70.5	–	dBc
HD3	Third-order harmonic distortion	F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–76	–	–	–73	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–71	–	–	–68	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–64	–57	–	–59	–53	dBc
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	–63.2	–	–	–61.2	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	–62.4	–	–	–61.7	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–84	–79	–	–86	–81	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–82	–	–	–73	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–75	–	–	–70	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–78	–72	–	–68	–68	dBc
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	–76.3	–	–	–80	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	–73.7	–	–	–77	–	dBc
		F_{OUT} = 2.4 GHz CW at –15 dBFS	–	–73	–	–	–67	–	dBc
		F_{OUT} = 3.5 GHz CW at –15 dBFS	–	–71	–	–	–67	–	dBc
		F_{OUT} = 4.2 GHz CW at –15 dBFS	–	–68.6	–	–	–72.1	–	dBc
		F_{OUT} = 4.9 GHz CW at –15 dBFS	–	–64.5	–	–	–68.1	–	dBc

Table 129: **RF-DAC Performance Characteristics for ZU39DR Devices–High Linearity Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
IM3	Two-tone, third-order intermodulation distortion	F_{OUT} = 1.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–78.5	–	–	–78	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–71	–	–	–69.5	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–68.5	–61	–	–62	–56	dBc
		F_{OUT} = 4.2 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–74.7	–	–	–64.7	–	dBc
		F_{OUT} = 4.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–73.9	–	–	–66.4	–	dBc
		F_{OUT} = 240 MHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–85	–80	–	–86	–77	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–80.5	–	–	–84	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–78.5	–	–	–80	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–78	–73	–	–82	–78	dBc
		F_{OUT} = 4.2 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–74.7	–	–	–78.9	–	dBc
		F_{OUT} = 4.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–73.9	–	–	–78.1	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–73	–	–	–77	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–73	–	–	–77	–	dBc
		F_{OUT} = 4.2 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–67.3	–	–	–71.5	–	dBc
		F_{OUT} = 4.9 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–63.7	–	–	–68.6	–	dBc

Notes:

1. RF-DAC sampling rate is 6.4 GS/s using external sampling clock, DAC in mixed-mode for F_{OUT} > 3.2 GHz.
2. Typical values are specified at nominal voltage, T_j = 25°C.
3. Excludes HD2, HD3.

Table 130: **RF-DAC Performance Characteristics for ZU2xDR Devices–Low Noise Mode**

Symbol	Parameter	Comments/Conditions[1]		20 mA Mode			32 mA Mode			Units
				Min	Typ[2]	Max	Min	Typ[2]	Max	
ACLR	Adjacent channel leakage ratio	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB (by temperature range)	E or I	–	–83	–78	–	–81	–76	dBc
			M	–	–83	–77	–	–81	–76	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–79	–	–	–79	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–76	–	–	–78	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB		–	–71	–65	–	–70	–64	dBc
	Adjacent channel leakage ratio using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–81	–	–	–79	–	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–69	–	–	–69	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–67	–	–	–67	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB		–	–66	–	–	–65	–	dBc
OOB[3]	Spurious out-of-band emissions	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–84	–	–	–78	–	dBm/MHz
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–82	–	–	–77	–	dBm/MHz
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB		–	–81	–	–	–76	–	dBm/MHz
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB		–	–82	–	–	–77	–	dBm/MHz
NSD	Noise spectral density averaged across the 1st Nyquist zone	F_{OUT} = 240 MHz CW at 0 dBFS		–	–166	–163.5	–	–163	–160.5	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS		–	–162	–	–	–160	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS		–	–161	–	–	–159	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS		–	–165	–162.5	–	–165	–161.5	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS		–	–164	–	–	–163	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS		–	–164	–	–	–163	–	dBm/Hz
	Noise spectral density averaged across the 1st Nyquist zone using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_{OUT} = 240 MHz CW at 0 dBFS		–	–166	–	–	–165	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS		–	–161	–	–	–159	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS		–	–160	–	–	–158	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS		–	–165	–	–	–163	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS		–	–164	–	–	–162	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS		–	–163	–	–	–161	–	dBm/Hz
	Noise spectral density averaged across the 2nd Nyquist zone	F_{OUT} = 3.5 GHz CW at 0 dBFS		–	–158	–155.5	–	–156	–152.5	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS (by temperature range)	E or I	–	–159	–156.5	–	–159	–156	dBm/Hz
			M	–	–159	–156.5	–	–159	–155	dBm/Hz
	Noise spectral density averaged across the 2nd Nyquist zone using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_{OUT} = 3.5 GHz CW at 0 dBFS		–	–158	–	–	–156	–	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS		–	–159	–	–	–159	–	dBm/Hz

Table 130: **RF-DAC Performance Characteristics for ZU2xDR Devices–Low Noise Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion and Fs/2	F_{OUT} = 240 MHz CW at 0 dBFS	68.5	77	–	66	74	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	76	–	–	74	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	73	–	–	71	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	61	69	–	60	68.5	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	65	74	–	65	73	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	73	–	–	73	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	71	–	–	70	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	64	–	–	64.5	–	dBc
		F_{OUT} = 2.4 GHz CW at –15 dBFS	–	66	–	–	65	–	dBc
		F_{OUT} = 3.5 GHz CW at –15 dBFS	–	58	–	–	60	–	dBc
HD2	Second-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–71	–	–	–64	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–67	–	–	–63	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–67	–	–	–63	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–57	–	–	–56	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–75	–	–	–67	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–64	–	–	–61	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–64	–	–	–61	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–58	–	–	–57	–	dBc
HD3	Third-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–82	–69.5	–	–79	–64	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–75	–	–	–71	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–70	–	–	–63	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–62	–55	–	–59.5	–54	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–76	–62	–	–73	–60	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–73	–	–	–67	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–68	–	–	–62.5	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–66	–55	–	–63	–52	dBc
		F_{OUT} = 2.4 GHz CW at –15 dBFS	–	–67	–	–	–61	–	dBc
		F_{OUT} = 3.5 GHz CW at –15 dBFS	–	–63	–	–	–61	–	dBc

Table 130: **RF-DAC Performance Characteristics for ZU2xDR Devices–Low Noise Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
IM3	Two-tone, third-order intermodulation distortion	F_{OUT} = 240 MHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–84	–69	–	–82	–67	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–79	–	–	–77	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–73	–	–	–76	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–68	–60	–	–63	–56	dBc
		F_{OUT} = 240 MHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–79	–65	–	–72	–62	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–70	–	–	–69	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–67	–	–	–67	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–67	–57	–	–67	–56	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–70	–	–	–70	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–69	–	–	–65	–	dBc

Notes:

1. RF-DAC sampling rate is 6.4 GS/s using external sampling clock, DAC in mixed-mode for F_{OUT} > 3.2 GHz.
2. Typical values are specified at nominal voltage, T_j =25°C.
3. Excludes HD2, HD3.

Table 131: **RF-DAC Performance Characteristics for ZU39DR Devices–Low Noise Mode**

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
ACLR	Adjacent channel leakage ratio	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–83	–78	–	–81	–76	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–79	–	–	–79	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–76	–	–	–78	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–71	–65	–	–70	–64	dBc
		F_C = 4.2 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–70.1	–	–	–71	–	dBc
		F_C = 4.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–69	–	–	–70.7	–	dBc
	Adjacent channel leakage ratio using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–81	–	–	–79	–	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–69	–	–	–69	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–67	–	–	–67	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–66	–	–	–65	–	dBc
		F_C = 4.2 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–65.4	–	–	–65.4	–	dBc
		F_C = 4.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–64.3	–	–	–64.4	–	dBc
OOB[3]	Spurious out-of-band emissions	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–84	–	–	–78	–	dBm/MHz
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–82	–	–	–77	–	dBm/MHz
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–81	–	–	–76	–	dBm/MHz
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–82	–	–	–77	–	dBm/MHz
		F_C = 4.2 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–82	–	–	–77	–	dBm/MHz
		F_C = 4.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–82	–	–	–77	–	dBm/MHz

Table 131: **RF-DAC Performance Characteristics for ZU39DR Devices–Low Noise Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
NSD	Noise spectral density averaged across the 1st Nyquist zone	F_{OUT} = 240 MHz CW at 0 dBFS	–	–166	–163.5	–	–163	–160.5	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–162	–	–	–160	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–161	–	–	–159	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–165	–162.5	–	–165	–161.5	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–164	–	–	–163	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–164	–	–	–163	–	dBm/Hz
	Noise spectral density averaged across the 1st Nyquist zone using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_{OUT} = 240 MHz CW at 0 dBFS	–	–166	–	–	–165	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–161	–	–	–159	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–160	–	–	–158	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–165	–	–	–163	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–164	–	–	–162	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–163	–	–	–161	–	dBm/Hz
	Noise spectral density averaged across the 2nd Nyquist zone	F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–158	–155.5	–	–156	–152.5	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–159	–156.5	–	–159	–156	dBm/Hz
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	–158	–	–	–156	–	dBm/Hz
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	–159	–	–	–159	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	–158	–	–	–156	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	–159	–	–	–159	–	dBm/Hz
	Noise spectral density averaged across the 2nd Nyquist zone using internal PLL to sample RF-DAC with F_{REF} = 256 MHz	F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–158	–	–	–156	–	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–159	–	–	–159	–	dBm/Hz
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	–158	–	–	–156	–	dBm/Hz
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	–159	–	–	–159	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	–158	–	–	–156	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	–159	–	–	–159	–	dBm/Hz
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion and Fs/2	F_{OUT} = 240 MHz CW at 0 dBFS	68.5	77	–	66	74	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	76	–	–	74	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	73	–	–	71	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	61	69	–	60	68.5	–	dBc
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	70.6	–	–	70.4	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	70	–	–	69.2	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	65	74	–	65	73	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	73	–	–	73	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	71	–	–	70	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	64	–	–	64.5	–	dBc
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	64.5	–	–	63.2	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	64.1	–	–	64.2	–	dBc
		F_{OUT} = 2.4 GHz CW at –15 dBFS	–	66	–	–	65	–	dBc
		F_{OUT} = 3.5 GHz CW at –15 dBFS	–	58	–	–	60	–	dBc
		F_{OUT} = 4.2 GHz CW at –15 dBFS	–	62.5	–	–	63.8	–	dBc
		F_{OUT} = 4.9 GHz CW at –15 dBFS	–	58.9	–	–	60	–	dBc

Table 131: **RF-DAC Performance Characteristics for ZU39DR Devices–Low Noise Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
HD2	Second-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–71	–	–	–64	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–67	–	–	–63	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–67	–	–	–63	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–57	–	–	–56	–	dBc
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	–56.7	–	–	–54.7	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	–59.5	–	–	–56.1	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–64	–	–	–61	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–64	–	–	–58	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–58	–	–	–57	–	dBc
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	–59.1	–	–	–56.6	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	–63.7	–	–	–59.6	–	dBc
HD3	Third-order harmonic distortion	F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–75	–	–	–71	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–70	–	–	–63	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS	–	–62	–55	–	–59.5	–54	dBc
		F_{OUT} = 4.2 GHz CW at 0 dBFS	–	–62.8	–	–	–61.1	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS	–	–62.3	–	–	–61.6	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–76	–62	–	–73	–60	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–73	–	–	–67	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–68	–	–	–62.5	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS	–	–66	–55	–	–63	–52	dBc
		F_{OUT} = 4.2 GHz CW at –10 dBFS	–	–63	–	–	–61.7	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS	–	–62.9	–	–	–62.5	–	dBc
		F_{OUT} = 2.4 GHz CW at –15 dBFS	–	–67	–	–	–61	–	dBc
		F_{OUT} = 3.5 GHz CW at –15 dBFS	–	–63	–	–	–61	–	dBc
		F_{OUT} = 4.2 GHz CW at –15 dBFS	–	–67.8	–	–	–70.2	–	dBc
		F_{OUT} = 4.9 GHz CW at –15 dBFS	–	–62.8	–	–	–64.7	–	dBc

Table 131: **RF-DAC Performance Characteristics for ZU39DR Devices–Low Noise Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1]	20 mA Mode			32 mA Mode			Units
			Min	Typ[2]	Max	Min	Typ[2]	Max	
IM3	Two-tone, third-order intermodulation distortion	F_{OUT} = 240 MHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–84	–69	–	–82	–67	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–79	–	–	–77	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–73	–	–	–76	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–68	–60	–	–63	–56	dBc
		F_{OUT} = 4.2 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–69.3	–	–	–64.7	–	dBc
		F_{OUT} = 4.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–69.2	–	–	–65.5	–	dBc
		F_{OUT} = 240 MHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–79	–65	–	–72	–62	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–70	–	–	–69	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–67	–	–	–67	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–67	–57	–	–67	–56	dBc
		F_{OUT} = 4.2 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–65.9	–	–	–66.1	–	dBc
		F_{OUT} = 4.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–65	–	–	–65.1	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–70	–	–	–70	–	dBc
		F_{OUT} = 3.5 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–69	–	–	–65	–	dBc
		F_{OUT} = 4.2 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–66.4	–	–	–67.1	–	dBc
		F_{OUT} = 4.9 GHz F_1, F_2 at –21 dBFS, Δf = 20 MHz	–	–62.9	–	–	–64.8	–	dBc

Notes:

1. RF-DAC sampling rate is 6.4 GS/s using external sampling clock, DAC in mixed-mode for F_{OUT} > 3.2 GHz.
2. Typical values are specified at nominal voltage, T_j = 25°C.
3. Excludes HD2, HD3.

Table 132: **Main RF-DAC Performance Characteristics for ZU4xDR Devices–Low Noise Mode**

Symbol	Parameter	Comments/Conditions[1, 2]	6.4 mA			32 mA			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
ACLR	Adjacent channel leakage ratio measured with external sampling clock forwarded between tiles	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–81.1	–78.8	–	–81.1	–77	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–76.6	–	–	–77.6	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–75.1	–	–	–76.9	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 9 GS/s	–	–68.6	–65.2	–	–73.4	–67.3	dBc
		F_C = 4.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 8.5 GS/s	–	–66.5	–61.3	–	–69.2	–61.8	dBc
		F_C = 5.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–67.3	–	–	–69.6	–	dBc
	Adjacent channel leakage ratio with F_{REF} = 500 MHz[5] measured with sampling clock generated from internal RF PLL and forwarded between tiles	F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 9 GS/s	–	–66.1	–	–	–67.9	–	dBc
		F_C = 4.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, , F_S = 8.5 GS/s	–	–64.2	–	–	–64.9	–	dBc
		F_C = 5.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–63.2	–	–	–63.6	–	dBc
OOB[4]	Spurious out-of-band emissions	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–95.2	–	–	–80.4	–	dBm/MHz
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–93.2	–	–	–77.0	–	dBm/MHz
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–94.6	–	–	–78.5	–	dBm/MHz
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 9 GS/s	–	–95.3	–	–	–83.5	–	dBm/MHz
		F_C = 4.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 8.5 GS/s	–	–92.2	–	–	–83.4	–	dBm/MHz
		F_C = 5.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–91.2	–	–	–84.2	–	dBm/MHz

Table 132: **Main RF-DAC Performance Characteristics for ZU4xDR Devices–Low Noise Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1, 2]	6.4 mA			32 mA			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
NSD	Noise spectral density measured with external sampling clock forwarded between tiles	F_{OUT} = 240 MHz CW at 0 dBFS	–	–164.3	–163.9	–	165.6	–165	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–163.5	–	–	–158.2	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–163.4	–	–	–157.4	–	dBm/Hz
		F_{OUT}= 3.5 GHz at 0 dBFS, F_S = 9 GS/s	–	–163.2	–162.6	–	–155.8	–154.3	dBm/Hz
		F_{OUT} = 4.9 GHz at 0 dBFS, F_S = 8.5 GS/s	–	–160.8	–159.6	–	–154.5	–152.1	dBm/Hz
		F_{OUT} = 5.9 GHz at 0 dBFS	–	–160.2	–	–	–154.4	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–	–	–	–163.9	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–	–	–	–162.3	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–	–	–	–161.9	–	dBm/Hz
		F_{OUT}= 3.5 GHz at –10 dBFS, F_S = 9 GS/s	–	–	–	–	–161.6	–	dBm/Hz
		F_{OUT} = 4.9 GHz at –10 dBFS, F_S = 8.5 GS/s	–	–	–	–	–158.6	–	dBm/Hz
		F_{OUT} = 5.9 GHz at –10 dBFS	–	–	–	–	–156.9	–	dBm/Hz
	Noise spectral density with F_{REF} = 500 MHz[5] measured with sampling clock generated from internal RF PLL and forwarded between tiles	F_{OUT} = 240 MHz CW at 0 dBFS	–	–164.3	–163.9	–	–165.5	–164.1	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–163.4	–	–	–157.5	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–163.1	–	–	–156.1	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–	–	–	–163.9	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–	–	–	–162.1	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–	–	–	–161.5	–	dBm/Hz
		F_{OUT} = 3.5 GHz CW at 0 dBFS, F_S = 9 GS/s	–	–162.8	–	–	–154.4	–151.3	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS, F_S = 9 GS/s	–	–	–	–	–161	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at 0 dBFS, F_S = 8.5 GS/s	–	–160.2	–	–	–152.5	–148.6	dBm/Hz
		F_{OUT} = 4.9 GHz CW at –10 dBFS, F_S = 8.5 GS/s	–	–	–	–	–157.9	–	dBm/Hz
		F_{OUT} = 5.9 GHz CW at 0 dBFS	–	–159.7	–	–	–152.5	–	dBm/Hz
		F_{OUT} = 5.9 GHz CW at –10 dBFS	–	–	–	–	–156.5	–	dBm/Hz

Table 132: **Main RF-DAC Performance Characteristics for ZU4xDR Devices–Low Noise Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1, 2]	6.4 mA			32 mA			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion and Fs/2	F_{OUT} = 240 MHz CW at 0 dBFS	71.9	77.1	–	66.7	73.6	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS		73.1	–		70.0	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS		74.3	–		70.0	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS, F_S = 9 GS/s	64.7	72.0	–	62.7	70.0	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS, F_S = 8.5 GS/s		65.9	–		66.1	–	dBc
		F_{OUT} = 5.9 GHz CW at 0 dBFS		64.7	–		65.1	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–	–		72.6	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–	–		67.3	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–	–		69.2	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS, F_S = 9 GS/s	–	–	–	60.7	67.1	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS, F_S = 8.5 GS/s	–	–	–	56.9	64.0	–	dBc
		F_{OUT} = 5.9 GHz CW at –10 dBFS	–	–	–		62.9	–	dBc
HD2	Second-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–72.9	–	–	–62.8	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–61.1	–	–	–60.0	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–58.1	–	–	–59.3	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS, F_S = 9 GS/s	–	–63.7	–	–	–59.4	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS, F_S = 8.5 GS/s	–	–52.8	–	–	–53.1	–	dBc
		F_{OUT} = 5.9 GHz CW at 0 dBFS	–	–50.8	–	–	–50.7	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–		–	–	–62.6	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–		–	–	–59.8	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–		–	–	–59.5	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS, F_S = 9 GS/s	–		–	–	–58.6	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS, F_S = 8.5 GS/s	–		–	–	–52.7	–	dBc
		F_{OUT} = 5.9 GHz CW at –10 dBFS	–		–	–	–50.5	–	dBc

Table 132: **Main RF-DAC Performance Characteristics for ZU4xDR Devices–Low Noise Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1, 2]	6.4 mA			32 mA			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
HD3	Third-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–78.6	–68.9	–	–73.4	–68.1	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–71.0	–	–	–68.0	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–71.9	–	–	–71.8	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS, F_S = 9 GS/s	–	–69.4	–62.5	–	–60.2	–51.4	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS, F_S = 8.5 GS/s	–	–69.8	–60.5	–	–59.6	–51.4	dBc
		F_{OUT} = 5.9 GHz CW at 0 dBFS	–	–69.7	–	–	–60.0	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–	–	–	–73.1	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–	–	–	–67.2	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–	–	–	–65.4	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS, F_S = 9 GS/s	–	–	–	–	–60.4	–50.9	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS, F_S = 8.5 GS/s	–	–	–	–	–62.5	–50.8	dBc
		F_{OUT} = 5.9 GHz CW at –10 dBFS	–	–	–	–	–60.3	–	dBc

Table 132: **Main RF-DAC Performance Characteristics for ZU4xDR Devices–Low Noise Mode** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1, 2]	6.4 mA			32 mA			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
IM3	Two-tone, third-order inter-modulation distortion	F_{OUT} = 240 MHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–80.5	–70.6	–	–82.5	–73.5	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–74.2	–	–	–73.4	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–72.4	–	–	–73.3	–	dBc
		F_{OUT} = 3.5 GHz, F_S = 9 GS/s F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–69.3	–62.8	–	–72.6	–62.2	dBc
		F_{OUT} = 4.9 GHz, F_S = 8.5 GS/s F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–70.8	–63.5	–	–64.3	–55.3	dBc
		F_{OUT} = 5.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–70.7	–	–	–63.7	–	dBc
		F_{OUT} = 240 MHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–	–	–	–73.5	–	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–	–	–	–70.5	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–	–	–	–68.3	–	dBc
		F_{OUT} = 3.5 GHz, F_S = 9 GS/s F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–	–	–	–66.9	–57.4	dBc
		F_{OUT} = 4.9 GHz, F_S = 8.5 GS/s F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–	–	–	–66.6	–56.6	dBc
		F_{OUT} = 5.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–	–	–	–65.9	–	dBc

Notes:

1. RF-DAC sampling rate is 10 GS/s using an external sampling clock, except when specified. DAC configured in real mode, PAR is computed on the real digital waveform at the DAC input: 10*log10(max(dac_input^2)/mean(dac_input^2)). The PAR of the complex base-band version (relative to envelope) of the same signal is approximately 3 dB less.
2. The DAC tiles are characterized using the on-chip clock forwarding configuration from tile 1 (bank 229), except when mentioned in the parameter condition column.
3. Typical values are specified at nominal voltage, T_j = 40°C.
4. Excludes HD2, HD3.
5. See the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for internal PLL information.

Table 133: **RF-DAC Mode Performance Benchmark for ZU4xDR Devices**

Symbol	Parameter	Comments/Conditions[1, 2]	20 mA Low Noise Mode			20 mA High Linearity Mode			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
ACLR	Adjacent channel leakage ratio measured with external sampling clock forwarded between tiles	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–85.0	–80.7	–	–83.0	–77.7	dBc
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–79.4	–	–	–82.8	–	dBc
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–78.4	–	–	–81.4	–	dBc
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 9 GS/s	–	–73.6	–68.0	–	–74.2	–68.5	dBc
		F_C = 4.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 8.5 GS/s	–	–71.5	–66.0	–	–71.9	–68.5	dBc
		F_C = 5.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–71.5	–	–	–72.4	–	dBc
	Adjacent channel leakage ratio with F_{REF} = 500 MHz[5] measured with sampling clock generated from internal RF PLL and forwarded between tiles	F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 9 GS/s	–	–68.0	–	–	–68.2	–	dBc
		F_C = 4.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 8.5 GS/s	–	–65.8	–	–	–65.9	–	dBc
		F_C = 5.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–64.1	–	–	–64.3	–	dBc
OOB[4]	Spurious out-of-band emissions	F_C = 240 MHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–83.7	–	–	–83.7	–	dBm/MHz
		F_C = 1.9 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–85.1	–	–	–90.5	–	dBm/MHz
		F_C = 2.4 GHz, single 3.84 MHz QPSK, PAR = 7.6 dB	–	–85.6	–	–	–91.0	–	dBm/MHz
		F_C = 3.5 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 9 GS/s	–	–88.5	–	–	–91.3	–	dBm/MHz
		F_C = 4.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB, F_S = 8.5 GS/s	–	–88.7	–	–	–85.6	–	dBm/MHz
		F_C = 5.9 GHz, single 18 MHz 16QAM, PAR = 8.6 dB	–	–88.8	–	–	–85.4	–	dBm/MHz

Table 133: **RF-DAC Mode Performance Benchmark for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1, 2]	20 mA Low Noise Mode			20 mA High Linearity Mode			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
NSD	Noise spectral density measured with external sampling clock forwarded between tiles	F_{OUT} = 240 MHz CW at 0 dBFS	–	–164.4	–163.9	–	–158.4	–152	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–160.4	–	–	–157.5	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–159.9	–	–	–157.4	–	dBm/Hz
		F_{OUT}= 3.5 GHz at 0 dBFS, F_S = 9 GS/s	–	–158.8	–157.5	–	–155.6	–150.6	dBm/Hz
		F_{OUT} = 4.9 GHz at 0 dBFS, F_S = 8.5 GS/s	–	–157.3	–155.2	–	–156.1	–153.4	dBm/Hz
		F_{OUT} = 5.9 GHz at 0 dBFS	–	–157.0	–	–	–155.8	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–163.8	–	–	–161.2	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–163.0	–	–	–156.4	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–162.9	–	–	–155.3	–	dBm/Hz
		F_{OUT}= 3.5 GHz at –10 dBFS, F_S = 9 GS/s	–	–162.7	–	–	–153.9	–	dBm/Hz
		F_{OUT} = 4.9 GHz at –10 dBFS, F_S = 8.5 GS/s	–	–159.9	–	–	–158.1	–	dBm/Hz
		F_{OUT} = 5.9 GHz at –10 dBFS	–	–158.3	–	–	–156.8	–	dBm/Hz
	Noise spectral density with F_{REF} = 500 MHz[5] measured with sampling clock generated from internal RF PLL and forwarded between tiles	F_{OUT} = 240 MHz CW at 0 dBFS	–	–164.3	–163.7	–	–158.4	–152.0	dBm/Hz
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–159.9	–	–	–157.3	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–158.9	–	–	–156.8	–	dBm/Hz
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–163.8	–	–	–161.3	–	dBm/Hz
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–162.9	–	–	–156.5	–	dBm/Hz
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–162.6	–	–	–155.3	–	dBm/Hz
		F_{OUT} = 3.5 GHz CW at 0 dBFS, F_S = 9 GS/s	–	–157.6	–154.9	–	–155	–150.4	dBm/Hz
		F_{OUT} = 3.5 GHz CW at –10 dBFS, F_S = 9 GS/s	–	–162.4	–	–	–154	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at 0 dBFS, F_S = 8.5 GS/s	–	–155.6	–	–	–154.8	–	dBm/Hz
		F_{OUT} = 4.9 GHz CW at –10 dBFS, F_S = 8.5 GS/s	–	–159.6	–	–	–157.9	–	dBm/Hz
		F_{OUT} = 5.9 GHz CW at 0 dBFS	–	–155.5	–	–	–154.6	–	dBm/Hz
		F_{OUT} = 5.9 GHz CW at –10 dBFS	–	–158.1	–	–	–156.7	–	dBm/Hz

Table 133: **RF-DAC Mode Performance Benchmark for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1, 2]	20 mA Low Noise Mode			20 mA High Linearity Mode			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
SFDR	Spurious free dynamic range excluding second- and third-order harmonic distortion and Fs/2	F_{OUT} = 240 MHz CW at 0 dBFS	71.0	78.0	–	78.3	80.4	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	74.5	–	–	79.8	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	73.6	–	–	78.7	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS, F_S = 9 GS/s (E/I speed grade)	65.1	71.8	–	70.5	77.7	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS, F_S = 9 GS/s (M speed grade)	64.9	71.8	–	69.8	77.7	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS, F_S = 8.5 GS/s	61.2	68.0	–	65.7	73.8	–	dBc
		F_{OUT} = 5.9 GHz CW at 0 dBFS	–	66.9	–	–	72.3	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	73.5	–	–	79.4	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	70.8	–	–	78.1	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	70.0	–	–	77.7	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS, F_S = 9 GS/s (E/I speed grade)	60.9	66.8	–	71.6	75.9	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS, F_S = 9 GS/s (M speed grade)	60.6	66.8	–	67.0	75.9	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS, F_S = 8.5 GS/s	57.3	63.8	–	66.2	70.4	–	dBc
		F_{OUT} = 5.9 GHz CW at –10 dBFS	–	62.7	–	–	69.0	–	dBc
HD2	Second-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–71.8	–	–	–87.5	–	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–64.9	–	–	–77.5	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–63.0	–	–	–71.9	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS, F_S = 9 GS/s	–	–66.1	–	–	–74.1	–	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS, F_S = 8.5 GS/s	–	–55.9	–	–	–62.8	–	dBc
		F_{OUT} = 5.9 GHz CW at 0 dBFS	–	–53.1	–	–	–59.0	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–70.9	–	–	–87.4	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–64.0	–	–	–77.3	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–62.7	–	–	–70.6	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS, F_S = 9 GS/s	–	–63.3	–	–	–74.5	–	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS, F_S = 8.5 GS/s	–	–55.0	–	–	–62.5	–	dBc
		F_{OUT} = 5.9 GHz CW at –10 dBFS	–	–52.2	–	–	–58.6	–	dBc

Table 133: **RF-DAC Mode Performance Benchmark for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1, 2]	20 mA Low Noise Mode			20 mA High Linearity Mode			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
HD3	Third-order harmonic distortion	F_{OUT} = 240 MHz CW at 0 dBFS	–	–78.8	–69.7	–	–83.1	–79.8	dBc
		F_{OUT} = 1.9 GHz CW at 0 dBFS	–	–71.4	–	–	–71.9	–	dBc
		F_{OUT} = 2.4 GHz CW at 0 dBFS	–	–72.5	–	–	–74.2	–	dBc
		F_{OUT} = 3.5 GHz CW at 0 dBFS, F_S = 9 GS/s	–	–67.5	–58.6	–	–69.6	–59.5	dBc
		F_{OUT} = 4.9 GHz CW at 0 dBFS, F_S = 8.5 GS/s	–	–66.4	–57.5	–	–67.1	–61.8	dBc
		F_{OUT} = 5.9 GHz CW at 0 dBFS	–	–67.4	–	–	–68.2	–	dBc
		F_{OUT} = 240 MHz CW at –10 dBFS	–	–77.1	–	–	–87.7	–	dBc
		F_{OUT} = 1.9 GHz CW at –10 dBFS	–	–68.6	–	–	–84.2	–	dBc
		F_{OUT} = 2.4 GHz CW at –10 dBFS	–	–68.4	–	–	–84.8	–	dBc
		F_{OUT} = 3.5 GHz CW at –10 dBFS, F_S = 9 GS/s	–	–66.7	–56.4	–	–73.7	–65.1	dBc
		F_{OUT} = 4.9 GHz CW at –10 dBFS, F_S = 8.5 GS/s	–	–65.6	–53.4	–	–78.7	–74.8	dBc
		F_{OUT} = 5.9 GHz CW at –10 dBFS	–	–63.7	–	–	–78.0	–	dBc

Table 133: **RF-DAC Mode Performance Benchmark for ZU4xDR Devices** *(cont'd)*

Symbol	Parameter	Comments/Conditions[1, 2]	20 mA Low Noise Mode			20 mA High Linearity Mode			Units
			Min	Typ[3]	Max	Min	Typ[3]	Max	
IM3	Two-tone, third-order inter-modulation distortion	F_{OUT} = 240 MHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–83.3	–73.8	–	–89.3	–86.8	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–78.0	–	–	–86.4	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–76.6	–	–	–82.0	–	dBc
		F_{OUT} = 3.5 GHz, F_S = 9 GS/s F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–75.3	–66.8	–	–73.3	–63.5	dBc
		F_{OUT} = 4.9 GHz, F_S = 8.5 GS/s F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–72.3	–61.3	–	–71.0	–64.8	dBc
		F_{OUT} = 5.9 GHz F_1, F_2 at –6 dBFS, Δf = 20 MHz	–	–72	–	–	–70.7	–	dBc
		F_{OUT} = 240 MHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–80.6	–	–	–89.1	–	dBc
		F_{OUT} = 1.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–72.3	–	–	–82.0	–	dBc
		F_{OUT} = 2.4 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–69.7	–	–	–79.7	–	dBc
		F_{OUT} = 3.5 GHz, F_S = 9 GS/s F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–67.8	–57.7	–	–78.5	–75.1	dBc
		F_{OUT} = 4.9 GHz, F_S = 8.5 GS/s F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–66.9	–56.9	–	–73.3	–70.9	dBc
		F_{OUT} = 5.9 GHz F_1, F_2 at –16 dBFS, Δf = 20 MHz	–	–65.6	–	–	–73.2	–	dBc

Notes:

1. RF-DAC sampling rate is 10 GS/s using an external sampling clock, except when specified. PAR is defined by 10*log10(max(RF_signal^2) / mean(RF_signal^2)) .
2. The DAC tiles are characterized using the on-chip clock forwarding configuration from tile 1 (bank 229), except when mentioned in the parameter condition column.
3. Typical values are specified at nominal voltage, T_j = 40°C.
4. Excludes HD2, HD3.
5. See *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for internal PLL information.

RF Converters Clocking Characteristics

Table 134: **RF Converters Clocking Characteristics for ZU2xDR Devices**

Symbols	Parameter	Comments/Conditions	Min	Typ[1]	Max	Units
F_{IN}	Tile clock input frequency range	F_{REF} range restrictions apply when the PLL is used. The F_S range restriction applies when PLL is bypassed.	102.40625	–	6554	MHz
R[2]	Frequency input division ratio	Possible values are 1, 2, 3, 4 Only available when using internal PLL	1	1	1	
F_{REF}	Reference input frequency $F_{REF} = F_{IN}/R$	On-chip PLL activated	102.40625	–	615	MHz
F_S	Input sampling frequency	PLL bypassed, quad ADC tile configuration	500	–	2058	MHz
		PLL bypassed, dual ADC tile configuration	1000	–	4096	MHz
		PLL bypassed, DAC	500	–	6554	MHz
V_{IN}	Input clock range[3]	Into 100Ω differential, on-die termination	0.9	–	1.8	V_{PPD}
R_{ODT}	Input resistance	On-die differential termination[4]	95	100	110	Ω
α	Input duty cycle		48	–	52	%
F_{OUT}	F_{PLL} output	PLL output frequency range[5]	500	–	6554	MHz
Sync	Channel to channel synchronized delay skew	Using multi-tile synchronization (MTS) feature on a single device	–1	0	1	$1/F_S$
PN[6]	Phase noise[7]	Offset = 100 kHz	–	–127	–121.2	dBc/Hz
		Offset = 1 MHz	–	–130	–127.3	dBc/Hz
		Offset = 2.5 MHz	–	–136	–132.6	dBc/Hz
		Offset = 10 MHz	–	–146	–142.7	dBc/Hz
RS[8]	Reference spur		–	–70	–	dBc
RHS[8]	Reference harmonic spur	Offset from carrier <800 MHz	–	–70	–	dBc
		Offset from carrier >800 MHz	–	–80	–	dBc

Notes:

1. Typical values are specified at nominal voltage, T_j = 40°C.
2. Only R=1 is characterized.
3. Maximum input voltage peak-to-peak is $V_{ADC\_AVCCAUX}$. Only AC coupling mode is supported for this input.
4. See the S parameter file information for more details on input characteristics.
5. The internal PLL uses an integer reference divider (R), an integer feedback divider, and an integer output divider for enhanced oscillator performance on the output range.
6. Phase noise specification applies for a reference frequency of 245.760 MHz using a division ratio = 1 and sufficient jitter performance of the reference (equal or better than Crystek Microwave's CRBSCS-01-245.760).
7. Normalized to 1 GHz carrier.
8. Assuming same reference frequency is used in all RF-DACs/RF-ADCs. Reference spurs levels are normalized to 1 GHz carrier. Reference spurs are found at $F_{OUT} \pm N \times F_{REF}$, where N = 1 for RS and N is an integer greater than 1 for RHS.

Table 135: **RF Converters Clocking Characteristics for ZU39DR Devices**

Symbols	Parameter	Comments/Conditions	Min	Typ[1]	Max	Units
F_{IN}	Tile clock input frequency range	F_{REF} range restrictions apply when the PLL is used. The F_S range restriction applies when PLL is bypassed.	102.40625	–	6554	MHz
R[2]	Frequency input division ratio	Possible values are 1, 2, 3, 4 Only available when using internal PLL	1	1	1	

Table 135: **RF Converters Clocking Characteristics for ZU39DR Devices** *(cont'd)*

Symbols	Parameter	Comments/Conditions	Min	Typ[1]	Max	Units
F_{REF}	Reference input frequency $F_{REF} = F_{IN}/R$	On-chip PLL activated	102.40625	–	615	MHz
F_S	Input sampling frequency	PLL bypassed, quad ADC tile configuration	500	–	2220	MHz
		PLL bypassed, DAC	500	–	6554	MHz
V_{IN}	Input clock range[3]	Into 100Ω differential, on-die termination	0.9	–	1.8	V_{PPD}
α	Input duty cycle		48	–	52	%
F_{OUT}	F_{PLL} output	PLL output frequency range[4]	500	–	6554	MHz
Sync	Channel to channel synchronized delay skew	Using multi-tile synchronization (MTS) feature on a single device	–1	0	1	$1/F_S$
PN[5]	Phase noise[6]	Offset = 100 kHz	–	–127	–121.2	dBc/Hz
		Offset = 1 MHz	–	–130	–127.3	dBc/Hz
		Offset = 2.5 MHz	–	–136	–132.6	dBc/Hz
		Offset = 10 MHz	–	–146	–142.7	dBc/Hz
RS[7]	Reference spur		–	–70	–	dBc
RHS[7]	Reference harmonic spur	Offset from carrier <800 MHz	–	–70	–	dBc
		Offset from carrier >800 MHz	–	–80	–	dBc

Notes:

1. Typical values are specified at nominal voltage, T_j = 40°C.
2. Only R=1 is characterized.
3. Maximum input voltage peak-to-peak is $V_{ADC\_AVCCAUX}$. Only AC coupling mode is supported for this input.
4. The internal PLL uses an integer reference divider (R), an integer feedback divider, and an integer output divider for enhanced oscillator performance on the output range.
5. Phase noise specification applies for a reference frequency of 245.760 MHz using a division ratio = 1 and sufficient jitter performance of the reference (equal or better than Crystek Microwave's CRBSCS-01-245.760).
6. Normalized to 1 GHz carrier.
7. Assuming same reference frequency is used in all RF-DACs/RF-ADCs. Reference spurs levels are normalized to 1 GHz carrier. Reference spurs are found at $F_{OUT} \pm N \times F_{REF}$, where N = 1 for RS and N is an integer greater than 1 for RHS.

Table 136: **RF Converters Clocking Characteristics for ZU4xDR Devices**

Symbols	Parameter	Comments/Conditions	Min	Typ[1]	Max	Units
F_{IN}[2]	Tile clock input frequency range	F_{REF} range restrictions apply when the PLL is used. The F_S range restriction applies when PLL is bypassed.	102.40625	–	10000	MHz
R[3]	Frequency input division ratio	Possible values are 1, 2, 3, 4 Only available when using internal PLL	1	1	1	
F_{REF}	Reference input frequency $F_{REF} = F_{IN}/R$	On-chip PLL activated	102.40625	–	615	MHz
F_S	Input sampling frequency	PLL bypassed, quad ADC tile configuration	500	–	2500	MHz
		PLL bypassed, dual ADC tile configuration	500	–	5000	MHz
		PLL bypassed, DAC	500	–	10000	MHz
V_{IN}	Input clock range[4]	Into 100Ω differential, on-die termination	0.9	–	1.8	V_{PPD}
α	Input duty cycle		48	–	52	%
SR	Input clock slew rate		4	–	–	V/ns

Table 136: **RF Converters Clocking Characteristics for ZU4xDR Devices** *(cont'd)*

Symbols	Parameter	Comments/Conditions	Min	Typ[1]	Max	Units
F_{OUT}	F_{PLL} output	RF-ADC PLL output frequency range[5]	500	–	5000	MHz
		RF-DAC PLL output Low frequency range[5]	500	–	6882	MHz
		RF-DAC PLL output High frequency range[5]	7863	–	10000	MHz
Sync	Channel to channel synchronized delay skew	Using multi-tile synchronization (MTS) feature on a single device	–1	0	1	$1/F_S$
PN_ADC[6]	Phase noise for the RF-ADC[7]	Offset = 100 kHz	–	–127.0	–124.1	dBc/Hz
		Offset = 1 MHz	–	–130.7	–128.1	dBc/Hz
		Offset = 2.5 MHz	–	–136.0	–135.3	dBc/Hz
		Offset = 10 MHz	–	–148.1	–143.2	dBc/Hz
PN_DAC[6]	Phase noise for the RF-DAC[7]	Offset = 100 kHz	–	–126.0	–121.7	dBc/Hz
		Offset = 1 MHz	–	–130.7	–128.0	dBc/Hz
		Offset = 2.5 MHz	–	–135.8	–135.3	dBc/Hz
		Offset = 10 MHz	–	–147.3	–144.2	dBc/Hz
RS[8]	Reference spur		–	–70	–	dBc
RHS[8]	Reference harmonic spur	Offset from carrier <800 MHz	–	–70	–	dBc
		Offset from carrier >800 MHz	–	–80	–	dBc

Notes:

1. Typical values are specified at nominal voltage, T_j = 40°C.
2. External full-rate clocking assumes best case achievable P to N skew from an external clock source. Consult the *UltraScale Architecture PCB Design User Guide* (UG583) for information on the impact of DAC maximum sample rate and external clocking skew imbalance.
3. Only R=1 is characterized.
4. Maximum input voltage peak-to-peak of $V_{RFDC\_CLK\_IN}$ is equal to $V_{ADC\_AVCCAUX}$. Only AC coupling mode is supported for this input.
5. The internal PLL uses an integer reference divider (R), an integer feedback divider, and an integer output divider for enhanced oscillator performance on the output range. The internal PLL does not supply a carrier between the Low and High frequency range of the DAC tile.
6. Phase noise specification applies for a reference frequency of 245.760 MHz using a division ratio = 1 and sufficient jitter performance of the reference (equal or better than the Rohde and Schwarz SMB100A: RF continuous wave generator).
7. Normalized to 1 GHz carrier.
8. Assuming same reference frequency is used in all RF-DACs/RF-ADCs. Reference spurs levels are normalized to 1 GHz carrier. Reference spurs are found at $F_{OUT} \pm N \times F_{REF}$, where N = 1 for RS and N is an integer greater than 1 for RHS. The specification is derated by 3 dB when distributing a reference frequency to multiple PLLs.

Table 137: **Analog_SYSREF Clocking Characteristics**

Symbol	Parameter	Comments/Conditions	Min	Typ	Max	Units
V_{IN}	Input range	Into 100Ω differential, on-die termination	0.4	–	3.6	V_{PPD}
Jitter	SYSREF jitter	RMS jitter from 100 Hz to 20 MHz	–	–	1	ps
F_{SYSREF}	SYSREF frequency		0.4	–	10	MHz
Slew rate	Input clock slew rate	20% to 80%	2	–	–	V/ns
Pulse width	Input clock pulse width		50	–	–	ns
DC Coupling Input Parameters						
V_{IH}	Input High		0.2	–	1.8	V
V_{CM}	Common mode		0.1	–	1.7	V
V_{IL}	Input Low		0	–	1.6	V

SD-FEC Integrated Block

The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists the Zynq UltraScale+ RFSoCs that include the SD-FEC integrated block.

Table 138: **SD-FEC Clock Frequencies**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
$F_{CORECLKMAX}$	Maximum core frequency	667	667	667	667	MHz
$F_{INTERFACECLKMAX}$	Maximum interface clock frequency	400	400	400	400	MHz

PL System Monitor Specifications

Table 139: **PL SYSMON Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy[1]						
Resolution			10	–	–	Bits
Integral nonlinearity[2]	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity[2]	INL	T_j = –55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic T_j = –55°C to 125°C	–	–	±1	
Analog Inputs[2]						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
On-Chip Sensor Accuracy						
Temperature sensor error[1, 3]		T_j = –55°C to 125°C (with external REF)	–	–	±3	°C
		T_j = –55°C to 110°C (with internal REF)	–	–	±3.5	°C
		T_j = 110°C to 125°C (with internal REF)	–	–	±5	°C

Table 139: **PL SYSMON Specifications** *(cont'd)*

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Supply sensor error[4]		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with external REF)	–	–	±0.5	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –40°C to 100°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –55°C to 125°C (with external REF)	–	–	±2.0	%
		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with internal REF)	–	–	±1.0	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with internal REF)	–	–	±2.0	%
		All other supply voltages, T_j = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		All other supply voltages, T_j = –55°C to 125°C (with internal REF)	–	–	±2.5	%
Conversion Rate[5]						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference[6]						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the Analog Input section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a +4°C offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of ±3°C becomes +1°C to +7°C when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the Adjusting the Acquisition Settling Time section in the *UltraScale Architecture System Monitor User Guide* (UG580).
6. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

PL SYSMON I2C/PMBus Interfaces

Table 140: **PL SYSMON I2C Fast Mode Interface Switching Characteristics**

Symbol	Description[1]	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	µs
T_{SMFCKH}	SCL High time	0.6	–	µs
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 141: **PL SYSMON I2C Standard Mode Interface Switching Characteristics**

Symbol	Description[1]	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	µs
T_{SMSCKH}	SCL High time	4.0	–	µs
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Configuration Switching Characteristics

Table 142: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.85V		0.72V		
		-2	-1	-2	-1	
PL Power-up Timing Characteristics						
T_{PL}	PS_PROG_B PL latency	7.5	7.5	7.5	7.5	ms, Max
T_{POR}[1, 2]	Power-on reset from PL power-on to PL ready to configure (40 ms ramp rate time)	65	65	65	65	ms, Max
		0	0	0	0	ms, Min
	Power-on reset from PL power-on to PL ready to configure with POR override (2 ms ramp rate time)	15	15	15	15	ms, Max
		5	5	5	5	ms, Min
$T_{PS\_PROG\_B}$	PL program pulse width	250	250	250	250	ns, Min
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE3)	200	200	150	150	MHz, Max
DNA Port Switching						
F_{DNACK}	DNA port frequency (DNA_PORT)	200	200	175	175	MHz, Max
STARTUPE3 Ports						
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency	50.00	50.00	50.00	50.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance	±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted	4	4	4	4	ms, Max

Notes:

1. The T_{POR} specification begins when the last of the monitored supplies (V_{CCINT}, V_{CCAUX}, V_{CCBRAM}) reaches 95% of its recommended operating condition voltage.
2. The POR override (POR_OVERRIDE pin tied to V_{CCINT}) is applicable only when the monitored supplies ramp within the specified time.

Revision History

Date	Version	Description of Revisions
4/06/2021	1.8	Added package skews for the XQZU4xDR devices in Table 96. Added DAC maximum sample rate specification with clock forwarding feature to -2 device in Table 127. Updated Note 4 in Table 136.
4/01/2021	1.7	Added the production released XQZU48DR and XQZU49DR to Table 25, Table 26, and Table 27 in Vivado Design Suite 2020.2.2 v1.32, and where applicable in other sections of this data sheet. Decreased the 0 dB maximum attenuation in Table 120, Table 123, and the NSD averaged across the first nyquist zone in Table 121, and Table 124. Added E/I and M speed grade rows to HD3 and IM3 in Table 124. Added E/I and M speed grade rows to SFDR in Table 133. Reduced the maximum sample rate in RF-DAC Electrical Characteristics.
12/04/2020	1.6	Added the production released XCZU43DR, XCZU46DR, XCZU47DR, XCZU48DR, and XCZU49DR devices to Table 25, Table 26, and Table 27 in Vivado Design Suite 2020.2 v1.30, and where applicable in other sections of this data sheet. Revised the Summary to include specific voltages by device. Updated the symbol name $V_{RFDC\_CLK\_IN}$ in Absolute Maximum Ratings. Added Note 7 to Table 15. Added Note 10 to Table 17. Revised symbol and description of IOPLL_TO_FPD maximum frequency in Table 38. To specify that the PS-GTR for PCI Express is only supported by the common clock architecture, added Note 1 to Table 60. Added the capability for XC devices designing with Vivado Design Suite v2019.1.1 or later to increase the performance of the MIPI PHY transmitter/receiver in Table 72. Updated Note 1 in Table 94 Added the RF-ADC/RF-DAC to PL Interface Switching Characteristics section. Increased the maximum line rate of the QPLL0 -1 (V_{CCINT} = 0.85V) output divider 1 in Table 100 and updated Notes 2 and 3. Reorganized the Integrated RF-ADC Block and Integrated RF-DAC Block sections and the notes where the typical values are now specified at 40°C. Updated the typical *Return Loss* conditions and notes in each section. In the RF-ADC Electrical Characteristics section, Table 117, updated the common mode voltage descriptions. Clarified the meaning of all of the OIS parameter descriptions in the RF-ADC Performance Characteristics section. Updated the sampling rate Note 1 and revised the sample F_{REF} to 250 MHz in Table 118, Table 119, and Table 122. Added Table 137: Analog_SYSREF Clocking Characteristics.
6/05/2019	1.5	Production released the XCZU39DR device in -2I (V_{CCINT} = 0.85V) and -2LI (V_{CCINT} = 0.72V) speed/temperature grades throughout the data sheet for Vivado Design Suite 2019.1 v1.23 In the Integrated Interface Block for Interlaken section, removed package-specific limitation.
4/09/2019	1.4	Added the production released XQZU21DR and XQZU29DR devices in the -2I, -1I, -1M, and -1LI speed/temperature grades to Table 25, Table 26, and Table 27 in Vivado Design Suite 2018.3 or 2018.3.1 v1.23. This version also adds the ruggedized FFRD1156 and FFRF1760 packages to support the XQZU21DR and XQZU29DR. Updated Table 25 to Vivado Design Suite 2018.3.1 v1.23. Add the XQZU21DR and XQZU29DR devices to Table 9, Table 10, Table 88, Table 89, Table 90, Table 92, Table 93, and Table 96. Updated Note 1 in Table 35. Added LVDS component mode notes to Programmable Logic (PL) Performance Characteristics.

Date	Version	Description of Revisions
1/04/2019	1.3	Added the production released XQZU28DR device in the -2I, -1I, -1M, and -1LI speed/temperature grades to Table 25, Table 26, and Table 27 in Vivado Design Suite 2018.3 v1.23. Added military grade T_j to Table 2 and -1M to Table 3. Add the XQZU28DR devices to Table 9, Table 10, Table 88, Table 89, Table 90, Table 92, Table 93, and Table 96. Added the FFRE1156 and FFRG1517 packages to Table 1 and the Integrated Interface Block for Interlaken section. Updated Note 20 in Table 2. Updated Note 3 in Table 6, Table 7, Table 8. Updated the V_{IDIFF} description in Table 24. Revised minimum PS DDR data rates for all I-grade devices in Table 30. In Table 69, revised the Supply Sensor Error T_j conditions to –55°C. Updated the speed grade notes in Table 105. In Table 112, removed Note 1. Removed PCI Express Gen4 support in Table 113: Maximum Performance for PCIE4-based PCI Express Designs for ZU2xDR and ZU39DR Devices and Note 1, Note 2, and Note 3. In Table 118, added M-grade NSD F_{IN} = 3.5 GHz, the HD3 F_{IN} = 2.4 GHz, and IM3 F_{IN} = 3.5 GHz, F1, F2 at –7 dBFS and 20 MHz delta. In Table 128, added M-grade ACLR F_C = 3.5 GHz. In Table 130, added M-grade ACLR F_C = 240 MHz, and NSD F_{OUT} = 3.5 GHz CW at –10 dBFS. Added the MTS sync specification to Table 134.
8/01/2018	1.2	Added Note 20 to Table 2. Where applicable, added the -2LI (V_{CCINT} = 0.72V) speed/temperature grade specifications throughout this data sheet. Updated Table 25, Table 26, and Table 27 to production for the following devices/speed/temperature grades in Vivado Design Suite 2018.2.1 v1.21. XCZU21DR: -1LI (V_{CCINT} = 0.85V), and -2LI, -1LI (V_{CCINT} = 0.72V) XCZU25DR: -1LI (V_{CCINT} = 0.85V), and -2LI, -1LI (V_{CCINT} = 0.72V) XCZU27DR: -1LI (V_{CCINT} = 0.85V), and -2LI, -1LI (V_{CCINT} = 0.72V) XCZU28DR: -1LI (V_{CCINT} = 0.85V), and -2LI, -1LI (V_{CCINT} = 0.72V) XCZU29DR: -1LI (V_{CCINT} = 0.85V), and -2LI, -1LI (V_{CCINT} = 0.72V) In Table 11, added RF-DAC, RF-ADC, and SD-FEC power supply values. Added the -2LI specific values to Table 71 and added Note 4 to the LVDS RX DDR maximum data. Added -2LI specific values to Table 74, Table 80, Table 81, and Table 83. In Table 105 added Note 4. In Table 110, added -2LI. In Table 112, revised the calculated values from 322.223 to 322.266. Added Note 1. Edited Note 2 in Table 113. In Table 134, clarified the parameter description of F_{IN}, revised the maximum ratio of R and added Note 2, updated the minimum PLL output frequency range to 500 MHz, and revised Note 6. In Table 142, added Notes 1 and 2.

Date	Version	Description of Revisions
6/18/2018	1.1	Updated the RF-ADC, RF-DAC, and SD-FEC section in Absolute Maximum Ratings including adding V_{IN} and V_{ADC_IN}. Revised Note 14 in Table 2. Added ADC_R_{EXT} and DAC_R_{EXT} to DC Characteristics Over Recommended Operating Conditions. In Table 2, clarified the V_{CCO_PSIO} descriptions. Added the RF-DAC/RF-ADC power supply sequencing information to the PL Power-On/Off Power Supply Sequencing section. Updated Table 25, Table 26, and Table 27 to production for the following devices/speed/temperature grades in Vivado Design Suite 2018.2 v1.20. XCZU21DR: -2E, -2I, -2LE, -1E, -1I (V_{CCINT} = 0.85V), and -2LE (V_{CCINT} = 0.72V) XCZU25DR: -2E, -2I, -2LE, -1E, -1I (V_{CCINT} = 0.85V), and -2LE (V_{CCINT} = 0.72V) XCZU27DR: -2E, -2I, -2LE, -1E, -1I (V_{CCINT} = 0.85V), and -2LE (V_{CCINT} = 0.72V) XCZU28DR: -2E, -2I, -2LE, -1E, -1I (V_{CCINT} = 0.85V), and -2LE (V_{CCINT} = 0.72V) XCZU29DR: -2E, -2I, -2LE, -1E, -1I (V_{CCINT} = 0.85V), and -2LE (V_{CCINT} = 0.72V) Added Table 87. Updated the specifications in Table 88, Table 89, Table 90, Table 92, and Table 93. Added package skew data to Table 96. Revised the speed grade -1 (V_{CCINT} = 0.85) F_{GTYMAX} in Table 100, which also revised values in Table 105 and added Note 7. Revised and added data to Table 115, Table 118, Table 122, Table 128, Table 130, and Table 134. In Table 134, revised Note 7.
4/09/2018	1.0	Initial Xilinx release.

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