Zynq-7000 SoC
ZC706 Evaluation Kit

Getting Started Guide

UG961 (v6.0.2) July 1, 2018

This document applies to the following software versions: Vivado Design Suite 2014.3, 2014.4, and 2015.4.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/19/2012	1.0	Initial Xilinx release.
01/23/2013	2.0	Updated for ISE® Design Suite 14.4. **Chapter 1:** The ZC706 evaluation kit is based on the Zynq®-7000 XC7Z045-2FFG900C SoC. For additional information, see the Zynq-7000 SoC Overview datasheet (DS190) [Ref 1]., page 6 removed "Note: Users of the new Intel® Ivy Bridge . . ." Figure 1-1, the kit photograph, was replaced. In section ZC706 Evaluation Kit Contents, page 7, added this bullet on page 7: "ATX adapter cable, Xilinx part number 2600304." The *Key Features* section was removed, because features are listed in *ZC706 Evaluation Board for the Zynq-7000 XC7Z045 SoC User Guide* (UG954). **Chapter 2:** In Figure 2-2, the switch 4 position changed. In Hardware Test Setup, page 18, the *ZC706 Evaluation Kit Contents* section was removed. **Chapter 3:** A note was added on page 22 that though the procedures mention version 14.3, the user should find the latest version of tools online. In Recommended Motherboards, page 19, the boards are now Sandy Bridge and Ivy Bridge. Removed "Tip: The Intel X58 chipsets tend to show higher performance" from page 24. In Figure 3-3, J17 changed to J21. The Figure 3-4 figure title changed to "SW11 SD Boot Mode Settings" and the switch 3 position changed. Added new Figure 3-6 and step 10 above it. The ELF file in step 9, page 22 changed to `zynq_pcie_qt.elf`, `zynq_pcie_cmd.elf`. Installing ZC706 Board in the Host Computer Chassis, page 22 now ends with step 8, page 23. Connecting the HDMI cable was added in step 7, page 23. In Host Computer Bootup, page 23, replaced last sentences in step 1. Split step 1 into two steps to show two different actions. Replaced Figure 3-9 and added Table 3-1 to clarify LED settings. LED L and LED R were reversed in step 2 of Host Computer Bootup. Added to step , page 25. Replaced Figure 3-15 and Figure 3-16.
05/13/2013	3.0	Replaced all references to `zynq_pcie_trd_14_3.zip` with `zc706-pcie-trd-rdf0287.zip` throughout document. Identified location of the PMBus connector in Figure 2-1. Added Note describing SW4 DIP switch setting in ZC706 Evaluation Board Setup, page 9. Removed note on page 22 mentioning ISE Design Suite version 14.3. Updated Figure 3-11, Figure 3-12, and Figure 3-14 screen captures. Revised step 7, page 28. Updated Figure 3-17. Updated links to Xilinx documents and updated link to Zc702 Base TRD (wiki page) http://www.wiki.xilinx.com/Zc702+Base+TRD in Appendix A, Additional Resources.
08/01/2013	4.0	Updated ISE Design Suite from 14.5 to 14.6 (updated Figure 3-14).
12/20/2013	5.0	Updated ISE Design Suite references from version 14.6 to version 14.7. Updated links to latest standard link format throughout document. Replaced all references to `zc706-pcie-trd-rdf0287.zip` with `rdf0287-zc706-pcie-trd-14-7.zip` throughout document. Replaced all references in pathnames to `zc706-pcie-trd-rdf0287` with `rdf0287-zc706-pcie-trd-14-7` throughout document. Revised the FPGA Part numbers on page 7 to the correct format. Added reference to Xilinx PetaLinux SDK on page 17. Added caution note about power connections to J22 on the ZC706 board on page 20 and page 23. Revised power connector reference designator in Figure 3-3 from J18 to J22. Updated Figure 3-11, Figure 3-12, Figure 3-13, Figure 3-14, Figure 3-17 and Figure 3-18. Added Figure 3-19, Figure 3-20, and Figure 3-21 with each figure including an attribution statement for Big Buck Bunny. Added procedure starting at step 9, page 31 and ending at step 16, page 34. Reorganized links and references in Appendix A, Additional Resources and revised links to web pages and documents throughout document to conform to latest style convention.

Date	Version	Revision
01/21/2015	6.0	Updated document for Vivado Design Suite 2014.3. Replaced Figure 3-11 and Figure 3-12.
01/28/2015	6.0.1	Removed Vivado Design Suite version from document title.
07/01/2018	6.0.2	Editorial updates only. No technical content updates.

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Table of Contents

Introduction

Overview

The ZC706 evaluation kit is based on the Zynq®-7000 XC7Z045-2FFG900C SoC. For additional information, see the Zynq-7000 SoC Overview datasheet (DS190) [Ref 1].

A built-in self-test (BIST) and a PCIe® Targeted Reference Design (PCIe TRD) are provided for the ZC706 evaluation kit. The BIST provides a convenient way to test many of the board's features on power-up and upon reconfiguration. The PCIe TRD showcases various features and capabilities of the Zynq-7000 Z-7045 SoC for the embedded domain in a single package. The tutorials and reference designs available on the ZC706 web page can be used to further explore the capabilities of the ZC706 board and the Zynq-7000 SoC. For the most up-to-date information on the tutorial content provided with the ZC706 evaluation kit, see the ZC706 Evaluation Kit Documentation webpage.

Figure 1-1: **ZC706 Evaluation Kit**

ZC706 Evaluation Kit Contents

The ZC706 evaluation kit includes the following items:

- ZC706 evaluation board (EK-Z7-ZC706-G) featuring the XC7Z045-2FFG900C SoC
- Full seat Vivado® Design Suite: System Edition
  - Node-locked, Device-locked to the XC7Z045-2FFG900C SoC
- Board design files
  - Schematics
  - Board layout files
  - Bill of Material (BOM)
- Documentation
  - ZC706 Evaluation Kit Targeted Reference Design Documentation Advisory
- 12V AC adapter power supply
- Cables
  - RJ45 Ethernet cable
  - HDMI cable
  - Digilent USB JTAG Cable
  - USB Type-A to USB Mini-B cable
- Secure Digital (SD) multimedia card
- The Fedora 16.2 LiveDVD
- ATX adapter cable (Xilinx part number 2600304)

The evaluation kit contains all the software and reference designs, demonstrations, and documentation needed to help the user get started quickly.

For reference design files, documents, and board source files, see the ZC706 Evaluation Kit Documentation webpage.

For a list of key features available on the ZC706 evaluation board see the *ZC706 Evaluation Board for the Zynq-7000 XC7Z045 SoC User Guide* (UG954) [Ref 2].

ZC706 Evaluation Kit Built-In Self-Test

Introduction

The built-in self-test (BIST) tests many of the features of the ZC706 evaluation kit. BIST is available after programming the FPGA through JTAG.

Figure 2-1 provides an overview of the board features utilized by the BIST.

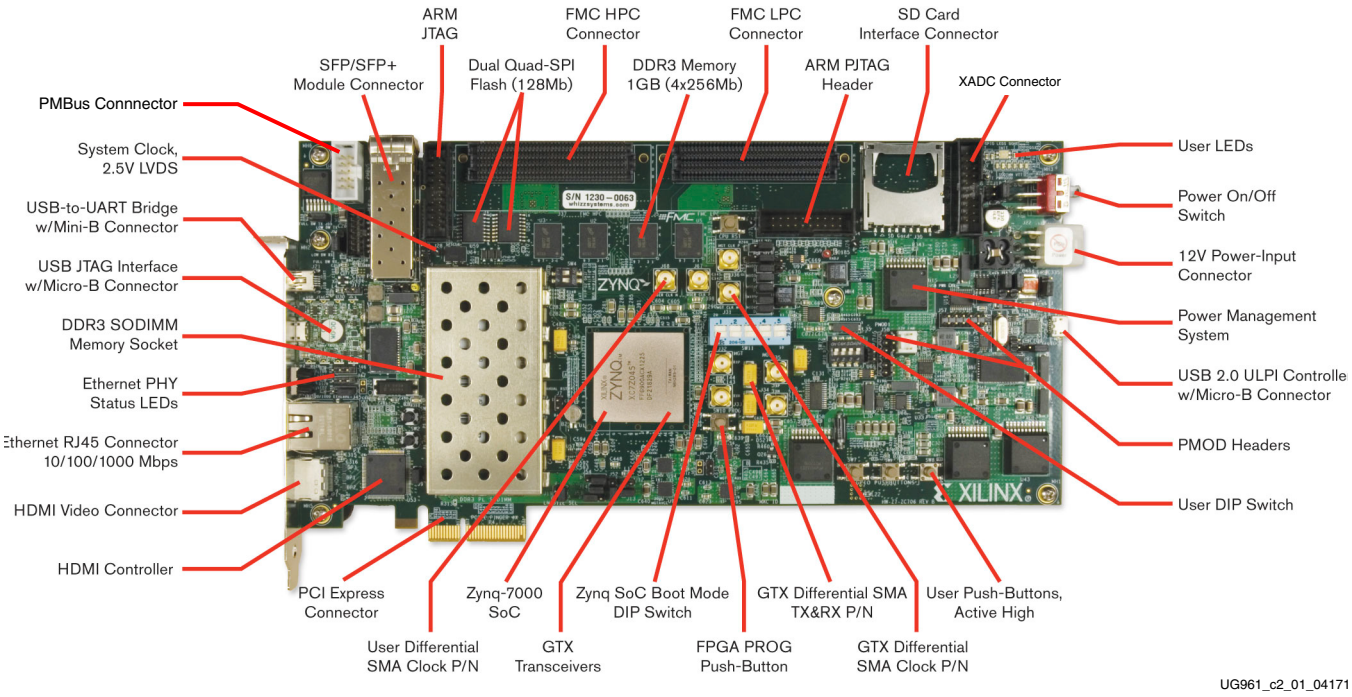

Figure 2-1: **ZC706 Board Features**

Note: For a list of key features available on the ZC706 evaluation board see the *ZC706 Evaluation Board for the Zynq-7000 XC7Z045 SoC User Guide* (UG954) [Ref 2].

Built-In Self-Test Setup Requirements

The prerequisites for testing the design in hardware are:

- ZC706 evaluation board with the Zynq-7000 XC7Z045 FFG900-2 SoC part
- USB to Type-A to Mini-B cable (for UART)
- Digilent JTAG USB Type-A to Micro-B cable
- AC power adapter (12 VDC)
- TeraTerm Pro terminal program or equivalent
- USB-UART drivers from Silicon Labs

Hardware Test Board Setup

This section details the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

ZC706 Evaluation Board Setup

To set the ZC706 jumpers and switches, verify the switch and jumper settings are set as listed in Figure 2-2.

IMPORTANT: *To run the BIST, SW4 must be set to `01` if using the USB Type-A to Micro-B cable provided in the kit, or to `10` if using the Platform Cable USB (II) JTAG cable.*

IMPORTANT: *For this application, the board should be set up as a stand-alone system, with power coming from the cord and AC adapter that comes with the ZC706 evaluation kit.*

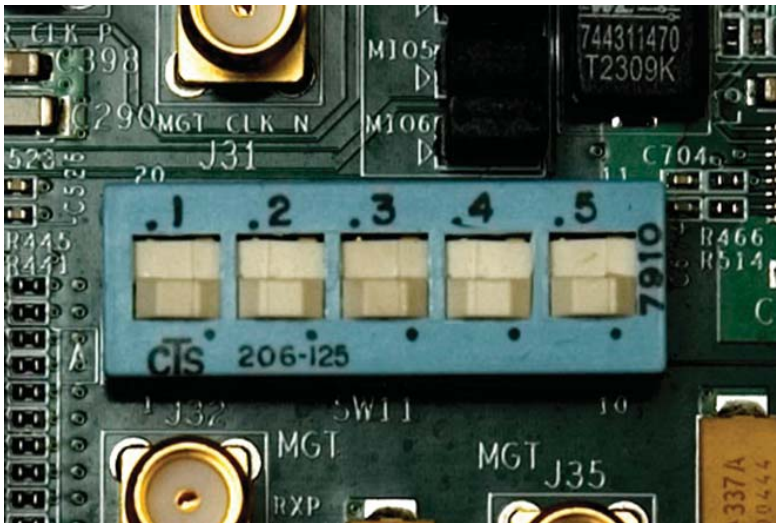

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Figure 2-2: **Switch Settings on the ZC706 Board**

Hardware Bring-Up

This section details the steps for hardware bring-up.

1. With the board switched off, plug a USB Mini-B cable into the UART port of the ZC706 board and your control PC.

2. With the board switched off, plug the Digilent JTAG cable into the JTAG port of the ZC706 board and your control PC.

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Figure 2-3: **ZC706 Board with the UART and Power Cables Attached**

3. Install the power cable 12V stand-alone power supply (included).
4. Switch the ZC706 board power to ON.

Install the Silicon Labs Driver

1. Run the downloaded executable UART-USB driver file, listed in Built-In Self-Test Setup Requirements, page 9. This enables UART-USB communications with a control PC (see Figure 2-4).

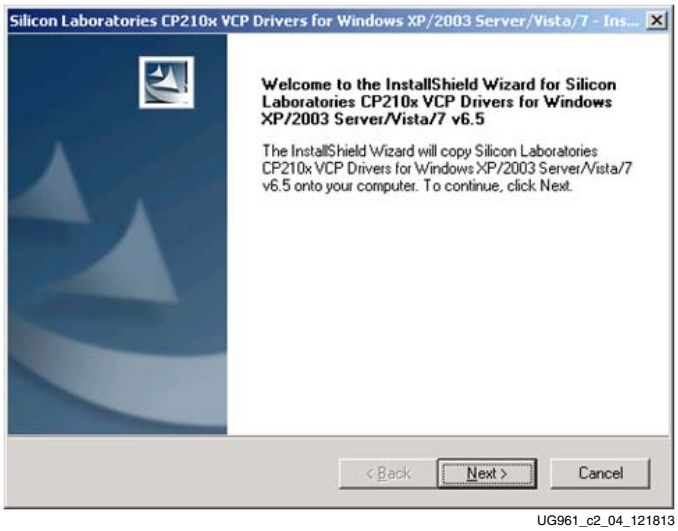

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Figure 2-4: **UART Cable Driver Installation**

2. Set the USB-UART connection to a known **PORT** in the Device Manager.
3. Right-click **My Computer** and select **Properties**.
4. Select the **Hardware** tab. Click the **Device Manager** button (Windows 7)**.**
5. Click **PORTS** (Windows 7).
6. Find the **Silicon Labs** device in the list, right-click it. Select **Properties**.
7. Click the **Port Settings** tab and the **Advanced...** button.
8. Select an open COM port between COM1 and COM4.

Note: Steps and diagrams refer to using a Windows XP or Windows 7 control PC.

Figure 2-5 shows the steps for setting the USB-UART Port.

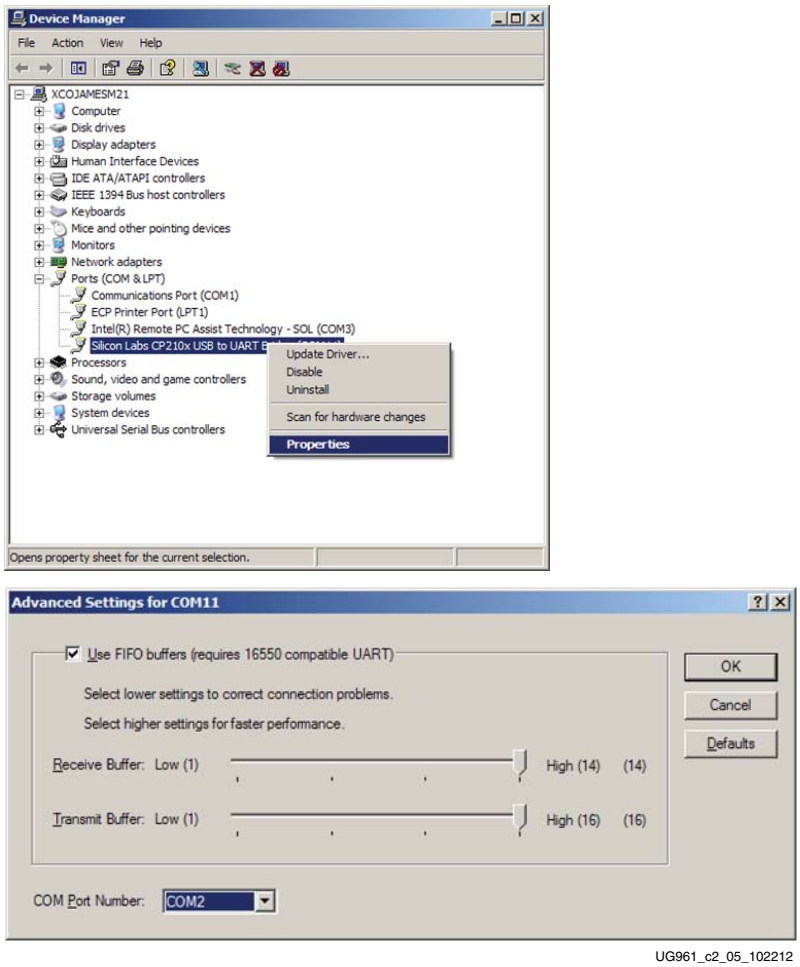

Figure 2-5: **Select the Port Settings after Installing the Silicon Labs Driver**

Unzip the Application Folder

1. Go to the ZC706 Evaluation Kit Documentation webpage and download the latest version of the ZC706 BIST design files.
2. Unzip the folder to the `C:/` drive.

Run the BIST Application

1. Start the installed terminal program.
2. Click **Setup > Serial Port...** and set Baud rate to 115200, parity to none, data bits to 8, and stop bits to 1.
3. Run the script file in `C:\zc706_bist\ready_for_download\zc706_bist.bat` (see Figure 2-6).

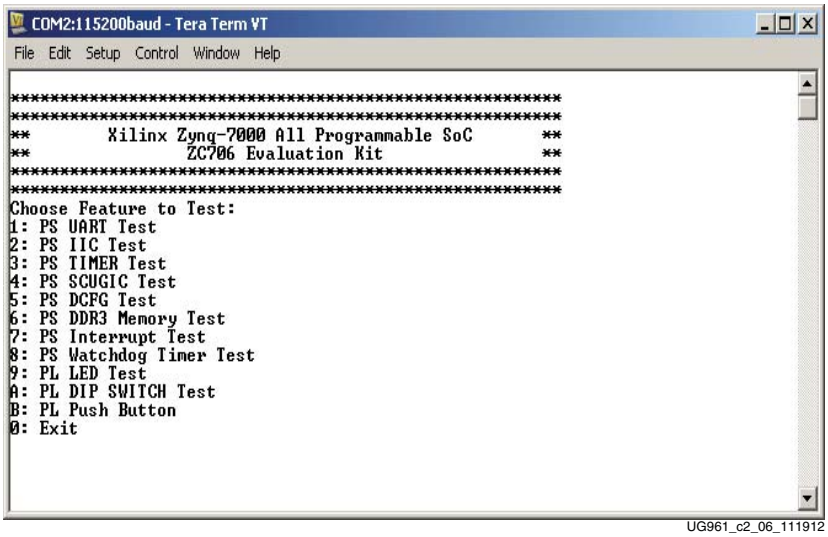

Figure 2-6: **The ZC706 BIST Menu**

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard non-volatile storage, see the ZC706 Evaluation Kit Documentation webpage.

Getting Started with the ZC706 PCIe Targeted Reference Design

Introduction

The Zynq®-7000 PCIe® Targeted Reference Design (TRD) expands the *Zynq-7000 SoC ZC702 Base Targeted Reference Design User Guide* (UG925) [Ref 3] by adding PCI Express® communication with a PCIe host system at PCIe x4 Gen2 speed. In the ZC702 Base TRD, the input of the video processing pipeline is generated by a test pattern generator in the FPGA logic. In this design, the input of the video processing pipeline is generated by an application on the PCIe host computer at 1080p60 resolution and transmitted to the ZC706 board through PCIe. The data is processed by video pipeline and passed back to the PCIe host system through PCIe. As the full 1080p60 video stream only takes up around 4 Gb/s, an additional data generator and a checker are implemented and connected to channel 1 of PCIe DMA, showcasing the maximum PCIe x4 Gen2 bandwidth achieved by the hardware.

The Zynq-7000 PCIe TRD demonstrates the following components working together:

- PCIe Endpoint (x4 Gen2)
- High speed serial transceivers
- High speed multichannel DMA interfacing to PCIe Endpoint
- Zynq-7000 Processing System (PS)
- Video DMA (VDMA) and Sobel filtering
- HDMI based display controller

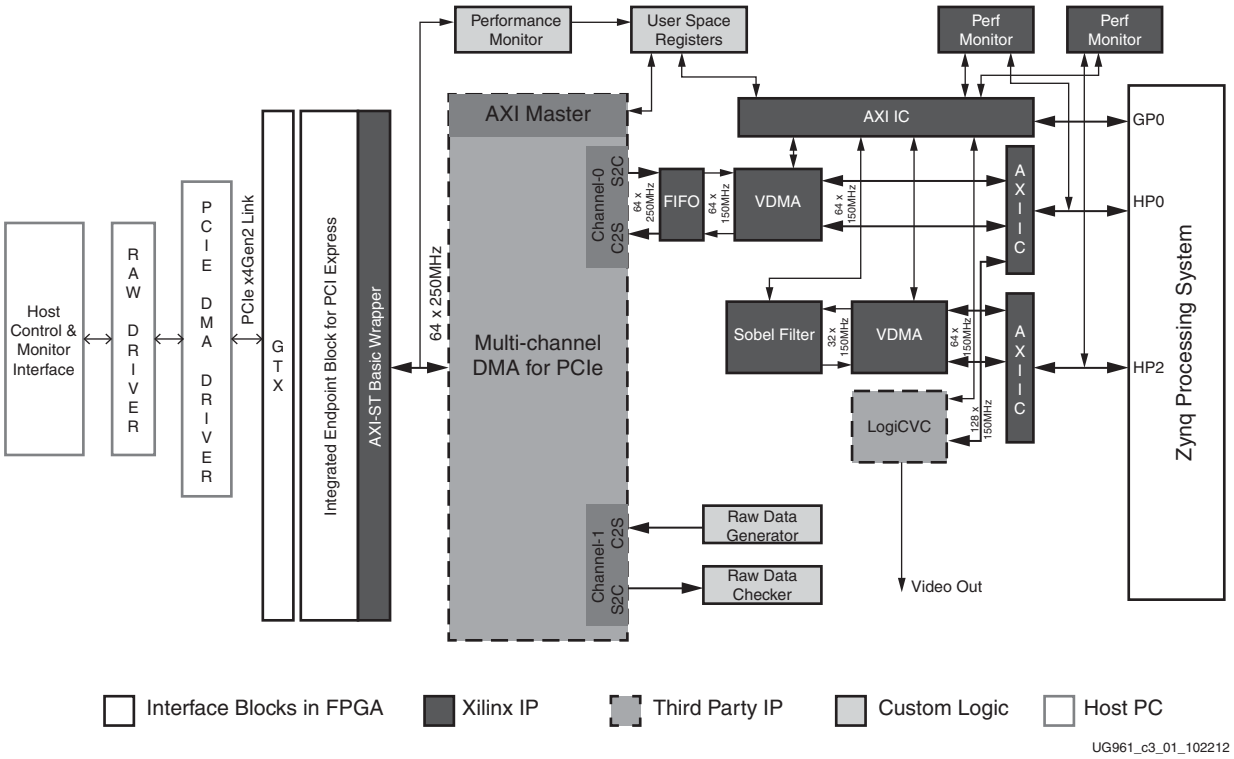

Figure 3-1: **Zynq-7000 PCIe TRD Block Diagram**

The design is a PCI Express based video processing card demonstrating these capabilities:

- PCIe based connectivity demonstration
  - PCI Express block of ZC7Z045 used in x4 Gen2 configuration
- PCI Express compatible high performance low latency multichannel DMA from third party vendor Northwest Logic.
  - Performance demonstration using traffic generator and checker running on FPGA hardware and PCIe host software containing PCIe root port
- ARM Cortex-A9 core processor processing and offload demonstration
  - Zynq-7000 SoC as an off-load device to process video data—The TRD provides an example with the Sobel filter in the Zynq-7000 SoC programmable logic (PL).
  - HDMI based display controller from third party vendor
  - Cortex-A9 in Zynq-7000 as a co-processor processing video data
  - An example design showing independent memory management in the PCIe host system and Cortex-A9 PS.

Key Components

The PCIe TRD features the following components:

- PCI Express v2.1 compliant x4 Endpoint operating at 5 Gb/s/lane/direction
  - PCIe transaction interface utilization engine
  - Message signal interrupt (MSI) and legacy interrupt support
- Bus mastering scatter-gather PCIe DMA to offload the PCIe host processor
  - Multichannel DMA
  - AXI4 Streaming interface for data
  - AXI4 interface for register space access
  - DMA performance engine
  - Full duplex operation
    - Independent transmit and receive channels
- Multichannel VDMA with programmable VSIZE and HSIZE
  - AXI4 compliant
  - Optional flush on frame sync
  - Optional frame advancement on error
- Multilayer display controller
  - Alpha blending, transparency, and move around support
  - Continuous switching mode support
- Sobel filter
  - AXI4 Stream interface
  - AXI4 Control interface
  - Supports image size up to 1080p
- Java based GUI running on the PCIe host system
  - Test control panel
  - PCIe performance monitoring
- A QT based GUI running on Zynq-7000 PS
  - Monitors power and die temperature
  - Zynq-7000 processing system's HP0 and HP2 performance numbers
  - CPU utilization

- Xilinx PetaLinux Software Development Kit (SDK) v2013.10

Data Flow

The TRD shows how the Zynq-7000 platform can be used as an off-load engine to the PCIe host machine it is connected to.

Video Processing and Offload Demonstration on Channel 0 of PCIe DMA

The user application in the PCIe host system repeatedly generates video frames of size 1920 x 1080 pixels containing 8 color bars. Software on the PCIe host system manages channel 0 of PCIe DMA to transmit the video stream from the PCIe host over x4 Gen2 PCIe links to the Zynq-7000 ZC706 board. PCIe DMA translates the stream of PCIe video data packets into AXI streaming data, which is in turn connected to a video DMA (VDMA). Software running on the Cortex-A9 processor manages the AXI VDMA and transfers the raw video frames into the PS DDR3 memory. The Sobel filter in the PL reads the image using another VDMA, performs edge detection on the raw image, and sends the data back to PS DDR3. The processed data in PS DDR3 can either be transferred back to PCIe host system using channel 0 of card-to-system (C2S) interface of PCIe DMA or be displayed on the monitor using the LogiCVC display controller. Due to limitations of the PS DDR3 bandwidth, the same data cannot be displayed and sent back to PCIe host system simultaneously. As in the Base TRD, this design also demonstrates hardware based Sobel filter for video processing.

Generator and Checker Demonstration on Channel 1 of PCIe DMA

A generator and checker on channel 1 of PCIe DMA allow the RX and TX paths to run independently. The hardware generator in the PL fabric generates data packets with an incremental sequence pattern. The software checker running on the PCIe host system verifies the incremental sequence pattern generated by the hardware generator. Independently, the driver running on the PCIe host system generates a stream of incremental data which is transferred through PCIe link by NWL PCIe DMA to the checker implemented in the PL fabric.

Hardware Test Setup

This section describes how to set up the ZC706 board, control computer, host computer, and software for the Zynq™-7000 PCIe® Targeted Reference Design.

Additional Materials

User-supplied materials include:

- Monitor supporting 1080p
- Two personal computers (PCs). See Computer Requirements.
- USB mouse (for use with the ZC706 board)

Computer Requirements

Running the Zynq-7000 PCIe TRD requires two PCs.

Control PC

The TRD requires an Intel processor-based laptop or desktop PC running the Windows 7 operating system. The computer must have an SD memory card receptacle, and one USB port to communicate with the ZC706 board.

Required Software

The software listed here must be installed on the control computer:

- Vivado Design Suite: System Edition.
  - Communications drivers and terminal program. See *Zynq-7000 SoC ZC706 PCI Express Targeted Reference Design User Guide* (UG963) [Ref 4] for details.

PCIe Host System Computer

An Intel processor-based desktop PC running Fedora Core 16 Linux operating system is required for the PCIe host system. The computer must have a PCIe v2.0 slot where the ZC706 board is installed in the open chassis of this computer.

Recommended Motherboards

The recommended PCI Express Gen2 PC system motherboards are:

- Sandy Bridge motherboard
- Ivy Bridge motherboard

Programming the ZC706 Board

The XC7Z045 SoC is configured from a bitstream in a 2 x 128 Mb Quad-SPI flash memory. This bitstream must first be loaded in the Quad-SPI flash memory from the SD card plugged into J30 on the ZC706 board.

Files for configuring the Zynq-7000 PCIe TRD are compiled in `zc706_pcie_trd.bin` which contains the `zynq_fsbl.elf` bitstream and `u-boot.elf` bitstream along with the Linux kernel, Linux file system image files, and Linux device tree binary files.

Extracting the Project Files

The Zynq-7000 PCIe Targeted Reference Design files are located in `rdf0287-zc706-pcie-trd-2014-3.zip` This file is available for download from the ZC706 Evaluation Kit Documentation webpage.

To extract the files:

1. Download `rdf0287-zc706-pcie-trd-2014-3.zip` to a working directory on the control computer.
2. Unzip the files contained in `rdf0287-zc706-pcie-trd-2014-3.zip`.

Programming the SD Card

On the control computer:

1. Plug the SD card into the SD card receptacle.
2. Navigate to the `rdf0287-zc706-pcie-trd-2014-3/ready_to_test/prog_qspi` directory and copy the entire content to the SD card.

   The `BOOT.BIN` file enables the PS to boot in the SD boot mode. The `zc706_pcie_trd.bin` file contains the TRD bitstream. The remaining files are required for Linux boot-up.

3. Unmount and remove the SD card from the computer and insert it into the SD card receptacle on the ZC706 board (Figure 3-2).

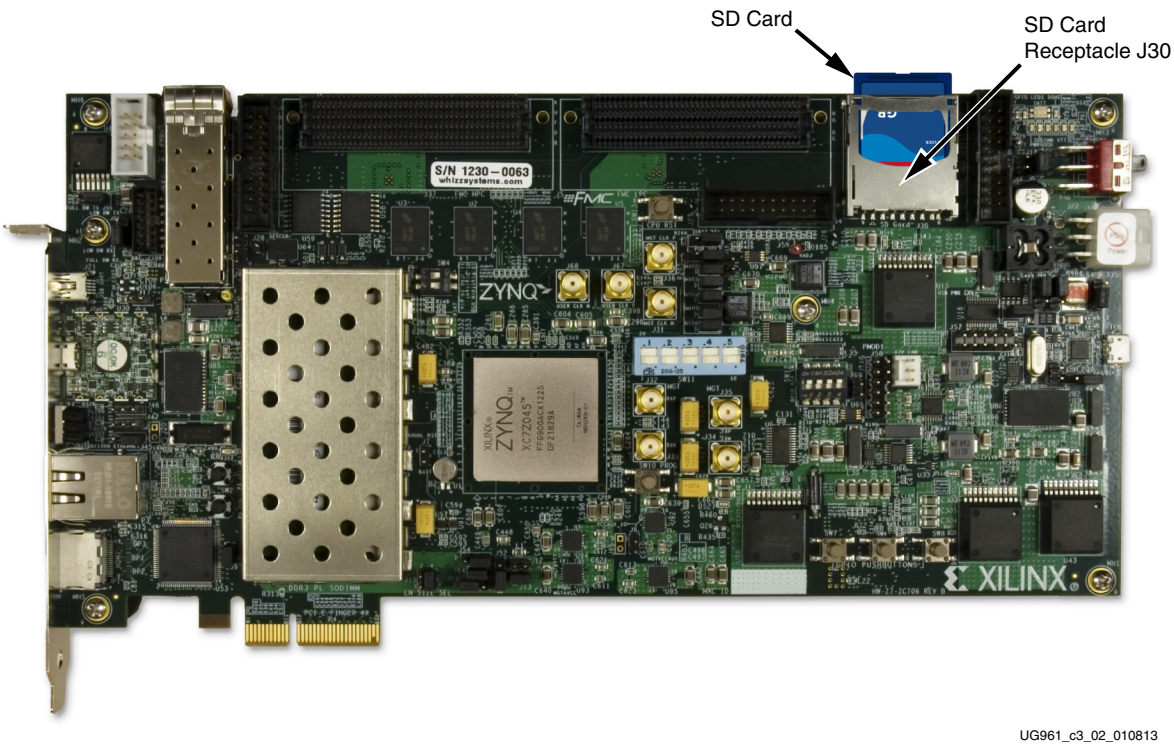

Figure 3-2: **SD Card Location**

Programming the Quad-SPI Flash Memory

This procedure programs the Quad-SPI flash memory with files from the SD card to run the Zynq-7000 PCIe TRD.

1. Complete the communications setup. (See *Zynq-7000 SoC ZC706 PCI Express Targeted Reference Design User Guide* (UG963) [Ref 4] for details.)
2. Power off the ZC706 board (SW12).
3. Verify the SD card is plugged into receptacle J30 as shown in Figure 3-3.
4. Connect the ZC706 board to the control computer and power supply as shown in Figure 3-3.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J22 on the ZC706 Evaluation Board. The ATX 6-pin connector has a different pinout than J22. Connecting an ATX 6-pin connector into J22 will damage the ZC706 Evaluation Board and void the board warranty.*

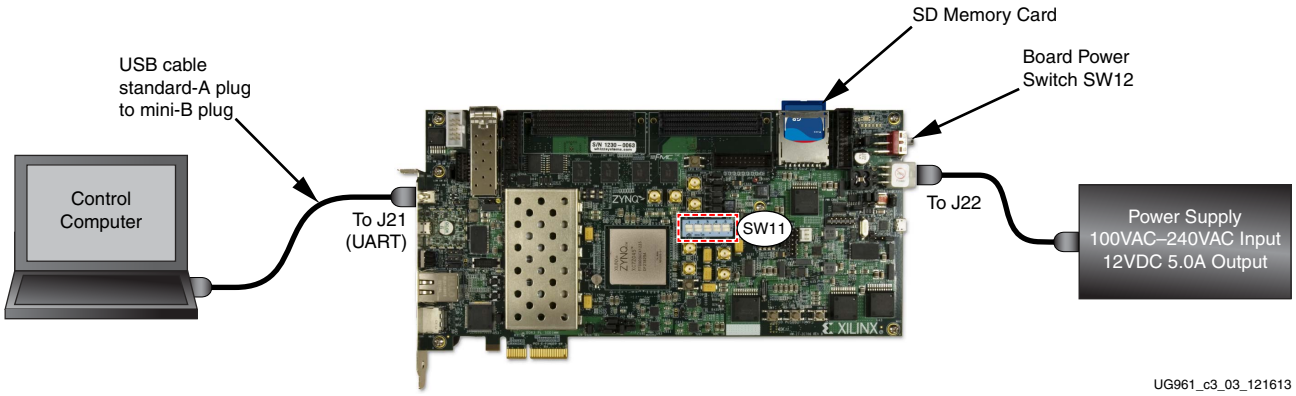

Figure 3-3: **ZC706 Board Programming Setup**

5. Set DIP switch SW11 as shown in Figure 3-4.

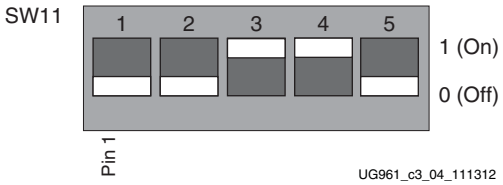

Figure 3-4: **SW11 SD Boot Mode Settings**

6. Power ON the control computer and start TeraTerm Pro using **115200** bits/s, **8** data bits, **None** parity, **1** stop bit, **None** flow control.
7. Power ON the ZC706 board (SW12). The `init.sh` script in the SD card loads the Quad-SPI flash memory with `zc706_pcie_trd.bin` and the Linux kernel images. Initialization progress is shown on the TeraTerm Pro display (Figure 3-5).

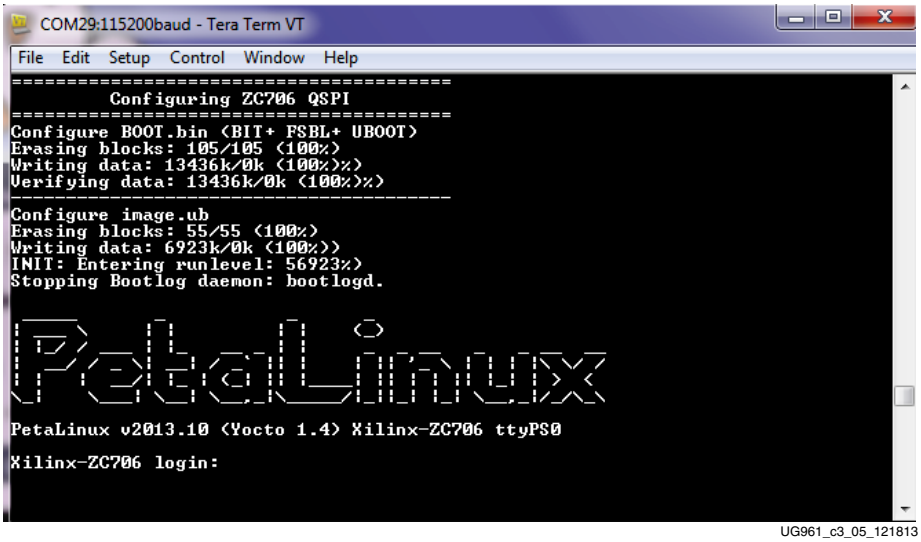

Figure 3-5: **Initialization Progress of the init.sh Script**

8. Initialization is complete when the `zynq>` prompt appears on the TeraTerm Pro display.
9. Navigate to the `rdf0287-zc706-pcie-trd-2014-3/ready_to_test/sd_image` directory and copy the entire contents to the SD card.
10. Set DIP switch SW11 for Quad SPI boot mode, as shown in Figure 3-6.

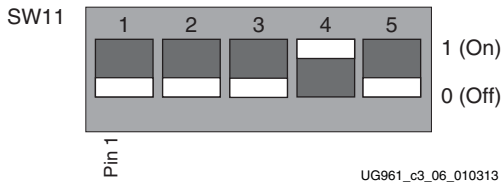

Figure 3-6: **SW11 Quad SPI Flash Memory Settings**

TRD Demonstration Setup

This section describes hardware bring-up, software bring-up, and using the application GUI.

Installing ZC706 Board in the Host Computer Chassis

When the ZC706 board is used inside a computer chassis power is provided from the ATX power supply peripheral connector through the ATX adapter cable shown in Figure 3-7.

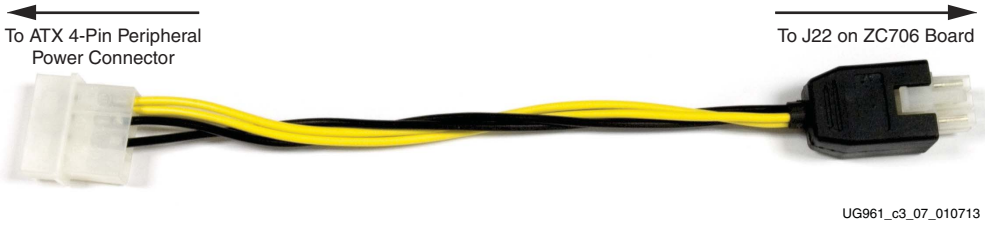

Figure 3-7: **ATX Power Supply Adapter Cable**

To install the ZC706 board in a computer chassis:

1. Remove all six rubber feet and standoffs from the ZC706 board. Replace the PCIe metal bracket using two of the removed screws.
2. Power down the host computer and remove the computer power cord.
3. Open the chassis, select a vacant PCIe expansion slot, and remove the expansion cover at the back of the chassis.
4. Plug the ZC706 board into the PCIe connector at this slot.
5. Install the top mounting bracket screw into the PC expansion cover retainer bracket to secure the ZC706 board in its slot.

IMPORTANT: *The ZC706 board is taller than standard PCIe cards. Ensure that the height of the card is free of obstructions.*

6. Connect the ATX power supply to the ZC706 board using the ATX power supply adapter cable as shown in Figure 3-8.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J22 on the ZC706 Evaluation Board. The ATX 6-pin connector has a different pinout than J22. Connecting an ATX 6-pin connector into J22 will damage the ZC706 Evaluation Board and void the board warranty.*

7. Connect one end of the HDMI cable to the ZC706 HDMI slot (P1) and the other end to the HDMI monitor (Figure 3-8).
8. Slide the ZC706 board power switch SW12 to the ON position.

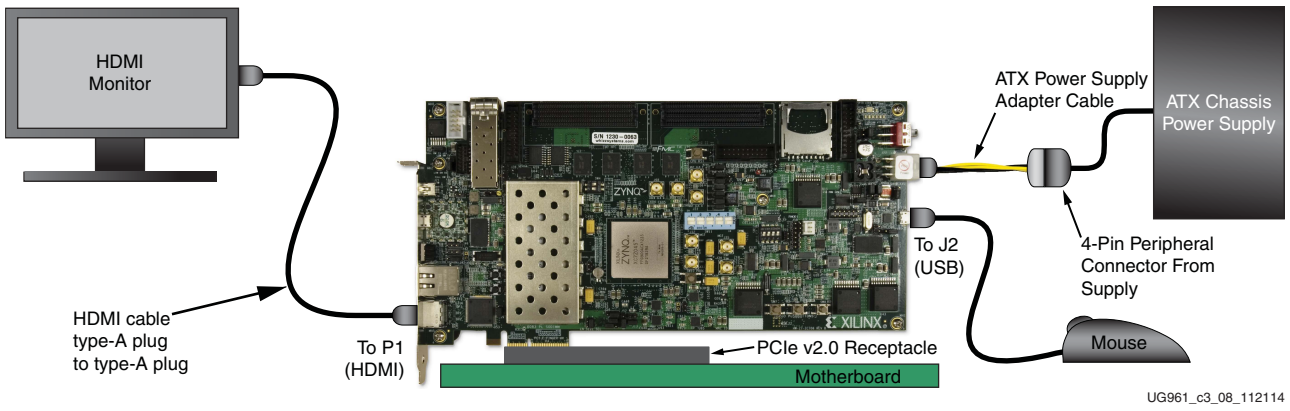

Figure 3-8: **ZC706 Board TRD Setup in Host Computer**

Installing Device Drivers

Host Computer Bootup

The procedures listed in this section require Linux super user access on the host computer. When using the Fedora 16 LiveDVD, super user access is granted by default. If not using the Fedora 16 LiveDVD, contact your system administrator for super user access.

If Fedora 16 is installed on the host computer hard disk, boot as a root-privileged user.

If Linux is not installed, place the Fedora 16 LiveDVD in the host computer CD-ROM drive and restart the computer.

The Fedora 16 Live Media is for Intel-compatible PCs and contains a complete, bootable 32-bit Fedora 16 environment with the proper packages installed for the TRD demonstration. The PC boots from the CD-ROM drive and logs into a liveuser account that has the kernel development root privileges required to install and remove device driver modules.

IMPORTANT: The BIOS boot order must be set so that the CD-ROM drive is the first drive in the boot order. To set the boot order, power on the computer and press the **DEL** or **F2** key. Set the boot order and save the change.

1. Switch SW12 on the ZC706 board to the ON position (as shown in Figure 3-9).

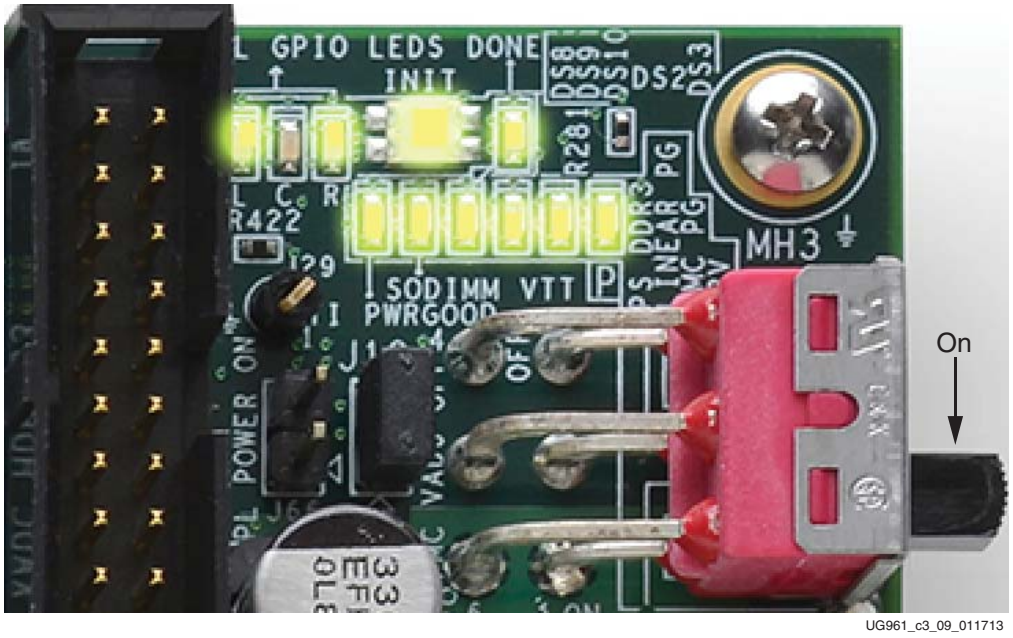

Figure 3-9: **SW12 in the ON Position**

2. Power on the PCIe host system. The Zynq-7000 PCIe TRD provides PCIe status on the GPIO LEDs near the ZC706 board power switch (Figure 3-9). The LEDs that should glow are listed in Table 3-1 (L is the left-most LED in row 1, and LED1 is the left-most LED in row 2.)

Table 3-1: **LEDS Showing PCIe Status**

Row	Labels					
Top Row	**L**	**C**	**R**	**INIT**	**DONE**	**DS10**
	Green *-BLINKING-*	Off	Green	Green	Green	Off
Bottom Row	**LED1**	**LED2**	**LED3**	**LED4**	**LED5**	**LED6**
	Green	Green	Green	Green	Green	Green

LED R and L should be ON and LED C should be OFF. The LEDs represent the following:

- LED R- PCIe link up
- LED C - User reset from PCIe IP

- LED L: User clock heartbeat LED

The images in Figure 3-10 are seen on the monitor during boot up. On the HDMI monitor connected to the ZC706 board, a Qt-based application appears that shows device power and temperature.

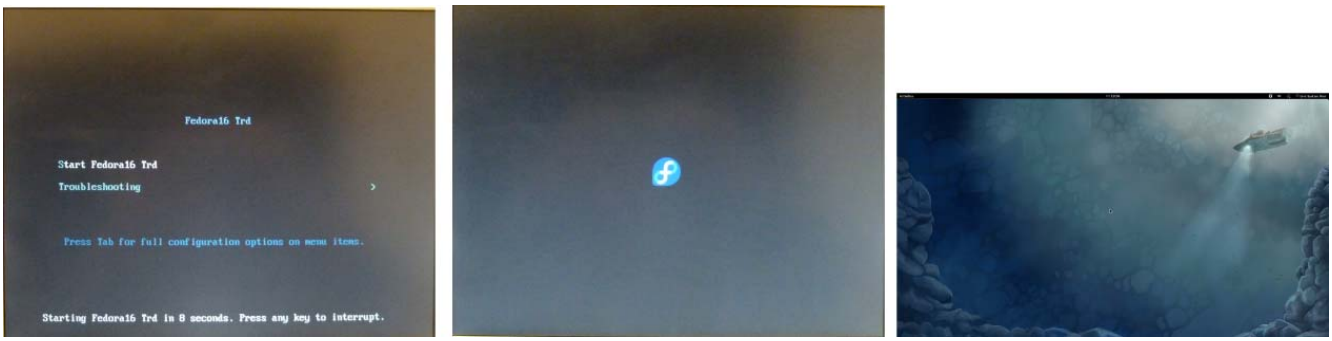

Figure 3-10: **Fedora 16 LiveDVD Boot Sequence**

Download `rdf0287-zc706-pcie-trd-2014-3.zip` from the ZC706 Evaluation Kit Documentation webpage and copy it to specific `/tmp` folder of PCIe host PC. Unzip the file. Change permission by typing **chmod 755 -R rdf0287-zc706-pcie-trd-2014-3** on a terminal so the files have execution permission. Double click on the copied `rdf0287-zc706-pcie-trd-2014-3.zip`.

The screen capture in Figure 3-11 shows the content of the `rdf0287-zc706-pcie-trd-2014-3.zip` folder.

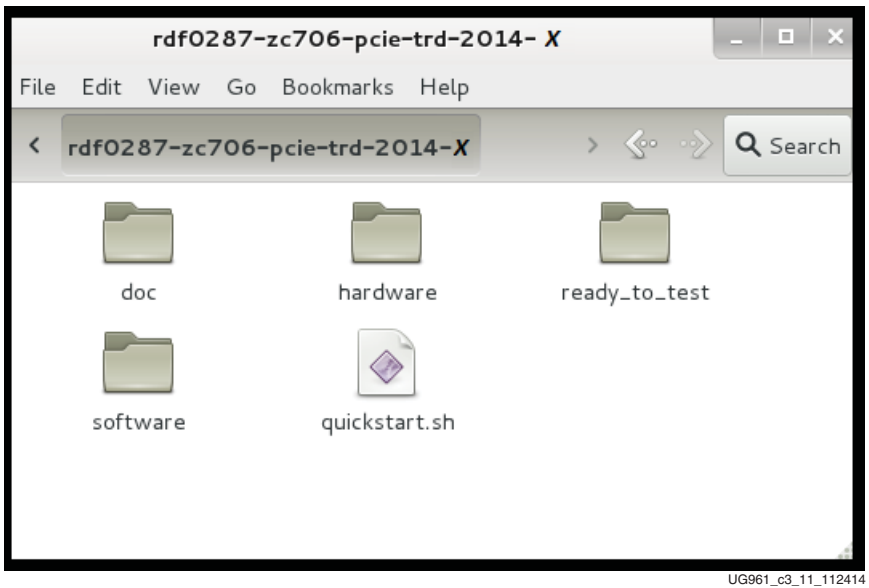

Figure 3-11: **Directory Structure of the ZC706 PCIe TRD**

Note: TRD name is displayed as rdf0287-zc706-pcie-trd-2014-X. X represents the particular tool version.

Example - 2014-3 & 2014-4

3. Double click on the `quickstart.sh` script. This script sets proper permission and invokes the driver installation GUI. Click **Run in Terminal** shown in Figure 3-12.

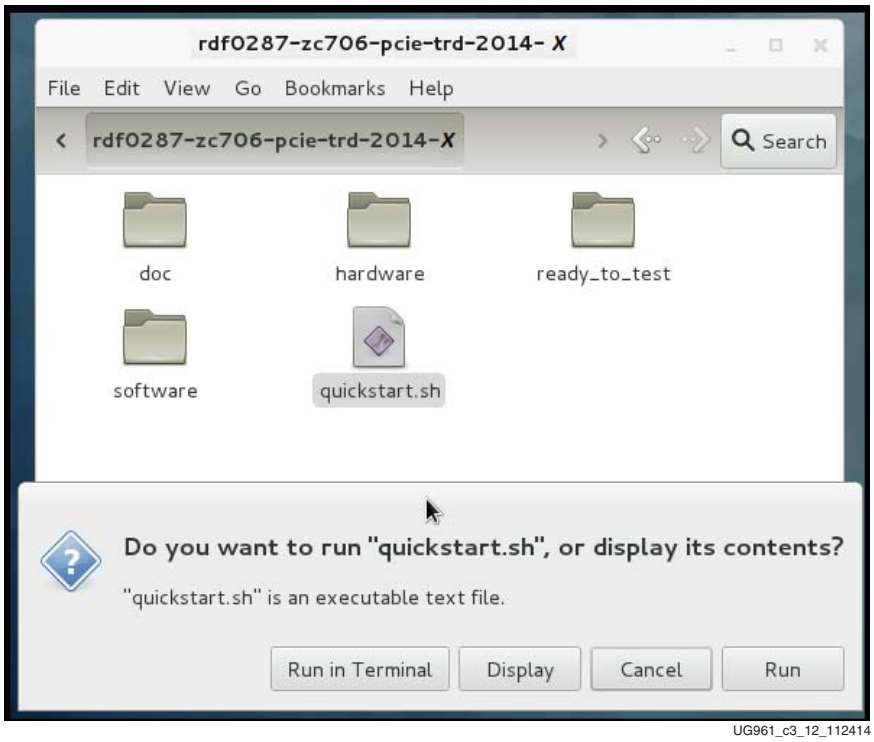

Figure 3-12: **Running Quickstart Script**

4. The GUI with driver installation option pops up as shown in Figure 3-13. This step installs all the software necessary for the host system to control, generate, and receive PCIe traffic to and from the ZC706 board and to monitor performance. The Driver installation

GUI has two buttons to install different drivers corresponding to Performance Demo and Video Demo. Click **Performance Demo Install**.

Figure 3-13: **Install Dialog Box of Zynq-7000 PCIe TRD**

5. After installing the performance mode driver, the control and monitor user interface pops up as shown in Figure 3-14. The control pane shows control parameters such as Sobel Filter and Video Out selection modes.

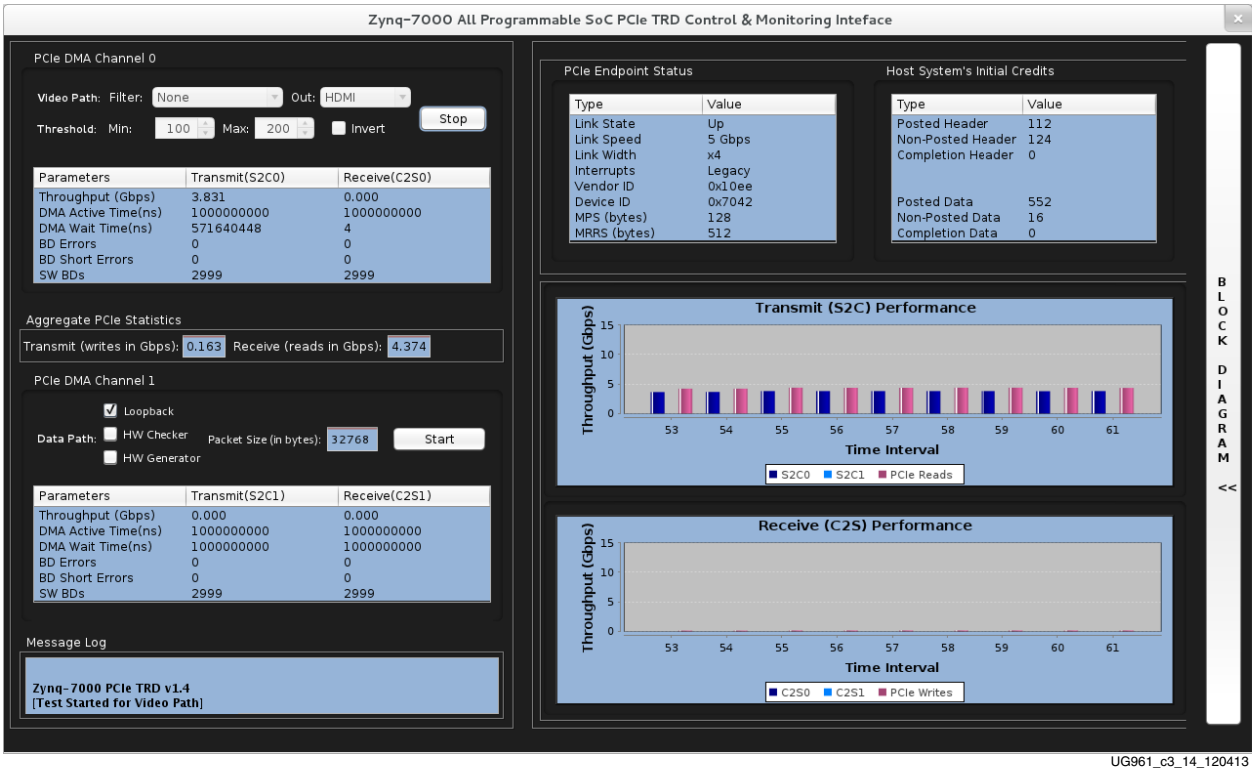

Figure 3-14: **Performance Mode GUI**

6. Click the **Start** button in the Video Path panel to start the PCIe host system generating a 1080p60 video stream and sending it over to the ZC706 board through PCIe. The video

stream is processed and displayed on the HDMI monitor or sent back to the host through PCIe, based on the test mode selected in the Video Out menu. The Performance Plots tab shows the system-to-card (S2C) and card-to-system (C2S) PCIe performance numbers.

You can select various test modes from the Sobel Filter drop-down menu:

- Select option **None** to display the frames on the monitor without Sobel.
- Select option **Sobel-HW** to display the frames on the monitor with HW Sobel.
- Select option **Sobel-SW** to display the frames on the monitor with SW Sobel.

You can select various test modes from the Video Out drop-down menu:

- Select option **HDMI** to display Sobel data on HDMI monitor.
- Select option **PCIe Host** to send data back to the PCIe host system.

For option Sobel Filter: **None** and Video Out: **HDMI**, video data from PCIe host system is directly sent to the display without being processed by the edge detection Sobel filter. A color bar pattern appears on the display as shown in Figure 3-15 for this option.

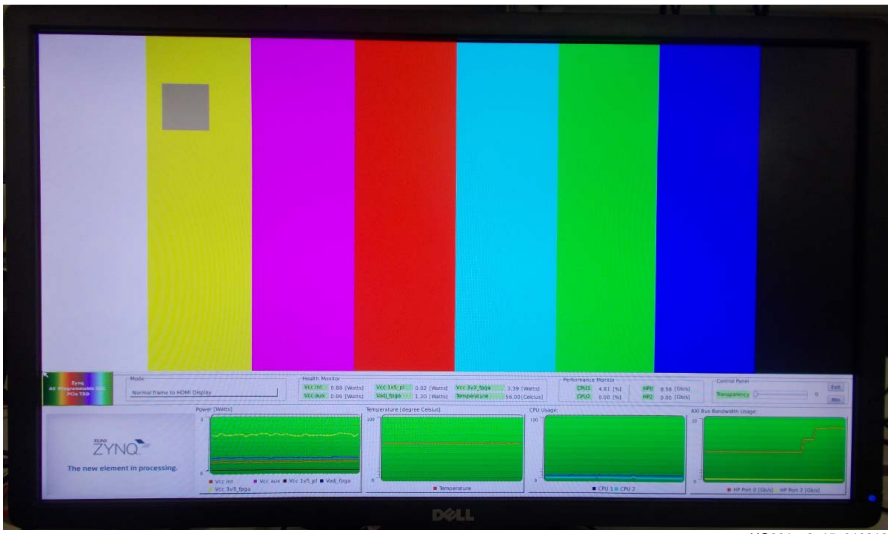

Figure 3-15: **HDMI Display for Color Bar Display**

7. For the options Sobel Filter: **Sobel-HW** and Video Out: **HDMI**, video data from the PCIe host system is directly processed by the edge detection Sobel filter in the PL based on **Max** and **Min** threshold values selection provided through the host GUI, then sent to the display. Edges of the color bar pattern appear on the display as shown in Figure 3-16 for this option without invert option. Optionally, the Sobel output video can be inverted by selecting **Invert** check box on the GUI.

Figure 3-16: **HDMI Display for Sobel Output Display**

For option Sobel Filter: **Sobel-SW** and Video Out: **HDMI**, video data from the PCIe host system is directly processed by the edge detection Sobel filter in the PS, then sent to the display. Edges of the color bar pattern appear on the display.

For option Video Out: **PCIe Host**, video data from PCIe host system is processed by Sobel filter in the PL or PS depending on mode selected in Sobel Filter, then sent back to the PCIe host system through PCIe. The data is not sent to the display. Sobel Filter: **None** is not a supported option when Video Out is set to **PCIe Host**.

The Qt GUI monitors the power of the device voltage rails and die temperature. The CPU utilization and PS HP port 0 and HP port 2 performance numbers are also periodically plotted. When the user selects Sobel Filter: **None** HP port 0 performance becomes 8 Gb/s and HP port 2 port performance becomes 0 Gb/s When the user selects Sobel Filter: **Sobel-HW** both HP port 0 and HP port 2 performance is close to 8 Gb/s. When you select Sobel Filter: Sobel-SW, the CPU2 performance becomes 100%, HP port 0 performance becomes close to 8 Gb/s, and HP port 2 performance becomes 0.

8. As noted in the discussion above, because a single HD stream of video data is insufficient to saturate available PCIe x4 Gen2 bandwidth, datapath 1 can be turned on to add additional PCIe traffic. Click on the **Start** button in the Data Path-1 panel to generate additional traffic. On this path, the user can vary packet sizes and see performance variation accordingly. Total PCIe BW is updated in the PCIe statistics panel and the performance plot. The user can select **Loopback**, **HW Generator**, and the **HW Checker** option in the GUI for Data Path-1 (Figure 3-17).

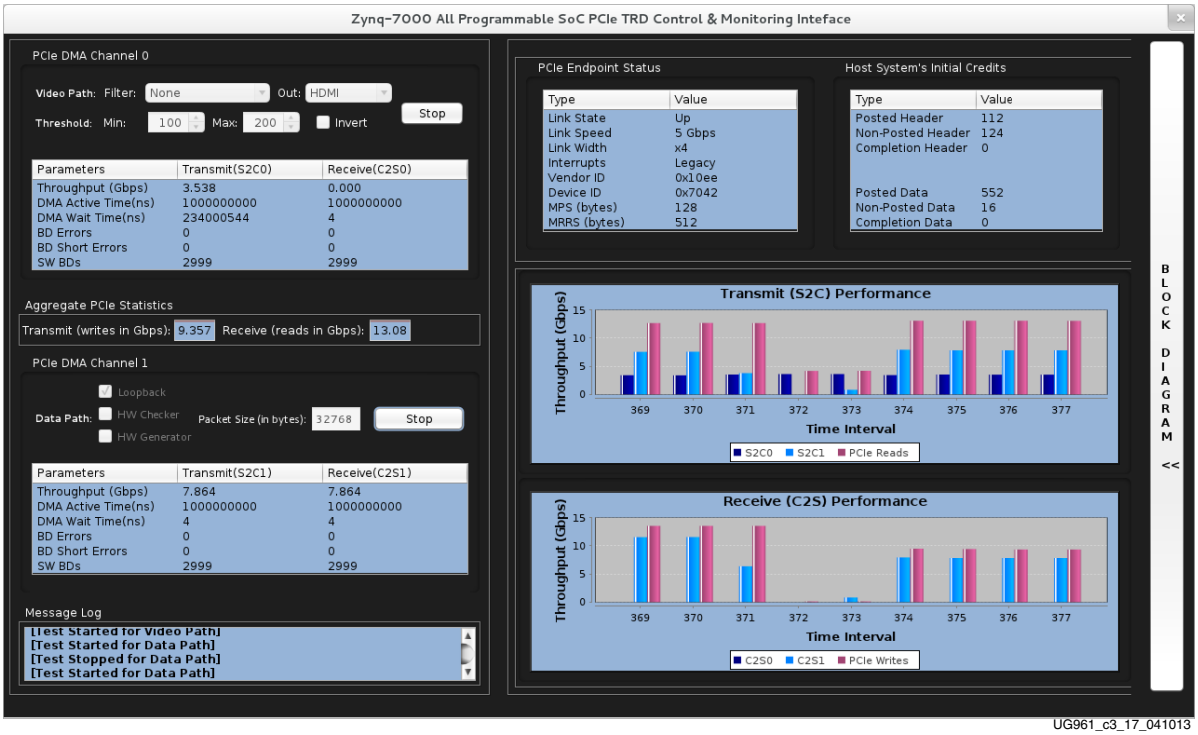

Figure 3-17: **Performance Mode Plots**

9. After installing the Video mode driver as described in step 4, page 26, the control and monitor user Interface pops up as shown in Figure 3-18. The control pane shows control parameters such as a video path browse option and sobel filter type selection.

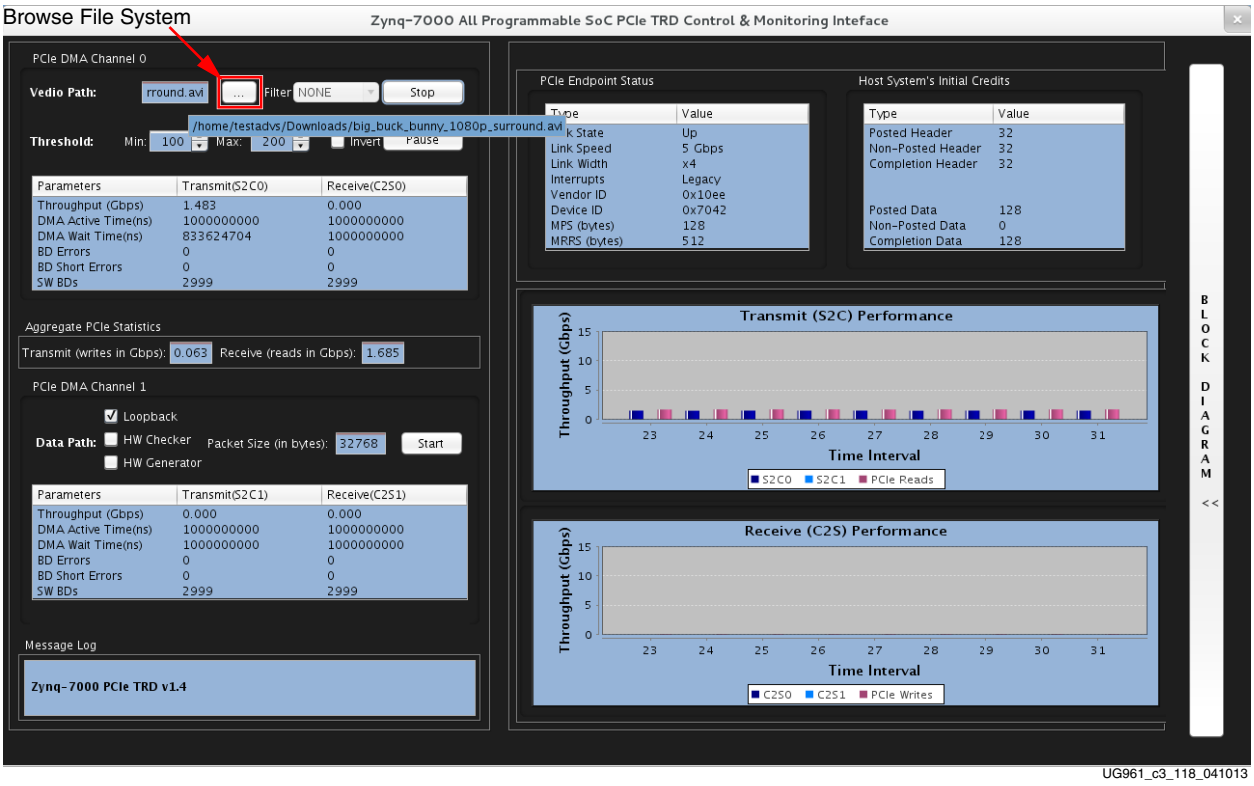

Figure 3-18: **Video Mode GUI**

10. To select a video file present on the host file system, click the browse file system button (Highlighted in Figure 3-18).

    Note: The video file used in this example and shown in Figure 3-19, Figure 3-20, and Figure 3-21 is Big Buck Bunny, available for free download from www.bigbuckbunny.org.

11. Click the **Start** button in the Video Path panel for sending the selected video file present in the Linux host system to the ZC706 board through the PCIe interface. The video stream is processed and displayed on the HDMI monitor. The **Performance Plots** tab shows the system-to-card (S2C) and card-to-system (C2S) PCIe performance numbers.

12. To select various test modes from the Filter drop-down menu:

    - Select **None** to display the frames on the monitor without sobel filtering.
    - Select **Sobel-HW** to display the frames on the monitor with hardware sobel filtering.
    - Select **Sobel-SW** to display the frames on the monitor with software sobel filtering.

    Click the **Pause** button (located below the **Start** button) to pause the video transmission.

The video being transmitted to the Zynq-7000 SOC is displayed on the host machine in it's original form through a vlc player window as shown in Figure 3-19.

Figure 3-19: **Video running on Host**

13. When the filter option is set to **None**, video data from PCIe host system is sent directly to the display without being processed by the edge-detection sobel filter. The transmitted video appears on the display as shown in Figure 3-20.

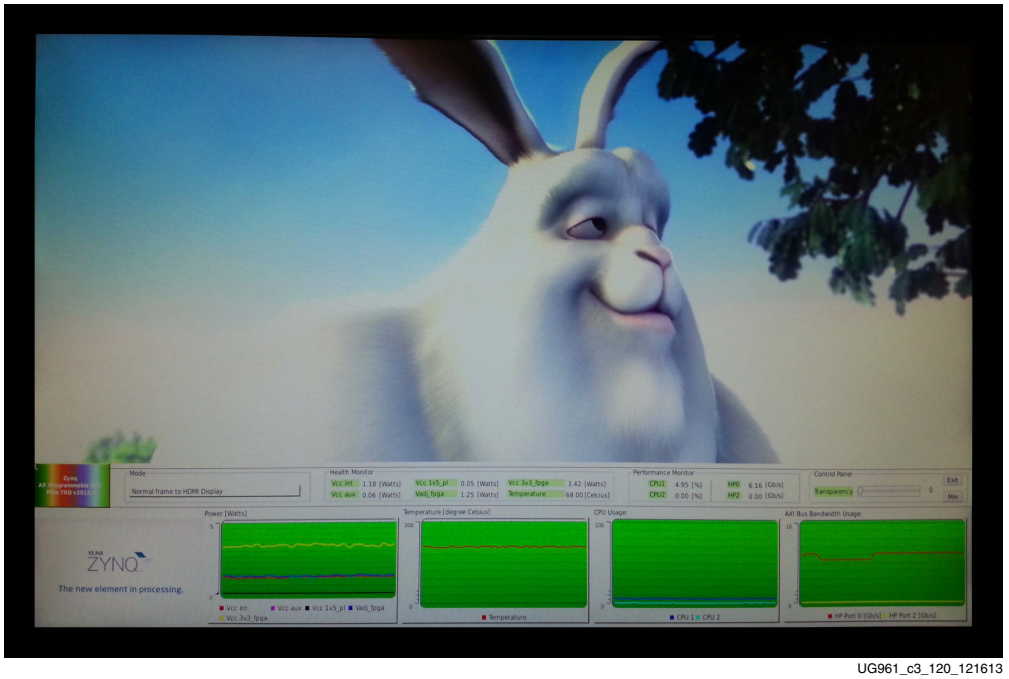

Figure 3-20: **Video running on HDMI Monitor with SOBEL set to None**

14. When the filter option is set to **Sobel-HW**, video data from the PCIe host system is processed directly by the edge-detection Sobel filter in the PL based on **Max** and **Min** threshold values selected and provided through the host GUI, and then sent to the display. Edges of the objects appear on the display as shown in Figure 3-21 when the invert option is not selected (not checked). Checking the invert option will invert the display.

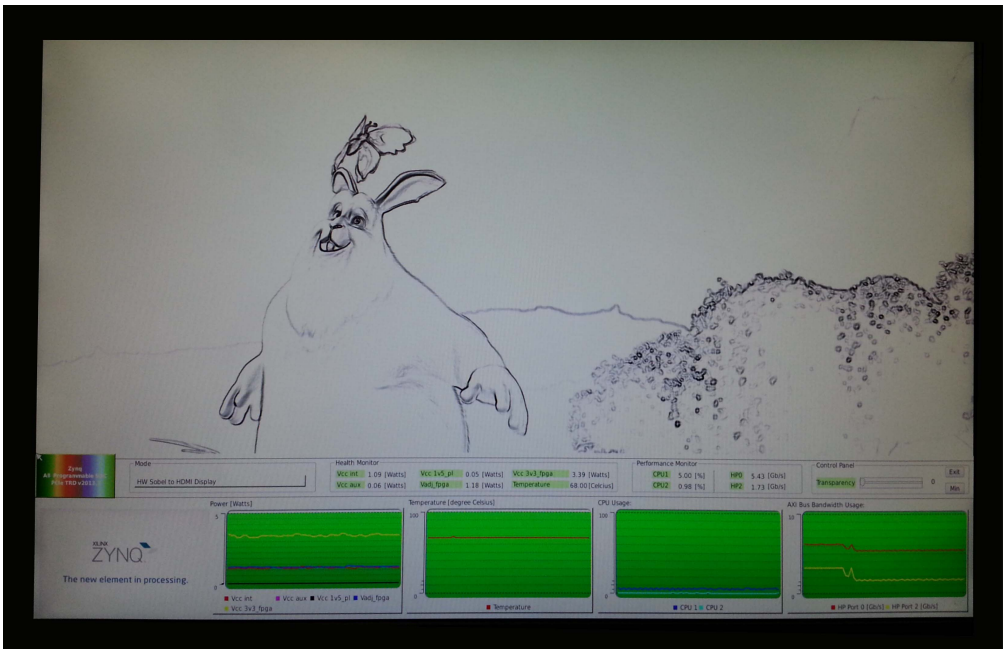

Figure 3-21: **Video running on HDMI Monitor with HW/SW SOBEL Filter**

When the filter option is set to **Sobel-SW**, video data from the PCIe host system is directly processed by the edge-detection Sobel filter in the PS, then sent to the display as shown in Figure 3-21.

15. Also, as mentioned in step 8, page 29, data path 1 (PCIe DMA Channel 1) can be turned on in this mode to showcase the PCIe x4 Gen2 bandwidth.

16. Click on the **Block Diagram** option to view the design block diagram as shown in Figure 3-22.

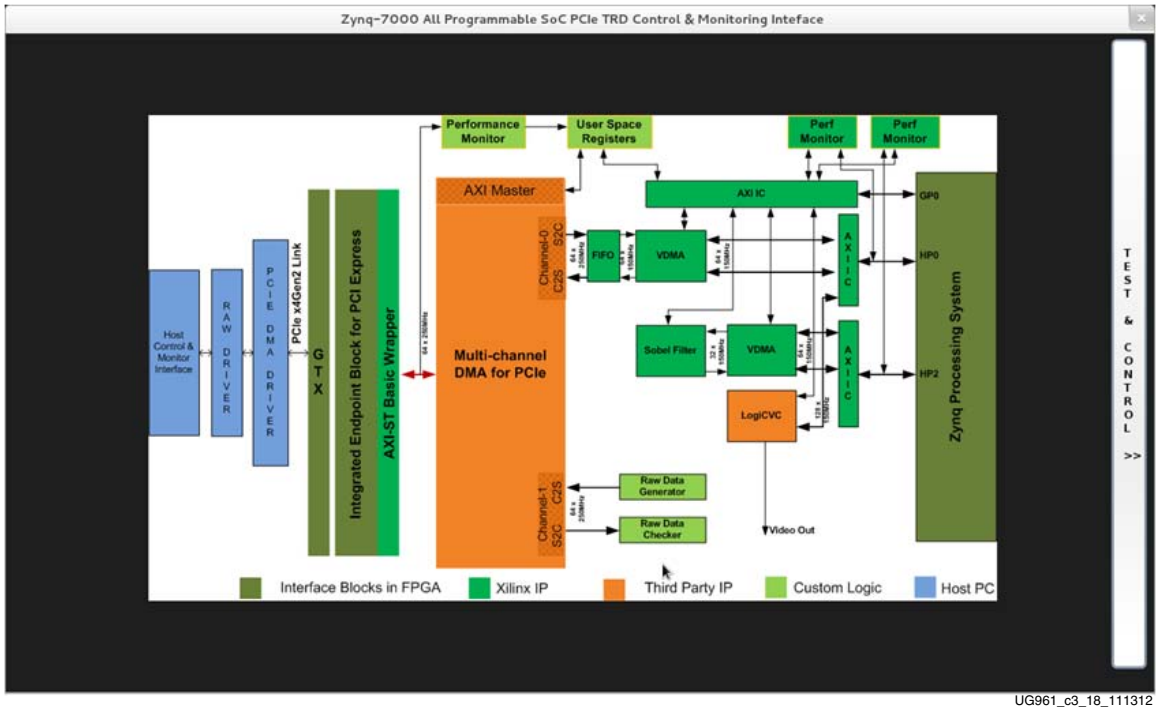

Figure 3-22: **Design Block Diagram**

17. Exit the Qt GUI by clicking the **Exit** button in the GUI as shown in Figure 3-23.

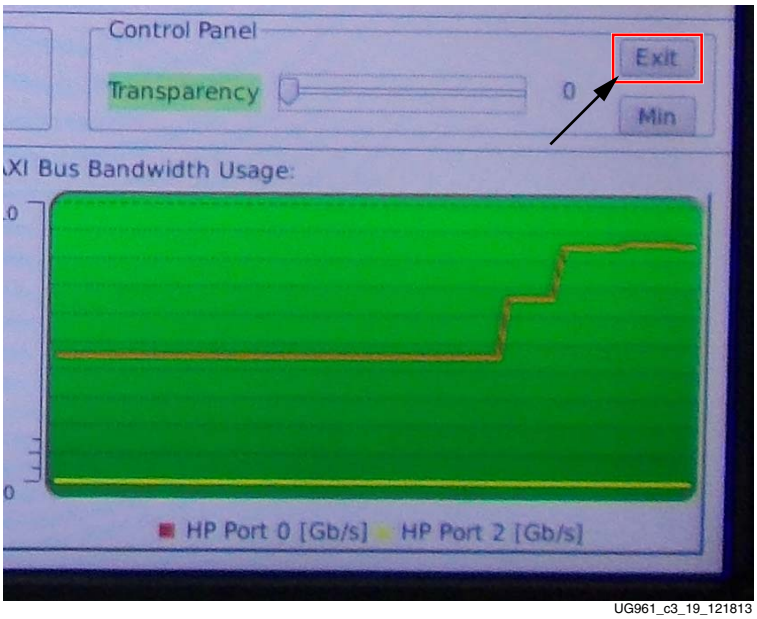

Figure 3-23: **Exiting the Qt GUI**

18. Close the GUI. This process uninstalls the driver on the PCIe host system and opens the landing page of the Zynq-7000 PCIe TRD. Uninstalling the driver requires the GUI to be closed first.

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the ZC706 Evaluation Kit and its documentation is available on these websites:

ZC706 Evaluation Kit

ZC706 Evaluation Kit Documentation

ZC706 Evaluation Kit Master Answer Record (AR 51899)

These Xilinx documents and sites provide supplemental material useful with this guide:

1. *Zynq-7000 Extensible Processing Platform Overview* (DS190)
2. *ZC706 Evaluation Board for the Zynq-7000 XC7Z045 SoC User Guide* (UG954)
3. *Zynq-7000 SoC ZC702 Base Targeted Reference Design User Guide* (UG925)
4. *Zynq-7000 SoC ZC706 PCI Express Targeted Reference Design User Guide* (UG963)
5. *LogiCORE IP Processor System Reset Module v5.0* (PG164)
6. *LogiCORE IP AXI Interconnect* (PG059)

7. *LogiCORE IP AXI Video Direct Memory Access Product Guide* (PG020)
8. *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054)
9. *Zynq-7000 SoC Technical Reference Manual* (UG585)
10. *Quick Front-to-Back Overview Tutorial: PlanAhead Design Tool* (UG673)
11. *ISE Design Suite 14: Release Notes, Installation, and Licensing* (UG798)
12. *Zynq-7000 SoC Software Developers Guide* (UG821)
13. *Zynq-7000 SoC: Concepts, Tools, and Techniques (CTT) A Hands-On Guide to Effective Embedded System Design* (UG873)
14. *Zynq-7000 SoC: ZC702 Evaluation Kit and Video and Imaging Kit Getting Started Guide* (UG926)
15. Zynq-7000 SoC webpage
16. Zynq-7000 SoCs Product Table
17. Xilinx PetaLinux Software Development Kit webpage

These external websites provide supplemental material useful with this guide:

18. Ayera Technologies
TeraTerm Pro terminal program
19. PCI-SIG
PCI Express specifications
20. ARM Information Center
AMBA AXI4-stream protocol specification
21. Fedora Project
(Fedora operating system information and downloads)
22. Silicon Labs
Si570, Si5324C, CP2103GM, USB to UART Bridge, VCP Drivers
23. Northwest Logic
PCI Express® Solution, DMA Back End Core
24. Open Source Linux (Xilinx Wiki)
Developer resources
25. Install Xilinx Tools (Xilinx Wiki)
ARM GNU tools
26. GitHub
Xilinx open source ARM Git repository
27. Using Git (Xilinx Wiki)
Git installation instructions and information

28. Device Tree Main Page
Device Tree Wiki

29. Xylon LogicBRICKS
logiCVC-ML Compact Multilayer Video Controller IP core, description and data sheet

30. QT Documentation
Documentation for the QT cross-platform UI and software application development framework

31. Using Git
A public Git tree for Xilinx open source projects

32. Install Xilinx Tools
Install Xilinx Tools is a part of Xilinx design flow

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