KCU116 Evaluation Board

User Guide

UG1239 (v1.2) September 28, 2018

XILINX

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/28/2018	1.2	Updated DDR4 Component Memory and Regulatory and Compliance Information. Added Electrostatic Discharge Caution.
05/03/2018	1.1	Updated Figure 3-19 and Table 3-18.
06/08/2017	1.0.2	Typographical update.
05/15/2017	1.0.1	Typographical update.
05/12/2017	1.0	Initial Xilinx release.

Table of Contents

Introduction

Overview

The KCU116 evaluation board for the Xilinx® Kintex® UltraScale+™ FPGA provides a hardware environment for developing and evaluating designs targeting the UltraScale+ XCKU5P-2FFVB676E device. The KCU116 evaluation board provides features common to many evaluation systems, including:

- DDR4 component memory
- High-definition multimedia interface (HDMI™)
- Four zSmall form-factor pluggable plus (zSFP+) connectors
- Eight-lane PCI Express® interface
- Ethernet PHY
- General purpose I/O
- Two UART interfaces

Other features can be supported using VITA-57.1 FPGA mezzanine cards (FMC) attached to the high pin count (HPC) FMC connector.

Additional Resources

See Appendix D, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the KCU116 evaluation board.

Block Diagram

A block diagram of the KCU116 evaluation board is shown in Figure 1-1.

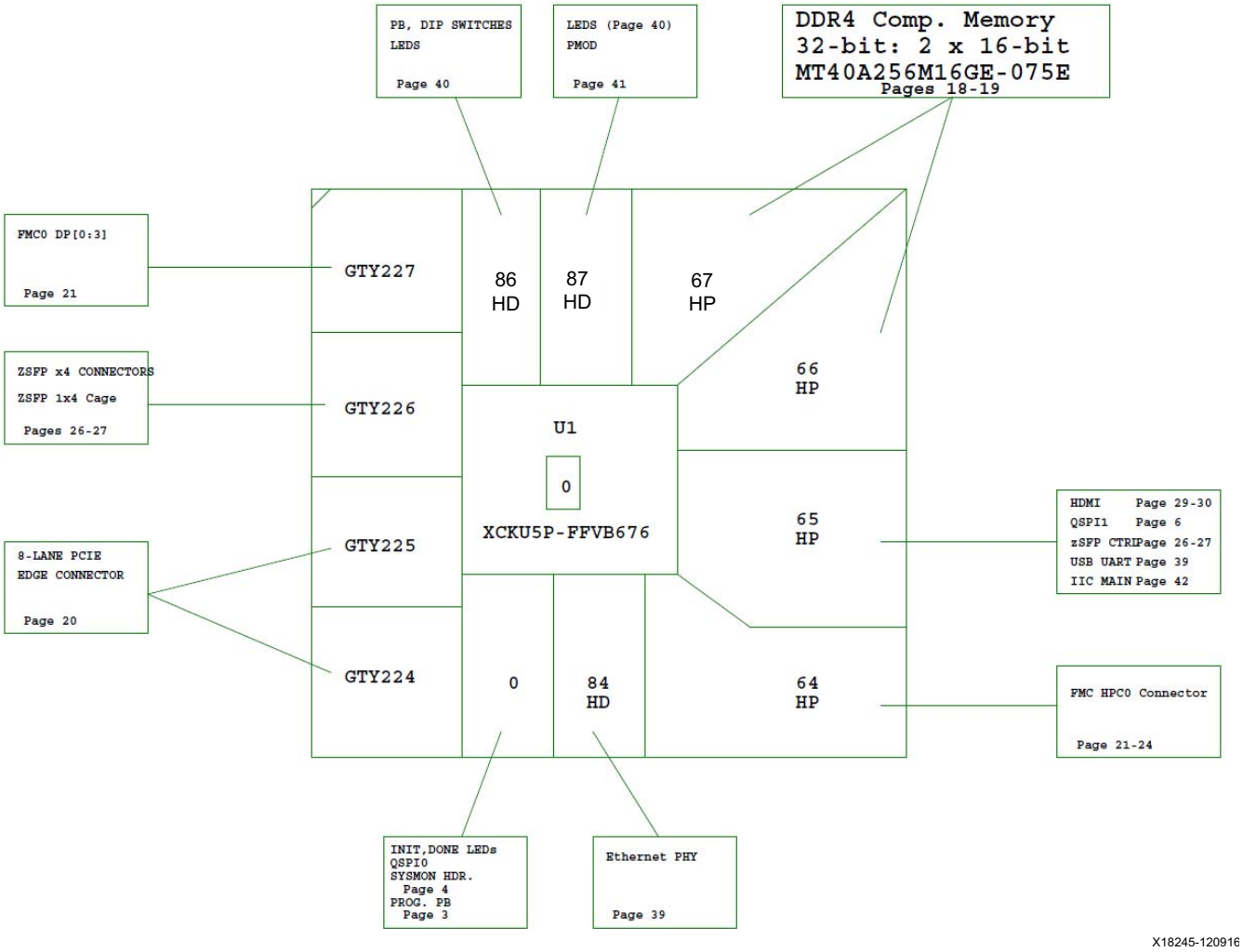

Figure 1-1: **KCU116 Evaluation Board Block Diagram**

Board Features

The KCU116 evaluation board features are listed in this section. Detailed information for each feature is provided in Component Descriptions in Chapter 3.

- Kintex UltraScale+ XCKU5P-2FFVB676E FPGA
- Zynq® SoC XC7Z010 based system controller with micro secure digital (SD) connector

- 1 GB DDR4 component memory (two [256 Mb x 16] devices)
- Two 256 Mb quad serial peripheral interface (QSPI) flash memory (dual Quad SPI)
- USB JTAG interface via Digilent module with micro-B USB connector
- Clock sources:
  - SI5335A quad clock generator
  - SI5328A programmable clock multiplier and jitter attenuator
  - Si570 I^2C programmable LVDS clock generator
  - Subminiature version A (SMA) connectors (differential)
- 16 GTY transceivers (four Quads)
  - FMC HPC connector (four GTY transceivers)
  - 8-lane PCI Express (eight GTY transceivers)
  - Four zSFP+ connectors (four GTY transceivers)
- PCIe® endpoint connectivity
  - Gen1 8-lane (x8)
  - Gen2 8-lane (x8)
  - Gen3 8-lane (x8)
- Four zSFP+ connectors in a 1 high x 4 wide form-factor cage
- Ethernet PHY SGMII interface with RJ-45 connector
- Dual USB-to-UART bridge with micro-B USB connector
- HDMI output codec with HDMI type-A connector
- I^2C bus
- Status LEDs
- User I/O
- Program_B pushbutton
- Pmod headers
- VITA 57.1 FMC HPC connector J5
- Power on/off slide switch SW1
- Power management with PMBus voltage monitoring through Maxim power controllers and GUI
- Single 10-bit 0.2 MSPS ADC system monitor (SYSMON) analog-to-digital front end
- Configuration options:

- Dual Quad SPI flash memory
- Micro-B USB J2 JTAG configuration port (Digilent module)
- Platform cable header J8 JTAG configuration port

Board Specifications

Dimensions

Height: 6.927 inch (17.59 cm)

Thickness (±5%): 0.061 inch (0.1549 cm)

Length: 9.5 inch (24.13 cm)

Note: A 3D model of this board is not available.

IMPORTANT: *The KCU116 board height exceeds the standard 4.376 inch (11.15 cm) height of a PCI Express card.*

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Chapter 2

Board Setup and Configuration

Electrostatic Discharge Caution

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.

Board Component Location

Figure 2-1 shows the KCU116 board component locations. Each numbered component shown in the figure is keyed to Table 2-1. Table 2-1 identifies the components, references the respective schematic page numbers, and links to a detailed functional description of the components and board features in Chapter 3.

IMPORTANT: Figure 2-1 *is for visual reference only and might not reflect the current revision of the board.*

CAUTION! *The KCU116 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.*

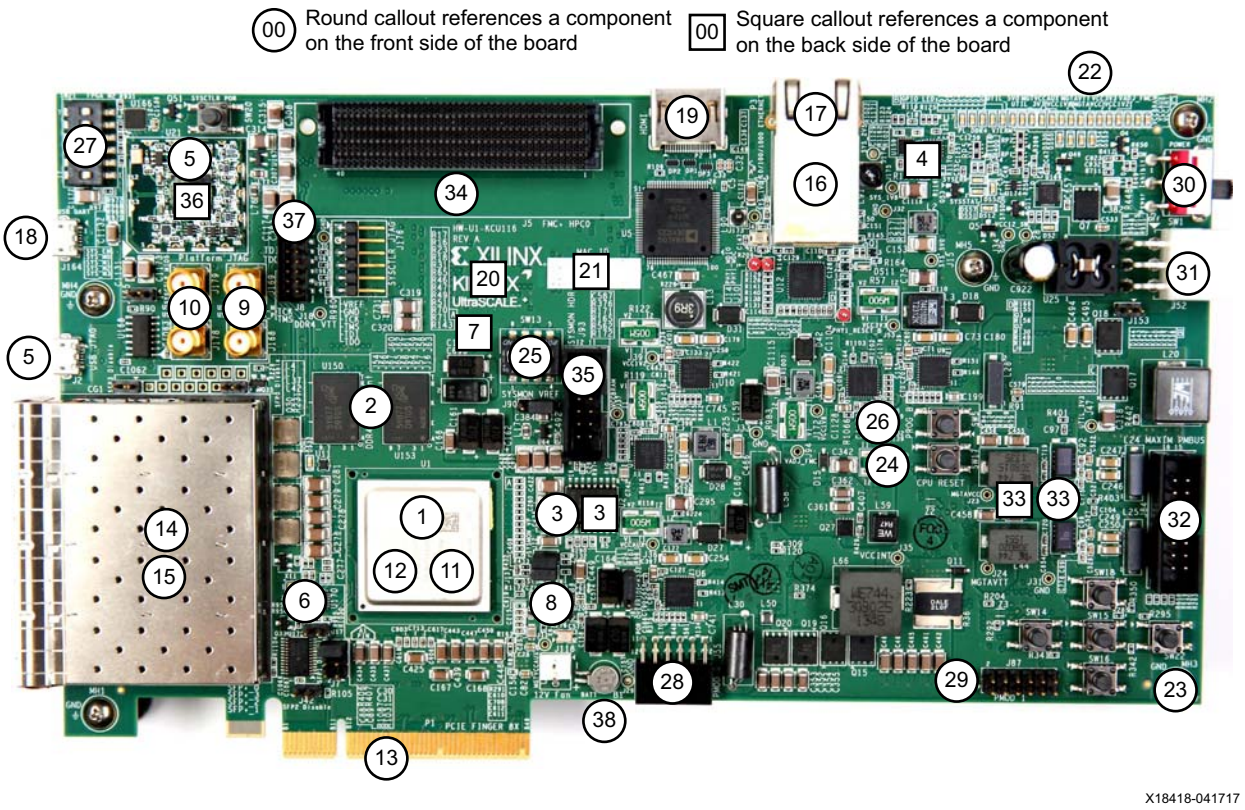

Figure 2-1: **KCU116 Evaluation Board Components**

Table 2-1: **KCU116 Board Component Descriptions**

Callout	Feature	Notes	Schematic Page Number
1	Kintex UltraScale+ XCKU5P-2FFVB676E Device, (with fan-sink on soldered FPGA)	XCKU5P-2FFVB676E Radian XLX041A	
2	DDR4 Component Memory, 1 GB (2x512 MB) (U150, U153)	Micron MT40A256M16GE-075E	18-19
3	Dual Quad SPI Flash Memory (2x256 Mb) (U2-U3)	Micron MT25QU01GBBB8ESF-0SIT U2 on top, U3 on bottom of board	4, 6
4	Micro-SD Card Interface, connector (J177)	Molex 5025700893 on bottom of board	35
5	USB JTAG Interface (U21), with micro-B connector (J2)	Digilent USB JTAG module Hirose ZX62D_AB_5P8	17
6	Clock Generation, multi-output clock generator, SYSCLK and other clocks, 1.8V LVDS (U170)	SI5335A-B02436-GM, four outputs: 300 MHz, 125 MHz, 90 MHz, 33.33 MHz	36
7	Programmable MGT User Clock, I^2C programmable user clock 3.3V LVDS (U56)	Silicon Labs SI570BAB0000544DG (default 156.250 MHz)	37
8	Jitter Attenuated Clock, (U20)	Silicon Labs SI5328C-C-GM	28

Table 2-1: **KCU116 Board Component Descriptions *(Cont'd)***

Callout	Feature	Notes	Schematic Page Number
9	User SMA Clock, user differential SMA clock P/N (J168/J169)	Rosenberger 32K10K-400L5	37
10	User SMA GPIO, user SMA GPIO connectors P/N (J178/J179)	Rosenberger 32K10K-400L5	37
11	GTY Transceivers 224 and 225	Embedded within FPGA U1	10
12	GTY Transceivers 226 and 227	Embedded within FPGA U1	11
13	PCI Express Endpoint Connectivity, PCI Express® connector (P1)	8-lane PCIe® card edge connector	20
14	zSFP/zSFP+ Module Connectors, connector SFP0 (J1), SFP3 (J6) top to bottom	Molex 170382-0001	26
15	zSFP/zSFP+ Module Connectors, connector SFP2 (J4), SFP1 (J3) top to bottom	Molex 170382-0001	27
16	10/100/1000 Mb/s Tri-Speed Ethernet PHY w/RJ45, SGMII mode only, (U12, P3)	TI DP83867ISRGZ Wurth 7499111221A	39
17	Ethernet PHY Status LEDs, LEDs are integrated into P3 bezel	Wurth 7499111221A with integrated status LEDs	39
18	Dual USB-to-UART Bridge, bridge (U166, adjacent to SW21 item 27) with micro-B connector (J164)	Silicon Labs CP2105-F01-GM bridge, Hirose ZX62D-AB-5P8 connector	38
19	HDMI Video Output, HDMI™ codec (U5), HDMI connector (P2)	Analog Devices ADV7511KSTZ-P Molex 47151-0011	29, 30
20	I2C Bus, MUX (U34, U135)	TI TCA9548APWR	42
21	I2C Bus, GPIO peripheral (U147)	TI TCA6416APWR	42
22	User GPIO LEDs, (DS37-DS44)	GPIO LEDs, GREEN 0603 Lumex SML-LX0603GW-TR	40
23	User Pushbuttons, active-High (SW14-SW16, SW18, SW22)	E-Switch TL3301EF100QG in north, south, east, west, center pattern	40
24	CPU Reset Pushbutton, user CPU RESET, active-High (SW17)	E-Switch TL3301EF100QG	40
25	GPIO DIP Switch, 4-pole, active-High (SW13)	C&K SDA04H1SBD	40
26	Program_B Pushbutton Switch, FPGA PROG pushbutton, active-Low (SW5)	E-Switch TL3301EF100QG	3
27	Switches, system controller MODE DIP switch, 6-pole, active-High (SW21)	C&K SDA06H1SBD	34
28	User Pmod GPIO Headers, female right-angle receptacle, 2X6 (J55)	Sullins PPPC062LJBN-RC	41
29	User Pmod GPIO Headers, vertical male header, 2x6 0.1 inch (J87)	Sullins PBC36DAAN	41
30	Power On/Off Slide Switch SW1	C&K 1201M2S3AQE2	44
31	Switches, 12V power input 2x6 connector (J52)	MOLEX-39-30-1060	44

Table 2-1: **KCU116 Board Component Descriptions *(Cont'd)***

Callout	Feature	Notes	Schematic Page Number
32	Monitoring Voltage and Current, 2x8 shrouded PMBus connector (J84)	ASSMAN AWHW16G-0202	43
33	KCU116 Board Power System, power management system (top and bottom)	Maxim MAX15301, MAX15303 and MAX20751 Digital P.O.L. controllers	44-58
34	FMC HPC Connector J5	Samtec ASP_134486_01	21-24
35	SYSMON Header J93, 2X6 shrouded (J93)	Molex 70246-1201	4
36	System Controller Zynq®-7000 AP SoC XC7Z010CLG225 (U161)	XC7Z010CLG225 on bottom of board	31-34
37	USB JTAG Interface, 2x7 2 mm shrouded JTAG cable connector (J8)	Molex 87832-1420	17
38	Encryption Key Battery Backup Circuit (B1)	Seiko TS518FE-FL35E	3

Default Switch and Jumper Settings

Switches

Default switch settings are listed in Table 2-2. Switch locations are shown in Figure 2-1. Table 2-2 also references the respective schematic page numbers.

Table 2-2: **Default Switch Settings**

Switch	Function	Default	Comments	Figure 2-1 Callout	Schematic Page
SW1	SPST slide switch	OFF	Board shipped with power switch off	1	44
SW13	4-pole GPIO DIP	0,0,0,0	Positions 1-4, GPIO	2	40
SW21	6-pole configuration DIP	0,0,0,0,0	Positions 1-5, Zynq-7000 AP SoC System Controller U161	3	34
SW21	6-pole configuration DIP	0	Position 6 FPGA U1 mode M2	3	34

Notes:

1. DIP switches are active-High (connected net is pulled High when DIP switch is closed=1).

Jumpers

Figure 2-2 shows the KCU116 board jumper header locations. Each numbered component shown in the figure is keyed to Table 2-3, which identifies the default jumper settings and references the respective schematic page numbers.

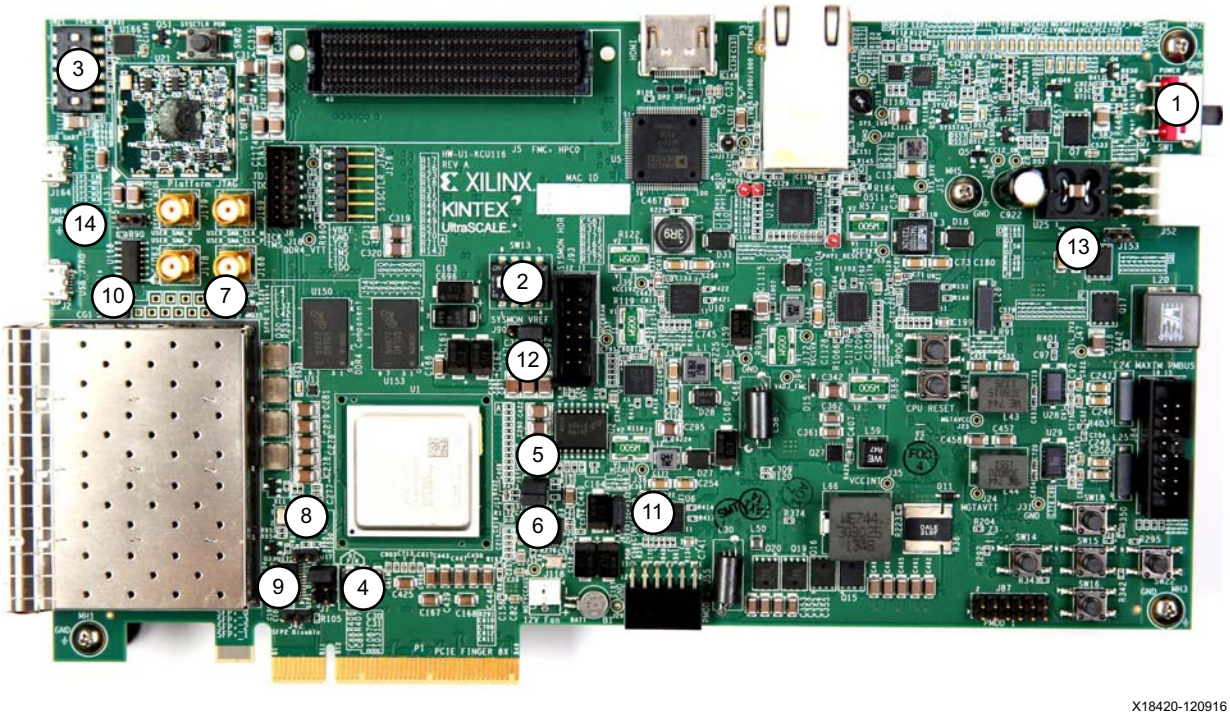

Figure 2-2: **KCU116 Board Header Jumper Locations**

Table 2-3: **Default Jumper Settings**

Jumper	Function	Default	Comments	Figure 2-2 Callout	Schematic Page
J7	PCIe lane size select	5-6	8-lane configuration	4	20
J12	SYSMON_VP	1-2	U1 VP pin P13 pull down 20.5K to GND	5	3
J13	SYSMON_VN	1-2	U1 VN pin R14 pull down 20.5K to GND	6	3
J16	zSFP0 TX enable	Off	Disable zSFP0 TX, allow FPGA control	7	26
J17	zSFP1 TX enable	Off	Disable zSFP1 TX, allow FPGA control	8	26
J42	zSFP2 TX enable	Off	Disable zSFP2 TX, allow FPGA control	9	27
J54	zSFP3 TX enable	Off	Disable zSFP3 TX, allow FPGA control	10	27
J85	POR override	2-3	U1 POR_OVERRIDE pin Y12 to GND	11	3
J90	SYSMON_VREFP select	1-2	SYSMON_VREFP = U64 1.25V VREF	12	3
J153	Maxim regulator inhibit	Off	Used only when programming power system	13	44
J165	System controller boot	Off	On = force Zynq-7000 AP SoC to boot in JTAG mode on power-up or reset	14	32

Installing the KCU116 Board in a PC Chassis

Installation of the KCU116 board inside an ATX-type computer chassis is required when developing or testing PCI Express functionality. When the KCU116 board is installed in the PCIe slot, power is provided from the ATX power supply 4-pin peripheral connector through the ATX adapter cable (Figure 2-3), which is plugged into J52 on the KCU116 board. The Xilinx® part number for this cable is 2600304. See [Ref 35] for ordering information.

Figure 2-3: **ATX Power Supply Adapter Cable**

To install the KCU116 board in a PC chassis:

1. On the KCU116 board, remove the six screws retaining the six rubber feet with their standoffs, and the PCIe bracket. Reinstall the PCIe bracket using two of the previously removed screws.
2. Power down the host computer and remove the power cord from the PC.
3. Open the PC chassis following the instructions provided with the PC.
4. Select a vacant PCIe expansion slot and remove the expansion cover (at the back of the chassis) by removing the screws on the top and bottom of the cover.
5. Plug the KCU116 board into the PCIe connector at this slot.
6. Install the top mounting bracket screw into the PC expansion cover retainer bracket to secure the KCU116 board in its slot.

IMPORTANT: *The KCU116 board is taller than standard PCIe cards. Ensure that the height of the card is free of obstructions.*

7. Connect the ATX power supply to the KCU116 board using the ATX power supply adapter cable as shown in Figure 2-3.
   a. Plug the 6-pin 2 x 3 Molex connector on the adapter cable into J52 on the KCU116 board.
   b. Plug the 4-pin 1 x 4 peripheral power connector from the ATX power supply into the 4-pin adapter cable connector.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J52 on the KCU116 evaluation board. The ATX 6-pin connector has a different pin out than J52. Connecting an ATX 6-pin connector into J52 damages the KCU116 evaluation board and voids the board warranty.*

8. Slide the KCU116 board power switch SW1 to the ON position. The PC can now be powered on.

FPGA Configuration

The KCU116 board supports two of the five UltraScale™ FPGA configuration modes:

- Quad SPI flash memory
- JTAG using:
  - USB JTAG configuration port (Digilent module U21)
  - Platform cable header J8

Each configuration interface corresponds to one or more configuration modes and bus widths, as listed in Table 2-4. The FPGA mode pins M1 and M0 are hard wired to logic 0 and 1, respectively. The FPGA mode pin M2 is wired to SW21 pin 6 (switch position 6), which has the default setting OPEN, enabling the M2 net to be pulled down to logic 0 (e.g., the FPGA default mode setting M[2:0] = 001), selecting the Quad SPI configuration mode.

Table 2-4: **Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	FPGA output
JTAG	101	x1	Not applicable

For complete details on configuring the FPGA, see *UltraScale Architecture Configuration User Guide* (UG570) [Ref 3].

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. Table 2-1, page 10 identifies the components, references the respective schematic page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in Table 2-1, page 10.

Component Descriptions

Kintex UltraScale+ XCKU5P-2FFVB676E Device

[Figure 2-1, callout 1]

The KCU116 board is populated with the Kintex® UltraScale+™ XCKU5P-2FFVB676E device. For more information on Kintex UltraScale+ FPGAs, see *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922) [Ref 1].

Encryption Key Battery Backup Circuit

The XCKU5P device U1 implements bitstream encryption key technology. The KCU116 board provides the encryption key backup battery circuit shown in Figure 3-1. The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCKU5P device U1 VCCBATT pin Y9. The battery supply current I_{BATT} specification is 150 nA maximum when the board power is off. B1 is charged from the SYS_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 KΩ current limit resistor. The nominal charging voltage is 1.42V.

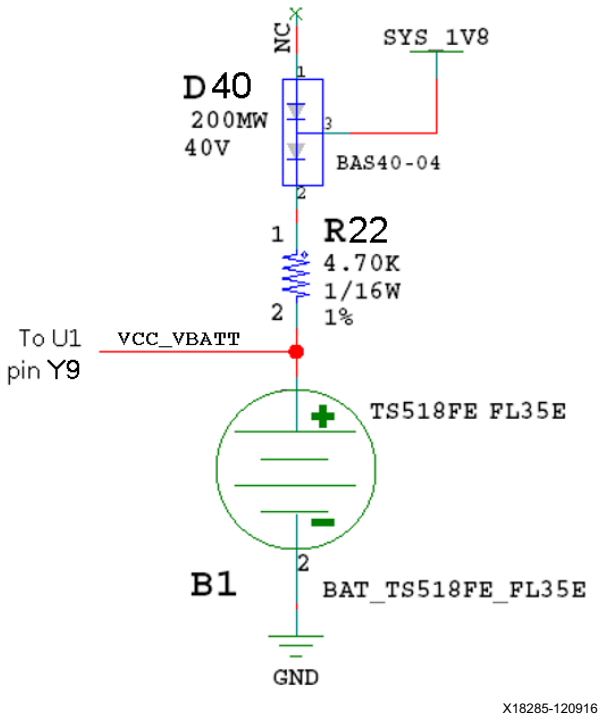

Figure 3-1: **Encryption Key Backup Circuit**

I/O Voltage Rails

There are seven I/O banks available on the XCKU5P device and the KCU116 board. The voltages applied to the FPGA I/O banks (shown in Figure 3-2) used by the KCU116 board are listed in Table 3-1.

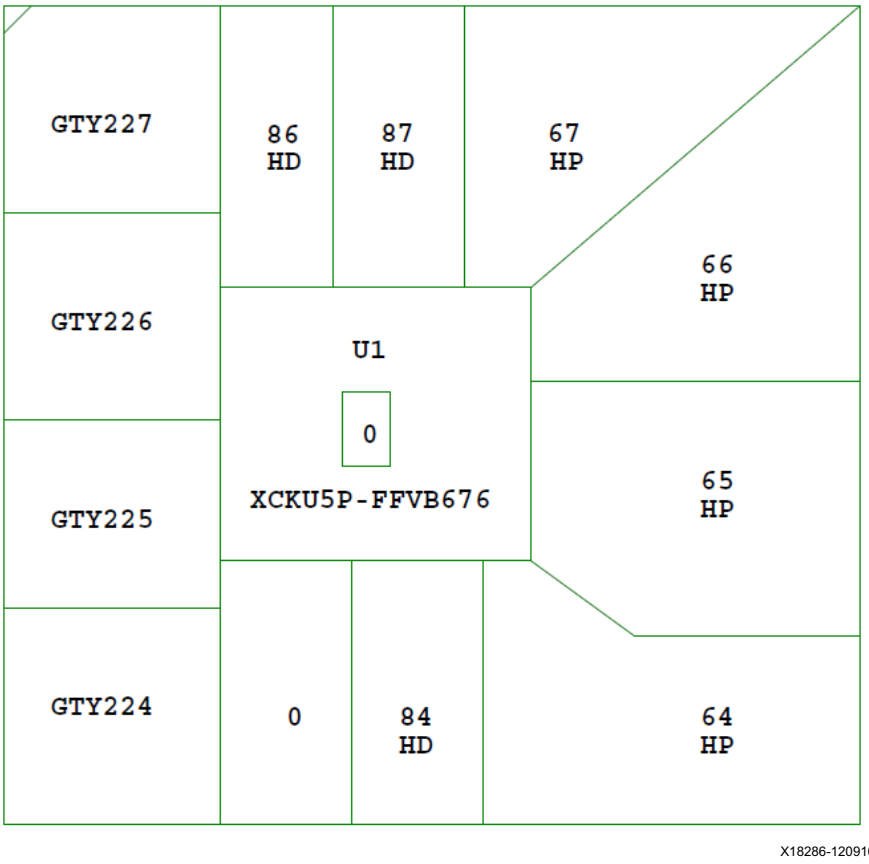

Figure 3-2: **UltraScale+ XCKU5P Bank Locations**

Table 3-1: **I/O Bank Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8	1.8V
HP Bank 64	VADJ_FMC	1.8V (default)
HP Bank 65	VCC1V8	1.8V
HP Bank 66	VCC1V2	1.2V
HP Bank 67	VCC1V2	1.2V
HP Bank 84	VCC3V3	3.3V
HR Bank 86	VCC3V3	3.3V
HR Bank 87	VCC3V3	3.3V

DDR4 Component Memory

[Figure 2-1, callout 2]

The 1 GB DDR4 component memory system is comprised of two 512 MB DDR4 SDRAM devices located at U150 and U153.

- Manufacturer: Micron
- Part Number: MT40A256M16GE-075E
- Description:
  - 4 Gb (256 Mb x 16)
  - 1.2V 96-ball TFBGA
  - DDR4-2666

The KCU116 XCKU5P FPGA DDR memory interface performance is documented in the *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922) [Ref 1].

This memory system is connected to the XCKU5P device HP banks 66 and 67.

The DDR4 0.6V VTT termination voltage (net DDR4_VTT) is sourced from the TI TPS51200DR linear regulator U35. The connections between the DDR4 component memories and XCKU5P device banks 66 and 67 are listed in Table 3-2.

The 1 GB DDR4 component memory system comprises two 512 MB DDR4 SDRAM devices (Micron MT40A256M16GE-075E) located at U150 and U153. This memory system is connected to the XCKU5P device HP banks 66 and 67. The DDR4 0.6V VTT termination voltage (net DDR4_VTT) is sourced from the TI TPS51200DR linear regulator U35. The connections between the DDR4 component memories and XCKU5P device banks 66 and 67 are listed in Table 3-2.

Table 3-2: **DDR4 Memory Connections to the FPGA**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
C22	DDR4_DQ0	POD12_DCI	G2	DQL0	U150
B24	DDR4_DQ1	POD12_DCI	F7	DQL1	U150
C23	DDR4_DQ2	POD12_DCI	H3	DQL2	U150
A24	DDR4_DQ3	POD12_DCI	H7	DQL3	U150
D21	DDR4_DQ4	POD12_DCI	H2	DQL4	U150
B22	DDR4_DQ5	POD12_DCI	H8	DQL5	U150
E21	DDR4_DQ6	POD12_DCI	J3	DQL6	U150
A25	DDR4_DQ7	POD12_DCI	J7	DQL7	U150
A19	DDR4_DQ8	POD12_DCI	A3	DQU0	U150

Table 3-2: **DDR4 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
C17	DDR4_DQ9	POD12_DCI	B8	DQU1	U150
A20	DDR4_DQ10	POD12_DCI	C3	DQU2	U150
B17	DDR4_DQ11	POD12_DCI	C7	DQU3	U150
B20	DDR4_DQ12	POD12_DCI	C2	DQU4	U150
A15	DDR4_DQ13	POD12_DCI	C8	DQU5	U150
B19	DDR4_DQ14	POD12_DCI	D3	DQU6	U150
B15	DDR4_DQ15	POD12_DCI	D7	DQU7	U150
C21	DDR4_DQS0_T	DIFF_POD12_DCI	G3	DQSL_T	U150
B21	DDR4_DQS0_C	DIFF_POD12_DCI	F3	DQSL_C	U150
A17	DDR4_DQS1_T	DIFF_POD12_DCI	B7	DQSU_T	U150
A18	DDR4_DQS1_C	DIFF_POD12_DCI	A7	DQSU_C	U150
A22	DDR4_DM0	POD12_DCI	E7	DML_B/DBIL_B	U150
C18	DDR4_DM1	POD12_DCI	E2	DMU_B/DBIU_B	U150
F18	DDR4_DQ16	POD12_DCI	G2	DQL0	U153
G21	DDR4_DQ17	POD12_DCI	F7	DQL1	U153
F19	DDR4_DQ18	POD12_DCI	H3	DQL2	U153
D20	DDR4_DQ19	POD12_DCI	H7	DQL3	U153
E18	DDR4_DQ20	POD12_DCI	H2	DQL4	U153
D19	DDR4_DQ21	POD12_DCI	H8	DQL5	U153
G20	DDR4_DQ22	POD12_DCI	J3	DQL6	U153
D18	DDR4_DQ23	POD12_DCI	J7	DQL7	U153
H17	DDR4_DQ24	POD12_DCI	A3	DQU0	U153
D16	DDR4_DQ25	POD12_DCI	B8	DQU1	U153
G16	DDR4_DQ26	POD12_DCI	C3	DQU2	U153
D15	DDR4_DQ27	POD12_DCI	C7	DQU3	U153
E15	DDR4_DQ28	POD12_DCI	C2	DQU4	U153
C16	DDR4_DQ29	POD12_DCI	C8	DQU5	U153
H16	DDR4_DQ30	POD12_DCI	D3	DQU6	U153
G17	DDR4_DQ31	POD12_DCI	D7	DQU7	U153
F20	DDR4_DQS2_T	DIFF_POD12_DCI	G3	DQSL_T	U153
E20	DDR4_DQS2_C	DIFF_POD12_DCI	F3	DQSL_C	U153
E16	DDR4_DQS3_T	DIFF_POD12_DCI	B7	DQSU_T	U153
E17	DDR4_DQS3_C	DIFF_POD12_DCI	A7	DQSU_C	U153

Table 3-2: **DDR4 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
H18	DDR4_DM2	POD12_DCI	E7	DML_B/DBIL_B	U153
G15	DDR4_DM3	POD12_DCI	E2	DMU_B/DBIU_B	U153
D25	DDR4_A0	SSTL12	P3	A0	U150, U153
D23	DDR4_A1	SSTL12	P7	A1	U150, U153
D26	DDR4_A2	SSTL12	R3	A2	U150, U153
D24	DDR4_A3	SSTL12	N7	A3	U150, U153
E26	DDR4_A4	SSTL12	N3	A4	U150, U153
C26	DDR4_A5	SSTL12	P8	A5	U150, U153
G22	DDR4_A6	SSTL12	P2	A6	U150, U153
B25	DDR4_A7	SSTL12	R8	A7	U150, U153
F22	DDR4_A8	SSTL12	R2	A8	U150, U153
C24	DDR4_A9	SSTL12	R7	A9	U150, U153
E25	DDR4_A10	SSTL12	M3	A10/AP	U150, U153
F23	DDR4_A11	SSTL12	T2	A11	U150, U153
E23	DDR4_A12	SSTL12	M7	A12/BC_B	U150, U153
B26	DDR4_A13	SSTL12	T8	A13	U150, U153
H26	DDR4_A14_WE_B	SSTL12	L2	WE_B/A14	U150, U153
F25	DDR4_A15_CAS_B	SSTL12	M8	CAS_B/A15	U150, U153
F24	DDR4_A16_RAS_B	SSTL12	L8	RAS_B/A16	U150, U153
H22	DDR4_BA0	SSTL12	N2	BA0	U150, U153
H21	DDR4_BA1	SSTL12	N8	BA1	U150, U153
G26	DDR4_BG0	SSTL12	M2	BG0	U150, U153
J26	DDR4_ACT_B	SSTL12	L3	ACT_B	U150, U153
Pulled LOW	DDR4_TEN	SSTL12	N9	TEN	U150, U153
L24	DDR4_ALERT_B	SSTL12	P9	ALERT_B	U150, U153
J25	DDR4_PAR	SSTL12	T3	PAR	U150, U153
H24	DDR4_ODT	SSTL12	K3	ODT	U150, U153
H23	DDR4_CS_B	SSTL12	L7	CS_B	U150, U153
M24	DDR4_CKE	SSTL12	K2	CKE	U150, U153
L25	DDR4_RESET_B	LVCMOS12	P1	RESET_B	U150, U153
G24	DDR4_CK_T	DIFF_SSTL12_DCI	K7	CK_T	U150, U153
G25	DDR4_CK_C	DIFF_SSTL12_DCI	K8	CK_C	U150, U153

The KCU116 dual DDR4 memory component interface adheres to the constraints guidelines documented in the "DDR3/DDR4 Design Guidelines" section of the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150) [Ref 5]. The KCU116 board DDR4 memory component interface is a 40Ω impedance implementation. For more details about the Micron DDR4 component memory, see the Micron MT40A256M16GE-075E data sheet at the Micron website [Ref 23].

Dual Quad SPI Flash Memory

[Figure 2-1, callout 3]

The Quad SPI flash memory located at U2 and U3 provides 2 x 1 Gb of nonvolatile storage that can be used for configuration and data storage.

- Part number: MT25QU01GBBB8ESF-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 8 bits
- Data rate: variable, depending on single, dual, or quad mode and whether the EMCCLK or the internal CCLK is used (bitstream configurable). See *UltraScale Architecture Configuration User Guide* (UG570) [Ref 3] for more information.

The connections between the SPI flash memories and the XCKU5P device are listed in Table 3-3.

Table 3-3: **Quad SPI Flash Memory Connections to FPGA U1**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Pin Number	Pin Name	Ref. Des.
AD11	QSPI0_DQ0	LVCMOS18	15	DQ0	U2
AC12	QSPI0_DQ1	LVCMOS18	8	DQ1	
AC11	QSPI0_DQ2	LVCMOS18	9	DQ2/VPP/WP_B	
AE11	QSPI0_DQ3	LVCMOS18	1	DQ3/HOLD_B	
Y11	QSPI_CLK	See Note 1	16	C	
AA12	QSPI0_CS_B	LVCMOS18	7	S_B	
N19	QSPI1_DQ0	LVCMOS18	15	DQ0	U3
P23	QSPI1_DQ1	LVCMOS18	8	DQ1	
N23	QSPI1_DQ2	LVCMOS18	9	DQ2/VPP/WP_B	
R21	QSPI1_DQ3	LVCMOS18	1	DQ3/HOLD_B	
Y11	QSPI_CLK	(1)	16	C	
R20	QSPI1_CS_B	LVCMOS18	7	S_B	

Notes:

1. For details on bank 0 pins, see the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 3].

Figure 3-3 shows the linear Quad SPI flash memory circuitry on the KCU116 evaluation board. For more details, see the Micron MT25QU01GBBB8ESF-0SIT data sheet at the Micron website [Ref 23].

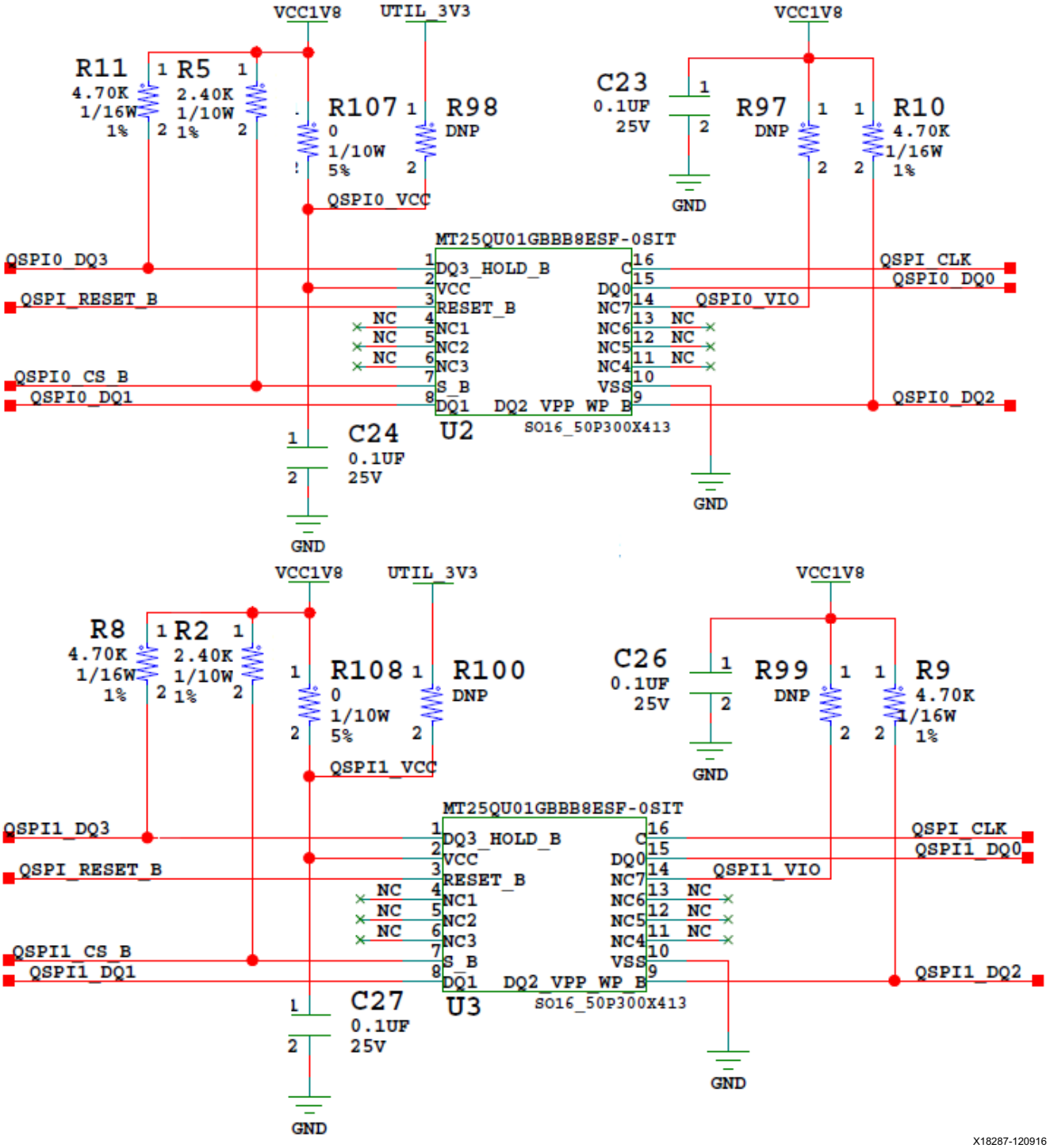

Figure 3-3: **Dual Quad SPI 2 Gb Flash Memory**

Micro-SD Card Interface

[Figure 2-1, callout 4]

The KCU116 board includes a secure digital input/output (SDIO) interface allowing the U161 XC7Z010 Zynq®-7000 SoC system controller access to general purpose nonvolatile micro-SD memory cards and peripherals. The micro-SD card slot is designed to support 50 MHz high speed micro-SD cards. The SDIO signals are connected to U161 XC7Z010 Zynq-7000 SoC system controller bank 500, which has its V_{CCO} set to SYS_1V8 1.8V. A MAX13035E level shifter is used between the XC7Z010 system controller (U161), and the micro-SD card connector (J177). Figure 3-4 shows the connections of the SD card interface on the KCU116 board.

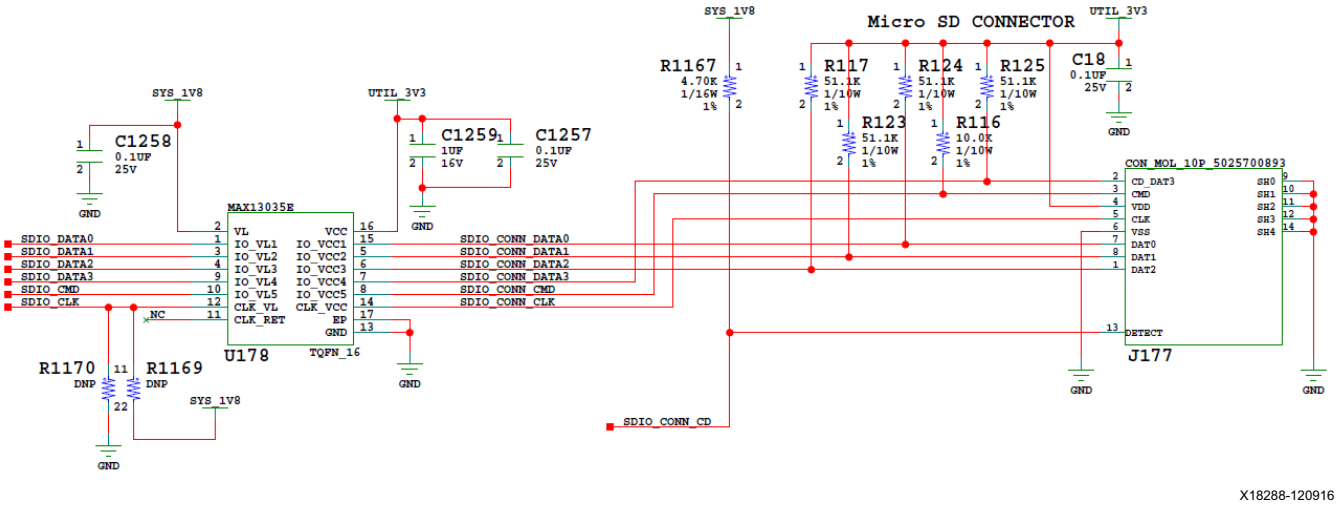

Figure 3-4: **SD Connector Circuit**

The connections between the SD card connector and system controller U161 are listed in Table 3-4.

Table 3-4: **SD Card Connections to System Controller U161**

XC7Z010 (U161)	Schematic Net Name	I/O Standard	Level Shifter (U178)				Schematic Net Name	SDIO Connector (J177)	
			Pin #	Pin Name	Pin Name	Pin #		Pin #	Pin Name
D6	SDIO_DATA0	LVCMOS18	1	IO_VL1	IO_VCC1	15	SDIO_CONN_DATA0	7	DAT0
C6	SDIO_DATA1	LVCMOS18	3	IO_VL2	IO_VCC2	5	SDIO_CONN_DATA1	8	DAT1
B9	SDIO_DATA2	LVCMOS18	4	IO_VL3	IO_VCC3	6	SDIO_CONN_DATA2	1	DAT2
D10	SDIO_DATA3	LVCMOS18	9	IO_VL4	IOVCC4	7	SDIO_CONN_DATA3	2	CD_DAT3
B10	DIO_CMD	LVCMOS18	10	IO_VL5	IO_VCC5	8	SDIO_CONN_CMD	3	CMD
B7	SDIO_CLK	LVCMOS18	12	CLK_VL	CLK_VCC	14	SDIO_CONN_CLK	5	CLK
D8	SDIO_CONN_CD	LVCMOS18	Direct Connect					13	DETECT

For more information on secure digital nonvolatile memory card technology, see the SanDisk [Ref 24] and SD Association [Ref 25] websites.

USB JTAG Interface

[Figure 2-1, callout 5]

JTAG configuration is provided through a Digilent onboard USB-to-JTAG configuration logic module (U21), in which a host computer accesses the KCU116 board JTAG chain through a type-A (host side) to micro-B (KCU116 board side J2) USB cable.

A 2 mm JTAG header (J8) is also provided in parallel for access by Xilinx® download cables, such as the Platform Cable USB II and the Parallel Cable IV. JTAG configuration is allowed at any time regardless of the FPGA mode pin settings. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pin M2 (which is wired to DIP SW21 pin 6, switch position 6). The JTAG chain of the KCU116 board is shown in Figure 3-5. For more details about the Digilent USB JTAG module, see the Digilent website [Ref 26].

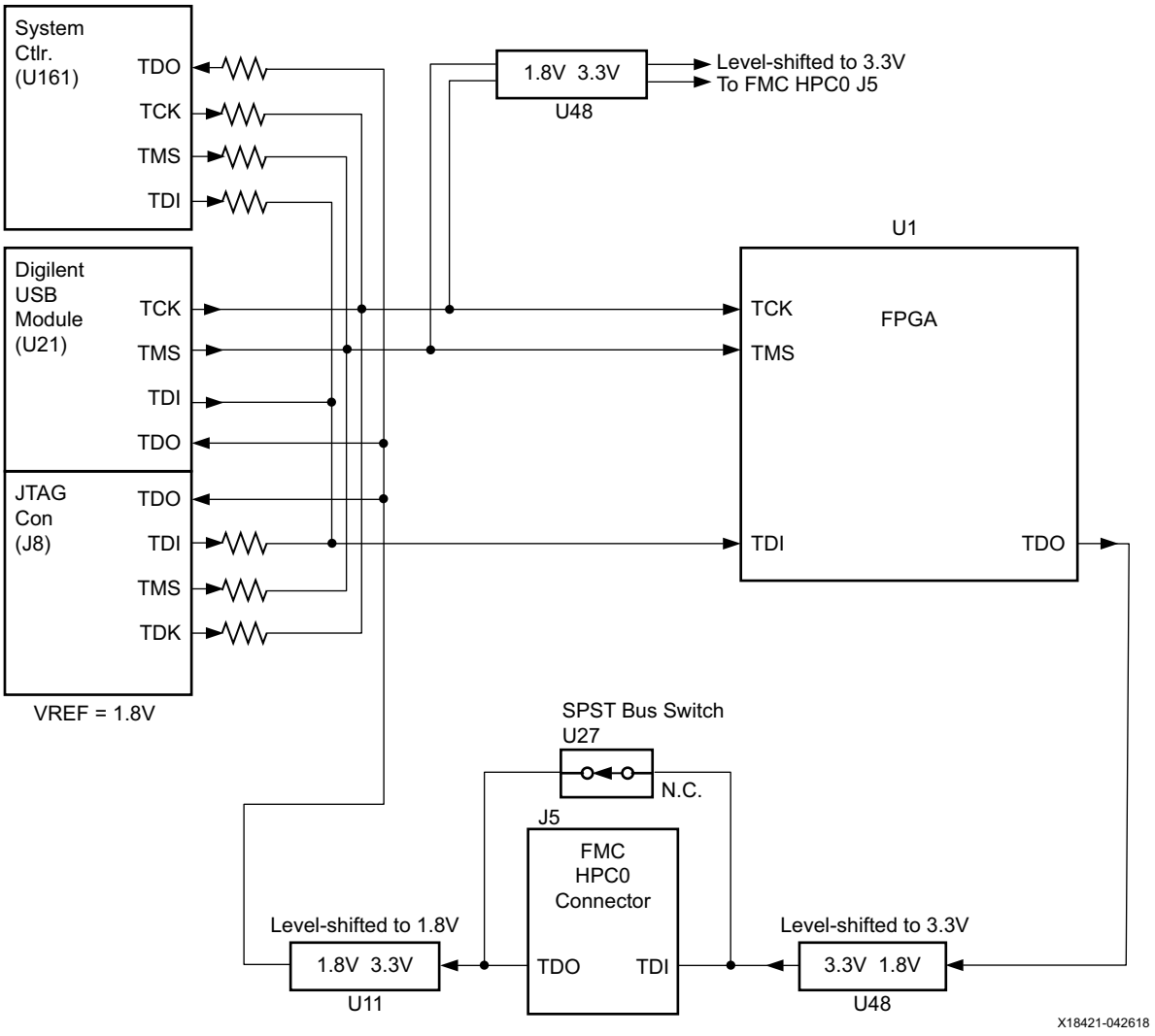

Figure 3-5: **JTAG Chain Block Diagram**

FMC Connector JTAG Bypass

When an FMC is attached to the KCU116 board, it is automatically added to the JTAG chain through an electronically controlled single-pole single-throw (SPST) switch U27. The SPST switch is in a normally closed state and transitions to an open state when the FMC is attached to J5. Switch U27 adds an attached HPC FMC to the FPGAs JTAG chain as determined by the FMC_HSPC0_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection through a device or bypass jumper to ensure that the JTAG chain connects to the FPGA U1.

Clock Generation

[Figure 2-1, callout 6]

The KCU116 evaluation board provides eight clock sources to the XCKU5P device as listed in Table 3-5.

Table 3-5: **KCU116 Board Clock Sources**

Clock Name	Clock Ref. Des.	Description
System clock 300 MHz	U170	Silicon Labs Si5335A 1.8V LVDS any frequency quad clock generator CLK0. See System Clock (SYSCLK_300_P and SYSCLK_300_N).
System clock 125 MHz	U170	Silicon Labs Si5335A 1.8V LVDS any frequency quad clock generator CLK1. See System Clock (CLK_125MHZ).
EMC clock 90 MHz	U170	Silicon Labs Si5335A 1.8V LVCMOS single-ended any frequency quad clock generator CLK2. See System Clock (FPGA_EMCCLK).
System control clock 33.333 MHz	U170	Silicon Labs Si5335A 1.8V LVCMOS single-ended any frequency quad clock generator CLK3. See System Clock (SYSCTLR_CLK).
User MGT clock 10 MHz–810 MHz	U56	Silicon Labs Si570 3.3V LVDS I^2C programmable oscillator, 156.250 MHz default. (USER_MGT_SI570_CLOCK_P and USER_MGT_SI570_CLOCK_N).
User SMA clock	J168(P), J169(N)	User clock input SMAs. See User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N).
Jitter attenuated clock	U20	Silicon Labs Si5328C LVDS precision clock multiplier/jitter attenuator. See Jitter Attenuated Clock (SFP_SI5328_OUT_P and SFP_SI5328_OUT_N).
Video clock 74.25 MHz	U179	Silicon Labs Si511 3.3V LVDS fixed frequency oscillator. See Video Clock (CLK_74_25_P and CLK_74_25_N).

Table 3-6 lists the FPGA connections for each clock.

Table 3-6: **KCU116 Clock Sources to XCKU5P FPGA U1 Connections**

Clock Source Ref.Des. and Pin	Schematic Net Name	I/O Standard	XCKU5P FPGA (U1) Pin
U170.22	SYSCLK_300_P(1)	LVDS	K22
U170.21	SYSCLK_300_N(1)	LVDS	K23
U170.18	CLK_125MHZ_P	LVDS	G12
U170.17	CLK_125MHZ_N	LVDS	F12
U170.14	FPGA_EMCCLK(2)	LVCMOS18	N21
U170.10	SYSCTLR_CLK(2)	LVCMOS18	U161.C7
U56.4	USER_MGT_SI570_CLOCK_P(1)	LVDS	M7
U56.5	USER_MGT_SI570_CLOCK_N(1)	LVDS	M6
J168.1	USER_SMA_CLOCK_P	LVDS	J23
J169.1	USER_SMA_CLOCK_N	LVDS	J24
U20.28	SFP_SI5328_OUT_P(1)	LVDS	P7
U20.29	SFP_SI5328_OUT_N(1)	LVDS	P6
U179.4	CLK_74_25_P	LVDS	D11
U179.5	CLK_74_25_N	LVDS	D10

Notes:
1. AC capacitively coupled, MGT connections I/O standard not applicable.
2. Series resistor terminated.

System Clock

[Figure 2-1, callout 6]

The system clock source is a Silicon Labs SI5335A quad clock generator/buffer (U170). The system clock (SYSCLK) is a LVDS 300 MHz clock sourced from the CLK0A output pair of U170. SYSCLK is wired to a clock capable (GC) input on programmable logic bank 66. The signal pair named SYSCLK_300_P and SYSCLK_300_N are connected to XCKU5P FPGA U1 (bank 66 pins K22 and K23, respectively).

- Clock generator: Silicon Labs SI5335A-B03426-GM (CLK0A 300 MHz)
- Low phase jitter of 0.7 pS RMS
- LVDS differential output

The system clock circuit is shown in Figure 3-6.

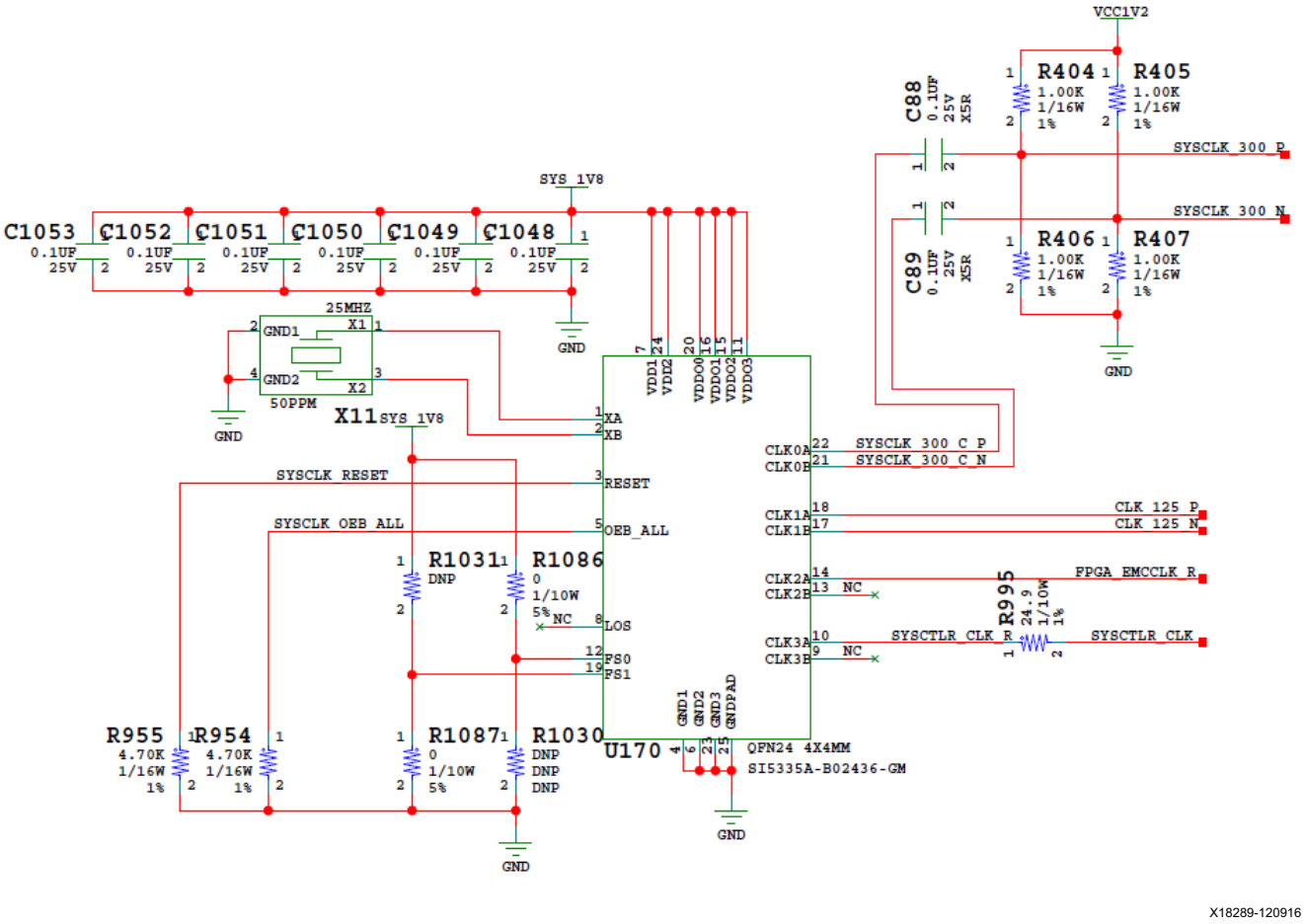

Figure 3-6: **KCU116 System Clock**

Three additional clocks are sourced from the U170 quad clock generator:

- 125 MHz LVDS signal pair CLK_125MHZ_P and CLK_125MHZ_N, connected to XCKU5P FPGA U1 bank 87 pins G12 and F12, respectively.
- 90.0 MHz single-ended 1.8V LVCMOS, series resistor coupled FPGA_EMCCLK, connected to XCKU5P FPGA U1 bank 65 dedicated EMCCLK input pin N21.
- 33.3333 MHz single-ended 1.8V LVCMOS, series resistor coupled SYSCTLR_CLK, connected to system controller XC7Z010 Zynq-7000 SoC U161 bank 500 dedicated PS_CLK input pin C7.

Programmable MGT User Clock

[Figure 2-1, callout 7]

The KCU116 evaluation board has a SI570 programmable low-jitter 3.3V LVDS differential oscillator (U56) connected (series capacitor AC coupled) to the FPGA U1 MGTY226 MGTREFCLK1 P/N inputs (pin M7 (P) and M6 (N)).

On power-up, the SI570 user clock defaults to an output frequency of 156.250 MHz. User applications or the system controller can change the output frequency within the range of 10 MHz to 810 MHz through an I^2C interface. Power cycling the KCU116 evaluation board resets the user clock to the default frequency of 156.250 MHz. The system controller can be configured to reprogram the Si570 U56 to a saved frequency immediately after board power-up.

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz-810 MHz)
- Frequency jitter: 50 ppm
- 3.3V LVDS differential output

The user MGT clock circuit is shown in Figure 3-7.

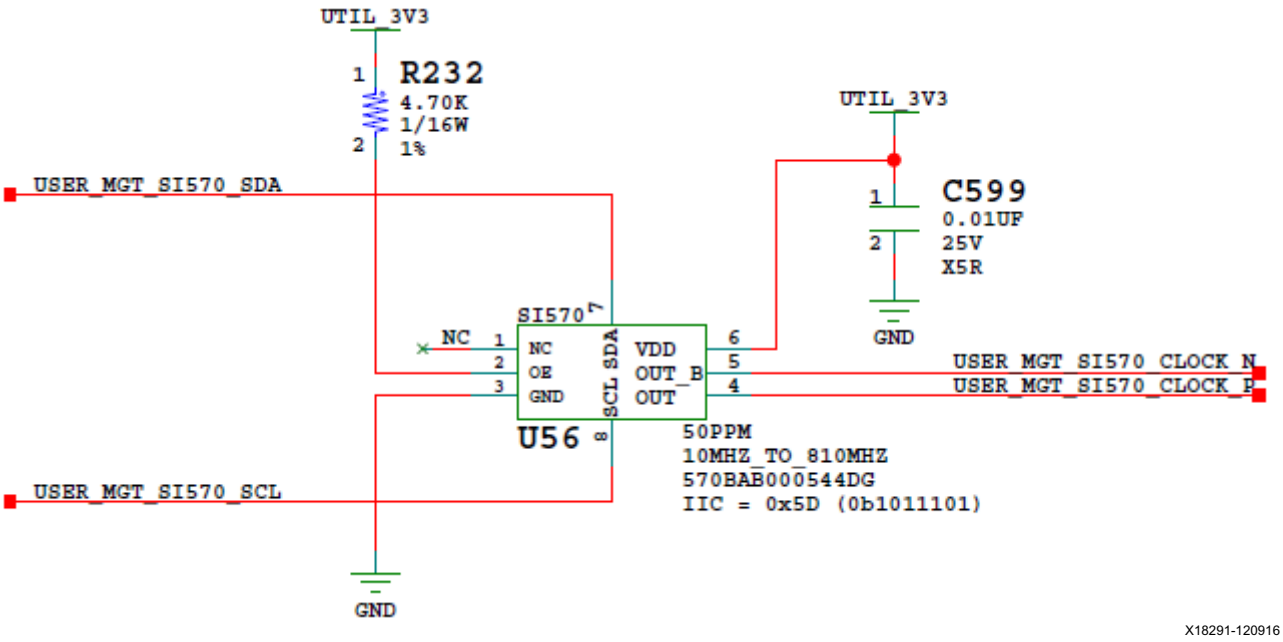

Figure 3-7: **KCU116 Board User Clocks**

User SMA Clock

[Figure 2-1, callout 9]

The KCU116 board provides a pair of SMAs for differential user clock input into FPGA U1 bank 66 (see Figure 3-8). The P-side SMA J168 signal USER_SMA_CLOCK_P is connected to U1 GC pin J23, with the N-side SMA J169 signal USER_SMA_CLOCK_N connected to U1 GC pin J24. Bank 66 V_{CCO} is 1.2V VCC1V2. The USER_SMA_CLOCK input voltage swing should not exceed 1.2V.

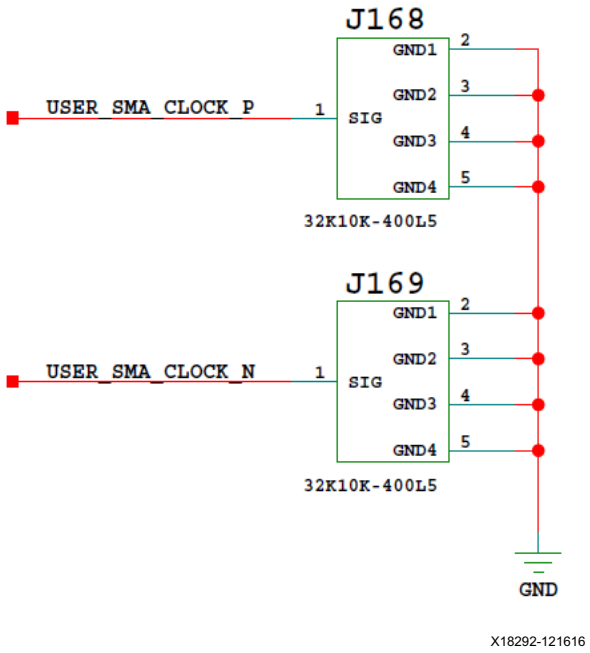

Figure 3-8: **User SMA Clock**

Jitter Attenuated Clock

[Figure 2-1, callout 8]

The KCU116 board includes a Silicon Labs SI5328C jitter attenuator U20. FPGA U1 user logic can implement a clock recovery circuit and then output this clock from a differential pair on I/O bank 84 (SFP_REC_CLOCK_P, FPGA U1 pin AB15 and SFP_REC_CLOCK_N, U1 pin AAB16) for jitter attenuation. The jitter attenuated clock (SFP_SI5328_OUT_P (U20 pin 28), SFP_SI5328_OUT_N (U20 pin 29)) is then routed as a series capacitor coupled reference clock to GTY Quad 226 inputs MGTREFCLK1P (U1 pin M7) and MGTREFCLK1N (U1 pin M6).

The primary purpose of this clock is to support common packet radio interface (CPRI™) or open base station architecture initiative (OBSAI) applications. These applications perform clock recovery from a user-supplied small form-factor pluggable (SFP/SFP+) module, and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTH transceiver. The jitter attenuated clock is shown in Figure 3-9.

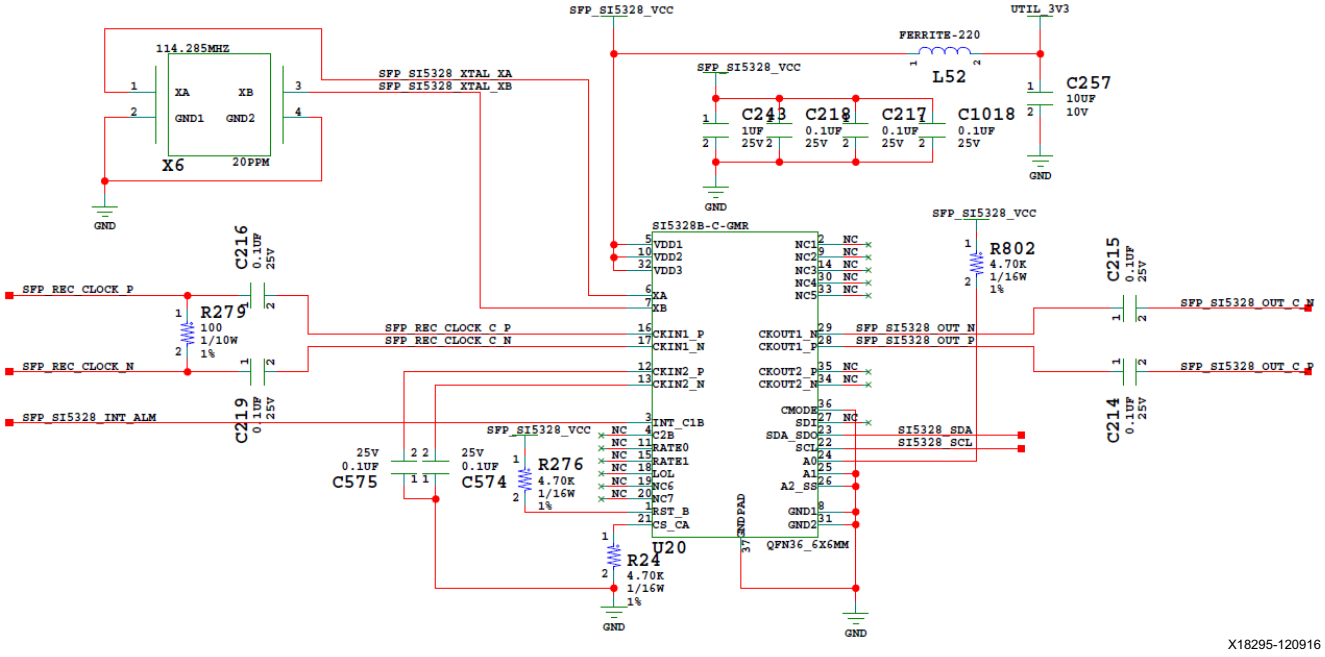

Figure 3-9: **Jitter Attenuated Clock**

Video Clock

[Figure 2-1, near callout 6, bottom of board]

The KCU116 evaluation board has a SI511B low-jitter 3.3V LVDS fixed frequency 74.25 MHz differential LVDS oscillator (U179) connected to the FPGA U1 bank 86 inputs pin D11 (P) and D10 (N).

- Fixed frequency oscillator: Silicon Labs Si511BBA74M2500BAG (74.25 MHz)
- Frequency jitter: 50 ppm
- 3.3V LVDS differential output

The video clock circuit is shown in Figure 3-10.

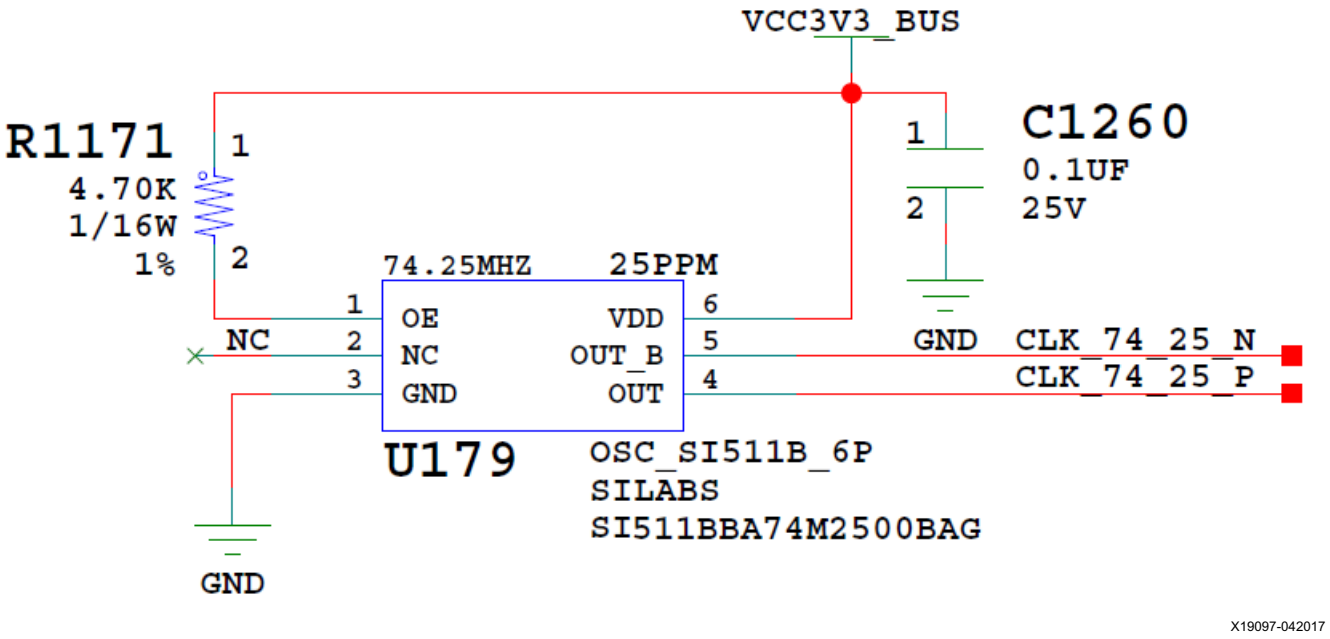

Figure 3-10: **Video Clock**

For more details on the Silicon Labs SI5335A, SI570, SI53340, SI5328C, and SI511B devices, see the Silicon Labs website [Ref 27].

See *UltraScale Architecture Clocking Resources User Guide* (UG572) [Ref 6] for UltraScale™ FPGA clocking information.

GTY Transceivers

[Figure 2-1, callouts 11, 12]

The KCU116 board provides access to 16 GTY transceivers:

- Eight of the GTY transceivers are wired to PCI Express® x8 edge connector (P1)
- Four of the GTY transceivers are wired to FMC HPC0 connector (J5)
- Four of the GTY transceivers are wired to zSFP/zSFP+ module connectors (J1, J3, J4, J6)

The GTY transceivers in the XCKU5P are grouped into four channels or quads. The reference clock for a quad can be sourced from the quad above or the quad below the GTY quad of interest. There are four GTY quads on the KCU116 board with connectivity as listed here (see Figure 3-11):

Quad 224:

- MGTREFCLK0 - not connected
- MGTREFCLK1 - not connected
- Contains four GTY transceivers allocated to PCIe® lanes 4-7

Quad 225:

- MGTREFCLK0 - PCIE_CLK_Q0_P/N PCIe edge connector clock
- MGTREFCLK1 - not connected
- Contains four GTY transceivers allocated to PCIe lanes 0-3

Quad 226:

- MGTREFCLK0 - SFP_SI5328_OUT_C_P/N
- MGTREFCLK1 - USER_MGT_SI570_CLOCK_C_P/N
- Contains four GTY transceivers allocated to zSFP modules 0-3

Quad 227:

- MGTREFCLK0 - FMC_HPC0_GBTCLK0_M2C_C_P/N
- MGTREFCLK1 - FMC_HPC0_GBTCLK1_M2C_C_P/N
- Contains four GTY transceivers allocated to FMC_HPC0_DP[3:0]

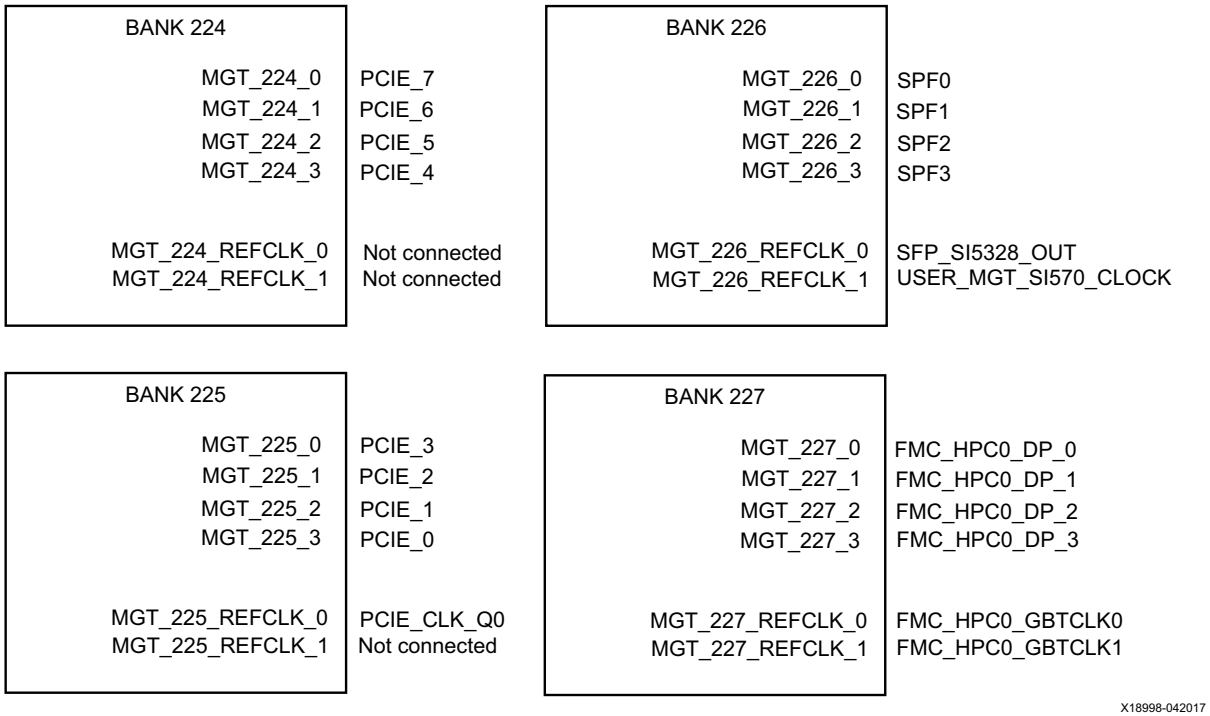

Figure 3-11: **GTY Bank Assignments**

Table 3-7 lists the GTY Banks 224 and 225 interface connections between FPGA U1 and 8-lane PCIe connector P1.

Table 3-7: **KCU116 FPGA U1 GTY Banks 224 and 225 Connections to PCIe Connector P1**

Transceiver Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 224	AFY	MGTYTXP0_224	PCIE_TX7_P(1)	A47	PERp7	PCIe Edge Connector P1
	AF6	MGTYTXN0_224	PCIE_TX7_N(1)	A48	PERn7	
	AF2	MGTYRXP0_224	PCIE_RX7_P	B45	PETp7	
	AF1	MGTYRXN0_224	PCIE_RX7_N	B46	PETn7	
	AE9	MGTYTXP1_224	PCIE_TX6_P(1)	A43	PERp6	
	AE8	MGTYTXN1_224	PCIE_TX6_N(1)	A44	PERn6	
	AE4	MGTYRXP1_224	PCIE_RX6_P	B41	PETp6	
	AE3	MGTYRXN1_224	PCIE_RX6_N	B42	PETn6	
	AD7	MGTYTXP2_224	PCIE_TX5_P(1)	A39	PERp5	
	AD6	MGTYTXN2_224	PCIE_TX5_N(1)	A40	PERn5	
	AD2	MGTYRXP2_224	PCIE_RX5_P	B37	PETp5	
	AD1	MGTYRXN2_224	PCIE_RX5_N	B38	PETn5	
	AC5	MGTYTXP3_224	PCIE_TX4_P(1)	A35	PERp4	
	AC4	MGTYTXN3_224	PCIE_TX4_N(1)	A36	PERn4	
	AB2	MGTYRXP3_224	PCIE_RX4_P	B33	PETp4	
	AB1	MGTYRXN3_224	PCIE_RX4_N	B34	PETn4	
	ABY	MGTREFCLK0P_224	NC	NA	NA	
	AB6	MGTREFCLK0N_224	NC	NA	NA	
	Y7	MGTREFCLK1P_224	NC	NA	NA	
	Y6	MGTREFCLK1N_224	NC	NA	NA	

Table 3-7: **KCU116 FPGA U1 GTY Banks 224 and 225 Connections to PCIe Connector P1 *(Cont'd)***

Transceiver Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 225	AA5	MGTYTXP0_225	PCIE_TX3_P(1)	A29	PERp3	PCIe Edge Connector P1
	AA4	MGTYTXN0_225	PCIE_TX3_N(1)	A30	PERn3	
	Y2	MGTYRXP0_225	PCIE_RX3_P	B27	PETp3	
	Y1	MGTYRXN0_225	PCIE_RX3_N	B28	PETn3	
	W5	MGTYTXP1_225	PCIE_TX2_P(1)	A25	PERp2	
	W4	MGTYTXN1_225	PCIE_TX2_N(1)	A26	PERn2	
	V2	MGTYRXP1_225	PCIE_RX2_P	B23	PETp2	
	V1	MGTYRXN1_225	PCIE_RX2_N	B24	PETn2	
	U5	MGTYTXP2_225	PCIE_TX1_P(1)	A21	PERp1	
	U4	MGTYTXN2_225	PCIE_TX1_N(1)	A22	PERn1	
	T2	MGTYRXP2_225	PCIE_RX1_P	B19	PETp1	
	T1	MGTYRXN2_225	PCIE_RX1_N	B20	PETn1	
	R5	MGTYTXP3_225	PCIE_TX0_P(1)	A16	PERp0	
	R4	MGTYTXN3_225	PCIE_TX0_N(1)	A17	PERn0	
	P2	MGTYRXP3_225	PCIE_RX0_P	B14	PETp0	
	P1	MGTYRXN3_225	PCIE_RX0_N	B15	PETn0	
	V7	MGTREFCLK0P_225	PCIE_CLK_QO_P(1)	A13	REFCLK+	
	V6	MGTREFCLK0N_225	PCIE_CLK_QO_N(1)	A14	REFCLK-	
	T7	MGTREFCLK1P_225	NC	NA	NA	
	T6	MGTREFCLK1N_225	NC	NA	NA	

Notes:

1. Series capacitor AC coupled.
2. MGT connections I/O standard not applicable.

Table 3-8 lists the GTY Bank 226 interface connections between FPGA U1 and the four zSFP connectors J1, J3, J4 and J6.

Table 3-8: **KCU116 FPGA U1 GTY Bank 226 Connections**

GTY Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 226	N5	MGTYTXP0_226	SFP0_TX_P	18	TD_P	SFP0 J1
	N4	MGTYTXN0_226	SFP0_TX_N	19	TD_N	
	M2	MGTYRXP0_226	SFP0_RX_P	13	RD_P	
	M1	MGTYRXN0_226	SFP0_RX_N	12	RD_N	
	L5	MGTYTXP1_226	SFP1_TX_P	18	TD_P	SFP1 J3
	L4	MGTYTXN1_226	SFP1_TX_N	19	TD_N	
	K2	MGTYRXP1_226	SFP1_RX_P	13	RD_P	
	K1	MGTYRXN1_226	SFP1_RX_N	12	RD_N	
	J5	MGTYTXP2_226	SFP2_TX_P	18	TD_P	SFP2 J4
	J4	MGTYTXN2_226	SFP2_TX_N	19	TD_N	
	H2	MGTYRXP2_226	SFP2_RX_P	13	RD_P	
	H1	MGTYRXN2_226	SFP2_RX_N	12	RD_N	
	G5	MGTYTXP3_226	SFP3_TX_P	18	TD_P	SFP3 J6
	G4	MGTYTXN3_226	SFP3_TX_N	19	TD_N	
	F2	MGTYRXP3_226	SFP3_RX_P	13	RD_P	
	F1	MGTYRXN3_226	SFP3_RX_N	12	RD_N	
	P7	MGTREFCLK0P_226	SFP_SI5328_OUT_C_P(1)	28	CKOUT1_P	SI5328B U20
	P6	MGTREFCLK0N_226	SFP_SI5328_OUT_C_N(1)	29	CKOUT1_N	
	M7	MGTREFCLK1P_226	USER_MGT_SI570_CLOCK_C_P(1)	4	OUT	SI570 U56
	M6	MGTREFCLK1N_226	USER_MGT_SI570_CLOCK_C_N(1)	5	OUT_B	

Notes:

1. Series capacitor AC coupled.
2. MGT connections I/O standard not applicable.

Table 3-9 lists the GTY Bank 227 interface connections between FPGA U1 and FMC HPC0 connector J5

Table 3-9: **KCU116 FPGA U1 GTY Bank 227 Connections**

GTY Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 227	F7	MGTYTXP0_227	FMC_HPC_DP0_C2M_P	C2	DP0_C2M_P	FMC HPC0 J5
	F6	MGTYTXN0_227	FMC_HPC_DP0_C2M_N	C3	DP0_C2M_N	
	D2	MGTYRXP0_227	FMC_HPC_DP0_M2C_P	C6	DP0_M2C_P	
	D1	MGTYRXN0_227	FMC_HPC_DP0_M2C_N	C7	DP0_M2C_N	
	E5	MGTYTXP1_227	FMC_HPC_DP1_C2M_P	A22	DP1_C2M_P	
	E4	MGTYTXN1_227	FMC_HPC_DP1_C2M_N	A23	DP1_C2M_N	
	C4	MGTYRXP1_227	FMC_HPC_DP1_M2C_P	A2	DP1_M2C_P	
	C3	MGTYRXN1_227	FMC_HPC_DP1_M2C_N	A3	DP1_M2C_N	
	D7	MGTYTXP2_227	FMC_HPC_DP2_C2M_P	A26	DP2_C2M_P	
	D6	MGTYTXN2_227	FMC_HPC_DP2_C2M_N	A27	DP2_C2M_N	
	B2	MGTYRXP2_227	FMC_HPC_DP2_M2C_P	A6	DP2_M2C_P	
	B1	MGTYRXN2_227	FMC_HPC_DP2_M2C_N	A7	DP2_M2C_N	
	B7	MGTYTXP3_227	FMC_HPC_DP3_C2M_P	A30	DP3_C2M_P	
	B6	MGTYTXN3_227	FMC_HPC_DP3_C2M_N	A31	DP3_C2M_N	
	A4	MGTYRXP3_227	FMC_HPC_DP3_M2C_P	A10	DP3_M2C_P	
	A3	MGTYRXN3_227	FMC_HPC_DP3_M2C_N	A11	DP3_M2C_N	
	K7	MGTREFCLK0P_227	FMC_HPC_GBTCLK0_M2C_C_P(1)	D4	GBTCLK0_M2C_P	
	K6	MGTREFCLK0N_227	FMC_HPC_GBTCLK0_M2C_C_N(1)	D5	GBTCLK0_M2C_N	
	H7	MGTREFCLK1P_227	FMC_HPC_GBTCLK1_M2C_C_P(1)	B20	GBTCLK1_M2C_P	
	H6	MGTREFCLK1N_227	FMC_HPC_GBTCLK1_M2C_C_N(1)	B21	GBTCLK1_M2C_N	

Notes:

1. Series capacitor AC coupled.
2. MGT connections I/O standard not applicable.

For additional information on GTY transceivers, see *UltraScale Architecture GTY Transceivers User Guide* (UG578) [Ref 7]. Also see *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182) [Ref 8]. For additional information about UltraScale PCIe functionality, see *UltraScale Devices Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide for Vivado Design Suite* (PG156) [Ref 18]. For additional information about the PCI Express standard, see [Ref 28].

PCI Express Endpoint Connectivity

[Figure 2-1, callout 13]

The 8-lane PCI Express edge connector P1 performs data transfers at the rate of 2.5 GT/s for Gen1 applications, 5.0 GT/s for Gen2 applications, and 8.0 GT/s for Gen3 applications. The PCIe transmit and receive signal data paths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair. See Table 3-7 for PCIe P1 to FPGA U1 connectivity details.

The XCKU5P-2FFVB676E device (-2 speed grade) included with the KCU116 board supports up to Gen3 x8.

The PCIe clock is input from the P1 edge connector. It is AC coupled to FPGA U1 through the MGTREFCLK0 pins of Quad 225. PCIE_CLK_Q0_P is connected to U1 pin V7, and the _N net is connected to pin V6. The PCI Express clock circuit is shown in Figure 3-12.

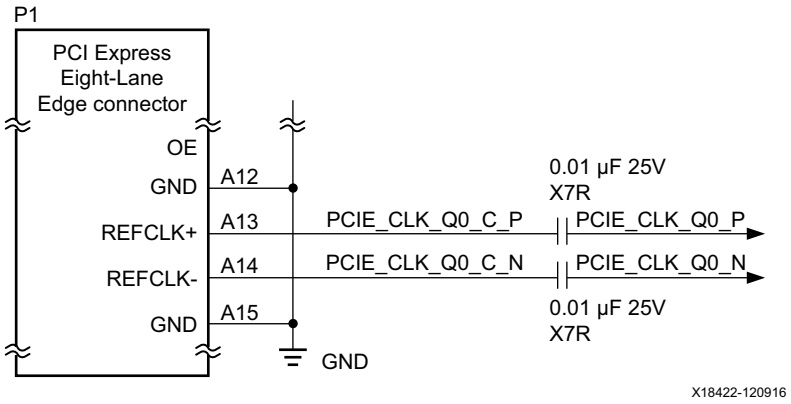

Figure 3-12: **PCI Express Clock**

The PCIe lane width/size is selected by jumper J7 shown in Figure 3-13. The default lane size selection is 8-lane (J7 pins 5 and 6 jumpered).

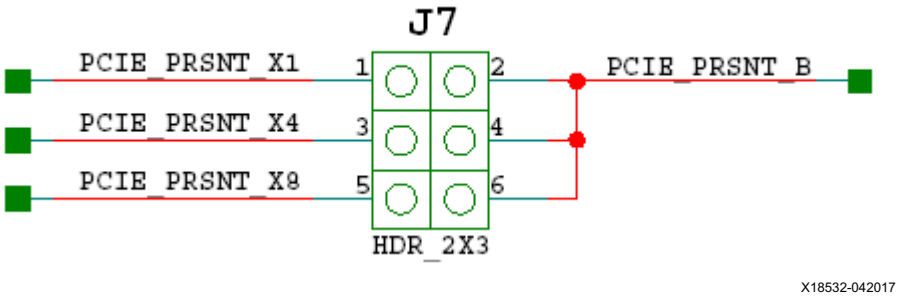

Figure 3-13: **PCI Express Lane Size Select Jumper J7**

Table 3-7, page 37 lists the PCIe P1 edge connector wiring to FPGA U1.

zSFP/zSFP+ Module Connectors

[Figure 2-1, callouts 14, 15]

The KCU116 board hosts four zSFP/zSFP+ J1, J3, J4, and J6 that accept zSFP or zSFP+ modules. The connectors are housed within a single quad zSFP cage assembly. Figure 3-14 shows the zSFP/zSFP+ module connector circuitry typical of the four implementations.

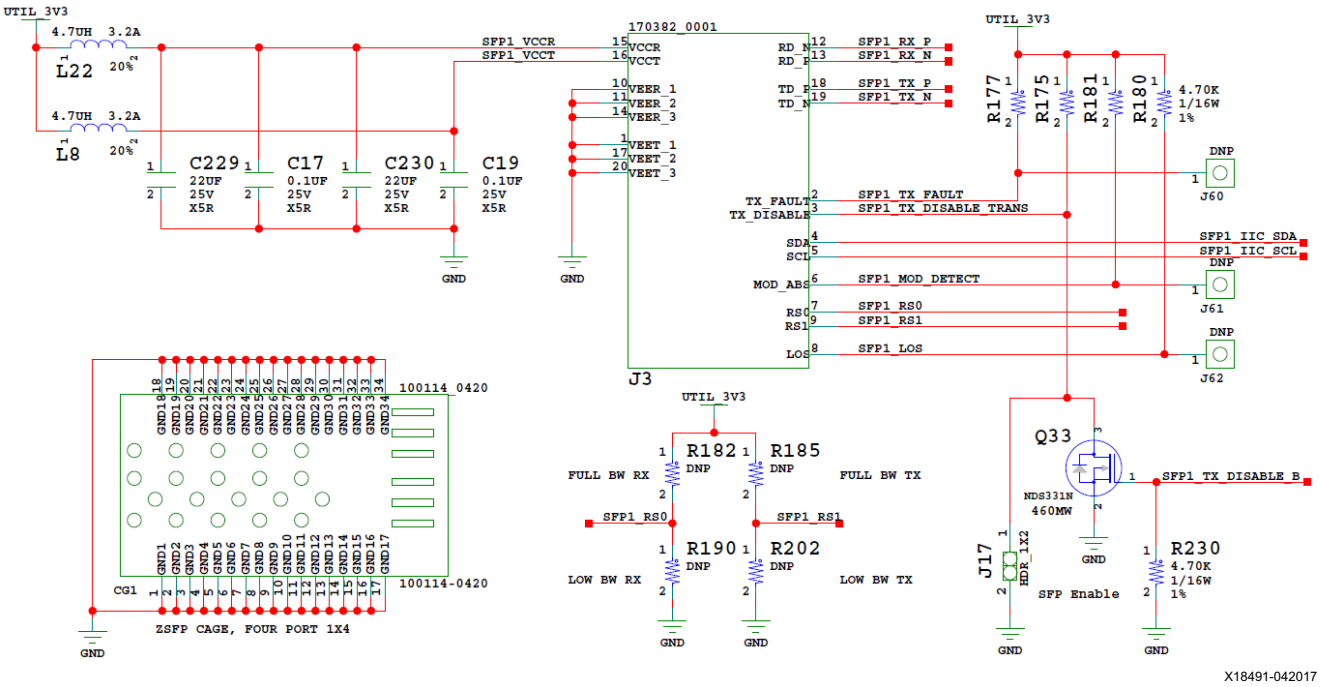

Figure 3-14: **zSFP/zSFP+ Module Connector**

Table 3-10 lists the zSFP+ module connections to FPGA U1.

Table 3-10: **KCU116 FPGA U1 to zSFP0-zSFP3 Module Connections**

FPGA (U1) Pin	Schematic Net Name	Pin Number	Pin Name	SFP/SFP+ Module
M2	SFP0_RX_P	13	RD_P	zSFP0 J1
M1	SFP0_RX_N	12	RD_N	
N5	SFP0_TX_P	18	TD_P	
N4	SFP0_TX_N	19	TD_N	
AB14	SFP0_TX_DISABLE_B	3	TX_DISABLE	

Table 3-10: **KCU116 FPGA U1 to zSFP0-zSFP3 Module Connections *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	Pin Number	Pin Name	SFP/SFP+ Module
K2	SFP1_RX_P	13	RD_P	zSFP1 J3
K1	SFP1_RX_N	12	RD_N	
L5	SFP1_TX_P	18	TD_P	
L4	SFP1_TX_N	19	TD_N	
AA14	SFP1_TX_DISABLE_B	3	TX_DISABLE	
H2	SFP2_RX_P	13	RD_P	zSFP2 J4
H1	SFP2_RX_N	12	RD_N	
J5	SFP2_TX_P	18	TD_P	
J4	SFP2_TX_N	19	TD_N	
AA15	SFP2_TX_DISABLE_B	3	TX_DISABLE	
F2	SFP3_RX_P	13	RD_P	zSFP3 J6
F1	SFP3_RX_N	12	RD_N	
G5	SFP3_TX_P	18	TD_P	
G4	SFP3_TX_N	19	TD_N	
Y15	SFP3_TX_DISABLE_B	3	TX_DISABLE	

Note: The SFP0_TX_DISABLE/SFP1_TX_DISABLE I/O standard LVCMOS33 and the GTY TX/RX connections I/O standard are not applicable.

Table 3-11 lists the zSFP+ module control and status connections.

Table 3-11: **zSFP0- zSFP3 Module Control and Status Connections**

zSFP Control/ Status Signal	Board Connection		SFP Module
SFP_TX_FAULT	Test Point J57	High = Fault	zSFP0 J1
		Low = Normal operation	
SFP_TX_DISABLE	Jumper J16	Off = SFP Disabled	
		On = SFP Enabled	
SFP_MOD_DETECT	Test Point J64	High = Module not present	
		Low = Module present	
SFP_RS0	PU R25/ PD R30	PU R25 = Full RX bandwidth	
		PD R30 = Reduced RX bandwidth	
SFP_RS1	PU R227/ PD R142	PU R227 = Full RX bandwidth	
		PD R142 = Reduced RX bandwidth	
SFP_LOS	Test Point J68	High = Loss of receiver signal	
		Low = Normal operation	

Table 3-11: **zSFP0- zSFP3 Module Control and Status Connections *(Cont'd)***

zSFP Control/ Status Signal	Board Connection		SFP Module
SFP_TX_FAULT	Test Point J60	High = Fault	zSFP1 J3
		Low = Normal operation	
SFP_TX_DISABLE(2)	Jumper J17	Off = SFP Disabled	
		On = SFP Enabled	
SFP_MOD_DETECT	Test Point J61	High = Module not present	
		Low = Module present	
SFP_RS0(1)(2)	PU R182/ PD R190	PU R182 = Full RX bandwidth	
		PD R190 = Reduced RX bandwidth	
SFP_RS1(1)(2)	PU R185/ PD R202	PU R185 = Full RX bandwidth	
		PD R202 = Reduced RX bandwidth	
SFP_LOS	Test Point J62	High = Loss of receiver signal	
		Low = Normal operation	
SFP_TX_FAULT	Test Point J63	High = Fault	zSFP2 J4
		Low = Normal operation	
SFP_TX_DISABLE(2)	Jumper J42	Off = SFP Disabled	
		On = SFP Enabled	
SFP_MOD_DETECT	Test Point J58	High = Module not present	
		Low = Module present	
SFP_RS0(1)(2)	PU R303/ PD R305	PU R25 = Full RX bandwidth	
		PD R30 = Reduced RX bandwidth	
SFP_RS1(1)(2)	PU R304/ PD R588	PU R227 = Full RX bandwidth	
		PD R142 = Reduced RX bandwidth	
SFP_LOS	Test Point J59	High = Loss of receiver signal	
		Low = Normal operation	

Table 3-11: **zSFP0- zSFP3 Module Control and Status Connections *(Cont'd)***

zSFP Control/ Status Signal	Board Connection		SFP Module
SFP_TX_FAULT	Test Point J65	High = Fault	zSFP3 J6
		Low = Normal operation	
SFP_TX_DISABLE	Jumper J54	Off = SFP Disabled	
		On = SFP Enabled	
SFP_MOD_DETECT	Test Point J66	High = Module not present	
		Low = Module present	
SFP_RS0(1)(2)	PU R589/ PD R605	PU R182 = Full RX bandwidth	
		PD R190 = Reduced RX bandwidth	
SFP_RS1(1)(2)	PU R590/ PD R606	PU R185 = Full RX bandwidth	
		PD R202 = Reduced RX bandwidth	
SFP_LOS	Test Point J67	High = Loss of receiver signal	
		Low = Normal operation	

Notes:

1. The RS0/RS1 PU/PD resistors are not populated. There are pull-down resistors built into the SFP/zSFP modules that select the lower bandwidth mode of the module.
2. Also available via I2C control. For this and additional information about the enhanced SFP+ module, see the SFF-8431 specification at the SFF-8431 specification website [Ref 29].

10/100/1000 Mb/s Tri-Speed Ethernet PHY

[Figure 2-1, callout 16]

The KCU116 board uses the TI DP83867ISRGZ Ethernet SGMII PHY at U12 for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports SGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Wurth 7499111221A RJ-45 connector (P3) with built-in magnetics. The U12 Ethernet PHY address is `11000`.

Figure 3-15 shows the Ethernet PHY circuitry.

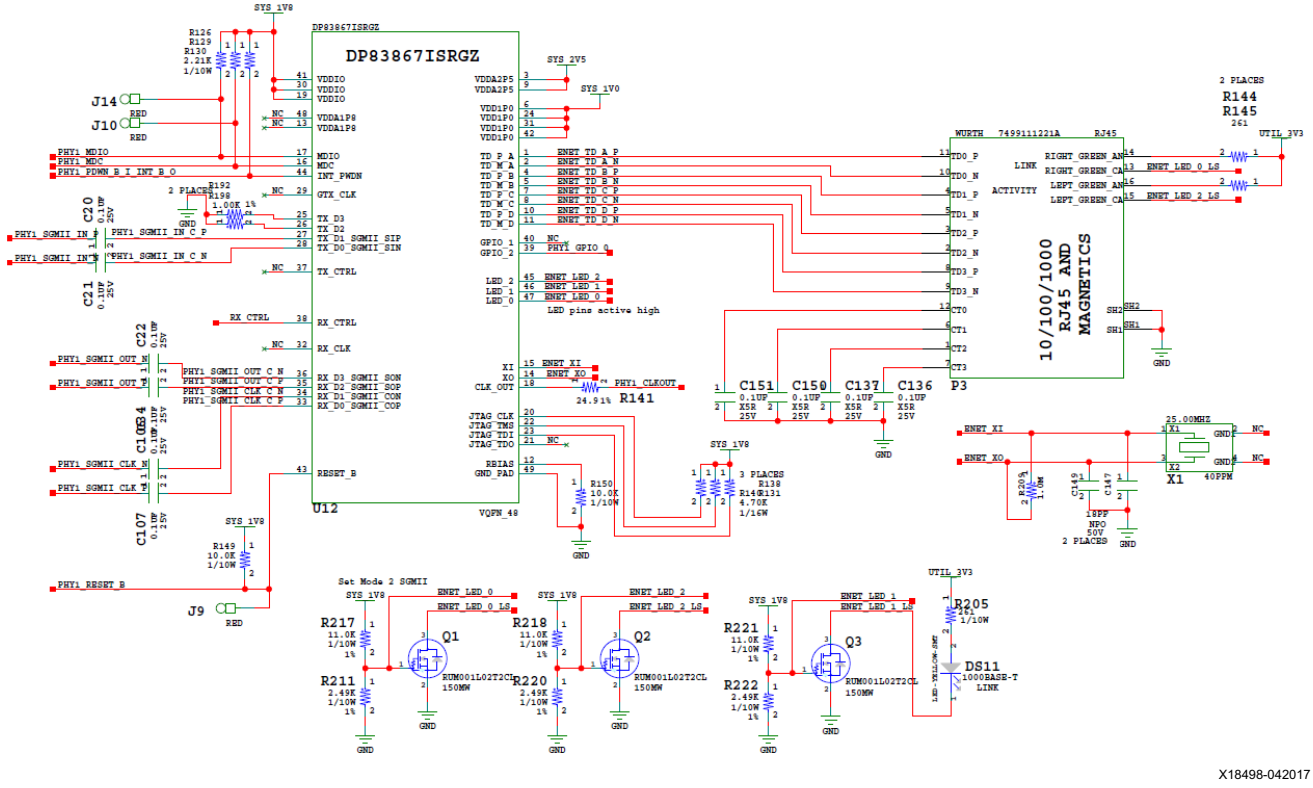

Figure 3-15: **KCU116 EPHY DP83867ISRG Circuit**

The Ethernet connections from XCKU5P FPGA U1 to the DP83867ISRGZ PHY device (U12) are listed in Table 3-12.

Table 3-12: **Ethernet Connections, XCKU5P MPSoC to the PHY Device**

FPGA (U1) Pin	Schematic Net Name	DP83867 PHY U12	
		Pin	Name
P25	PHY1_MDIO	17	MDIO
U25	PHY1_MDC	16	MDC
R25	PHY1_PDWN_B_I_INT_B_O	44	INT_PWDN
N24	PHY1_SGMII_IN_P	27	TX_D1_SGMII_SIP
P24	PHY1_SGMII_IN_N	28	TX_D0_SGMII_SIN
U26	PHY1_SGMII_OUT_P	35	RX_D2_SGMII_SOP
V26	PHY1_SGMII_OUT_N	36	RX_D3_SGMII_SON
T24	PHY1_SGMII_CLK_P	33	RX_D0_SGMII_COP
U24	PHY1_SGMII_CLK_N	34	RX_D1_SGMII_CON
AA23	PHY1_RESET_B	43	RESET_B
T25	PHY1_CLKOUT	18	CLK_OUT
P26	PHY1_GPIO_0	39	GPIO_2

Ethernet PHY Status LEDs

[Figure 2-1, callout 17]

The TI DP83867ISRGZ PHY U12 LED interface (LED_0, LED_2) uses the two status LEDs integrated into the metal frame of the P3 RJ-45 connector. These LEDs are visible on the left edge of the KCU116 board when it is installed into a PCIe slot in a PC chassis. The two PHY status LEDs are visible within the frame of the RJ-45 Ethernet jack as shown in Figure 3-16. As viewed from the front opening, the left green LED is the link activity indicator and the right green LED is the 1000BASE-T link mode indicator.

Figure 3-16: **KCU116 Ethernet PHY Status LEDs**

A separate discrete LED on top of the board (DS11, near U12) indicates link established.

The LED functions can be re-purposed with a LEDCR1 register write. LED_2 is assigned to ACT (activity indicator) and LED_0 indicates link established. For more Ethernet PHY details, see the TI DS83867 data sheet [Ref 31]. Details about the tri-mode Ethernet MAC core are provided in *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051) [Ref 10].

The LED functional description is show in Table 3-13.

Table 3-13: **Ethernet PHY LED Functional Description**

Pin		Type	Description
Name	No.		
LED_2	45	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable by means of LEDCR1[11:8] register bits. ***Note:*** This pin is a strap configuration pin for RGZ devices only.
LED_1	46	S, I/O, PD	By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable by means of LEDCR1[7:4] register bits.
LED_0	47	S, I/O, PD	By default, this pin indicates that a link is established. Additional functionality is configurable by means of LEDCR1[3:0] register bits.

Dual USB-to-UART Bridge

[Figure 2-1, callout 18]

The KCU116 evaluation board contains a Silicon Labs CP2105GM dual USB-to-UART bridge device (U166) that allows a connection to a host computer with a USB port. The USB cable is supplied in the KCU116 evaluation kit (standard type-A end to host computer, type micro-B end to KCU116 evaluation board connector J164). The CP2105GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the KCU116 evaluation board.

The dual UART interface connections are split between two components:

- UART1 SCI 4-wire interface is connected to the XCKU5P U1 FPGA
- UART2 ECI 2-wire interface is connected to the XC7Z010 U161 Zynq-7000 SoC system controller

Silicon Labs provides royalty-free virtual COM port (VCP) drivers for the host computer. These drivers permit the CP2105GM dual USB-to-UART Bridge to appear as a pair of COM ports to communications application software (for example, Tera Term or HyperTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the KCU116 evaluation board. The driver assigns the lower PC COM port number to UART2 and the higher PC COM port number to UART1.

The Silicon Labs CP2105GM dual USB-to-UART bridge circuit is shown in Figure 3-17.

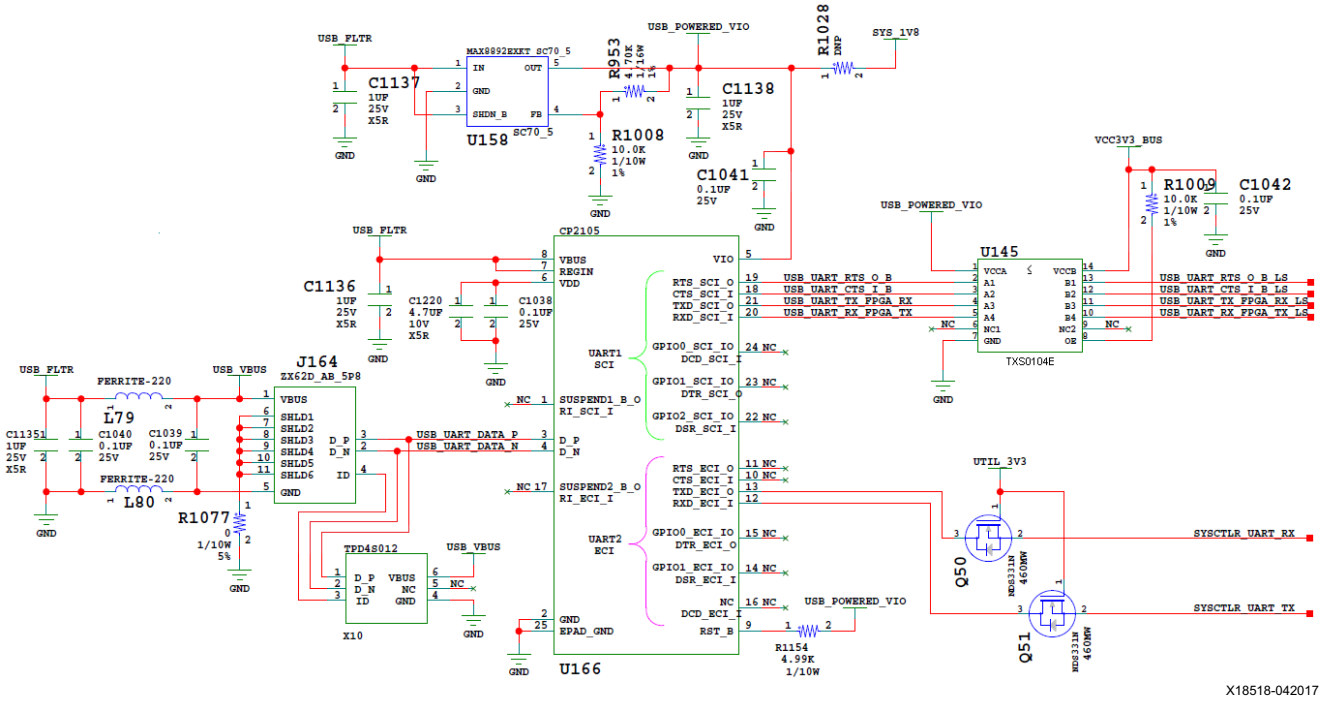

Figure 3-17: **KCU116 Dual UART CP2105GM**

Table 3-14 lists the CP2105GM connections to FPGA U1. The USB UART schematic nets are named from the perspective of the CP2105GM device (U166).

Table 3-14: **FPGA U1 to CP2105GM U166 Connections**

XC7Z010 SoC (U161)				Schematic Net Name	CP2105GM Device (U166)		
FPGA U1 Pin	Function	Direction	I/O Standard		Pin	Function	Direction
C12	TX	Output	LVCMOS18	SYSCTLR_UART_TX	12	RXD	Input
B15	RX	Input	LVCMOS18	SYSCTLR_UART_RX	13	TXD	Output
XCKU5P FPGA (U1)							
W12	RX	Input	LVCMOS18	USB_UART_TX	21	TXD	Output
W13	TX	Output	LVCMOS18	USB_UART_RX	20	RXD	Input
Y13	CTS	Output	LVCMOS18	USB_UART_CTS	18	CTS	Input
AA13	RTS	Input	LVCMOS18	USB_UART_RTS	19	RTS	Output

Table 3-15 lists the USB connector J164 pin assignments.

Table 3-15: **USB Connector J164 Pin Assignments**

USB Connector (J164)		Schematic Net Name	CP2105GM (U166)	
Pin	**Name**		**Pin**	**Name**
1	VBUS	USB_VBUS		
2	D_P	USB_UART_DATA_P	3	D_P
3	D_N	USB_UART_DATA_N	4	D_N
5	GND	USB_VBUS_GND		
		GND	2, 25	GND

For more technical information on the CP2105GM and the VCP drivers, see the Silicon Labs website [Ref 27].

Xilinx UART IP is expected to be implemented in the FPGA logic using IP. See the *AXI UART Lite LogiCORE IP Product Guide* (PG142) [Ref 11] for more information.

HDMI Video Output

[Figure 2-1, callout 19]

The KCU116 evaluation board provides HDMI™ video output using an Analog Devices ADV7511KSTZ-P HDMI transmitter at U5. The HDMI transmitter U5 is connected to XCKU5P FPGA bank 65 and its output is provided on a Molex 47151-0011 HDMI receptacle at P2. The ADV7511 supports 1080P 60 Hz, YCbCr 4:2:2 encoding via 18-bit input data mapping.

The KCU116 evaluation board supports these HDMI device interfaces:

- 18 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK
- Interrupt out pin to FPGA
- I^2C
- Sony/Philips digital interface format (SPDIF) audio

The HDMI U5 circuit is shown in Figure 3-18.

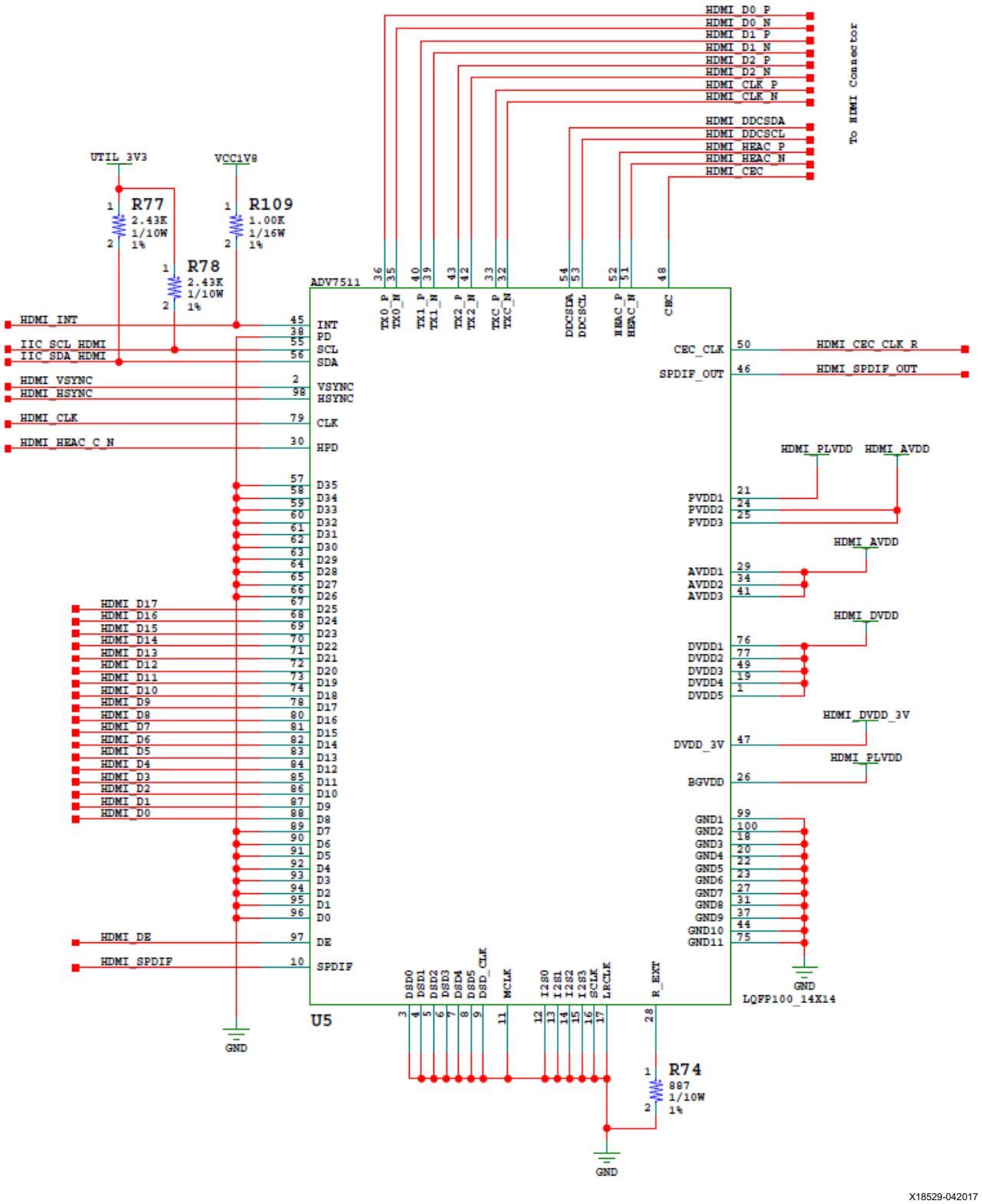

Figure 3-18: **HDMI Codec Circuit**

Table 3-16 lists the connections between the codec and the XCKU5P FPGA U1.

Table 3-16: **HDMI Codec U52 to XCKU5P FPGA U1 Connections**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	ADV7511 U52	
			Pin Number	Name
V21	HDMI_D0	LVCMOS18	88	D8
V22	HDMI_D1	LVCMOS18	87	D9
T22	HDMI_D2	LVCMOS18	86	D10
T23	HDMI_D3	LVCMOS18	85	D11
W19	HDMI_D4	LVCMOS18	84	D12
W20	HDMI_D5	LVCMOS18	83	D13
Y22	HDMI_D6	LVCMOS18	82	D14
Y23	HDMI_D7	LVCMOS18	81	D15
Y25	HDMI_D8	LVCMOS18	80	D16
Y26	HDMI_D9	LVCMOS18	78	D17
AA24	HDMI_D10	LVCMOS18	74	D18
AA25	HDMI_D11	LVCMOS18	73	D19
W25	HDMI_D12	LVCMOS18	72	D20
W26	HDMI_D13	LVCMOS18	71	D21
V23	HDMI_D14	LVCMOS18	70	D22
W23	HDMI_D15	LVCMOS18	69	D23
V24	HDMI_D16	LVCMOS18	68	D24
W24	HDMI_D17	LVCMOS18	67	D25
U20	HDMI_DE	LVCMOS18	97	DE
T20	HDMI_SPDIF	LVCMOS18	10	SPDIF
P20	HDMI_CLK	LVCMOS18	79	CLK
U21	HDMI_VSYNC	LVCMOS18	2	VSYNC
V19	HDMI_HSYNC	LVCMOS18	98	HSYNC
U19	HDMI_SPDIF_OUT	LVCMOS18	46	SPDIF_OUT
R26	HDMI_INT	LVCMOS18	45	INT

Notes: All HDMI nets in this table, except HDMI_INT, are series resistor coupled.

All HDMI nets in this table except HDMI_INT are series resistor coupled.

Table 3-17 lists the connections between the U5 ADV7511 codec and the HDMI connector P2.

Table 3-17: **HDMI ADV511 Codec U52 to P6 Connections**

ADV7511 (U54)		Schematic Net Name	HDMI Connector P6 Pin
Name	Pin		
TX0_P	36	HDMI_D0_P	7
TX0_N	35	HDMI_D0_N	9
TX1_P	40	HDMI_D1_P	4
TX1_N	39	HDMI_D1_N	6
TX2_P	43	HDMI_D2_P	1
TX2_N	42	HDMI_D2_N	3
TXC_P	33	HDMI_CLK_P	10
TXC_N	32	HDMI_CLK_N	12
DDCSDA	54	HDMI_DDCSDA	16
DDCSCL	53	HDMI_DDCSCL	15
HEAC_P	52	HDMI_HEAC_P	14
HEAC_N	51	HDMI_HEAC_N	19
CEC	48	HDMI_CEC	13

For more information about the Analog Devices ADV7511KSTZ-P, see the Analog Devices website [Ref 30]. For additional information about HDMI IP options, see the *DisplayPort LogiCORE Product Guide* (PG064) [Ref 19].

I2C Bus

[Figure 2-1, callouts 20, 21]

The KCU116 evaluation board implements a 2-to-1 I^2C bus arrangement. A single I^2C bus from each of the FPGA U1 XCKU5P (IIC_MAIN_SCL/SDA_LS) and system controller Zynq-7000 SoC U111 (SYSCTLR_I2C_SCL/SDA) are wired to the same I^2C bus via level-shifters (FPGA U1 is wired through level-shifter U162 and system controller U161 is wired through level-shifter U163). The *output* sides of U162 and U163 are wired in parallel to a common I^2C bus (IIC_SDA and _SCL_MAIN). This common I^2C bus is then routed to a pair of 1-to-8 channel I2C TI PCA9548 bus switches (U34 and U135) and a TI TCA6416A I2C GPIO expander (U147). The bus switches can operate at speeds up to 400 kHz.

The KCU116 evaluation board I^{2}C bus topology is shown in Figure 3-19.

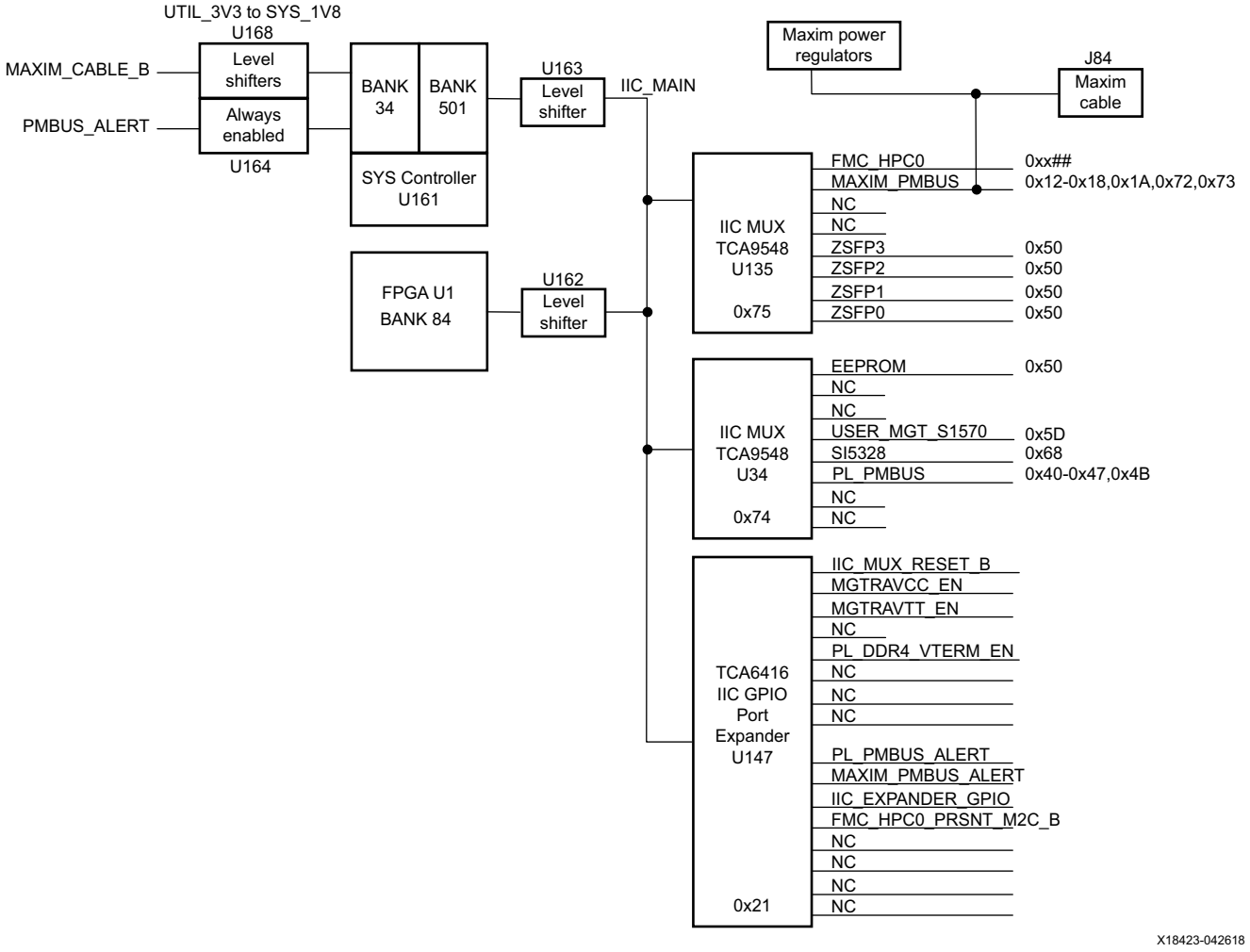

Figure 3-19: **I^{2}C Bus Topology**

User applications that communicate with devices on one of the downstream I²C buses must first set up a path to the desired target bus through the U34 or U135 bus switch at I²C address 0x74 (0b1110100) or 0x75 (0b111101), respectively. The TCA6416A address is 0x21 and the I/O expander powers up in input mode. Table 3-18 lists the address for each bus and the I2C address of the TCA9548 U34 and U135 bus switch target devices.

Table 3-18: **I2C Bus Addresses**

I2C Bus	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
TCA9548 8-Channel bus switch (U34)	N/A	0b1110100	0x74	U34 TCA9548
EEPROM_IIC_SDA/SCL	0	0b1010000	0x50	U12 M24C08
Not Used	1	N/A	N/A	N/A
Not Used	2	N/A	N/A	N/A
USER_MGT_SI570_CLOCK_SDA/SCL	3	0b1011101	0x5D	U32 SI570
Si5328_SDA/SCL	4	0b1101000	0x68	U57 SI5328C
PL_PMBUS_SDA/SCL (INA226)	5	0b1000000-0b1000111, 0b1001011	0x40-0x47, 0x4B	INA226
Not Used	6	N/A	N/A	N/A
Not Used	7	N/A	N/A	N/A
TCA9548 8-Channel bus switch (U135)	N/A	0b1110101	0x75	U135 TCA9548
FMC_HPC0_IIC_SDA/SCL	0	0bXXXXXXX	0xXX	J5 FMC HPC0
MAXIM_PMBUS_SDA/SCL	1	0b0010010-0b0011010, 0b1110010-0b1110011	0x12-0x1A, 0x72-0x73	MAX15301/3, MAX20751
Not Used	2	N/A	N/A	N/A
Not Used	3	N/A	N/A	N/A
SFP3_IIC_SDA/SCL	4	0b1010000	x50	J6 SFP3
SFP2_IIC_SDA/SCL	5	0b1010000	x50	J4 SFP2
SFP1_IIC_SDA/SCL	6	0b1010000	x50	J3 SFP1
SFP0_IIC_SDA/SCL	7	0b1010000	x50	J1 SFP0
TCA6416 I²C Port Expander	N/A	0b0100001	0x21	U147 TCA6416

Information about the PCA9548A and TCA6416A is available on the TI Semiconductor website [Ref 31].

Status and User LEDs

[Figure 2-1, callout 22]

Table 3-19 defines KCU116 board status and user LEDs.

Table 3-19: **KCU116 Board Status and User LEDs**

Reference Designator	Description
DS1	INIT
DS2	12V On
DS3	VCCAUX_PGOOD
DS4	VCC3V3_PGOOD
DS5	VCCINT_PGOOD
DS6	VADJ_FMC_PGOOD
DS7	VCC1V2_PGOOD
DS8	VCCBRAM_PGOOD
DS9	MGTAVTT_PGOOD
DS10	MGTAVCC_PGOOD
DS11	ENET PHY Link Established
DS12	SYS_5V0 On
DS21	VCC1V8_PGOOD
DS22	UTIL_5V0_PGOOD
DS25	UTIL_3V3_PGOOD
DS26	MGTVCCAUX_PGOOD
DS30	PL_DDR4_VTERM_0V60_PGOOD
DS32	Done
DS37	GPIO_LED_1
DS38	GPIO_LED_0
DS39	GPIO_LED_2
DS40	GPIO_LED_5
DS41	GPIO_LED_4
DS42	GPIO_LED_5
DS43	GPIO_LED_6
DS44	GPIO_LED_7
DS50	SYSCTLR INIT
DS51	SYSCTLR Status
DS52	SYSCTLR Done
DS53	SYS_2V5 On

Table 3-19: **KCU116 Board Status and User LEDs *(Cont'd)***

Reference Designator	Description
DS54	SYS_1VO On
DS55	SYS_1V8 On
DS57	SYSCTLR Error
EPHY P3 (Right) LED	ENET PHY LINK1000 Mode
EPHY P3 (Left) LED	ENET PHY Activity

User I/O

[Figure 2-1, callouts 22, 23, 24, 25]

The KCU116 board provides these user and general purpose I/O capabilities:

- Eight user LEDs (callout 22)
  - GPIO_LED[7-0]: DS44, DS43, DS42, DS41, DS40, DS39, DS37, DS38
- Five user pushbuttons and CPU reset switch (callouts 23, 24)
  - GPIO_SW_[NESWC]: SW18, SW22, SW16, SW14, SW15
  - CPU_RESET: SW17
- 4-position user DIP switch (callout 25)
  - GPIO_DIP_SW[3:0]: SW13

User GPIO LEDs

[Figure 2-1, callout 22]

Figure 3-20 shows the GPIO LED circuit.

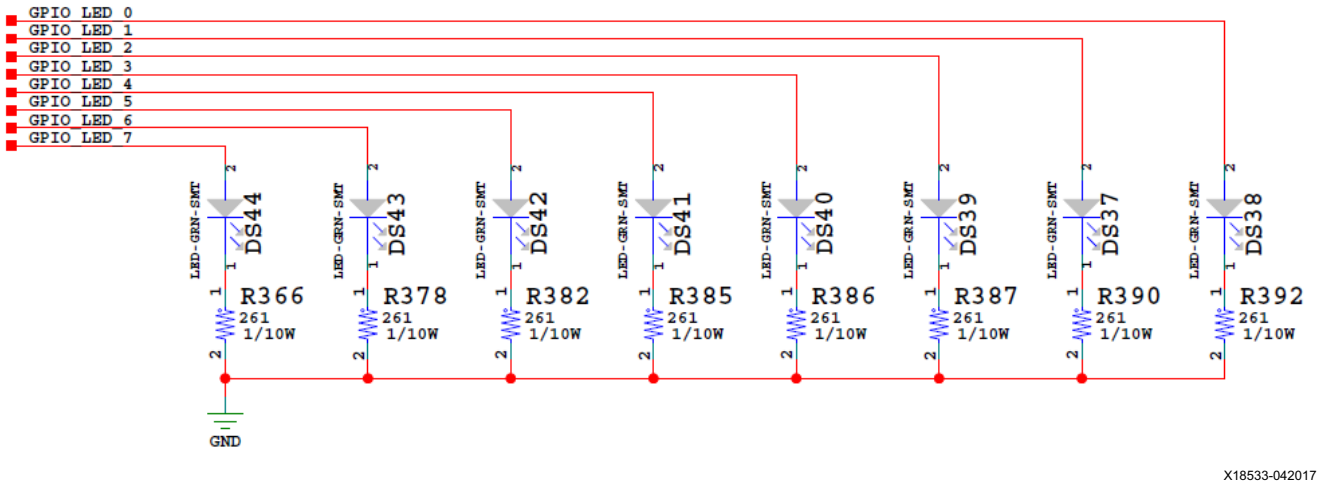

Figure 3-20: **User LEDs**

User Pushbuttons

[Figure 2-1, callout 24]

Figure 3-21 shows the user pushbuttons circuit.

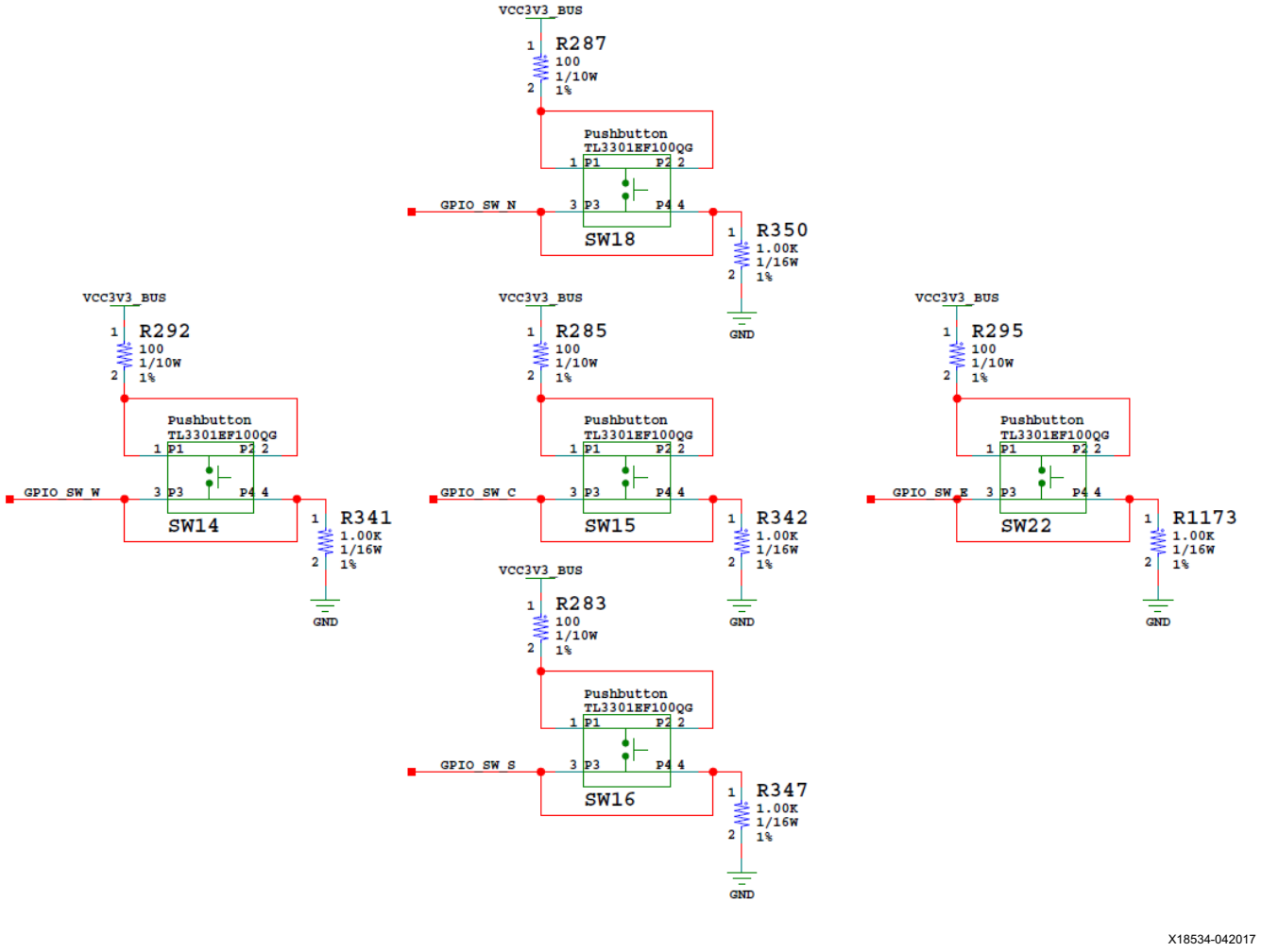

Figure 3-21: **User Pushbuttons**

User SMA GPIO

[Figure 2-1, callout 10]

The KCU116 board provides a pair of SMAs for differential user I/O into FPGA U1 bank 66 (see Figure 3-22). The P-side SMA J178 signal USER_SMA_P is connected to U1 pin K25, and the N-side SMA J179 signal USER_SMA_N is connected to U1 pin K26. Bank 66 V_{CCO} is 1.2V VCC1V2. The USER_SMA_CLOCK input voltage swing should not exceed 1.2V.

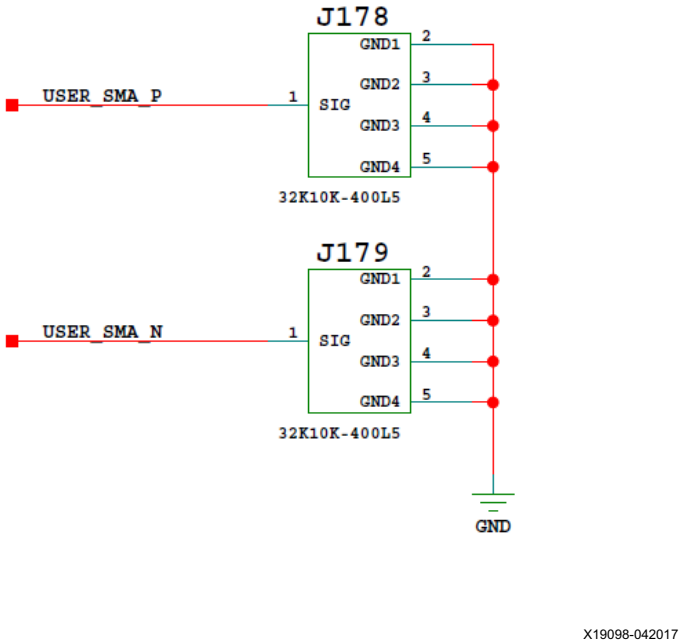

Figure 3-22: **User SMA GPIO**

CPU Reset Pushbutton

[Figure 2-1, callout 24]

Figure 3-23 shows the CPU reset pushbutton circuit.

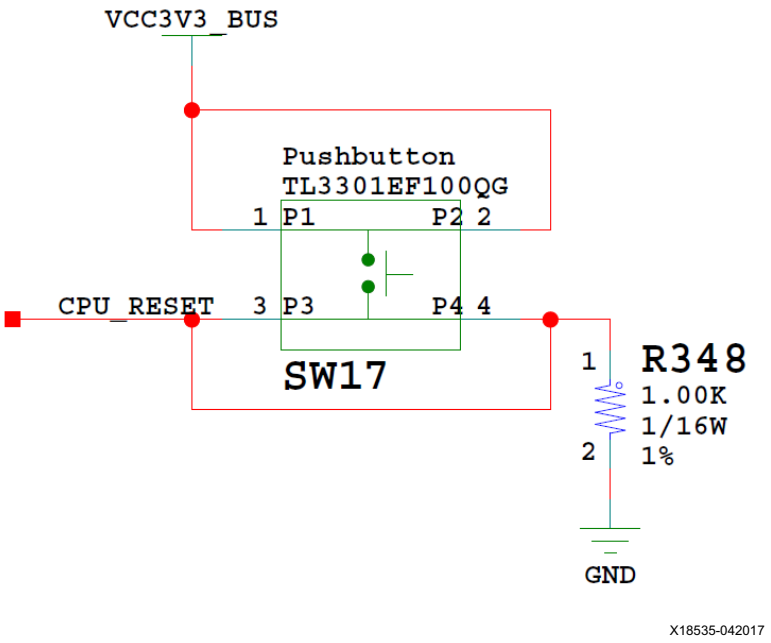

Figure 3-23: **CPU Reset Pushbutton**

GPIO DIP Switch

[Figure 2-1, callout 25]

Figure 3-24 shows the GPIO DIP switch circuit.

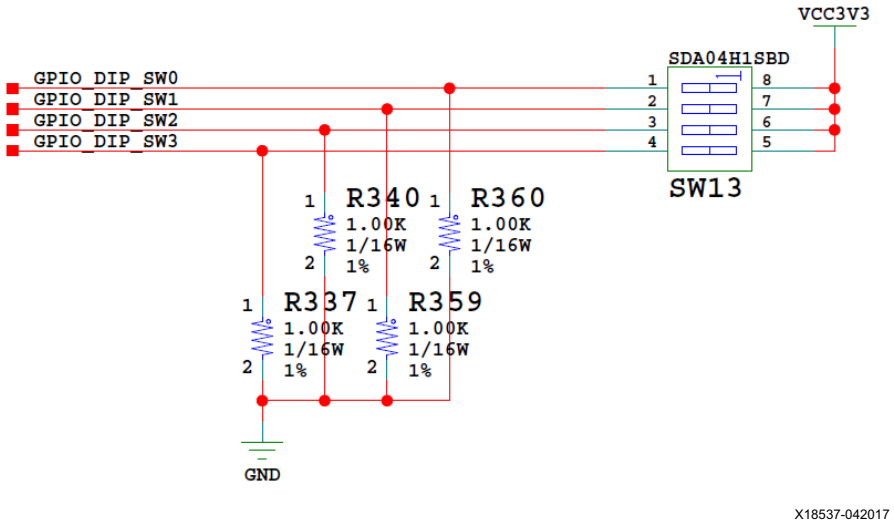

Figure 3-24: **GPIO DIP Switch**

Table 3-20 lists the GPIO connections to FPGA U1.

Table 3-20: **KCU116 GPIO Connections to FPGA U1**

FPGA Pin (U1)		Schematic Net Name	I/O Standard	GPIO
GPIO LEDs (active-High)				
BANK 86	C9	GPIO_LED_0	LVCMOS33	DS38.1
BANK 86	D9	GPIO_LED_1	LVCMOS33	DS37.1
BANK 86	E10	GPIO_LED_2	LVCMOS33	DS39.1
BANK 86	E11	GPIO_LED_3	LVCMOS33	DS40.1
BANK 86	F9	GPIO_LED_4	LVCMOS33	DS41.1
BANK 86	F10	GPIO_LED_5	LVCMOS33	DS42.1
BANK 86	G9	GPIO_LED_6	LVCMOS33	DS43.1
BANK 86	G10	GPIO_LED_7	LVCMOS33	DS44.1
Directional Pushbuttons (active-High)				
BANK 86	A10	GPIO_SW_N	LVCMOS33	SW18.3
BANK 86	B11	GPIO_SW_E	LVCMOS33	SW22.3
BANK 86	B10	GPIO_SW_W	LVCMOS33	SW14.3
BANK 86	C11	GPIO_SW_S	LVCMOS33	SW16.3

Table 3-20: **KCU116 GPIO Connections to FPGA U1 *(Cont'd)***

FPGA Pin (U1)		Schematic Net Name	I/O Standard	GPIO
BANK 86	A9	GPIO_SW_C	LVCMOS33	SW15.3
4-Pole DIP SW (active-High)				
BANK 86	G11	GPIO_DIP_SW0	LVCMOS33	SW13.1
BANK 86	H11	GPIO_DIP_SW1	LVCMOS33	SW13.2
BANK 86	H9	GPIO_DIP_SW2	LVCMOS33	SW13.3
BANK 86	J9	GPIO_DIP_SW3	LVCMOS33	SW13.4
CPU Reset Pushbutton (active-High)				
BANK 86	B9	CPU_RESET	LVCMOS33	SW17.3

User Pmod GPIO Headers

[Figure 2-1, callout 28]

The KCU116 evaluation board supports two Pmod GPIO headers J55 and J87. The Pmod nets are connected to FPGA U1 Bank 87. Pmod connector J55 is a right-angle receptacle and connector J87 is a vertical male pin header.

Figure 3-25 shows the GPIO Pmod headers J55 and J87.

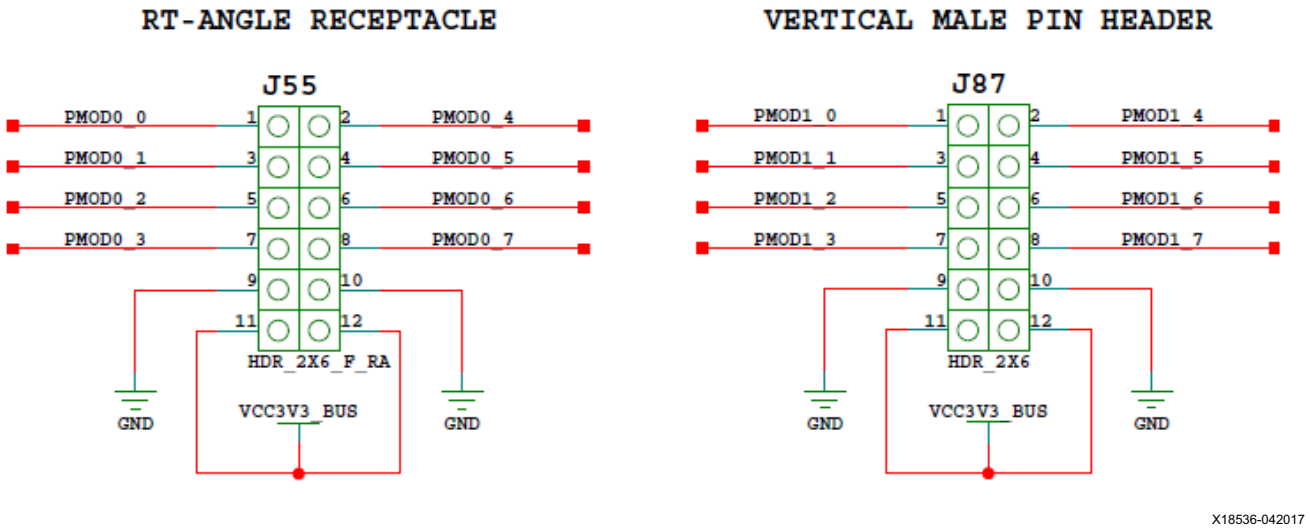

Figure 3-25: **Pmod Connectors J52 and J53 with Level Shifters U41 and U42**

Table 3-21 shows the level shifter U41 and U42 connections to FPGA U1

Table 3-21: **Pmod Connector J55, J87 Connections to FPGA U1**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	PMOD Conn. Pin
A14	PMOD0_0	LVCMOS33	J55.1
B14	PMOD0_1	LVCMOS33	J55.3
A12	PMOD0_2	LVCMOS33	J55.5
A13	PMOD0_3	LVCMOS33	J55.7
B12	PMOD0_4	LVCMOS33	J55.2
C12	PMOD0_5	LVCMOS33	J55.4
C13	PMOD0_6	LVCMOS33	J55.6
C14	PMOD0_7	LVCMOS33	J55.8
D13	PMOD1_0	LVCMOS33	J87.1
D14	PMOD1_1	LVCMOS33	J87.3
E12	PMOD1_2	LVCMOS33	J87.5
E13	PMOD1_3	LVCMOS33	J87.7
F13	PMOD1_4	LVCMOS33	J87.2
F14	PMOD1_5	LVCMOS33	J87.4
J14	PMOD1_6	LVCMOS33	J87.6
J15	PMOD1_7	LVCMOS33	J87.8

For more information about Pmod connector compatible Pmod modules, see the Digilent website [Ref 26].

Switches

[Figure 2-1, callouts 27, 31]

The KCU116 evaluation board includes a power on/off slide switch and a configuration pushbutton switch:

- Power on/off slide switch SW1 (callout 31)
- FPGA PROG_B SW4, active-Low (callout 27)

Power On/Off Slide Switch SW1

[Figure 2-1, callout 30]

The KCU116 board power switch is SW1. Sliding the switch actuator from the off to on position applies 12VDC power from the 6-pin mini-fit power input connector J52. The green LED DS2 illuminates when the KCU116 board power is on. See KCU116 Board Power System for details on the onboard power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J52 on the KCU116 evaluation board. The ATX 6-pin connector has a different pinout than J52. Connecting an ATX 6-pin connector into J52 damages the KCU116 evaluation board and voids the board warranty.*

The KCU116 evaluation kit includes the adapter cable shown in Figure 3-26 for powering the KCU116 board from the ATX power supply 4-pin peripheral connector. The Xilinx part number for this cable is 2600304, and is equivalent to the Sourcegate Technologies part number AZCBL-WH-1109-RA4. See [Ref 35] for ordering information.

Figure 3-26: **ATX Power Supply Adapter Cable**

Figure 3-27 shows the power connector J52, power switch SW1, and indicator LED DS2.

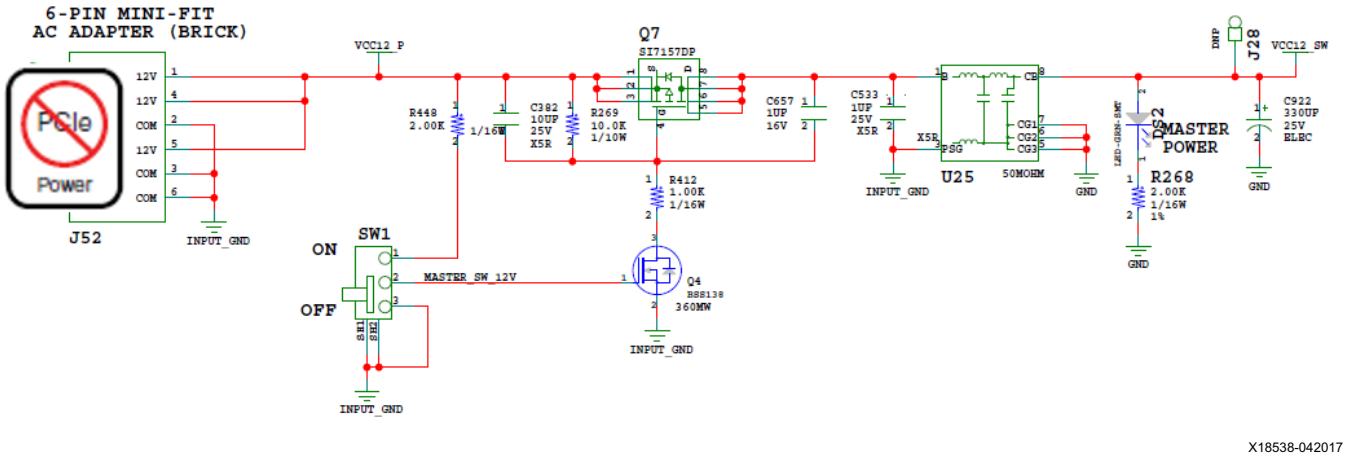

Figure 3-27: **Power On/Off Switch SW1**

Program_B Pushbutton Switch

[Figure 2-1, callout 26]

Switch SW5 grounds the XCKU5P FPGA U1 PROGRAM_B pin when pressed. This action clears the FPGA configuration. The FPGA_PROG_B signal is connected to XCKU5P FPGA U1 pin AB9. See *UltraScale Architecture Configuration User Guide* (UG570) [Ref 3] for further configuration details.

Figure 3-28 shows SW4.

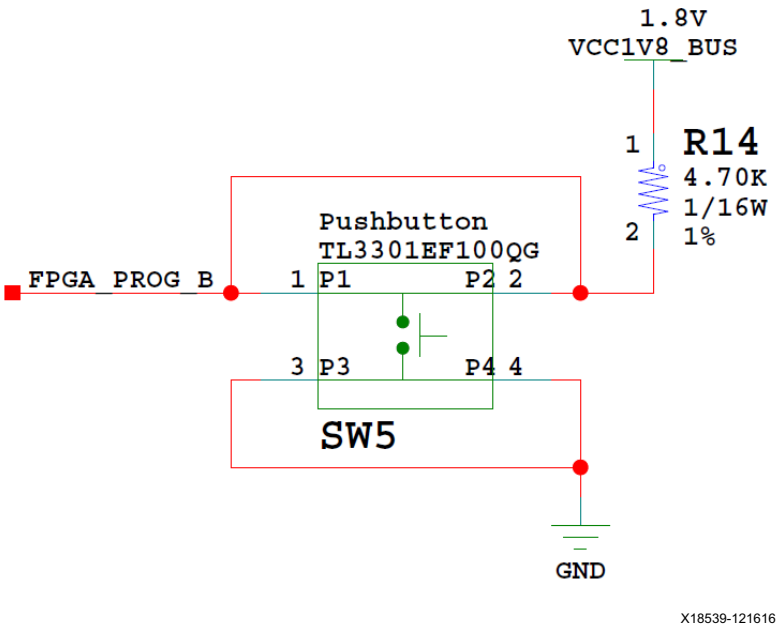

Figure 3-28: **Program_B Pushbutton Switch SW5**

FPGA Mezzanine Card Interface

[Figure 2-1, callout 34]

The KCU116 evaluation board supports the VITA 57.1 FPGA mezzanine card (FMC) specification by providing a subset implementation of the high pin count (HPC) connector at J5. The FMC connector uses a 10 x 40 form factor. The HPC connector is populated with 400 pins. The connector is keyed so that the mezzanine card faces away from the board when installed on the KCU116 evaluation board.

The connector type is the Samtec SEAF Series, 1.27 mm (0.050 in) pitch, which mates with the SEAM series connector. For more information about the SEAF series connectors, see the Samtec website [Ref 32]. For more information about the VITA 57.1 FMC specification, see the VITA FMC Marketing Alliance website [Ref 33].

FMC HPC Connector J5

[Figure 2-1, callout 34]

The 400 pin HPC connector defined by the FMC specification (Figure A-1) provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 10 GT transceivers
- 2 GT clocks
- 4 differential clocks
- 159 ground and 15 power connections

The HPC0 connector at J5 implements a subset of the full FMC HPC connectivity:

- 46 single-ended or 23 differential signal pairs (23 LA pairs: LA[00:22])
- 4 GTY transceivers
- 2 GTY clocks
- 1 differential clock
- 159 ground and 11 power connections

The KCU116 board FMC VADJ voltage VADJ_FMC for the J5 FMC connector is determined by the MAX15301 U63 voltage regulator described in KCU116 Board Power System.

Table 3-22 through Table 3-26 show the FMC HPC0 J5 to XCKU5P FPGA U1 connections in FMC connector section pairs.

Table 3-22: **J5 HPC FMC Section A/B Connections to FPGA U1**

J5 Pin	Schematic Net Name	I/O Standard	XCKU5P (U1) Pin	J5 Pin	Schematic Net Name	I/O Standard	XCKU5P (U1) Pin
A2	FMC_HPC0_DP1_M2C_P		C4	B1	NC		
A3	FMC_HPC0_DP1_M2C_N		C3	B4	NC		
A6	FMC_HPC0_DP2_M2C_P		B2	B5	NC		
A7	FMC_HPC0_DP2_M2C_N		B1	B8	NC		
A10	FMC_HPC0_DP3_M2C_P		A4	B9	NC		
A11	FMC_HPC0_DP3_M2C_N		A3	B12	NC		
A14	NC			B13	NC		
A15	NC			B16	NC		
A18	NC			B17	NC		
A19	NC			B20	FMC_HPC0_GBTCLK1_M2C_P	LVDS	H7
A22	FMC_HPC0_DP1_C2M_P		E5	B21	FMC_HPC0_GBTCLK1_M2C_N	LVDS	H6
A23	FMC_HPC0_DP1_C2M_N		E4	B24	NC		
A26	FMC_HPC0_DP2_C2M_P		D7	B25	NC		
A27	FMC_HPC0_DP2_C2M_N		D6	B28	NC		
A30	FMC_HPC0_DP3_C2M_P		B7	B29	NC		
A31	FMC_HPC0_DP3_C2M_N		B6	B32	NC		
A34	NC			B33	NC		
A35	NC			B36	NC		
A38	NC			B37	NC		
A39	NC			B40	NC		

Table 3-23: **J5 HPC FMC Section C/D Connections to FPGA U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
C2	FMC_HPC0_DP0_C2M_P		F7	D1	VADJ_1V8_PGOOD(3)		
C3	FMC_HPC0_DP0_C2M_N		F6	D4	FMC_HPC0_GBTCLK0_M2C_P		K7
C6	FMC_HPC0_DP0_M2C_P		D2	D5	FMC_HPC0_GBTCLK0_M2C_N		K6
C7	FMC_HPC0_DP0_M2C_N		D1	D8	FMC_HPC0_LA01_CC_P	LVDS	AC19
C10	FMC_HPC0_LA06_P	LVDS	Y20	D9	FMC_HPC0_LA01_CC_N	LVDS	AD19
C11	FMC_HPC0_LA06_N	LVDS	Y21	D11	FMC_HPC0_LA05_P	LVDS	AA19
C14	FMC_HPC0_LA10_P	LVDS	AF18	D12	FMC_HPC0_LA05_N	LVDS	AB19
C15	FMC_HPC0_LA10_N	LVDS	AF19	D14	FMC_HPC0_LA09_P	LVDS	AC18
C18	FMC_HPC0_LA14_P	LVDS	AE22	D15	FMC_HPC0_LA09_N	LVDS	AD18
C19	FMC_HPC0_LA14_N	LVDS	AF22	D17	FMC_HPC0_LA13_P	LVDS	AD23
C22	FMC_HPC0_LA18_CC_P	LVDS	AA22	D18	FMC_HPC0_LA13_N	LVDS	AE23
C23	FMC_HPC0_LA18_CC_N	LVDS	AB22	D20	FMC_HPC0_LA17_CC_P	LVDS	AD21
C26	NC			D21	FMC_HPC0_LA17_CC_N	LVDS	AE21
C27	NC			D23	NC		NA
C30	FMC_HPC0_IIC_SCL			D24	NC		NA
C31	FMC_HPC0_IIC_SDA			D26	NC		NA
C34	GA0 = 0 = GND			D27	NC		NA
C35	VCC12_SW			D29	FMC_HPC0_TCK_BUF		
C37	VCC12_SW			D30	FPGA_TDO_FMC_TDI_BUF		
C39	UTIL_3V3			D31	FMC_HPC0_TDO		
				D32	UTIL_3V3		
				D33	FMC_HPC0_TMS_BUF		
				D34	NC		
				D35	GA1 = 0 = GND		
				D36	UTIL_3V3		
				D38	UTIL_3V3		
				D40	UTIL_3V3		

Table 3-24: **J5 HPC FMC Section E/F Connections to FPGA U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
E2	NC	NA	NA	F1	FMC_HPC0_PG_M2C	LVCMOS33	H13
E3	NC	NA	NA	F4	NC	NA	NA
E6	NC	NA	NA	F5	NC	NA	NA
E7	NC	NA	NA	F7	NC	NA	NA
E9	NC	NA	NA	F8	NC	NA	NA
E10	NC	NA	NA	F10	NC	NA	NA
E12	NC	NA	NA	F11	NC	NA	NA
E13	NC	NA	NA	F13	NC	NA	NA
E15	NC	NA	NA	F14	NC	NA	NA
E16	NC	NA	NA	F16	NC	NA	NA
E18	NC	NA	NA	F17	NC	NA	NA
E19	NC	NA	NA	F19	NC	NA	NA
E21	NC	NA	NA	F20	NC	NA	NA
E22	NC	NA	NA	F22	NC	NA	NA
E24	NC	NA	NA	F23	NC	NA	NA
E25	NC	NA	NA	F25	NC	NA	NA
E27	NC	NA	NA	F26	NC	NA	NA
E28	NC	NA	NA	F28	NC	NA	NA
E30	NC	NA	NA	F29	NC	NA	NA
E31	NC	NA	NA	F31	NC	NA	NA
E33	NC	NA	NA	F32	NC	NA	NA
E34	NC	NA	NA	F34	NC	NA	NA
E36	NC	NA	NA	F35	NC	NA	NA
E37	NC	NA	NA	F37	NC	NA	NA
E39	VADJ _FMC_BUS			F38	NC	NA	NA
				F40	VADJ _FMC_BUS		

Table 3-25: **J5 HPC FMC Section G/H Connections to FPGA U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
G2	NC	NA	NA	H1	FMC_HPC0_VREF_A_M2C	NA	(3)
G3	NC	NA	NA	H2	FMC_HPC0_PRSNT_M2C_B	LVCMOS33	
G6	FMC_HPC0_LA00_CC_P	LVDS	AD20	H4	FMC_HPC0_CLK0_M2C_P	LVDS	AB21
G7	FMC_HPC0_LA00_CC_N	LVDS	AE20	H5	FMC_HPC0_CLK0_M2C_N	LVDS	AB22
G9	FMC_HPC0_LA03_P	LVDS	AB17	H7	FMC_HPC0_LA02_P	LVDS	Y17
G10	FMC_HPC0_LA03_N	LVDS	AC17	H8	FMC_HPC0_LA02_N	LVDS	AA17
G12	FMC_HPC0_LA08_P	LVDS	AE17	H10	FMC_HPC0_LA04_P	LVDS	AA20
G13	FMC_HPC0_LA08_N	LVDS	AF17	H11	FMC_HPC0_LA04_N	LVDS	AB20
G15	FMC_HPC0_LA12_P	LVDS	AC22	H13	FMC_HPC0_LA07_P	LVDS	AD16
G16	FMC_HPC0_LA12_N	LVDS	AC23	H14	FMC_HPC0_LA07_N	LVDS	AE16
G18	FMC_HPC0_LA16_P	LVDS	AD24	H16	FMC_HPC0_LA11_P	LVDS	Y18
G19	FMC_HPC0_LA16_N	LVDS	AD25	H17	FMC_HPC0_LA11_N	LVDS	AA18
G21	FMC_HPC0_LA20_P	LVDS	AF24	H19	FMC_HPC0_LA15_P	LVDS	AB24
G22	FMC_HPC0_LA20_N	LVDS	AF25	H20	FMC_HPC0_LA15_N	LVDS	AC24
G24	FMC_HPC0_LA22_P	LVDS	AE25	H22	FMC_HPC0_LA19_P	LVDS	AC26
G25	FMC_HPC0_LA22_N	LVDS	AE26	H23	FMC_HPC0_LA19_N	LVDS	AD26
G27	NC	NA	NA	H25	FMC_HPC0_LA21_P	LVDS	AB25
G28	NC	NA	NA	H26	FMC_HPC0_LA21_N	LVDS	AB26
G30	NC	NA	NA	H28	NC	NA	NA
G31	NC	NA	NA	H29	NC	NA	NA
G33	NC	NA	NA	H31	NC	NA	NA
G34	NC	NA	NA	H32	NC	NA	NA
G36	NC	NA	NA	H34	NC	NA	NA
G37	NC	NA	NA	H35	NC	NA	NA
G39	VADJ _FMC_BUS			H37	NC	NA	NA
				H38	NC	NA	NA
				H40	VADJ _FMC_BUS		

Table 3-26: **J5 HPC FMC Section J/K Connections to FPGA U1**

J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J5 Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
J2	NC	NA	NA	K1	NC	NA	NA
J3	NC	NA	NA	K4	NC	NA	NA
J6	NC	NA	NA	K5	NC	NA	NA
J7	NC	NA	NA	K7	NC	NA	NA
J9	NC	NA	NA	K8	NC	NA	NA
J10	NC	NA	NA	K10	NC	NA	NA
J12	NC	NA	NA	K11	NC	NA	NA
J13	NC	NA	NA	K13	NC	NA	NA
J15	NC	NA	NA	K14	NC	NA	NA
J16	NC	NA	NA	K16	NC	NA	NA
J18	NC	NA	NA	K17	NC	NA	NA
J19	NC	NA	NA	K19	NC	NA	NA
J21	NC	NA	NA	K20	NC	NA	NA
J22	NC	NA	NA	K22	NC	NA	NA
J24	NC	NA	NA	K23	NC	NA	NA
J25	NC	NA	NA	K25	NC	NA	NA
J27	NC	NA	NA	K26	NC	NA	NA
J28	NC	NA	NA	K28	NC	NA	NA
J30	NC	NA	NA	K29	NC	NA	NA
J31	NC	NA	NA	K31	NC	NA	NA
J33	NC	NA	NA	K32	NC	NA	NA
J34	NC	NA	NA	K34	NC	NA	NA
J36	NC	NA	NA	K35	NC	NA	NA
J37	NC	NA	NA	K37	NC	NA	NA
J39	NC	NA	NA	K38	NC	NA	NA
J39	NC	NA	NA	K40	NC	NA	NA

KCU116 Board Power System

[Figure 2-1, callout 33]

The KCU116 hosts a Maxim PMBus based power system. Each individual Maxim MAX15301, MAX15303, and MAX20751 voltage regulator has a PMBus interface. Figure 3-29 shows the KCU116 power system block diagram.

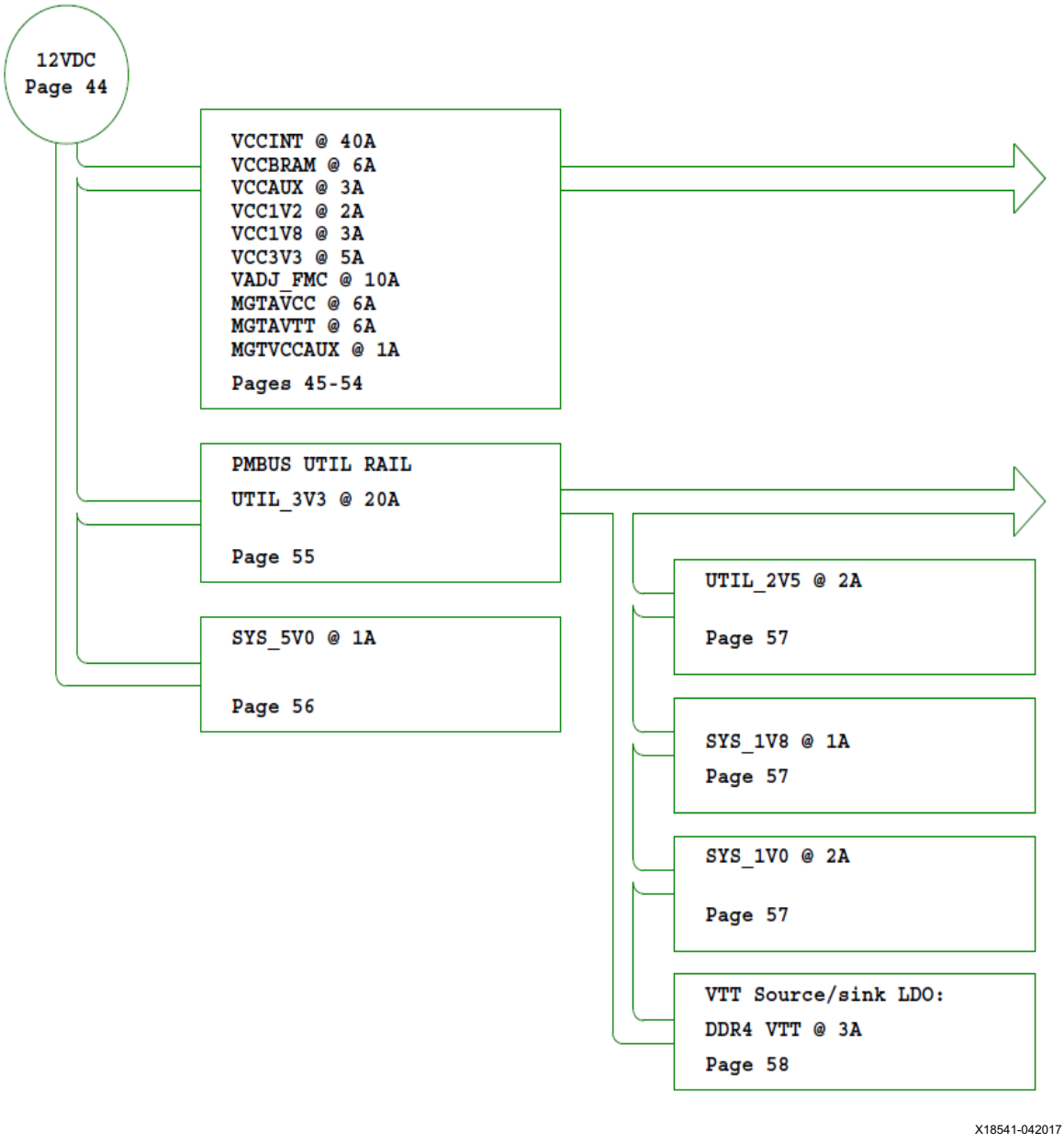

Figure 3-29: **KCU116 Power System Block Diagram**

The KCU116 evaluation board uses power regulators and PMBus compliant point of load (POL) controllers from Maxim Integrated Circuits to supply the core and auxiliary voltages listed in Table 3-27.

Table 3-27: **Onboard Power System Devices**

Rail Name	Power System Regulators					INA226 Power Monitor		Schematic Page Number
	Ref. Des.	Device Type	Vout (V)	Max. I (A)	Addr.	Addr.	Ref. Des.	
VCCINT	U47	MAX15301	0.85	40	0x13	0X40	U79	45
VCCBRAM	U7	MAX15303	0.85	6	0x14	0x41	U81	46
VCCAUX	U6	MAX15303	1.80	3	0x15	0x42	U80	47
VCC1V2	U10	MAX15303	1.20	2	0x16	0x43	U84	48
VCC1V8	U144	MAX15303	1.80	3	0x12	0x4B	U176	49
VCC3V3	U9	MAX15303	3.30	5	0x17	0x44	U16	50
VADJ_FMC	U63	MAX15303	1.80	10	0x18	0x45	U65	51
MGTAVCC	U95	MAX20751	0.90	6	0x72	0x46	U74	52
MGTAVTT	U96	MAX20751	1.20	6	0x73	0x47	U75	53
MGTVCCAUX	U14	MAX8869E	1.81	1	NA	NA	NA	54
UTIL_3V3	U49	MAX15301	3.30	20	0x1A	NA	NA	55
SYS_5V0	U8	MAX17502	5.00	1	NA	NA	NA	56
SYS_1V0	U155	MAX15053	1.00	2	NA	NA	NA	57
SYS_1V8	U159	MAX15027	1.80	1	NA	NA	NA	57
SYS_2V5	U156	MAX15053	2.50	2	NA	NA	NA	57
DDR4_VTT	U35	TPS51200	0.60	3	NA	NA	NA	58

The VADJ_FMC rail is programmed to 1.80V by default. This rail powers the FMC HPC0 (J5) VADJ pins and the XCKU5P FMC interface bank 64 (see Table 3-1, page 18).

Documentation describing PMBus programming for the Maxim InTune™ power controllers is available at the Maxim website [Ref 34]. The PCB layout and power system design meet the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 14].

Monitoring Voltage and Current

[Figure 2-1, callout 32]

Voltage and current monitoring and control are available for the Maxim power system controllers via the Maxim PowerTool software graphical user interface. The onboard Maxim PMBus MAX15301, MAX15303, and MAX20751 power controllers listed in Table 3-27 are accessed through the 2x8 keyed shrouded PMBus connector J84, which is provided for use with the Maxim PowerTool USB cable (Maxim part number MAXPOWERTOOL001#). This cable can be ordered from the Maxim Integrated website [Ref 34]. The associated Maxim PowerTool GUI can be downloaded from the Maxim website. This is the simplest and most convenient way to monitor the voltage and current values for the power rails listed in Table 3-27.

V_{CCINT}, V_{CCAUX}, and V_{CCBRAM} rail voltages can also be displayed via the SYSMON internal voltage measurement capability.

SYSMON Header J93

[Figure 2-1, callout 35]

UltraScale FPGAs provide an analog front-end (SYSMON) block. The SYSMON contains a single 10-bit 0.2 MSPS ADC. Consequently, the sequencer for SYSMON does not support simultaneous sampling mode or independent ADC mode. See the *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 20] for details on the capabilities of the analog front end. Figure 3-30 shows the KCU116 board SYSMON support features.

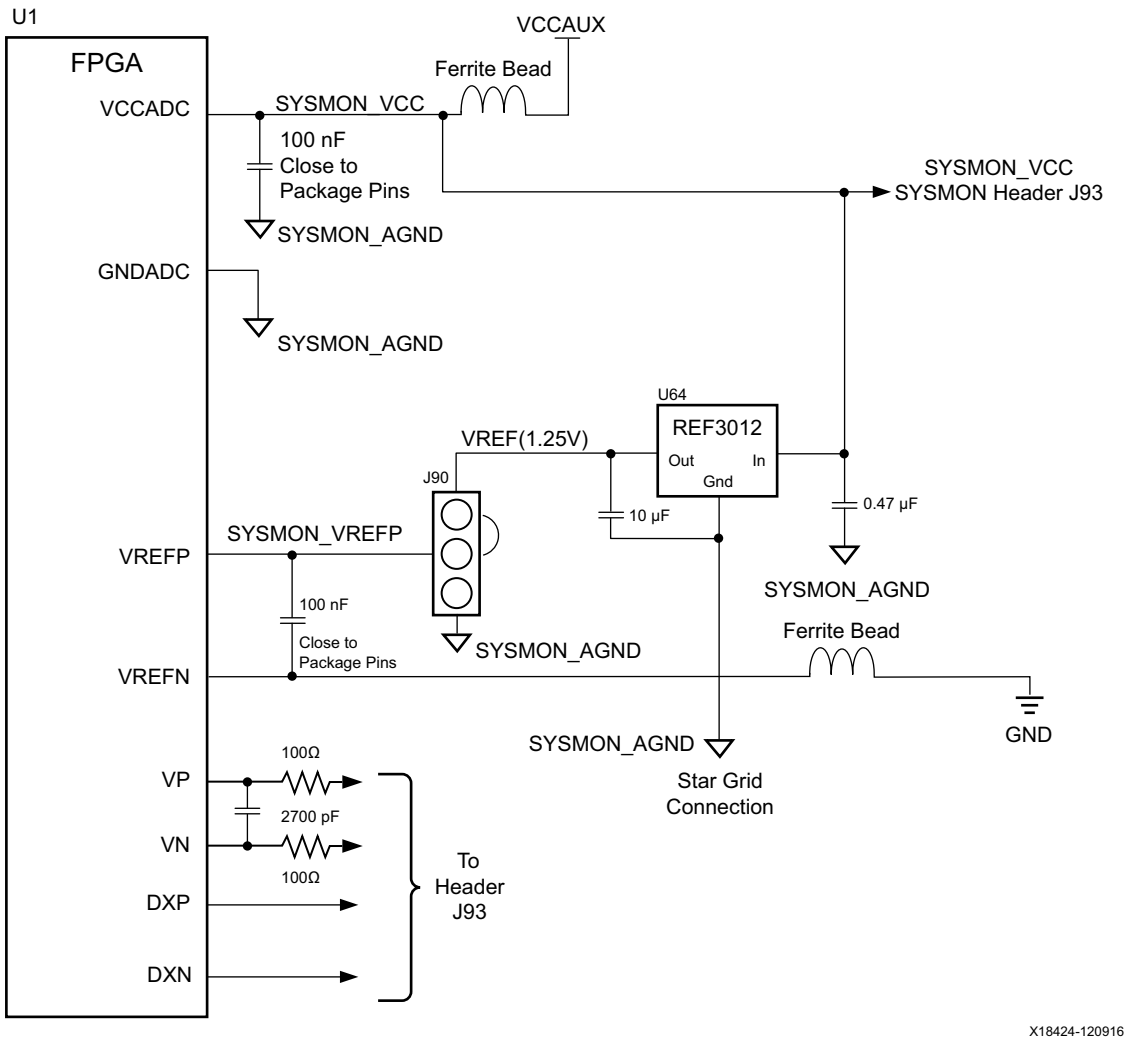

Figure 3-30: **KCU116 SYSMON and SYSMON Header J93 Voltage Source Options**

The KCU116 board supports both the internal FPGA sensor measurements and the external measurement capabilities of the SYSMON. Internal measurements of the die temperature, V_{CCINT}, V_{CCAUX}, and V_{CCBRAM} are available. Header J90 can be used to select either an external differential voltage reference (SYSMON_VREFP) or on-chip voltage reference (jumper J90 2-3) for the analog-to-digital converter.

For external measurements the SYSMON header (J93) is provided. This header can be used to provide analog inputs to the FPGA's dedicated VP/VN input channel. The VCCINT_VIN_R_P/N signals from the V_{CCINT} regulator circuit series current sense 0.002Ω resistor R36 are also made available at J93 pins 11 and 12.

Figure 3-31 shows the header connections.

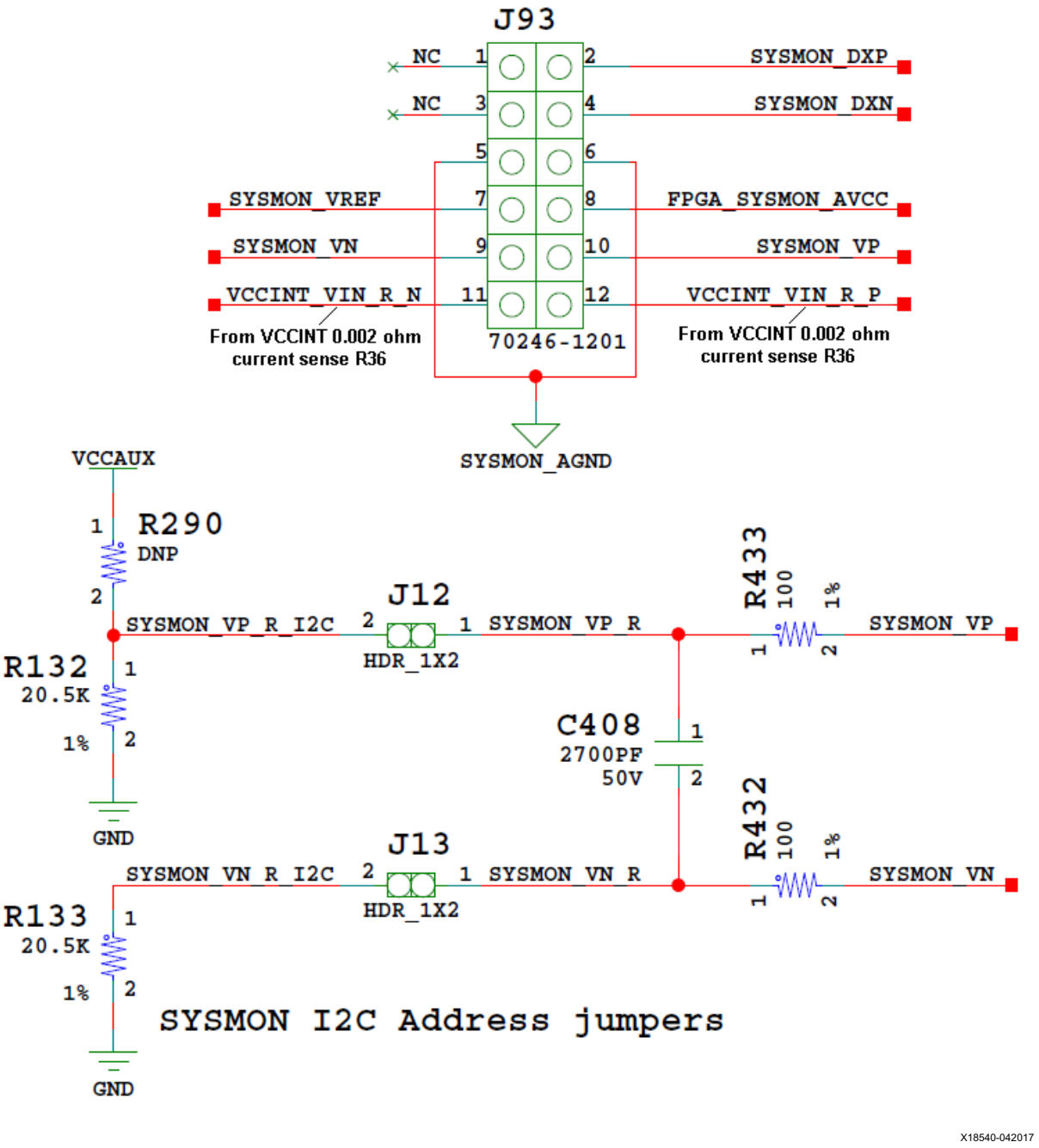

Figure 3-31: **SYSMON Header J93**

Table 3-28 describes the SYSMON header J93 pin functions.

Table 3-28: **SYSMON Header J93 Pinout**

Schematic Net Name	J93 Pin Number	Description
NC	1,3	No connect
SYSMON_DXP, SYSMON_DXN	2,4	Access to thermal diode
SYSMON_AGND	5,6	Analog ground reference
SYSMON_VREF	7	REF3012 U64 1.25V
SYSMON_VCC	8	Filtered V_{CCAUX} 1.80V
SYSMON_VN, SYSMON_VP	9,10	FPGA dedicated analog input channel for SYSMON
VCCINT_VIN_R_P/N	11,12	MAX15301 U47 V_{CCINT} series 0.002Ω R36 IR-drop taps

For more details on SYSMON, see the *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 20].

System Controller

[Figure 2-1, callout 36]

The KCU116 board includes an onboard Zynq® SoC multiprocessor XC7Z010 (U161) with system controller firmware. A host PC resident graphical user interface for the system controller (SCUI) is provided on the KCU116 website. The SCUI can be used to query and control select programmable features such as clocks, FMC functionality, and power systems. The KCU116 website also includes a *KCU116 System Controller Tutorial* (XTP465) [Ref 16] and KCU116 *Software Install and Board Setup Tutorial* (XTP464) [Ref 17]. A summary of the steps are:

1. Ensure the Silicon Labs VCP USB-UART drivers are installed on the host PC. See *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033) [Ref 15].
2. Download the SCUI host PC application.
3. Connect the micro-B USB cable to the KCU116 board USB-UART connector (J164).
4. Power-cycle the KCU116 board.
5. Launch the SCUI.

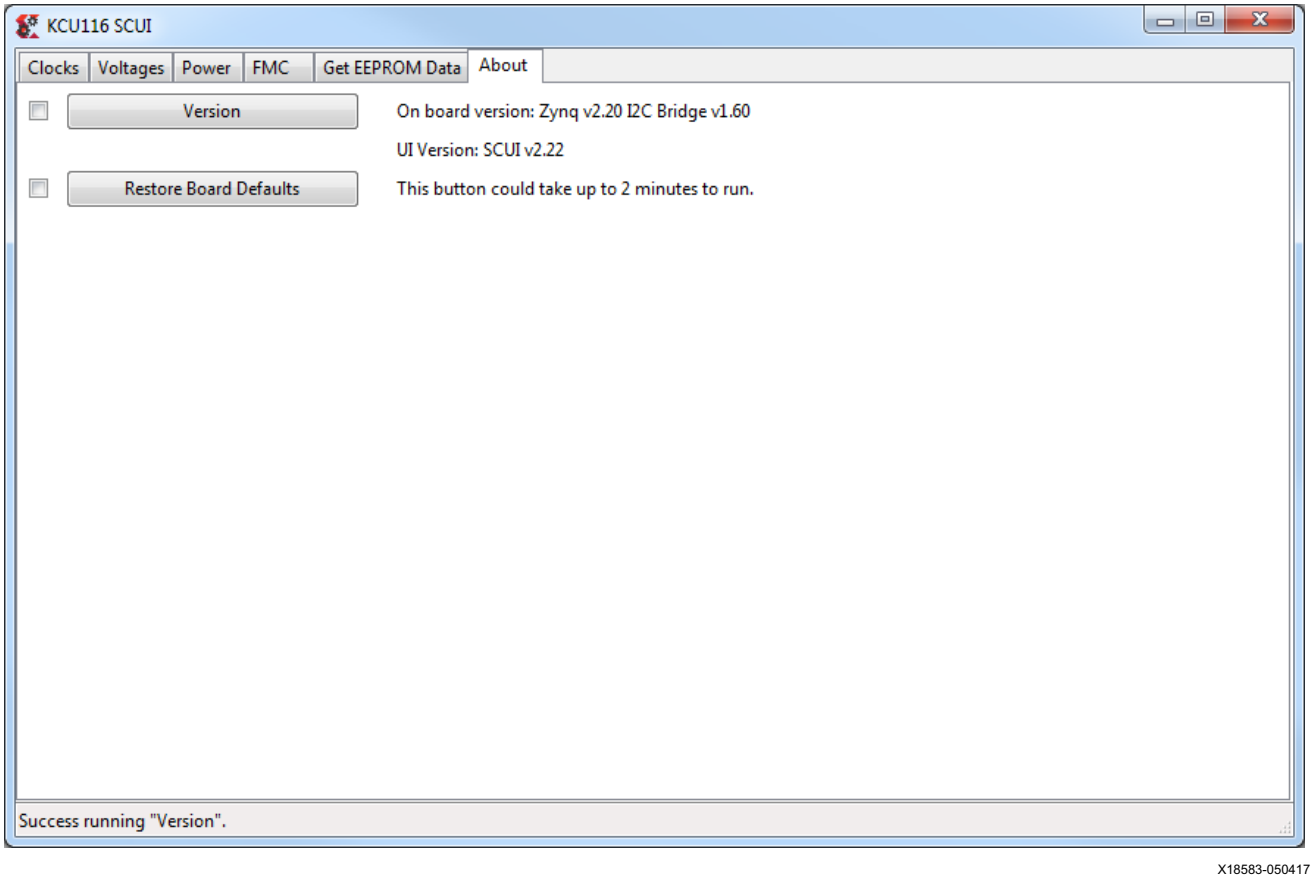

Figure 3-32: **KCU116 SCUI**

On first use of the SCUI, go to the **FMC** > **Set VADJ** > **Boot-up** tab and click **USE FMC EEPROM Voltage**. The SCUI buttons are grayed out during command execution and return to their original appearance when ready to accept a new command. See Figure 3-32.

See the *KCU116 System Controller Tutorial* (XTP465) [Ref 16] and the *KCU116 Software Install and Board Setup Tutorial* (XTP464) [Ref 17] for more information on installing and using the system controller utility.

For additional information on the Zynq-7000 SoC device I^2C controller, see the *Zynq-7000 SoC Overview Data Sheet* (DS190) [Ref 2] and the *Zynq-7000 SoC Technical Reference Manual* (UG585) [Ref 12].

VITA 57.1 FMC Connector Pinout

Overview

Figure A-1 shows the pinout of the FPGA mezzanine card (FMC) high pin count (HPC) J5 defined by the VITA 57.1 FMC specification. For a description of how the KCU116 evaluation board implements the FMC specification, see FPGA Mezzanine Card Interface, page 68.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

X18584-042017

Figure A-1: **FMC HPC Connector Pinout**

Appendix B

Xilinx Constraints File

Overview

The Xilinx® design constraints (XDC) file template for the KCU116 board is for designs targeting the KCU116 evaluation board. Net names in the constraints correlate with net names on the latest KCU116 evaluation board schematic. Users must identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 13] for more information.

The FMC connector J5 (HPC0) is connected to a 1.8V V_{ADJ} bank. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT: *The XDC file can be accessed on the Kintex UltraScale+ FPGA KCU116 Evaluation Kit website.*

Appendix C

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

KCU116 Evaluation Kit — Master Answer Record (AR 68360)

For Technical Support, open a Support Service Request.

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix D

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the KCU116 board and its documentation is available on the following websites.

KCU116 Evaluation Kit

KCU116 Evaluation Kit — Master Answer Record (AR 68360)

These Xilinx documents provide supplemental material useful with this guide:

1. *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922)
2. *Zynq-7000 All Programmable SoC Overview Data Sheet* (DS190)
3. *UltraScale Architecture Configuration User Guide* (UG570)
4. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
5. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
6. *UltraScale Architecture Clocking Resources User Guide* (UG572)
7. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
8. *UltraScale FPGAs Transceivers Wizard Product Guide for Vivado Design Suite* (PG182)
9. *UltraScale Architecture Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156)
10. *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051)
11. *AXI UART Lite LogiCORE IP Product Guide* (PG142)
12. *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585)
13. *Vivado Design Suite User Guide: Using Constraints* (UG903)
14. *UltraScale Architecture PCB Design User Guide* (UG583)
15. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)
16. *KCU116 System Controller Tutorial* (XTP465)
17. *KCU116 Software Install and Board Setup Tutorial* (XTP464)
18. *UltraScale Devices Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide for Vivado Design Suite* (UG156)
19. *DisplayPort LogiCORE Product Guide* (PG064)
20. *UltraScale Architecture System Monitor User Guide* (UG580)
21. For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the Xilinx documentation website.

The following websites provide supplemental material useful with this guide:

22. Xilinx, Inc: www.xilinx.com

    (XCKU5P-2FFVB676E)

23. Micron Technology: www.micron.com

    (MT40A256M16HA-083E, N25Q256A11ESF40F)

24. SanDisk Corporation: www.sandisk.com
25. SD Association: www.sdcard.org
26. Digilent: www.digilentinc.com

    (USB JTAG Module, Pmod Peripheral Modules)

27. Silicon Labs: www.silabs.com

    (Si5335A, Si570, Si53340, Si5328B)

28. PCI Express® standard: www.pcisig.com/specifications
29. SFF-8431 specification: ftp.seagate.com/sff
30. Analog Devices: www.analog.com/en/index.html

    (ADV7511KSTZ-P, ADP123, ADG707)

31. Texas Instruments: www.ti.com

    (TCA9548, PCA9544, DP83867ISRGZ)

32. Samtec, Inc.: www.samtec.com

    (SEAF series connectors)

33. VITA FMC Marketing Alliance: www.vita.com

    (FPGA Mezzanine Card (FMC) VITA 57.1 specification)

34. Maxim Integrated: http://www.maximintegrated.com/products/power/intune/ and http://www.maxim-ic.com/xilinx

    (Maxim power system devices, InTune™ Digital Power Solutions)

    InTune™ Digital PowerTool Software Version 1.08.02 is available. Users will have to create a Maxim account and login before they can see the link to download the GUI.

35. The Xilinx ATX cable part number 2600304 is manufactured by Sourcegate Technologies and is equivalent to the Sourcegate Technologies part number AZCBL-WH-11009.

Sourcegate only manufactures the latest revision, which is currently A4. To order, contact Aries Ang, aries.ang@sourcegate.net, +65 6483 2878 for price and availability. This is a custom cable and cannot be ordered from the Sourcegate website.

Please Read: Important Legal Notices