Kintex-7 FPGA Embedded Targeted Reference Design

User Guide

Vivado Design Suite 2013.2

UG985 (v1.0), August 29, 2013

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/29/2013	1.0	Initial Xilinx release.

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Chapter 2: Functional Description

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Introduction

The KC705 Embedded Kit MicroBlaze™ Processor Subsystem showcases various features of the KC705 evaluation board. The targeted reference designs (TRDs) are built around a MicroBlaze soft processor with various peripherals to enable embedded applications. Two designs are provided as part of the TRD: the KC705_System (BIST system) and the video demonstration system. Along with these designs, a stand-alone software application and webserver-based application are provided.

The BIST design provides a platform to jump start embedded system development on the KC705 evaluation platform. It provides a MicroBlaze processor based embedded platform that can be used to develop complex systems. The video demonstration is a superset of the BIST system and demonstrates these capabilities:

- MicroBlaze processor running at 150 MHz
- Four pipelined video streams system capable of showcasing up to 23 Gb/s data throughput
- 64-bit DDR controller running at 800 MHz
- 29 AXI-Lite slaves controlled and configured by the MicroBlaze processor
- 12 AXI MM masters in video data flow
- Four AXI MM interconnects connected in hierarchical fashion
- Two AXI-Lite interconnects connected in hierarchical fashion
- Multiplexing capability of internally generated test patterns or external video
- Integration of third-party video display controller, logiCVC, capable of supporting multiple video streams
- Modular-based video system in which any video pipeline can be easily added or removed

This document explains the functional architecture of the hardware and software components of the TRD. To build hardware and software for this TRD, see the Wiki page:

[Xilinx KC705 Embedded Kit MicroBlaze Processor Subsystem Targeted Reference Design](#)

Chapter 2

Functional Description

Introduction

This chapter describes the hardware design, software system, and software application components of both the BIST system and the video demonstration system.

Hardware Architecture

BIST Hardware Platform

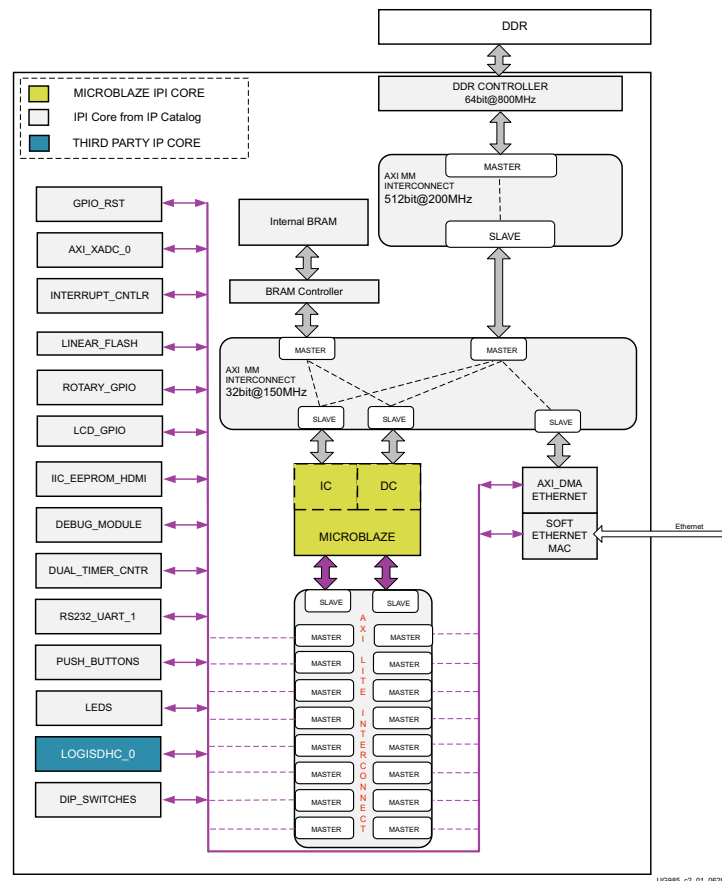The block diagram of the KC705 MicroBlaze processor subsystem is shown in Figure 2-1.

Figure 2-1: **BIST Hardware Block Diagram**

Note: Connections between the AXI-Lite interconnect and other peripherals are shown as buses for better graphical representation. The actual connections are point-to-point between each master port of interconnect to the corresponding peripheral.

This system is implemented in the Kintex®-7 XC7K325TFFG900-2 FPGA using the Vivado® Design Suite. The device utilization for the system is listed in Table 2-1.

Table 2-1:   **Hardware Utilization of BIST Design Device XC7K325TFFG900-2**

FPGA Components	Total Available	Used	% of Used
LUTs	203,800	28,912	14.18
I/Os	500	239	47.79
FPGA Logic Memory			
RAMB36E1	445	30	6.74
RAMB18E1	890	3	0.33
Slice registers	407,600	32,316	7.92

Note: Device resource utilization results are indicative and are dependent on the version of the implementation tool. Exact results might vary with the version of the tool.

The advantage of implementing this system in an FPGA is that the system can easily be expanded and customized in these ways:

- Configure/modify the MicroBlaze processor.
- Configure/modify the existing peripherals.
- Increase the amount of internal RAM.
- Remove peripherals that are not needed in the user's application. For example, remove one of the GPIO instances.
- Add instances of Xilinx IP that are from the Xilinx IP catalog or a third-party IP.
- Add AXI IP or custom logic in the top-level wrapper.
- Add custom logic that either interfaces to the MicroBlaze processor embedded system or is totally independent.

System Features

Processor Block

- 32-bit MicroBlaze processor with 8 KB instruction cache (I-cache) and 8 KB data cache (D-cache):
  - Hardware barrel shifter
  - Memory management unit (MMU):
    - Provides full MMU functionality
    - Controls effective-address to physical-address mapping
    - Provides memory protection with two memory protection zones
- 8 KB local memory for instructions and data
- Debug module
- Interrupt controller
- Dual 32-bit timer/counter

Memory

- 1 GB 64-bit wide 800 MHz DDR3 SDRAM
- 64 KB internal block RAM
- 128 MB linear (parallel) flash
- Secure digital high-capacity (SDHC) controller
- 1 KB IIC EEPROM

Input/Output

- Three general-purpose input controllers:
  - 5-bit pushbutton controller
  - 4-bit DIP switch interface
  - 3-bit rotary switch interface
- Two general-purpose output controllers:
  - 7-bit LCD interface
  - 8-bit LED interface
- 16550 UART:
  - Software configurable baud rate, data width, parity, and stop bits
- 10/100/1000 Mb/s Tri-mode Ethernet MAC (TEMAC):
  - GMII interface to PHY
  - Scatter-gather direct memory access (DMA)
- axi_xadc:
  - Software configurable XADC block includes a dual 12-bit, 1 MSPS analog-to-digital convertor (ADC) and on-chip sensors

BIST Address Map

The address map of the MicroBlaze Processor Subsystem is shown in Table 2-2.

Table 2-2: **KC705 MicroBlaze Processor Subsystem Address Map**

Instance	Peripheral	Base Address	High Address
microblaze_0	I-cache/D-cache	0x80000000	0xFFFFFFFF
LocalMemory_Cntlr_D	lmb_bram_if_cntlr	0x00000000	0x00001FFF
LocalMemory_Cntlr_I	lmb_bram_if_cntlr	0x00000000	0x00001FFF
Interrupt_Cntlr	axi_intc	0x40100000	0x4010FFFF
debug_module	mdm	0x40200000	0X4020FFFF
Dual_Timer_Counter	axi_timer	0x40300000	0X4030FFFF
RS232_Uart_1	axi_uart16550	0x40400000	0x4040FFFF
Push_Buttons_5Bits	axi_gpio	0x40500000	0x4050FFFF
LEDs_8Bits	axi_gpio	0x40600000	0x4060FFFF
DIP_Switches_4Bits	axi_gpio	0x40700000	0x4070FFFF

Table 2-2: **KC705 MicroBlaze Processor Subsystem Address Map** *(Cont'd)*

Instance	Peripheral	Base Address	High Address
LCD_GPIO	axi_gpio	0x40800000	0x4080FFFF
ROTARY_GPIO	axi_gpio	0x40900000	0x4090FFFF
IIC_EEPROM	axi_iic	0x40A00000	0x40A0FFFF
Logisdhc_0	logisdhc	0x40B00000	0x40B0FFFF
axi_xadc_0	axi_xadc	0x40D00000	0x40D0FFFF
Linear_Flash	axi_emc	0x48000000	0x4FFFFFFF
AXI_DMA_Ethernet	axi_dma	0x50000000	0x5000FFFF
Soft_Ethernet_MAC	axi_ethernet	0x50100000	0X5013FFFF
DDR3_SDRAM	axi_7series_ddrx	0x80000000	0xBFFFFFFF
Internal_BRAM	axi_bram_cntl	0xC0000000	0xC000FFFF

BIST System Configuration

Clocking Methodology and Considerations

This system runs off a reference clock frequency of 200 MHz from the differential clock source on the board. The AXI MM and streaming masters/slaves operate at 150 MHz, the AXI-Lite and streaming masters/slaves operate at 100 MHz, and the DDR3 memory runs at 800 MHz. Table 2-3 shows the system clocks.

Table 2-3: **System Clocks**

Clock Signal	Source	Frequency (MHz)	Use
CLK _P, CLK_N	External differential clock	200	Input clock provided from the board to MIG 7 series IP
Mig_clk_200	MIG 7 series	200	• Reference clock for TEMAC • Input to Clocking Wizard IP and also used for AXI MM Interface
clk_100MHz	MIG 7 series	100	Low-speed slave clocks for AXI_Lite_0 interconnect
clk_150MHz	Clocking Wizard	150	Clock for MicroBlaze processor and instruction local memory bus (ILMB)/data local memory bus (DLMB) block RAM
ethernet_clk_125	Clocking Wizard	125	TEMAC GTX reference clock

Clocks Generator Configuration

Clocks are generated by the clock generator. Based on the user's clock configuration inputs, the clock generator determines the correct configuration of the PLLs. The clock generator configuration settings are listed in Table 2-4.

Table 2-4: **Clock Generator Configuration Settings**

Component	Frequency (MHz)	Phase	Buffered
Input Clock			
CLK	200.000000		
Processor			
microblaze_0	150.000000	0	TRUE
Buses			
axi4_0	200.000000	0	TRUE
axi4lite_0	100.000000	0	TRUE
Peripherals			
proc_sys_reset_0			
• Slowest_sync_clk	100.000000	0	TRUE
Interrupt_Cntlr			
• S_AXI_ACLK	100.000000	0	TRUE
ilmb			
• LMB_CLK	150.000000	0	TRUE
dlmb			
• LMB_CLK	150.000000	0	TRUE
debug_module			
• S_AXI_ACLK	100.000000	0	TRUE
Dual_Timer_Counter			
• S_AXI_ACLK	100.000000	0	TRUE
Internal_BRAM			
• S_AXI_ACLK	100.000000	0	TRUE
RS232_Uart_1			
• S_AXI_ACLK	100.000000	0	TRUE
Push_Buttons_5Bits			
• S_AXI_ACLK	100.000000	0	TRUE
LEDs_8Bits			
• S_AXI_ACLK	100.000000	0	TRUE
DIP_Switches_4Bits			

Table 2-4: **Clock Generator Configuration Settings** *(Cont'd)*

Component	Frequency (MHz)	Phase	Buffered
• S_AXI_ACLK	100.000000	0	TRUE
LCD_GPIO			
S_AXI_ACLK	100.000000	0	TRUE
ROTARY_GPIO			
• S_AXI_ACLK	100.000000	0	TRUE
Linear_Flash			
• S_AXI_ACLK	100.000000	0	TRUE
• RdClk	100.000000	0	TRUE
IIC_EEPROM			
• S_AXI_ACLK	100.000000	0	TRUE
DDR3_SDRAM			
• sys_clk	200.000000	0	TRUE
• ui_clk	200.000000	0	TRUE
• ui_add_clk_0	100.000000	0	TRUE
AXI_DMA_Ethernet			
• s_axi_lite_aclk	100.000000	0	TRUE
• m_axi_sg_aclk	150.000000	0	TRUE
• m_axi_mm2s_aclk	150.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
Soft_Ethernet_MAC			
• S_AXI_ACLK	100.000000	0	TRUE
• AXI_STR_TXD_ACLK	150.000000	0	TRUE
• AXI_STR_TXC_ACLK	150.000000	0	TRUE
• AXI_STR_RXD_ACLK	150.000000	0	TRUE
• AXI_STR_RXS_ACLK	150.000000	0	TRUE
• GTX_CLK	125.000000	0	TRUE
• REF_CLK	200.000000	0	TRUE
axi_xadc_0			
• S_AXI_ACLK	100.000000	0	TRUE
logisdhc_0			
• sd_base_clk	100.000000	0	TRUE
• S_AXI_ACLK	100.000000	0	TRUE

Table 2-4: **Clock Generator Configuration Settings** *(Cont'd)*

Component	Frequency (MHz)	Phase	Buffered
Top-Level Output Clock Ports			
• ddr_ck	800.000000	0	FALSE
• sd_clk	12.500000	0	FALSE

Reset

Resets for the MicroBlaze processor subsystem are generated from the active-High reset input from the board. The external board reset is filtered and synchronized to the system clock. The AXI interconnect reset signals are active-Low and are sequenced coming out of reset in this order:

1. Bus structures come out of reset.

2. Peripheral(s) come out of reset 16 clocks later.

3. The CPU comes out of reset 16 clocks after the peripherals.

Resets to the MicroBlaze processor subsystem are generated by the Proc Sys Reset IP core.

MicroBlaze Processor Configuration

The MicroBlaze processor is configured for performance optimization with a hardware barrel shifter and an MMU, and is optimized for speed.

The hardware barrel shifter can shift or rotate a data word by any number of bits in a single clock cycle. Data shifting is a required element of many key operations such as address generation and arithmetic functions. The action of a barrel shifter can be emulated in software, but this takes valuable time which is not available in real-time applications.

In the processor subsystem, full MMU functionality is enabled, including virtual memory address translation. In virtual mode, the MMU translates effective addresses into physical addresses. The MMU also supports memory protection, which allows small blocks of memory to be individually protected from unauthorized access.

The I-cache master and D-cache master are both enabled, each with a cache size of 8 KB. In addition, the I-cache and D-cache execute burst transactions up to eight data beats (8 x 32-bits). The cacheable block of the system is accessed through the axi4_0 interconnect where the Kintex-7 FPGA AXI DDRX memory controller and other high-speed slave peripherals are connected. The data port (DP) master of the MicroBlaze processor is enabled and connected to the axi4lite_0 interconnect where the low-speed slaves (like the axi_gpio and axi_timer) are connected (slaves that have register functionality or slaves that do not generate burst transactions).

Exceptions are generated for all illegal opcodes, unaligned data accesses, and bus errors. More information about the MMU, exceptions, I-cache, D-cache, and performance optimization can be found in the UG081, *MicroBlaze Processor Reference Guide Embedded Development Kit*.

AXI Interconnect Configuration

There are three AXI interconnects inside the KC705 MicroBlaze processor subsystem: axi4_0, axi_mm_mb, and axi4lite_0. The axi4_0 and axi_mm_mb interconnects are for masters and slaves that fully utilize the AMBA® AXI4™ protocol. This includes masters

like the MicroBlaze processor I-cache and D-cache, and axi_dma masters. The axi_7series_ddrx is connected as a slave to this interconnect. This system is a subset of the video demonstration system which has four AXI interconnects connected in hierarchical fashion. The hierarchical connection allows better timing closure and expansion of current hardware to support more AXI masters. It also helps in better floorplanning of the design. In this system also, the two interconnects (axi4_0 and axi_4_0_mb) are connected in hierarchical fashion, which allows design symmetry with the video demonstration design where multiple masters and slaves are connected through multiple interconnects to share the load.

The axi4lite_0 interconnect is for masters and slaves that are geared for the AXI4-Lite™ protocol (32-bit interface, supports only single transactions). This includes masters like the MicroBlaze processor instruction port and data port. In this design, the MicroBlaze processor instruction port is not connected. Slaves connected to this interconnect have register maps or user logic that does not contain high-speed logic like bursting. The axi_gpio and axi_timer IP cores are examples of slaves connected to the axi4lite_0 interconnect.

Interrupt Controller Configuration

The axi_intc contains one AXI4-Lite interface slave connection. The master connected to the axi_intc on the axi4lite_0 interconnect is the MicroBlaze processor DP. The MicroBlaze processor subsystem shows the internal interrupts generated in the embedded system and the priority ordering of the interrupts (Table 2-5).

Table 2-5: **MicroBlaze Processor Subsystem Interrupt Priorities**

Signal	Source	Description
AXI_DMA_Ethernet_mm2s_introut[1]	axi_dma	Transmit complete interrupt from the DMA.
AXI_DMA_Ethernet_s2mm_introut	axi_dma	Receive complete interrupt from the DMA.
Soft_Ethernet_MAC_INTERRUPT	axi_ethernet	Interrupt condition in the Ethernet has occurred, as indicated in the TEMAC Interrupt Status register.
Dual_Timer_Counter_Interrupt	axi_timer	In Generate Mode, indicates that the counter rolled over. In Capture Mode, the interrupt event is the capture event.
IIC_EEPROM_Intr	axi_iic	Interrupt condition in the IIC controller has occurred, as indicated in the IIC Interrupt Status register.
RS232_Uart_1_Intr	axi_uart16550	Interrupt condition in the UART 16550 has occurred, as indicated in the UART Interrupt Identification register.
logisdhc_0_interrupt	logisdhc	Interrupt from SDHC Controller.
xadc_Irpt[2]	axi_xadc	Interrupt condition in the XADC has occurred, as indicated in the XADC Interrupt Status register.

Notes:

1. This signal has the highest priority.
2. This signal has the lowest priority.

Dual Timer/Counter

The axi_timer contains one AXI4-Lite interface slave connection. The master connected to the axi_timer through the shared mode on the axi4lite_0 interconnect is the MicroBlaze processor DP. The axi_timer core is configured to provide two 32-bit timers.

debug_module

This instance includes a UART with a configurable slave bus interface that is configured for the AXI4-Lite interface. The MicroBlaze processor DP port is the master connected to the debug_module slave connections through the shared mode on the axi4lite_0 interconnect. The UART TX and RX signals are transmitted over the FPGA JTAG port to and from the Xilinx Microprocessor Debug (XMD) tool.

axi_bram_ctrl Configuration

The axi_bram_ctrl contains one AXI4 interface slave connection. The slave's data width is configured for 32 bits using the AXI4 interface. Masters connected to the axi_bram_ctrl are the MicroBlaze processor I-cache and D-cache through the AXI_4_0 interconnect, using the shared mode.

The C_S_AXI_SUPPORTS_NARROW_BURST is set to zero because all masters inside the system are 32 bits. This parameter should be set to one when connecting to masters bigger than 32 bits inside the design. Setting the parameter to zero allows for resource savings.

axi_7series_ddrx Configuration

The axi_7series_ddrx allows the user to use the Memory Interface Generator (MIG) to configure the memory controller. The axi_7series_ddrx contains one AXI4 interface slave connection. The slave's data width is configured for 512 bits. The DDRX controller is configured to support data throughput up to 100 Gb/s (512 bits x 200 MHz) whereas a 64-bit DDR memory can also support up to 100 Gb/s with an operating frequency of 800 MHz (64 bits x 1.6 Gb/s).

Masters connected to the axi_7series_ddrx through the AXI MM interconnects are I-cache and D-cache ports of the MicroBlaze processor, scatter-gather (SG), memory-map-to-stream (MM2S), and stream-to-memory-map (S2MM) ports of the DMA Ethernet controller. Masters have the ability of issuing one or more transactions to the interconnect. The read acceptance and write acceptance limit of the axi_7series_ddrx controller are both set to 32.

IIC Controller Configuration

The axi_iic contains one AXI4-Lite interface slave connection. The master connected to the axi_iic through the shared mode on the axi4lite_0 interconnect is the MicroBlaze processor DP.

The IIC controller supports 7-bit or 10-bit addressing and contains 16-byte transmit and receive FIFOs. It can be configured for standard mode operation (100 KHz) or fast mode operation (>100 KHz-400 KHz).

In the MicroBlaze processor subsystem, the IIC controller is used to interface to the IIC EEPROM and is configured for standard mode operation (100 KHz) with 7-bit addressing.

Linear Flash Controller Configuration

The axi_emc contains one AXI4-Lite interface slave connection. The master connected to the axi_emc through the shared mode on the axi4lite_0 interconnect is the MicroBlaze processor DP.

The axi_emc is used to interface with the external linear flash device (16-bit wide 128 Mb Numonyx Flash device PC28F00AP30TF). The flash controller is configured to execute multiple memory access cycles to match memory bank x data width to AXI data width (C_INCLUDE_DATAWIDTH_MATCHING_0 = 1).

GPIO Configuration

The axi_gpio contains one AXI4-Lite interface slave connection. The master connected to the axi_gpio instances through the shared mode on the axi4lite_0 interconnect is the MicroBlaze processor DP.

The axi_gpio core is instantiated five times in the system to allow the embedded system to control and access the push buttons (Push_Buttons_5Bits), DIP switches (DIP_Switches_4Bits), LCD interface (LCD_GPIO), rotary switch (ROTARY_GPIO), and LEDs (LEDs_8Bits).

- The Push_Buttons_5Bits instance is an input-only GPIO with a width of 5 bits.
- The DIP_Swithes_4Bits instance is an input-only GPIO with a width of 4 bits.
- The LEDs_8Bits instance is an output-only GPIO with a width of 8 bits.
- The LCD_GPIO instance is an output-only GPIO with a width of 7 bits.
- The ROTARY_GPIO instance is an input-only GPIO with a width of 3 bits.

UART Configuration

The axi_uart16550 contains one AXI4-Lite interface slave connection. The master connected to the axi_uart16550 through the shared mode on the axi4lite_0 interconnect is the MicroBlaze processor DP.

The UART core is configured to use interrupts. The baud rate, data bits, and parity settings are controlled through software.

axi_dma

The axi_dma is connected to the axi_ethernet by means of the AXI-Stream protocol. The AXI-Stream interface width is 32 bits for the axi_ethernet. The MM2S interface is equivalent to transmit (TX) and the S2MM is equivalent to receive (RX). The MM2S, S2MM, and SG interfaces are connected to the AXI_4_0 interconnect. The axi4lite_0 connection of the core is connected to the axi4lite_0 interconnect.

Note: The AXI interface slave connection clock on the axi_dma drives the axi_dma SG engine.

Ethernet Configuration

The axi_ethernet contains one AXI4-Lite interface slave connection and two AXI-Stream interfaces. The MicroBlaze processor DP port is the master connected to the axi_ethernet slave connections through the shared mode on the axi4lite_0 interconnect. The two AXI-Stream interfaces are connected to the stream interface of the axi_dma IP.

The TEMAC is configured to support a GMII/MII PHY interface and contains internal 4 KB transmit and receive FIFOs. In addition, TX and RX checksum offloading is enabled. On power-up or on reset, the onboard PHY is configured to operate in GMII mode with the PHY address set to 00001. The TEMAC can run at 10 Mb/s, 100 Mb/s, or 1,000 Mb/s depending on the network to which it is attached.

axi_xadc Configuration

The axi_xadc IP core consists of these major blocks:

- AXI4-Lite Interface Module
- XADC Core Logic
- XADC Hard Macro

The MicroBlaze processor DP port is connected as a master to the AXI-Lite interface of axi_xadc. Read and write transactions at the AXI4 are translated into equivalent XADC core logic and XADC hard macro transactions by the AXI4-Lite Interface Module.

Interrupt controller logic is included in the XADC core logic by setting the parameter C_INCLUDE_INTR = 1. The XADC hard macro can be accessed via both the JTAG Test Access Port (TAP) and the axi_xadc IP core. When simultaneous access of the XADC hard macro occurs, the JTAGLOCKED port can be asserted high by JTAG TAP. In this scenario, the axi_xadc IP core is not allowed to do any read/write access from/to the DRP or FPGA logic.

logisdhc Configuration

This is a third-party IP core used for accessing SD cards on KC705 board. The logisdhc IP contains one AXI4-Lite interface slave connection. The MicroBlaze processor DP port is the master and is connected to the logisdhc slave connections through the shared mode on the axi4lite_0 interconnect. The SD base clock is 100 MHz. The clock generator lock output is connected to the base clock input of the IP core to ensure that the clocks are stable well in advance.

Video Demonstration Hardware Platform

This design provides a MicroBlaze processor based embedded platform that can be used to develop complex video systems. The block diagram for the KC705 MicroBlaze processor subsystem is shown in Figure 2-2.
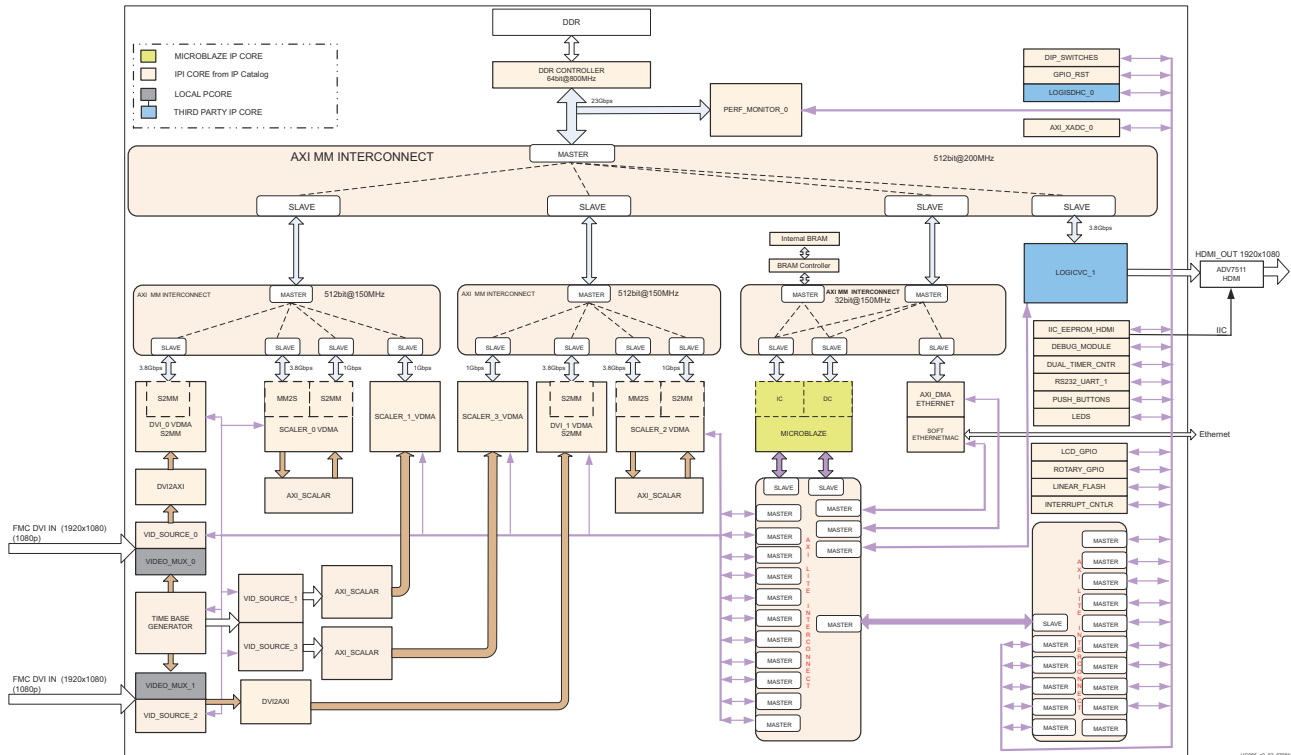

Figure 2-2: **Video Demonstration Block Diagram**

Note: Connections between the AXI-Lite interconnect and other peripherals are shown as buses only for better graphical representation. The actual connections are point-to-point between each master port of interconnect to the corresponding peripheral.

This system is implemented in the Kintex-7 XC7K325TFFG900-2 FPGA using the Vivado Design Suite. The device utilization for the system is listed in Table 2-6:

Table 2-6: **Hardware Utilization of Video Demonstration Design Device XC7K325TFFG900-2**

FPGA Components	Total Available	Used	% of Used
LUTs	203,800	28,912	14.18
I/Os	500	239	47.79
FPGA Logic Memory			
RAMB36E1	445	30	6.74
RAMB18E1	890	3	0.33
Slice registers	407,600	32,316	7.92

Note: Device resource utilization results are indicative and are dependent on the implementation tool versions. Exact results might vary with the version of the tool.

System Features

Processor Block

- MicroBlaze 32-bit processor with 8 KB I cache and 8 KB D cache
    - Hardware barrel shifter
    - MMU:
        - Provides full MMU functionality
        - Controls effective-address to physical-address mapping
        - Provides memory protection with two memory protection zones
- 64 KB local memory for instructions and data
- Debug module
- Interrupt controller
- Dual 32-bit timer/counter

Memory

- 1 GB 64-bit wide 800 MHz DDR3 SDRAM
- 64 KB internal block RAM
- 128 MB linear (parallel) flash
- SDHC controller
- 2GB SD card
- 1 KB IIC EEPROM

Input/Output

- Three general purpose input controllers:
    - 5-bit pushbutton controller
    - 4-bit DIP switch interface
    - 3-bit rotary switch interface
- Two general purpose output controllers:
    - 7-bit LCD interface
    - 8-bit LED interface
- 16550 UART
    - Software configurable baud rate, data width, parity, and stop bits
- 10/100 /1000 Mb/s TEMAC
    - GMII interface to PHY
    - Scatter-gather DMA
- axi_xadc
    - Software configurable XADC block includes a dual 12-bit, 1 MSPS ADC and on-chip sensors

Video Processing

- VSRC_SEL:
    - Video multiplexer for external video and internally generated test patterns
- AXI interconnect:
    - Four AXI MM Interconnects connected in a hierarchical fashion with 512-bit AXI MM interconnect running at 200 MHz
    - Two AXI_Lite_0 interconnects connected in a hierarchical fashion
    - Twelve AXI masters connected to AXI MM interconnect
    - Thirty-two AXI Lite slaves connected to AXI Lite interconnect
- Performance monitor: captures throughput values on the AXI interface of DDR controller
- logiCVC: AXI-based third-party display controller capable of supporting up to five layers of video display along with the alpha blending feature
- v_tc: AXI-based internal video timing control signal generator
- AXI TPG: AXI-based test pattern generator
- AXI Scaler: AXI-based scaler that scales the video frame from 1920 x 1080 to 960 x 540
- DVI Scaler: digital visual interface (DVI) in-line scaler that scales the video frame from 1920 x 1080 to 960 x 540

Video Data Throughput Calculations

Data throughput calculation for the video demonstration is:

- 1080p pixel clock frequency = (2200 pixels) x (1125 rows) x (60 frames/sec) = 148.5 MHz
- For one full frame write or read AXI data:

    (1920 active pixels) x (1080 active rows) x (32 bits/pixel) x (60 frames/sec) = 3.71 Gb/s (approximate)
- For one scaled frame write or read AXI data:

    (960 active pixels) x (540 active rows) x (32 bits/pixel) x (60 frames/sec) = 1 Gb/s (approximate)
- Stream 1 throughput:
    - DVI 0 video direct memory access (VDMA) S2MM (one full frame write) = 3.71 Gb/s
    - SCALER 0 VDMA MM2S (one full frame read) = 3.71 Gb/s
    - SCALER 0 VDMA S2MM (one scaled frame write) = 1 Gb/s
- Stream 2 throughput:
    - SCALER 1 VDMA S2MM (one scaled frame write) = 1 Gb/s
- Stream 3 throughput:
    - DVI 1 VDMA S2MM (one full frame write) = 3.71 Gb/s
    - SCALER 2 VDMA MM2S(one full frame read) = 3.71 Gb/s
    - SCALER 2 VDMA S2MM (one scaled frame write) = 1 Gb/s
- Stream 4 throughput:
    - SCALER 3 VDMA S2MM (one scaled frame write) = 1 Gb/s

- Display controller throughput:
  - logiCVC MM2S(one full frame rea) = 3.71 Gb/s
- Total throughput for displaying four scaled video streams on the video data is 23 Gb/s (11.5 Gb/s for write and 11.5 Gb/s for read)

Video Demonstration System Address Map

The address map of the MicroBlaze processor subsystem is listed in Table 2-7.

Table 2-7: **KC705 MicroBlaze Processor Subsystem Address Map**

Instance	Peripheral	Base Address	High Address
microblaze_0	I-cache/D-cache	0x80000000	0xFFFFFFFF
LocalMemory_Cntlr_D	lmb_bram_if_cntlr	0x00000000	0x00001FFF
LocalMemory_Cntlr_I	lmb_bram_if_cntlr	0x00000000	0x00001FFF
axi_perf_mon_1	axi_perf_mon	0x40000000	0x4000FFFF
Interrupt_Cntlr	axi_intc	0x40100000	0x4010FFFF
debug_module	mdm	0x40200000	0X4020FFFF
Dual_Timer_Counter	axi_timer	0x40300000	0X4030FFFF
RS232_Uart_1	axi_uart16550	0x40400000	0x4040FFFF
Push_Buttons_5Bits	axi_gpio	0x40500000	0x4050FFFF
LEDs_8Bits	axi_gpio	0x40600000	0x4060FFFF
DIP_Switches_4Bits	axi_gpio	0x40700000	0x4070FFFF
LCD_GPIO	axi_gpio	0x40800000	0x4080FFFF
ROTARY_GPIO	axi_gpio	0x40900000	0x4090FFFF
IIC_EEPROM	axi_iic	0x40A00000	0x40A0FFFF
Logisdhc_0	logisdhc	0x40B00000	0x40B0FFFF
gpio_rst_mux	axi_gpio	0x40C00000	0x40C0FFFF
axi_xadc_0	axi_xadc	0x40D00000	0x40D0FFFF
Linear_Flash	axi_emc	0x48000000	0x4FFFFFFF
AXI_DMA_Ethernet	axi_dma	0x50000000	0x5000FFFF
Soft_Ethernet_MAC	axi_ethernet	0x50100000	0X5013FFFF
vid_source_0	axi_tpg	0x50200000	0x5020FFFF
DVI_IN_0_VDMA	axi_vdma	0x50300000	0x5030FFFF
SCALER_0_VDMA	axi_vdma	0x50400000	0x5040FFFF
timebase_0	v_tc	0x50500000	0X5050FFFF
vid_source_1	axi_tpg	0x50600000	0x5060FFFF
SCALER_1_VDMA	axi_vdma	0x50700000	0X5070FFFF
vid_source_2	axi_tpg	0x50800000	0x5080FFFF

Table 2-7: **KC705 MicroBlaze Processor Subsystem Address Map** *(Cont'd)*

Instance	Peripheral	Base Address	High Address
DVI_IN_1_VDMA	axi_vdma	`0x50900000`	`0X5090FFFF`
SCALER_2_VDMA	axi_vdma	`0x50A00000`	`0X50A0FFFF`
vid_source_3	axi_tpg	`0x50B00000`	`0x50B0FFFF`
SCALER_3_VDMA	axi_vdma	`0x50C00000`	`0X50C0FFFF`
logicvc_1	logicvc	`0x50D00000`	`0X50D0FFFF`
Internal_BRAM	axi_bram_ctrl	`0xC0000000`	`0xC000FFFF`
DDR3_SDRAM	axi_7series_ddrx	`0x80000000`	`0xBFFFFFFF`

Video Demonstration System Configuration

Clocking Methodology and Considerations

This is the same as in the BIST system (see Clocking Methodology and Considerations).

Clock Generator Configuration

Clocks are generated by the clock generator. Based on the user's clock configuration inputs, the clock generator determines the correct configuration of the PLLs. The clock generator configuration settings are shown in Table 2-8.

Table 2-8: **Clock Generator Configuration Settings**

Component	Frequency (MHz)	Phase	Buffered
Input Clock			
CLK	200.000000		
Processor			
microblaze_0	150.000000	0	TRUE
Buses			
axi4_0	150.000000	0	TRUE
axi4lite_0	100.000000	0	TRUE
Peripherals			
proc_sys_reset_0			
• Slowest_sync_clk	100.000000	0	TRUE
Interrupt_Cntlr			
• S_AXI_ACLK	100.000000	0	TRUE
ilmb			
• LMB_CLK	150.000000	0	TRUE
dlmb			
• LMB_CLK	150.000000	0	TRUE
debug_module			

Table 2-8: **Clock Generator Configuration Settings** *(Cont'd)*

Component	Frequency (MHz)	Phase	Buffered
• S_AXI_ACLK	100.000000	0	TRUE
Dual_Timer_Counter			
• S_AXI_ACLK	100.000000	0	TRUE
Internal_BRAM			
• S_AXI_ACLK	100.000000	0	TRUE
RS232_Uart_1			
• S_AXI_ACLK	100.000000	0	TRUE
Push_Buttons_5Bits			
• S_AXI_ACLK	100.000000	0	TRUE
LEDs_8Bits			
• S_AXI_ACLK	100.000000	0	TRUE
DIP_Switches_4Bits			
• S_AXI_ACLK	100.000000	0	TRUE
LCD_GPIO			
• S_AXI_ACLK	100.000000	0	TRUE
ROTARY_GPIO			
• S_AXI_ACLK	100.000000	0	TRUE
Linear_Flash			
• S_AXI_ACLK	100.000000	0	TRUE
• RdClk	100.000000	0	TRUE
IIC_EEPROM			
• S_AXI_ACLK	100.000000	0	TRUE
DDR3_SDRAM			
• sys_clk	200.000000	0	TRUE
• ui_clk	200.000000	0	TRUE
• ui_add_clk_0	100.000000	0	TRUE
AXI_DMA_Ethernet			
• s_axi_lite_aclk	100.000000	0	TRUE
• m_axi_sg_aclk	150.000000	0	TRUE
• m_AXI_MM2S_aclk	150.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
Soft_Ethernet_MAC			
• S_AXI_ACLK	100.000000	0	TRUE
• AXI_STR_TXD_ACLK	150.000000	0	TRUE
• AXI_STR_TXC_ACLK	150.000000	0	TRUE

Table 2-8: **Clock Generator Configuration Settings** *(Cont'd)*

Component	Frequency (MHz)	Phase	Buffered
• AXI_STR_RXD_ACLK	150.000000	0	TRUE
• AXI_STR_RXS_ACLK	150.000000	0	TRUE
• GTX_CLK	125.000000	0	TRUE
• REF_CLK	200.000000	0	TRUE
axi_xadc_0			
• S_AXI_ACLK	100.000000	0	TRUE
logisdhc_0			
• sd_base_clk	100.000000	0	TRUE
• S_AXI_ACLK	100.000000	0	TRUE
vid_source_0			
• S_AXI_ACLK	100.000000	0	TRUE
• clk	150.000000	0	TRUE
DVI_0_2_AXI_SM			
• fmc_hpc_dvidp_dvii_clk	150.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
DVI_IN_0_VDMA			
• s_axis_s2mm_aclk	150.000000	0	TRUE
• s_axi_lite_aclk	100.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
SCALER_0_VDMA			
• s_axis_s2mm_aclk	150.000000	0	TRUE
• m_axis_mm2s_aclk	150.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
• m_AXI_MM2S_aclk	150.000000	0	TRUE
• s_axi_lite_aclk	100.000000	0	TRUE
SCALER_0			
• m_AXI_MM2S_aclk	150.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
timebase_0			
• video_clk_in	150.000000	0	TRUE
vid_source_1			
• S_AXI_ACLK	100.000000	0	TRUE
• clk	150.000000	0	TRUE
TPG_0_SCALE_2_AXI_SM			
• fmc_hpc_dvidp_dvii_clk	150.000000	0	TRUE

Table 2-8: **Clock Generator Configuration Settings** *(Cont'd)*

Component	Frequency (MHz)	Phase	Buffered
• m_axi_s2mm_aclk	150.000000	0	TRUE
SCALAR_1_VDMA			
• s_axis_s2mm_aclk	150.000000	0	TRUE
• s_axi_lite_aclk	100.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
vid_source_2			
• S_AXI_ACLK	100.000000	0	TRUE
• clk	150.000000	0	TRUE
DVI_1_2_AXI_SM			
• fmc_hpc_dvidp_dvii_clk	150.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
DVI_IN_1_VDMA			
• s_axis_s2mm_aclk	150.000000	0	TRUE
• s_axi_lite_aclk	100.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
SCALER_2_VDMA			
• s_axis_s2mm_aclk	150.000000	0	TRUE
• m_axis_mm2s_aclk	150.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
• m_AXI_MM2S_aclk	150.000000	0	TRUE
• s_axi_lite_aclk	100.000000	0	TRUE
SCALER_2			
• m_AXI_MM2S_aclk	150.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
vid_source_3			
• S_AXI_ACLK	100.000000	0	TRUE
• clk	150.000000	0	TRUE
TPG_2_SCALE_2_AXI_SM			
• fmc_hpc_dvidp_dvii_clk	150.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
SCALAR_3_VDMA			
• s_axis_s2mm_aclk	150.000000	0	TRUE
• s_axi_lite_aclk	100.000000	0	TRUE
• m_axi_s2mm_aclk	150.000000	0	TRUE
LOGICVC			

Table 2-8: **Clock Generator Configuration Settings** *(Cont'd)*

Component	Frequency (MHz)	Phase	Buffered
• S_AXI_ACLK	100.000000	0	TRUE
• mclk	150.000000	0	TRUE
• vclk	150.000000	0	TRUE
dvi_24_to_16bit_ycbcr_0			
• clk	150.000000	0	TRUE
Top-Level Output Clock Ports			
• ddr_ck	800.000000	0	FALSE
• sd_clk	12.500000	0	FALSE
• hdmi_clk	150.000000	0	FALSE

Reset

Configuration details are the same as in the BIST system (see Reset).

MicroBlaze Processor Configuration

Configuration details are the same as in the BIST system (see MicroBlaze Processor Configuration).

Dual Timer/Counter

Configuration details are the same as in the BIST system (see Dual Timer/Counter).

debug_module

Configuration details are the same as in the BIST system (see debug_module).

axi_bram_ctrl Configuration

Configuration details are the same as in the BIST system (see axi_bram_ctrl Configuration).

axi_7series_ddrx Configuration

Configuration details are the same as in the BIST system (see axi_7series_ddrx Configuration).

IIC Controller Configuration

Configuration details are the same as in the BIST system (see IIC Controller Configuration).

Linear Flash Controller Configuration

Configuration details are the same as in the BIST system (see Linear Flash Controller Configuration).

GPIO Configuration

Configuration details are the same as in the BIST system (see GPIO Configuration).

UART Configuration

Configuration details are the same as in the BIST system (see UART Configuration).

axi_dma

Configuration details are the same as in the BIST system (see axi_dma).

Ethernet Configuration

Configuration details are the same as in the BIST system (see Ethernet Configuration).

axi_xadc Configuration

Configuration details are the same as in the BIST system (see axi_xadc Configuration).

logisdhc Configuration

Configuration details are the same as in the BIST system (see logisdhc Configuration).

AXI Interconnect Configuration

Two types of interconnects are implemented in the system. The AXI_MM type of interconnect is for masters and slaves that fully utilize the AXI4 protocol for high-throughput data exchange. The AXI_Lite type is for masters and slaves that are geared for the AXI4-Lite protocol (32-bit interface, supports only single transactions).

Four AXI_MM interconnects (axi4_0, axi_mm_mb, axi_mm_video12, and axi_mm_video34) are connected in a hierarchical fashion. This allows for better timing closure and expansion of current hardware to support more AXI masters. It also helps in floorplanning of the design. The axi4_0 interconnect is configured for 512-bit width and operates at 200 MHz. A total of 12 masters are connected in the design, and the DDRX controller is the only slave connected to axi4_0 that is accessible to all the masters.

The design is partitioned so that the MicroBlaze processor and Ethernet DMA are connected to axi_mm_mb, the first two video pipelines (four VDMA masters) are connected to axi_mm_video12, and the last two video pipelines (four VDMA masters) are connected to axi_mm_video34. Apart from this, the logiCVC display controller is another master on the axi4_0 interconnect. This design can be expanded to support more video pipelines to either axi_mm_video12 or axi_mm_video34 interconnects. Each of these two interconnects can support 12 more masters.

Two AXI_lite interconnects (axi4lite_0 and axi4lite_1) are connected in hierarchical fashion. The MicroBlaze processor is the master for axi4lite_0, and axi4lite_1 is connected as one of the slaves to axi4lite_0. Slaves connected to this interconnect have register maps or user logic that does not contain high-speed logic like bursting. A total of 32 slaves are connected to the MicroBlaze processor through these two interconnects. All interconnects are configured for 32-bit widths and operate at 100 MHz. The axi_gpio and axi_timer IP cores are examples of slaves connected to the axi4lite_0 interconnect.

Video Source Select

Video Source Select multiplexes between internally generated test patterns or external video. The output of this block is given to the DVI2AXI block. Selection is through a GPIO register bit (position 4 of the GPIO reset register: `0x40C00000`). Two instances of this block handle multiplexing of the two external video streams.

Video Timing Controller

The v_tc is one of the AXI_Lite slaves to the MicroBlaze processor connected through the axi4lite_0 interconnect. Time base is configured to work in generate mode by setting the parameter GENERATE_EN. It is configured to generate timing control signals for a video resolution of 1080p. Timing control signals generated from this block are common for all the video test patterns generated internally.

DVI2AXI

This block converts a video input consisting of parallel video data, video syncs, blanks, and data enable to an AXI4-Stream™ master bus that follows the AXI4-Stream Video protocol. This functionality is achieved using Video In to AXI4-Stream core. This core handles the asynchronous clock boundary crossing between the video clock domain and the AXI4-Stream clock domain. Two instances of this IP are implemented in the system to support two external video streams.

AXI_SCALAR

This block scales down the video frame by a factor of four, i.e., from a 1920 x 1080 input resolution, AXI_SCALAR generates video with a resolution of 960 x 540. It has two streaming interfaces that are connected to the S2MM and MM2S channels of Scalar VDMA. Two instances of this IP are connected to scale two video pipelines.

DVI_SCALAR

This block scales down the video frame by a factor of four. The functionality of DVI_SCALAR is the same as AXI_SCALAR, provided it scales the video image dynamically before writing it into the memory. However, AXI_SCALAR reads the frame from memory, scales it, and writes it back to the frame in a different location of the memory. The input interface of this block is the DVI interface, and the output interface is a streaming interface towards the S2MM channel of the SCALAR VDMA. Two instances of this IP are connected to two scale video pipelines.

vid_source

The vid_source contains one AXI4-Lite interface slave connection. The master connected to the vid_source on the axi4lite_0 interconnect is the MicroBlaze processor DP. Different video patterns can be generated inside the FPGA by configuring pattern select registers. Four instances of the IP are implemented in the system to generate four different test patterns.

DVI_IN_0_VDMA

DVI_IN_0_VDMA has two interfaces: one is the 32-bit streaming interface towards the DVI2AXI block, and the other is a 64-bit AXI MM interface towards the axi_mm_video12 interconnect. The S2MM channel is enabled, and the

C_PRMRY_IS_ACLK_ASYNC parameter is set because the clocks connected to the VDMA are of different frequencies. User register slices on all channels are set to 8. The S2MM line buffer is set to 4096, and the burst length is set to 256. Write FIFO delay in the interconnect settings is enabled with a FIFO delay of 512. The AXI MM and AXI Streaming interfaces operate at 150 MHz, and the AXI-Lite interface operates at 100 MHz. The MicroBlaze processor acts as a master for the Lite interface of the VDMA that is used for register configuration.

SCALER_0_VDMA

SCALER_0_VDMA has four interfaces: two are 32-bit streaming interfaces towards the AXI_SCALAR block, and the other two are a 64-bit AXI MM interface towards the axi_mm_video12 interconnect. Both S2MM and MM2S channels are enabled, and the C_PRMRY_IS_ACLK_ASYNC parameter is set because clocks connected to the VDMA are of different frequencies. User register slices on all channels are set to eight. The S2MM line buffer is set to 4096, and burst length is set to 256. The MM2S line buffer is set to 256, and the burst length is set to 256. Write FIFO delay in the interconnect settings is enabled with a FIFO delay of 512. The AXI MM and AXI Streaming interfaces operate at 150 MHz, and the AXI-Lite interface operates at 100 MHz. The MicroBlaze processor acts as a master for the lite interface of the VDMA that is used for register configuration.

SCALER_1_VDMA

SCALER_1_VDMA has two interfaces: one is the 32-bit streaming interface towards the DVI SCALAR block, and the other is the 64-bit AXI MM interface towards the axi_mm_video12 interconnect. The S2MM channel is enabled, and the C_PRMRY_IS_ACLK_ASYNC parameter is set because clocks connected to the VDMA are of different frequencies. User register slices on all channels are set to 8. The S2MM line buffer is set to 4096, and the burst length is set to 256. Write FIFO delay in the interconnect settings are enabled with a FIFO delay of 512. The AXI MM and AXI Streaming interfaces operate at 150 MHz, and the AXI-Lite interface operates at 100 MHz. The MicroBlaze processor acts as a master for the Lite interface of the VDMA that is used for register configuration.

DVI_IN_1_VDMA

DVI_IN_1_VDMA has two interfaces: one is the 32-bit streaming interface towards the DVI2AXI block, and the other is a 64-bit AXI MM interface towards the axi_mm_video34 interconnect. The S2MM channel is enabled and the

C_PRMRY_IS_ACLK_ASYNC parameter is set because clocks connected to the VDMA are of different frequencies. User register slices on all channels are set to 8. The S2MM line

buffer is set to 4096, and the burst length is set to 256. Write FIFO delay in the interconnect settings is enabled with a FIFO delay of 512. The AXI MM and AXI Streaming interfaces operate at 150 MHz, and the AXI-Lite interface operates at 100 MHz. The MicroBlaze processor acts as a master for the Lite interface of the VDMA that is used for register configuration.

SCALER_2_VDMA

SCALER_2_VDMA has four interfaces: two are 32-bit streaming interfaces towards the AXI SCALAR block, and the other two are a 64-bit AXI MM interface towards the axi_mm_video34 interconnect. Both the S2MM and MM2S channels are enabled, and the C_PRMRY_IS_ACLK_ASYNC parameter is set because clocks connected to VDMA are of different frequencies. User register slices on all channels are set to 8. The S2MM line buffer is set to 4096, and the burst length is set to 256. The MM2S line buffer is set to 256, and the burst length is set to 256. Write FIFO delay in the interconnect settings is enabled with a FIFO delay of 512. The AXI MM and AXI Streaming interfaces operate at 150 MHz, and the AXI-Lite interface operates at 100 MHz. The MicroBlaze processor acts as a master for the Lite interface of the VDMA that is used for register configuration.

SCALER_3_VDMA

SCALER_3_VDMA has two interfaces: one is the 32-bit streaming interface towards the DVI SCALAR block, and the other is a 64-bit AXI MM interface towards the axi_mm_video34 interconnect. The S2MM channel is enabled, and the C_PRMRY_IS_ACLK_ASYNC parameter is set because clocks connected to the VDMA are of different frequencies. User register slices on all channels are set to 8. The S2MM line buffer is set to 4096, and the burst length is set to 256. Write FIFO delay in the interconnect settings is enabled with a FIFO delay of 512. The AXI MM and AXI Streaming interfaces operate at 150 MHz, and the AXI-Lite interface operates at 100 MHz. The MicroBlaze processor acts as a master for the Lite interface of the VDMA that is used for register configuration.

logiCVC

The Xylon logiCVC is a third-party display controller. It has three interfaces: an AXI4-Lite interface slave connection controlled by the MicroBlaze processor, an AXI MM interface towards the AXI MM interconnect, and a video output interface towards the 24bit_16bit_ycbcr converter. The AXI MM data width is configured as 128. Configured for five layers, which includes one background layer, the data width of all the layers is configured as 24 bits. User register slices on all channels are set to 8. The FIFO depth towards the interconnect is set as 512. Frame sync for each layer is controlled by the frame sync out of the VDMAs corresponding to each video pipeline.

Interrupt Controller Configuration

The axi_intc contains one AXI4-Lite interface slave connection. The master connected to the axi_intc on the axi4lite_0 interconnect is the MicroBlaze processor DP. Table 2-9 lists the internal interrupts generated in the embedded system and the priority ordering of the interrupts.

Table 2-9: **MicroBlaze Processor Subsystem Interrupt Priorities**

Signal	Source	Description
AXI_DMA_Ethernet_mm2s_introut[1]	axi_dma	Transmit complete interrupt from the DMA.
AXI_DMA_Ethernet_s2mm_introut	axi_dma	Receive complete interrupt from the DMA.
Soft_Ethernet_MAC_INTERRUPT	axi_ethernet	Interrupt condition in the Ethernet has occurred, as indicated in the TEMAC Interrupt Status register.
Dual_Timer_Counter_Interrupt	axi_timer	In Generate mode, indicates that the counter rolled over. In Capture mode, the interrupt event is the capture event.
IIC_EEPROM_Intr	axi_iic	Interrupt condition in the IIC controller has occurred, as indicated in the IIC Interrupt Status register.
RS232_Uart_1_Intr	axi_uart16550	Interrupt condition in the UART 16550 has occurred, as indicated in the UART Interrupt Identification register.
logisdhc_0_interrupt	logisdhc	Interrupt from SDHC controller.
DVI_IN_0_VDMA_s2mm_introut	DVI_IN_0_VDMA	S2MM interrupt from DVI_IN_0 VDMA.
SCALER_0_VDMA_mm2s_introut	SCALER_0_VDMA	MM2S interrupt from SCALER_0 VDMA.
SCALER_0_VDMA_s2mm_introut	SCALER_0_VDMA	S2MM interrupt from SCALER_0 VDMA.
timebase_0_IP2INTC_Irpt	timebase_0	Interrupt from the VTC timing control signal generator.
SCALER_1_VDMA _s2mm_introut	SCALER_1_VDMA	S2MM interrupt from SCALER_1_VDMA.
DVI_IN_1_VDMA_s2mm_introut	DVI_IN_1_VDMA	S2MM interrupt from DVI_IN_1_VDMA.
SCALER_2_VDMA_mm2s_introut	SCALER_2_VDMA	MM2S interrupt from SCALER_2 VDMA.
SCALER_2_VDMA_s2mm_introut	SCALER_2_VDMA	S2MM interrupt from SCALER_2 VDMA.
SCALER_3_VDMA_s2mm_introut	SCALER_3_VDMA	S2MM interrupt from SCALER_3_VDMA.
logicvc_interrupt	logiCVC	Interrupt from logiCVC.
xadc_Irpt[2]	axi_xadc	Interrupt condition in the XADC has occurred, as indicated in the XADC Interrupt Status register.

Notes:
1. This signal has the highest priority.
2. This signal has the lowest priority.

Software Architecture

This section explains the software architecture for Kintex-7 Embedded TRD. This TRD has three applications:

- BIST console application
- BIST webserver application
- Video demonstration application

BIST Console Application

A monolithic application is created to run peripheral tests. Depending on inputs, the standalone drivers are invoked. The block diagram of software architecture for the BIST console application is shown in Figure 2-3. The upper portion of this diagram shows the main application flow, and the lower portion shows the sub-applications. The user can select a particular test to run by choosing an option provided in this application.
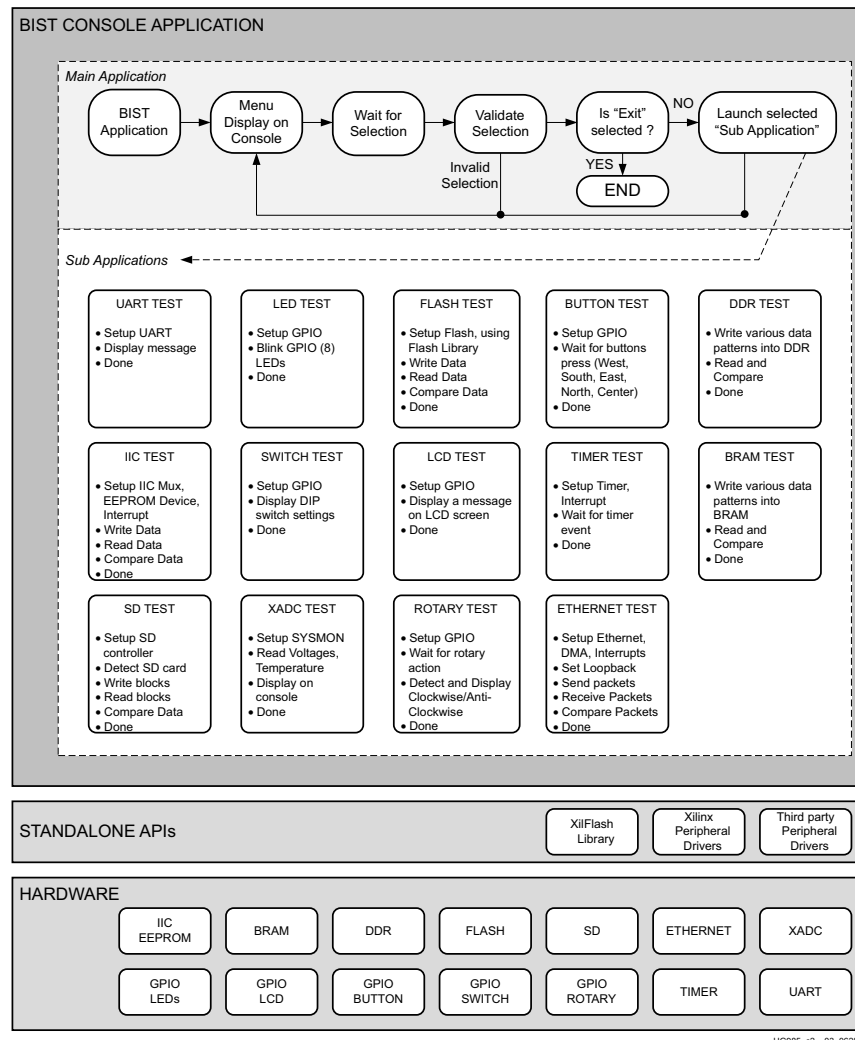
Figure 2-3: **Software Architecture for BIST Console Application**

BIST Webserver Application

The BIST webserver application is a multi-thread application to run the peripheral tests. This application has two major components:

- Target software, executing on Kintex-7
- Webserver software, executing on host PC

The webserver on the host PC provides the user interface. The selections are communicated to the target, tests are executed on the target, and the results are transported back to the host PC and displayed.

Target Software

The target software architecture is shown in Figure 2-4. Here, the main function spawns the network thread and the remaining threads are spawned in the execution process.
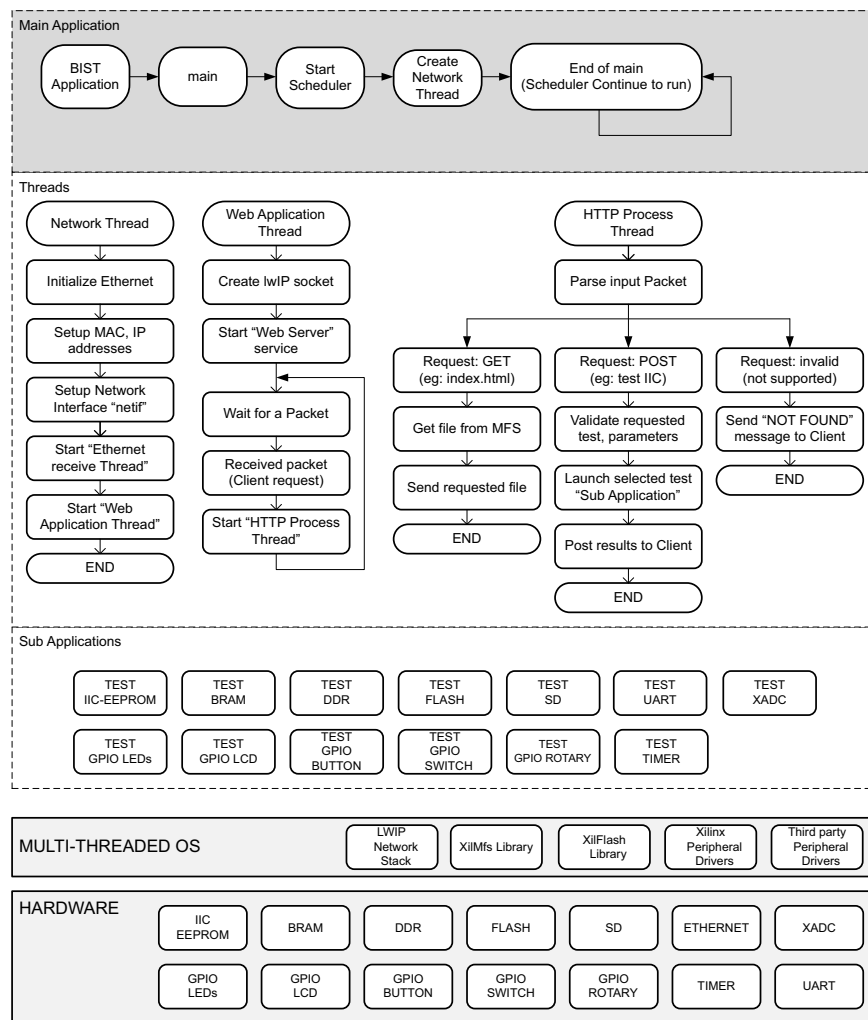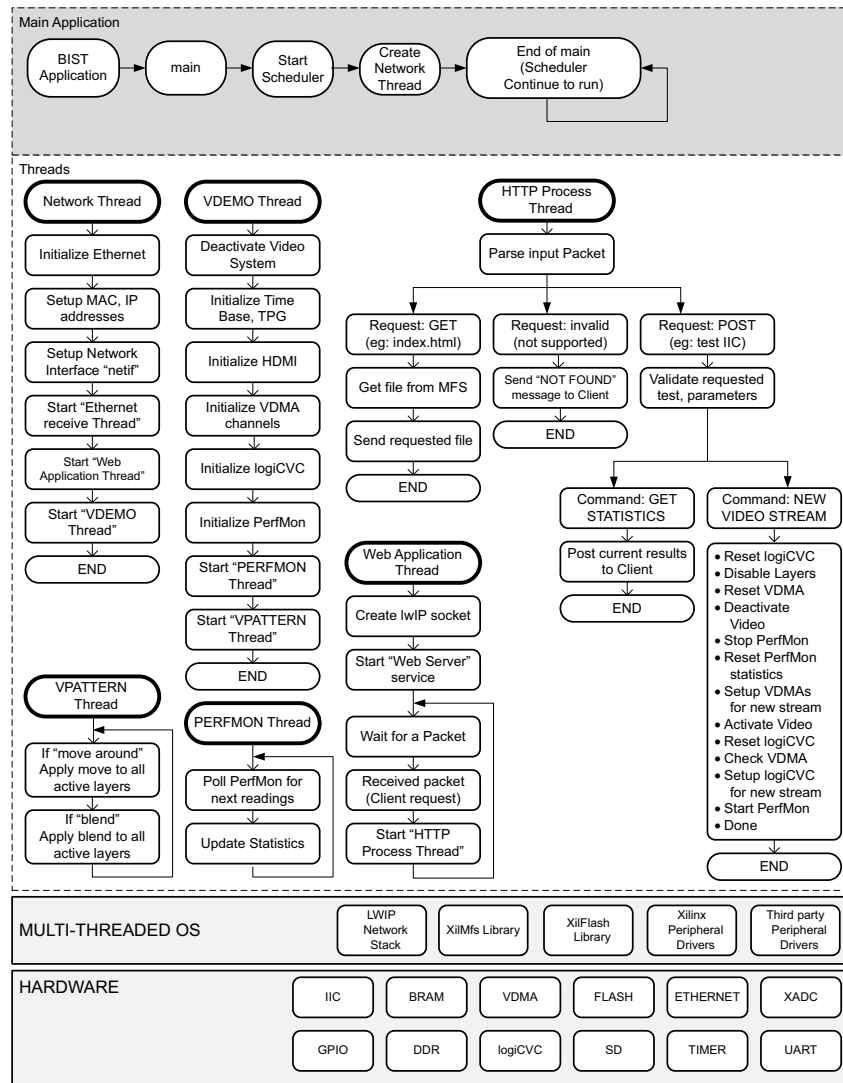

Figure 2-4:   **Software Architecture for BIST Webserver Application (Target Software)**

BIST Webserver

The BIST webserver is the second part of this application and it runs on the host PC. Figure 2-5 depicts the software architecture for the BIST webserver application, which is designed around HTTP and JavaScript.

UG985_c2_05_062513
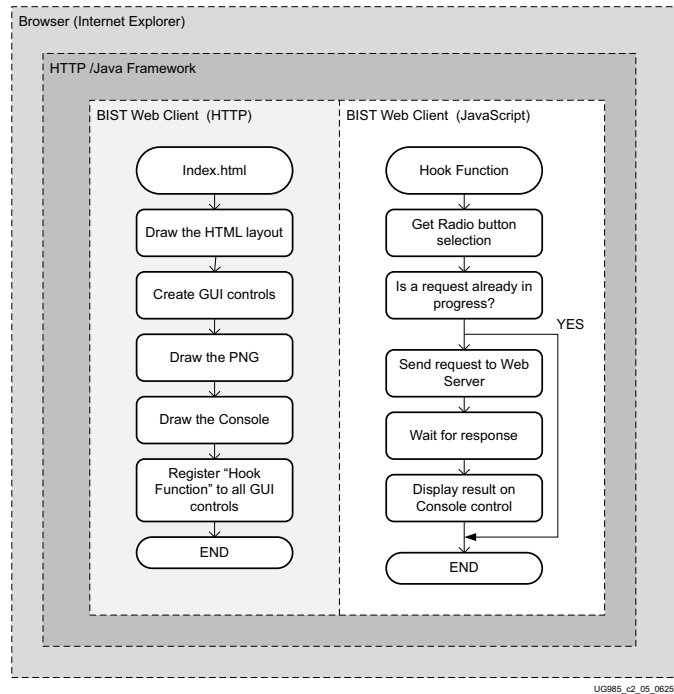
Figure 2-5: **Software Architecture for BIST Webserver Application (Server Software)**

Video Demonstration Application

The video demonstration application uses a webserver to display the video selection menu, video stream controls, and to plot various graphs, such as throughput data, on-chip temperature, and on-chip voltages (V_{CCINT} and V_{CCAUX}). It is a multi-thread application with two major components:

- Target software, executing on Kintex-7
- Webserver software, executing on the host PC

The webserver on the host PC provides the user interface. The selections are communicated to the target, tests are executed on the target, and the results are transported back to the host PC and displayed.

Target Software

The target software architecture is shown in Figure 2-6. Here, the main function spawns the network thread and the remaining threads are spawned in the execution process.

Figure 2-6:   **Software Architecture for Video Demonstration Application (Target Software)**

Video Demonstration Webserver

The webserver is the second part of this application that runs on the host PC. Figure 2-7 shows the software architecture for the video demonstration webserver application. It is designed around HTTP and JavaScript. The JavaScript has three hook functions to handle the user events and HTTP events. Additionally, JavaScript handles the graph to be plotted with the help of SVG Viewer.
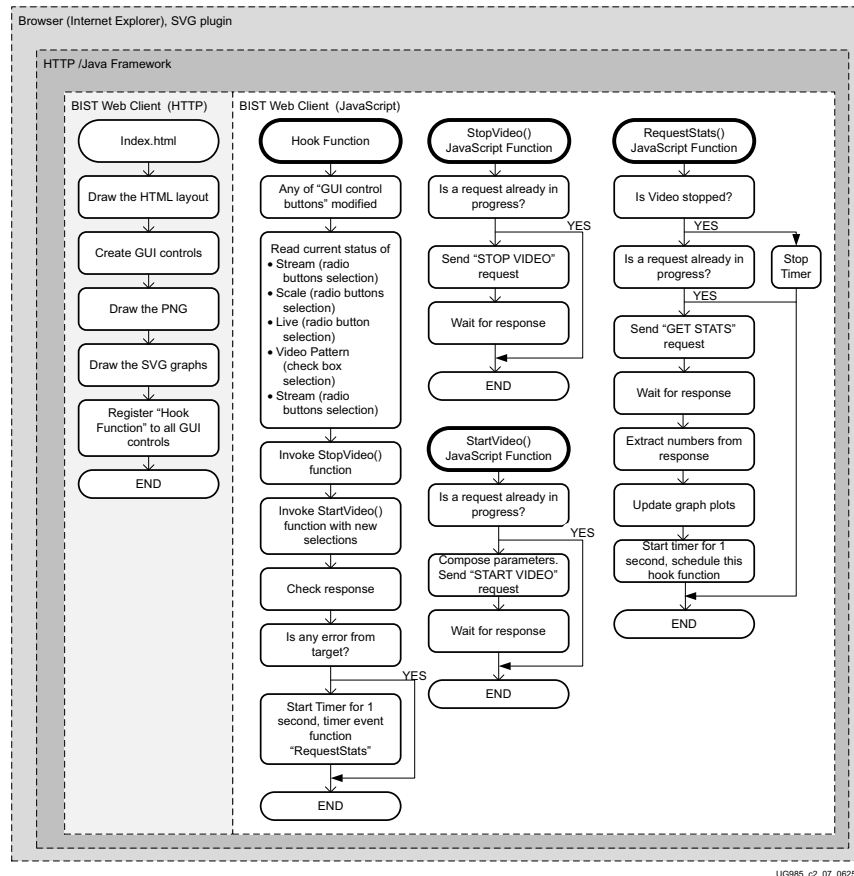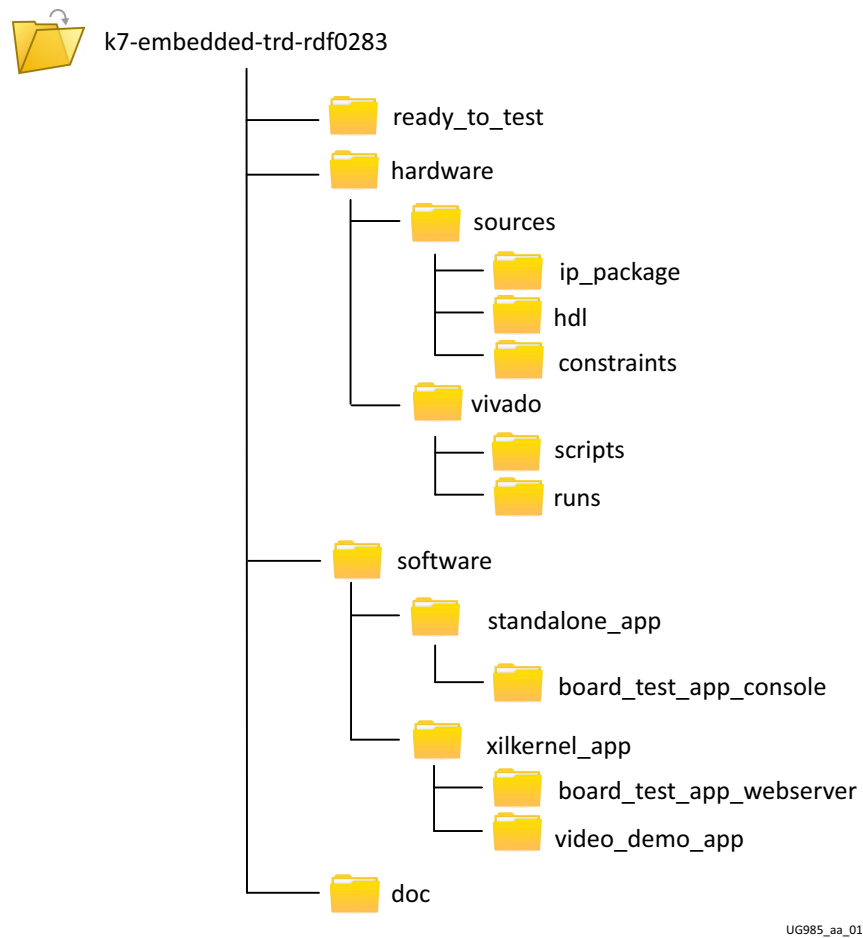

Figure 2-7: **Software Architecture for Video Demonstration Application (Server Software)**

Directory Structure

KC705 Embedded TRD Directory Structure

Figure A-1 shows the top-level directory structure of the KC705 embedded TRD.

Figure A-1: **KC705 Embedded TRD Directory Structure**

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Appendix B

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support

For continual updates, add the Answer Record to your my Alerts:

www.xilinx.com/support/myalerts

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and trouble shooting tips.

Further Resources

The most up to date information related to the KC705 board and its documentation is available on the following websites.

The Xilinx Kintex-7 FPGA Embedded Kit product page:

www.xilinx.com/kc705

The Kintex-7 FPGA Embedded Kit - Known Issues and Release Notes Master Answer Record AR# 52970

These documents provide supplemental material useful with this user guide:

- UG913, *Getting Started with the Kintex-7 FPGA KC705 Embedded Kit*
- UG081, *MicroBlaze Processor Reference Guide Embedded Development Kit*
- UG029, *ChipScope Pro Software and Cores User Guide*
- UG810, *KC705 Evaluation Board for the Kintex-7 FPGA User Guide*
- UG643, *OS and Libraries Document Collection*
- UG883, *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide (Vivado Design Suite)*
- UG893, *Vivado Design Suite User Guide: Using the Vivado IDE*
- *Kintex-7 FPGA Embedded Kit Targeted Reference Design Documentation Advisory*

- AMBA AXI4-Stream Protocol Specification:
  infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ihi0051a/index
- Xylon IP Cores Web page: www.logicbricks.com/Products/logiCVC-ML.aspx