XADC Layout Guidelines

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XAPP554 (v1.1) February 13, 2013

Summary

The Xilinx analog-to-digital converter (XADC) is a precision mixed signal measurement system. Like any other mixed signal/analog circuitry, the XADC performance can be impacted by a suboptimum printed circuit board (PCB) layout. This application note describes in detail a number of simple layout guidelines to help a board designer achieve the best possible performance from the XADC.
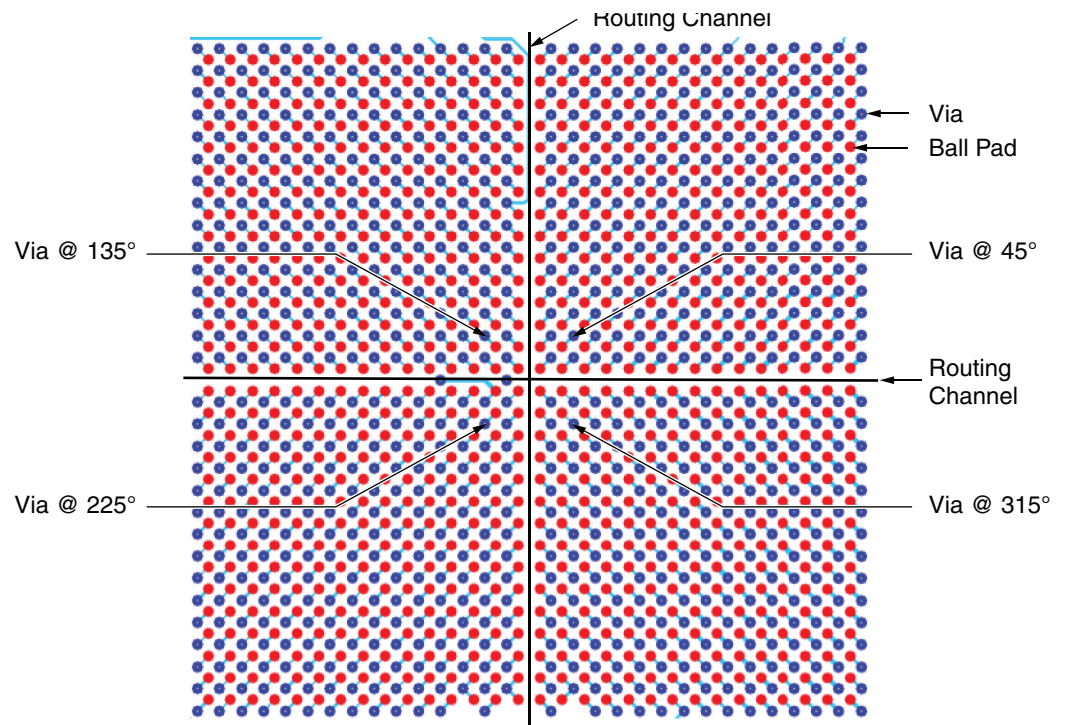
Introduction

This application note illustrates XADC PCB layout guidelines as they have been implemented on the Kintex™-7 FPGA KC705 evaluation kit [Ref 1]. This board reflects the typical complexity of a practical FPGA-based system with a lot of potential aggressor noise sources that can impact the XADC performance. Even in this environment, the highest level of performance can be achieved from the XADC within the Kintex-7 device XC7K325T. This XADC performance can be measured using the Agile Mixed Signal (AMS) evaluation platform that is bundled with the KC705 Evaluation Kit. Appendix, page 12 shows a number of performance measurements taken using the evaluation kit.

Signals required for the XADC are grouped into three categories that are dealt with separately in this document:

- Analog Inputs, page 3
- External XADC Reference Voltage, page 6
- Power Supply and Ground, page 9

High-Level Layout Guidelines

Routing critical signals to the center pins of a ball grid array (BGA) package can be extremely challenging due to the pad and via density associated with the balls of the BGA and the large number of signals. By breaking the BGA into four quadrants, and by staggering the vias as shown in Figure 1, wide channels can be made available for routing differential signals on inner and bottom layers of the PCB.

Figure 1: **BGA Staggered Pads**

The wide routing channels can be of significant benefit for routing differential signals, such as differential clocks or the XADC reference, or for widening supply and ground traces to minimize their impedance back to their source. For example, in the KC705 layout four parallel XADC traces could be routed in this routing channel. This would be done using two 4 mil traces (XADC reference lines V_{RefN} and V_{RefP}) and two 8 mil traces (XADC power (V_{CCADC}) and ground (GNDADC)) with 7 mil spacings. The routing channels also allow for the reference and supply decoupling capacitors in the center of the array on the bottom of the board. This technique is taken advantage of extensively later in this application note and on the KC705 board layout itself.

Putting thought into component placement before starting the layout design process can be extremely valuable. Such planning can significantly reduce the number of layout iterations, and can help make the appropriate trade-offs early in the design phase. Figure 2 shows high-level placement of the critical components on the KC705 evaluation board.

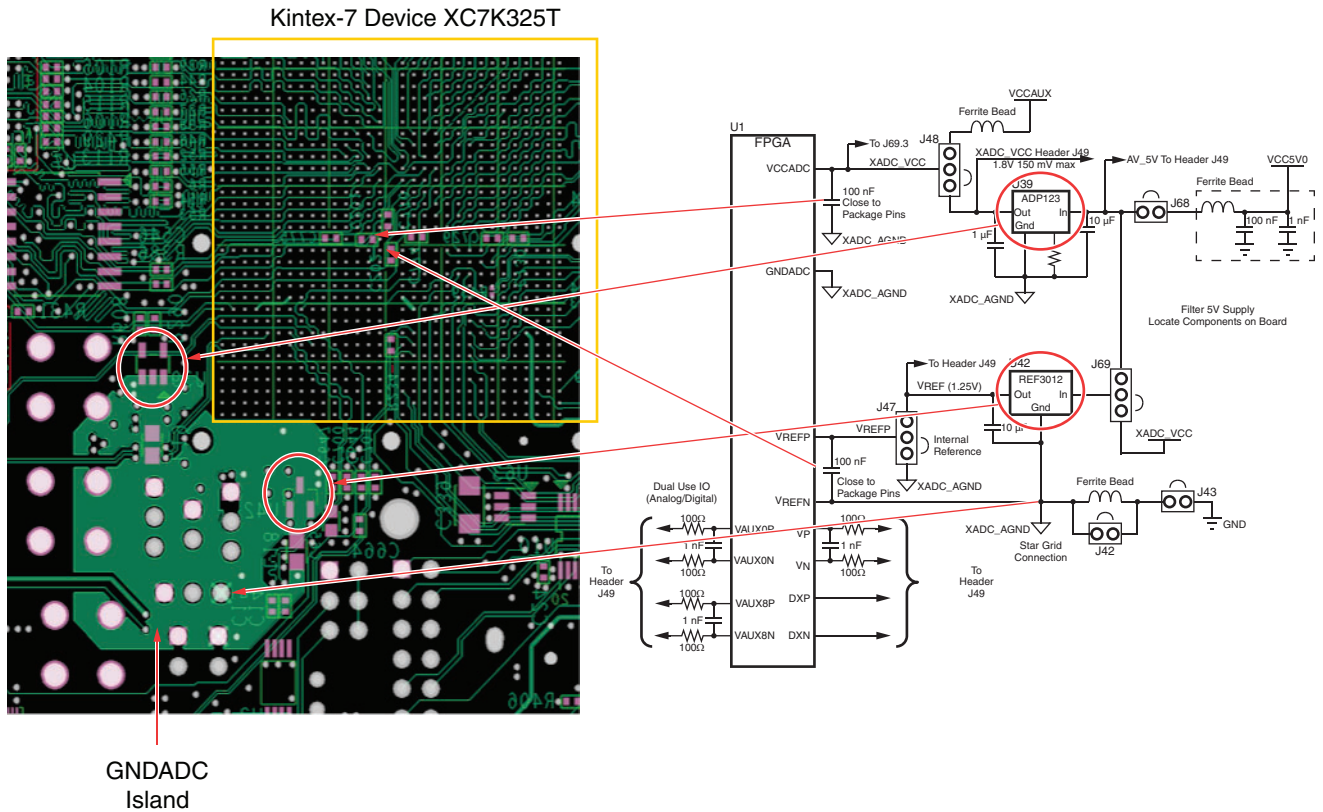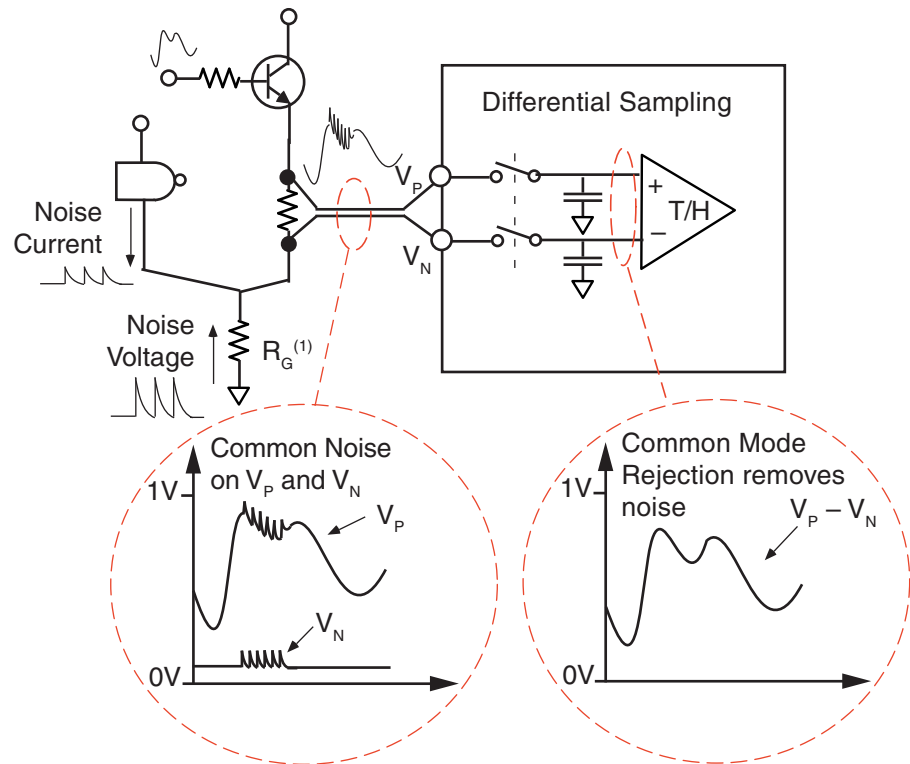Kintex-7 Device XC7K325T

GNDADC
Island

X554_02_020113

Figure 2: **High-Level Placement of Critical Components on the KC705 Evaluation Board**

Subsequent sections of this application note provide more detailed direction for routing and component placement for each of the three signal types mentioned in Introduction, page 1.

Analog Inputs

In many cases, the analog signals that the XADC is digitizing are coming from some distance away and might be driven by relatively high impedance, such as a resistive divider. In such an environment, there is a significant risk that the analog inputs pick up unwanted interference or noise from adjacent digital signals or clock sources. Anti-alias filters can help reduce the impact of this noise (see Anti-Aliasing Filter, page 5). However, some noise can make its way to the ADC inputs and impact measurement accuracy. Therefore every effort should be made to minimize the pick-up and impact of such interferences.

The XADC has the added benefit that each of its 17 analog inputs is differential. Each channel has both an N and a P input. The XADC digitizes the voltage difference between the P and N inputs for a given channel. This XADC feature ensures excellent common-mode noise rejection, because any signal common to both inputs is removed by the conversion process. This sampling and rejection is illustrated in Figure 3.

Note 1: R_G is Common Ground Impedance.

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Figure 3: **Differential Sampling and Common-Mode Rejection**

A complete cancellation only occurs when the signals on the P and N input have the exact same magnitude, phase, and frequency. In reality, without careful consideration, exact matching is very difficult to achieve, especially at high frequencies.

Routing

Due to the differential sampling technique, channel input pairs (the P and N input signals) should be routed as close as possible to one another (minimum spacing). On the KC705 layout, 5 mil (127 micron) traces were placed at a spacing of 6 mils (150 microns) wherever possible. This helps ensure that any interference, specifically EMI, that is picked up on one line is also picked up on the other line with the same magnitude and phase. The loop area is also reduced, which should help minimize the susceptibility of the input pair circuitry to picking up EMI. The high common-mode rejection of the differential sampling can be leveraged to remove these unwanted signals. These lines do not need to have matched impedance. They only need to be routed as close to one another as possible.

Interference due to electrical coupling between an active net (an aggressor), both analog and digital, and the analog inputs must be avoided by adding a shield or by separating nets. The mechanism for this interference is likely to be parasitic capacitance. It is likely that this parasitic capacitance between the analog inputs and the aggressor are very different, causing the magnitude and phase of the interference to be different on each of the inputs. In this case, the differential sampling becomes less valuable. Interference from an analog aggressor, such as a neighboring channel, is possibly even more problematic because the interference is normally in the bandwidth of interest. Thus, the anti-aliasing filter does not minimize the interference as it might for a high-frequency digital signal.

Shielding the analog inputs both horizontally and vertically also has a positive impact on the coupling to the critical analog input nets. Given the digitally intensive environment that FPGAs are normally in, shielding vertically (metal shields on PCB layers above and below critical

analog signals) is absolutely necessary because it provides a significant barrier to various aggressors that can be present in a system that uses an FPGA. Shielding horizontally (shield on the same PCB layer) is only necessary if the layout is significantly dense that aggressor signals are routed close to the analog inputs or if the source impedance is large (for example, where a resistor divider is being used). On the KC705 evaluation board, the analog input traces are routed on the bottom of the board. Because there are few traces on this layer, it was easy to route the analog inputs far enough away that horizontal shielding was not necessary. It was also assumed that a low impedance source (operational amplifier) would be driving the XADC. A minimum distance of 30 mil (762 microns) was used between pairs of analog inputs on the KC705 board layout. This was probably too aggressive, and a safer distance between pairs would be 100 mil (2540 microns). If the source is a resistor divider, shielding of the analog input pairs from other analog input pairs is recommended.The analog inputs are shielded vertically by a solid ground plane. Figure 4 shows one of the analog input traces being routed from the XADC header to the anti-aliasing capacitors.
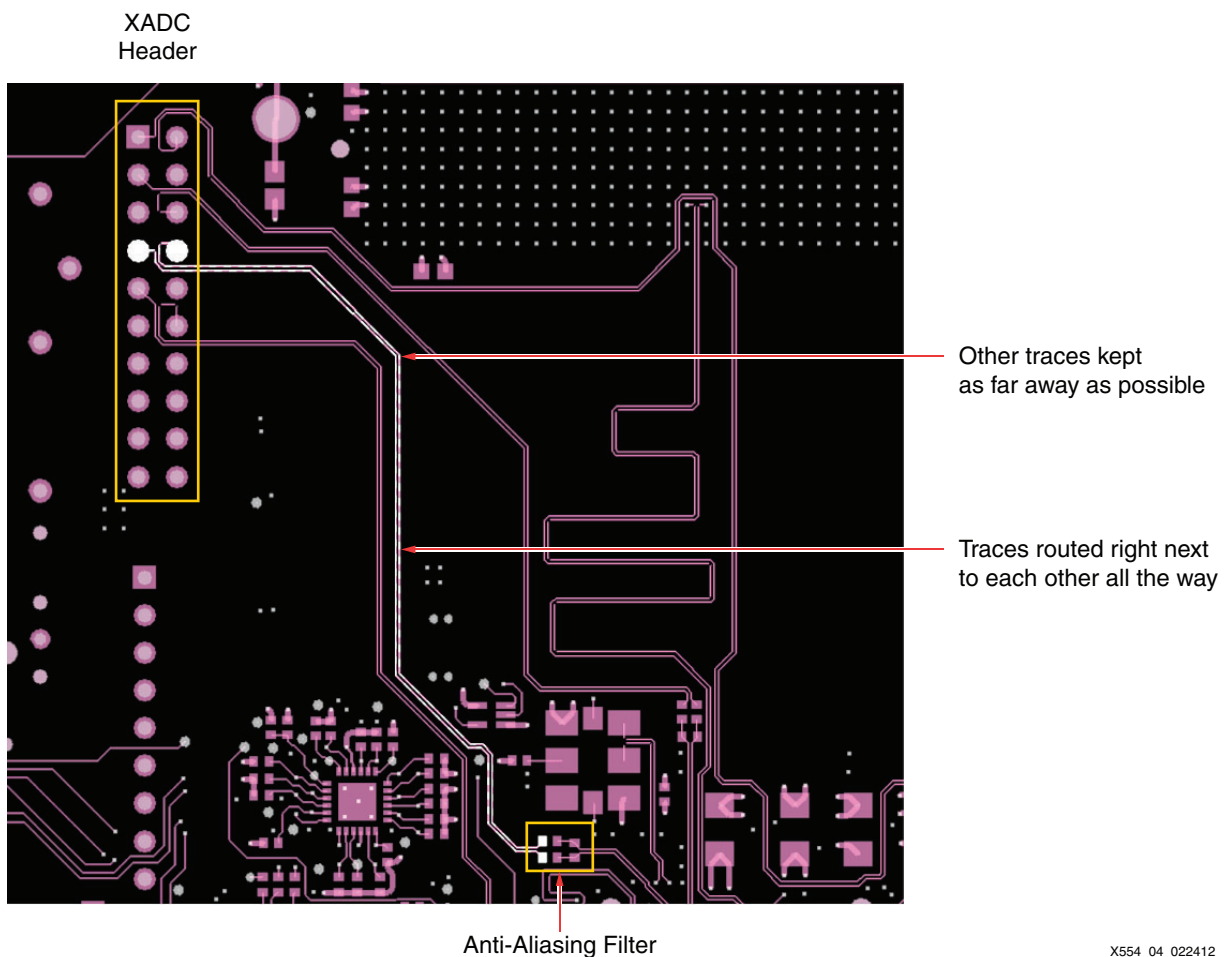

XADC
Header

Other traces kept
as far away as possible

Traces routed right next
to each other all the way

Anti-Aliasing Filter

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Figure 4: **Analog Input Routing**

In summary, it is best to route the P and N nets close together. The P and N nets should be kept well away from any possible aggressor and use shielding if and where possible.

Anti-Aliasing Filter

Although the techniques previously discussed describe how to minimize the interference picked up along the way, it is inevitable that some high-frequency interference that might not be common to both signals is picked up. These unwanted signals or interferences due to the sampling process of the ADC can alias back into the bandwidth of interest and thus impact the

performance of the system.To avoid these interferences impacting the performance of the XADC, an anti-aliasing filter (AAF, a simple RC filter) should be placed as close as possible to the XADC analog inputs. No more than 400 mil or 10 mm is a good rule of thumb for how far the AAF should be from the edge of the package. If the RC filter is not placed close enough to the device, more interference could be picked up after the AAF. This interference cannot be removed and is seen at the output of the XADC. Figure 5 shows the layout for the AAF on the KC705 board. The figure shows how the AAFs for AUX0, AUX8, and VP/VN have been placed adjacent to the device itself.
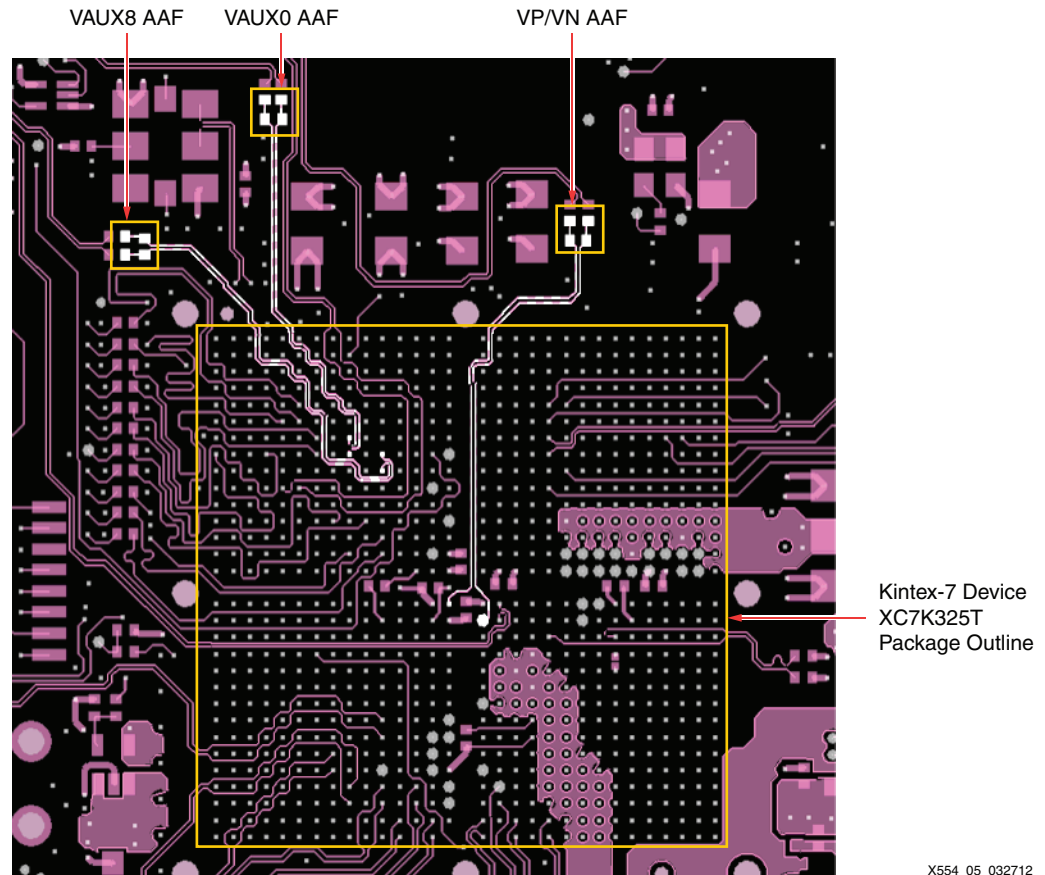

VAUX8 AAF   VAUX0 AAF   VP/VN AAF

Kintex-7 Device
XC7K325T
Package Outline

X554_05_032712

Figure 5:   **Anti-Aliasing Filter Locations on the KC705 Board**

The selection of the type of capacitor used as part of the AAF is very important, especially if T_{HD} is a concern. It is recommended, where possible, to use a capacitor with a negative-positive zero (NP0) or COG[1] dielectric. If that type of dielectric is not available, a capacitor with an X7R dielectric will suffice.
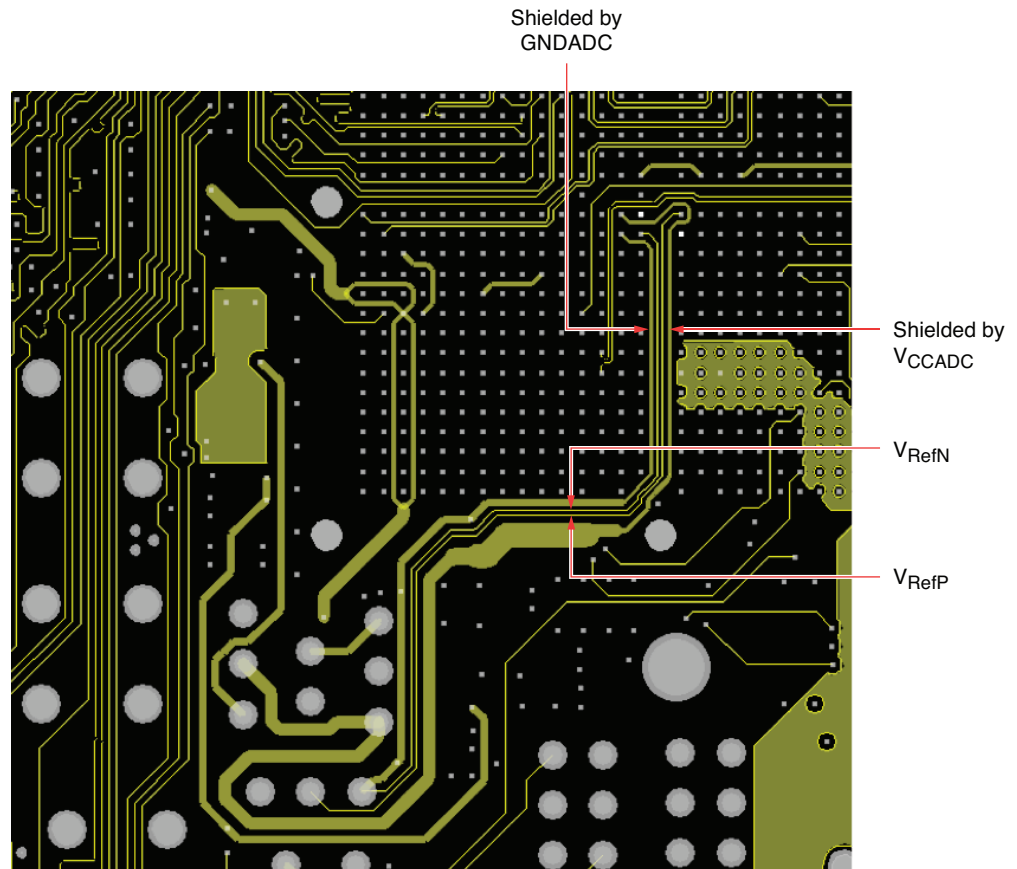
External XADC Reference Voltage

As with any ADC, the XADC is only as good as the reference voltage it is provided. For this reason, careful consideration is needed when laying out the reference circuitry. The XADC has two dedicated reference inputs, V_{RefP} and V_{RefN}. Similar to the analog inputs, the actual reference voltage that the XADC uses is the difference in voltage between these two nets. Recommendations for the specifications for the external reference can be found in *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* [Ref 2].

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1. Electronic Industries Alliance (EIA) three-character code for the material capacitance-temperature slope.

Routing

The V_{RefP} and V_{RefN} lines should be treated in a similar way to the analog inputs themselves. The two lines should be routed as close as possible to one another. (On the KC705 board layout, 5 mil (127 micron) traces were placed 6 mils or 150 microns apart wherever possible.) They should be shielded vertically and horizontally by a low-impedance quiet ground or quiet supply, such as GNDADC or V_{CCADC}. Shielding is more important for the reference because there is no AAF on the reference to limit any high-frequency noise. The 0.1 μF decoupling capacitor helps with filtering the noise, but only at very high frequencies. The channels that are made available by staggering the vias should be used to ensure that the reference can be shielded all the way to the decoupling capacitor without weaving through any vias. Figure 6 shows how this was achieved on the KC705 evaluation board.
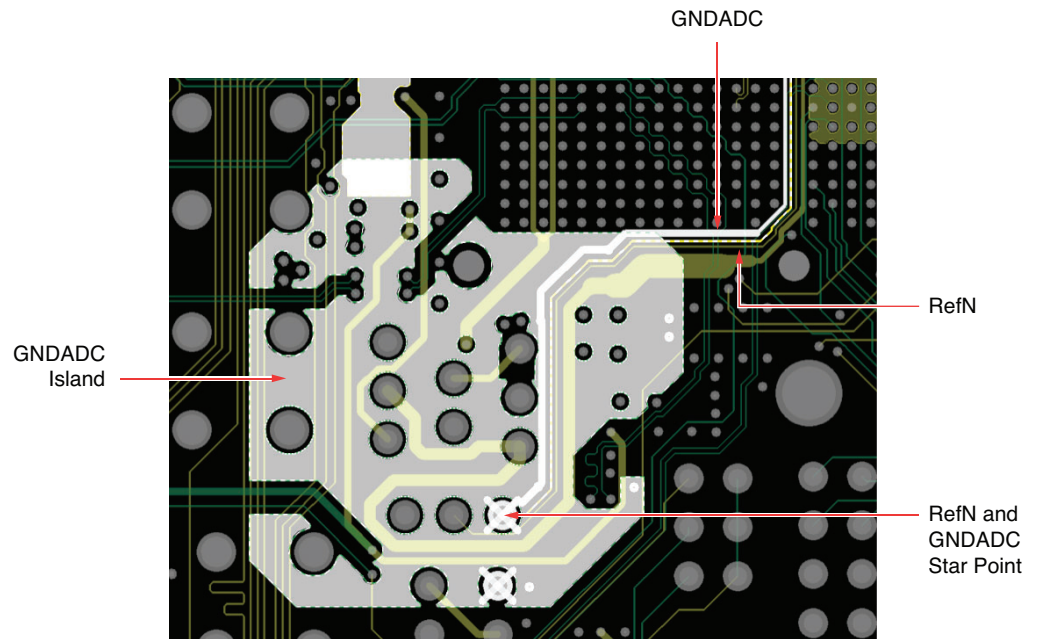

Figure 6: **Reference Shielding on the KC705 Evaluation Board**

The V_{RefN} net should be star-connected to the ground reference of the reference IC (REF3012) or as close to it as possible. The reference IC develops a constant 1.25V between its output and its ground reference pin. When the ground reference moves so does the output of the reference, and thus V_{RefP} moves. If the V_{RefN} moves along with the reference output, the actual XADC reference voltage does not move because it looks at the difference between V_{RefP} and V_{RefN}. The reference then seen by the XADC should not move due to noise on the ground. By sensing the ground reference of the reference IC with V_{RefN}, the ground reference and the XADC move together.

The reference ground and V_{RefN} net are tied to a GNDADC island on the KC705 evaluation board, as shown in Figure 7.
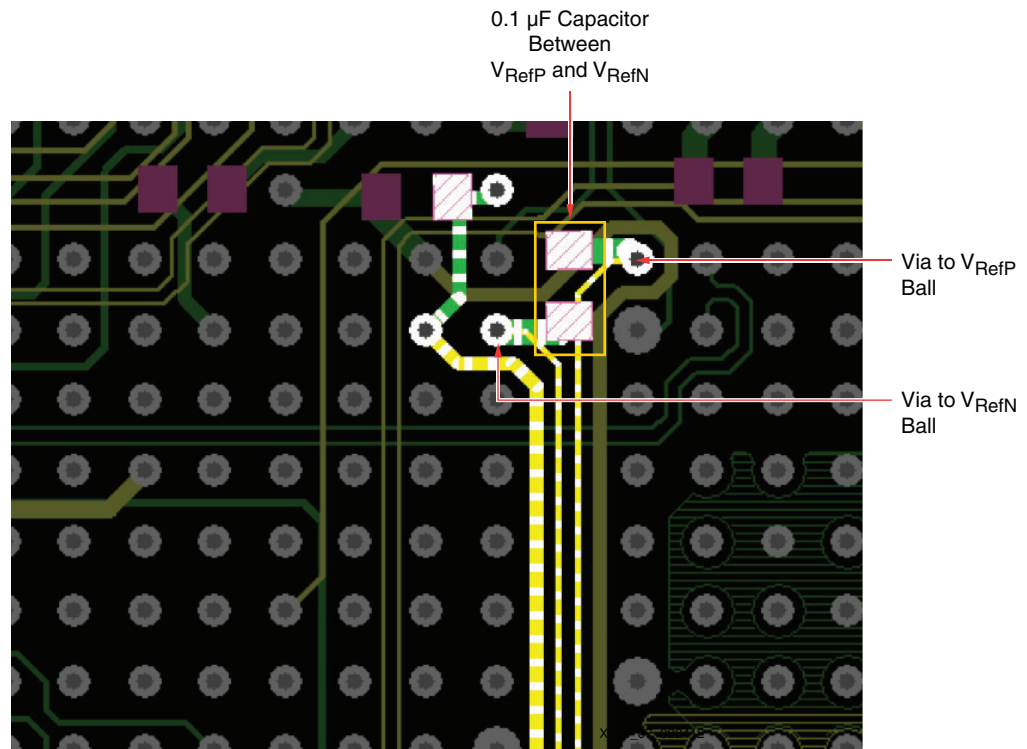
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Figure 7: **RefN Star Connection to GNDADC**

Because these reference lines do not carry any current, they can be relatively thin traces, especially those reference lines on the source side of the decoupling capacitor. The traces on the KC705 board were 5 mil (127 microns) wide.

Decoupling

The main purpose of the decoupling capacitor is to provide a charge reservoir that has as little impedance as possible between the decoupling capacitor and the V_{RefP} and V_{RefN} package balls themselves. Having a small impedance ensures that the reference line does not show a significant change in voltage due to switching activity within the XADC. The recommended circuit diagram for the XADC is to have two decoupling capacitors, a large capacitor of 10 µF, and a smaller capacitor of 0.1 µF. The smaller 0.1 µF capacitor should go on the underside of the board as close as possible to the vias associated with the V_{RefN} and V_{RefP} balls. This placement ensures that the inductance between the ball and the decoupling capacitor is not too large. An inductance of 2 nH is acceptable. Figure 8 shows the 100 nF decoupling capacitor location on the KC705 board.

0.1 µF Capacitor
Between
V_{RefP} and V_{RefN}

Via to V_{RefP}
Ball

Via to V_{RefN}
Ball

X554_08_022412

Figure 8: **Reference Decoupling on the KC705 Board**

Power Supply and Ground

The XADC runs from a 1.8V supply, V_{CCADC}, and requires a maximum current of 25 mA. For optimum XADC noise performance, it is best to keep the supply voltage and associated ground, GNDADC, as quiet as possible. *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide* [Ref 3] presents two options for powering the XADC:

• The first option is to power V_{CCADC} with V_{CCAUX} and use a ferrite bead in series to provide isolation from high-frequency noise on the V_{CCAUX} supply. This option is only recommended for use in basic monitoring applications.

• The second option is to use an additional linear regulator such as the ADP123 to provide the 1.8V V_{CCADC} supply. This option is needed if the full performance of the XADC is required.

The ground connection for the XADC (GNDADC) should be connected to the digital or system ground through a ferrite bead. Use of the ferrite bead enables a path for the DC currents back to ground and also provides isolation from any high-frequency noise present on the ground.

The XADC requires a 100 nF decoupling capacitor to reduce the magnitude of transients due to internal switching within the XADC.

Routing

Maintaining the lowest impedance possible on the power supply and ground lines for the XADC is very important, especially between the ball and the decoupling capacitor. If impedance, especially inductance, is too large, large transients might occur on the supply as charge is being pulled from its source due to switching in the XADC block itself. These transients can get into the core signal channel of the XADC inadvertently, impacting the performance of the XADC.

The ideal layout would have a GNDADC and a V_{CCADC} island that extends as close as possible to the corresponding decoupling capacitor and associated FPGA pins and balls. If constraints

allow, the layout could have a complete analog ground and power planes. Where this layout is not possible, GNDADC and a V_{CCADC} should be routed using traces that are as wide as possible from the island to the FPGA pins and the decoupling capacitors. All the additional external analog circuitry should be placed within and reference this ground island. This component placement is shown in Figure 2, page 3.

For the KC705 board layout, there is a GNDADC island that extends to the edge of the Kintex-7 device package. The channel created by staggering the vias associated with the BGA balls brings as wide a trace as possible to the BGA ball for GNDADC. The KC705 board layout uses an 8 mil (203.2 micron) trace width. This trace also serves as a shield for the reference, as shown in Figure 9.
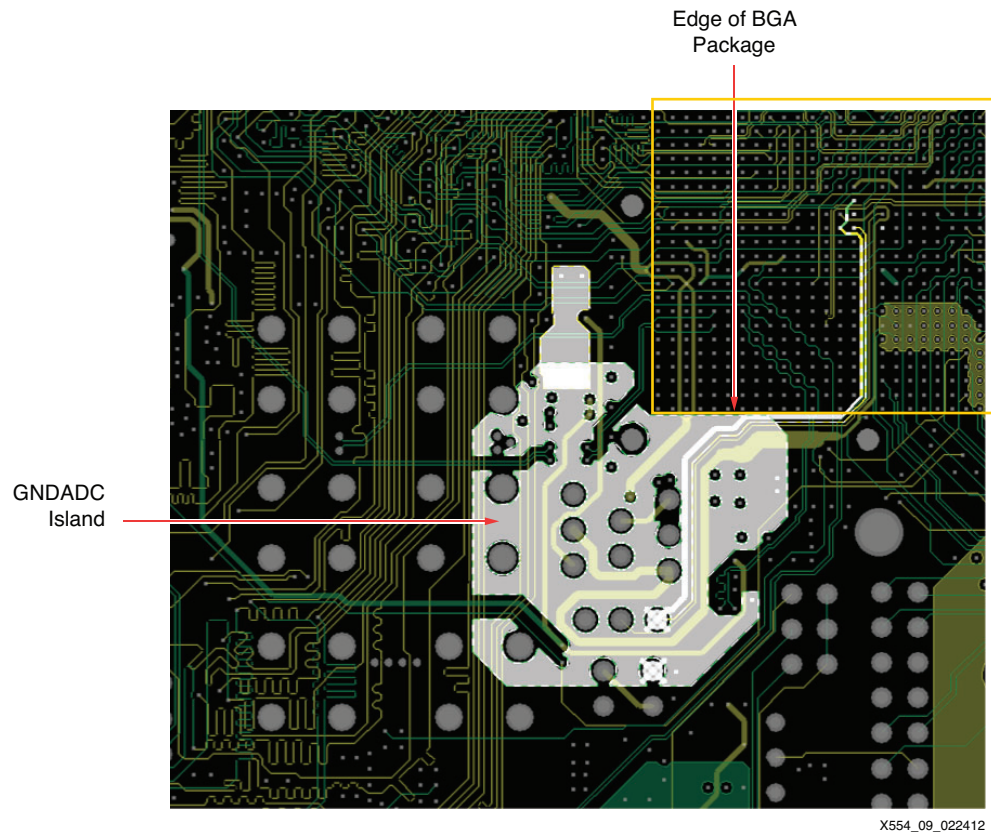

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Figure 9: **GNDADC Island and Trace to Ball**

It was not possible to have a V_{CCADC} island, so as wide a trace as possible was routed from the source to the decoupling capacitor and BGA ball, again using the channel created by staggering the vias. The trace width on the KC705 board layout was 8 mil (203.2 micron) in the routing channels under the FPGA and 25 mil (635 micron) outside. The V_{CCADC} net was also used as a shield for the reference nets. The routing of V_{CCADC} is shown in Figure 10.
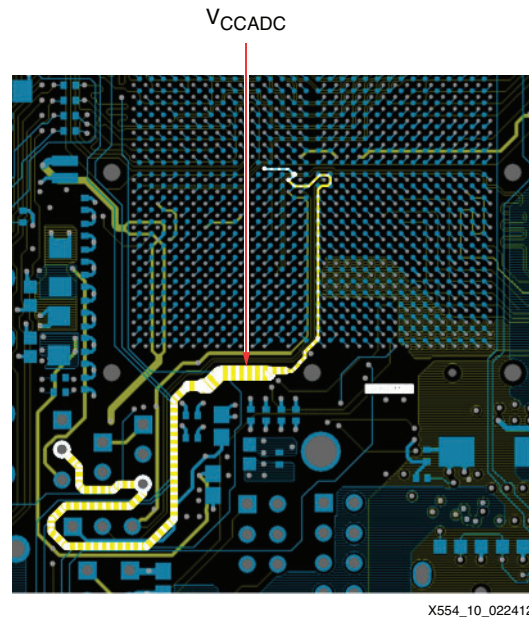
V_{CCADC}

X554_10_022412

Figure 10: **V_{CCADC} Routing**

Decoupling

Given that the XADC power and ground pins are typically in the center of the BGA, the decoupling capacitors should be placed on the underside of the board as close as possible to the point directly under the via's associated ball. Two vias should be placed between the balls and the underside of the board connected where possible with top-level metal to minimize the inductance between the FPGA balls and the decoupling capacitor. The inductance between the ball and the decoupling capacitor should be kept at or below 2 nH for optimum performance. A cross section of this via structure is shown in Figure 11.
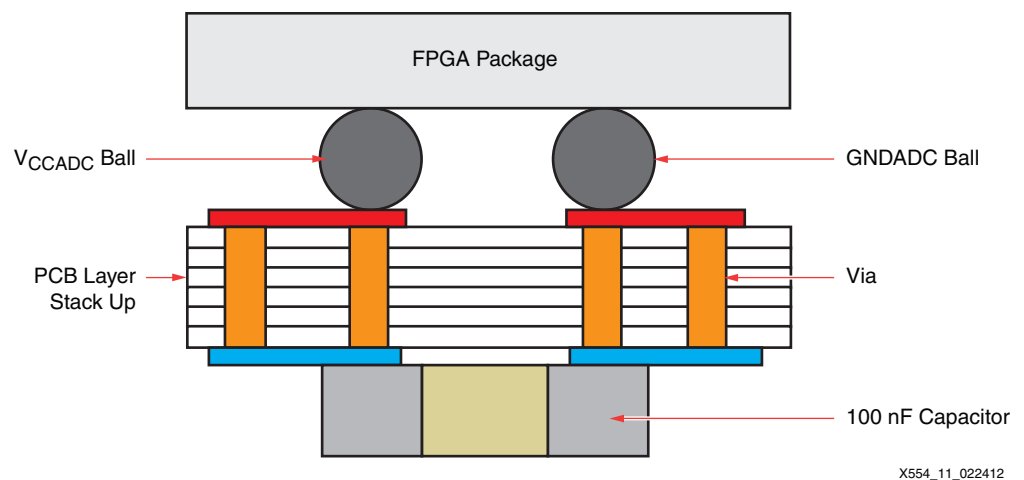

X554_11_022412

Figure 11: **Ideal Power Supply Decoupling Layout**

For the KC705 board layout, the two vias and the ball on the top layer of the board for the V_{CCADC} net could not be connected. Instead, a single via to the ball is connected to the next available signal layer where the two vias are shorted together with metal as wide as possible. A cross section of this layout is shown in Figure 12. This alternative is functionally as close as could be achieved to having two vias connected with top-level metal and provides negligible performance degradation. The Mentor Graphics HyperLynx and ANSYS SIwave tools were used to calculate the inductance from both the V_{CCADC} ball and the GNDADC ball as 1 nH and

2.2 nH, respectively. These numbers also correlate to hand calculations that were based on notes from Texas Instruments [Ref 4].
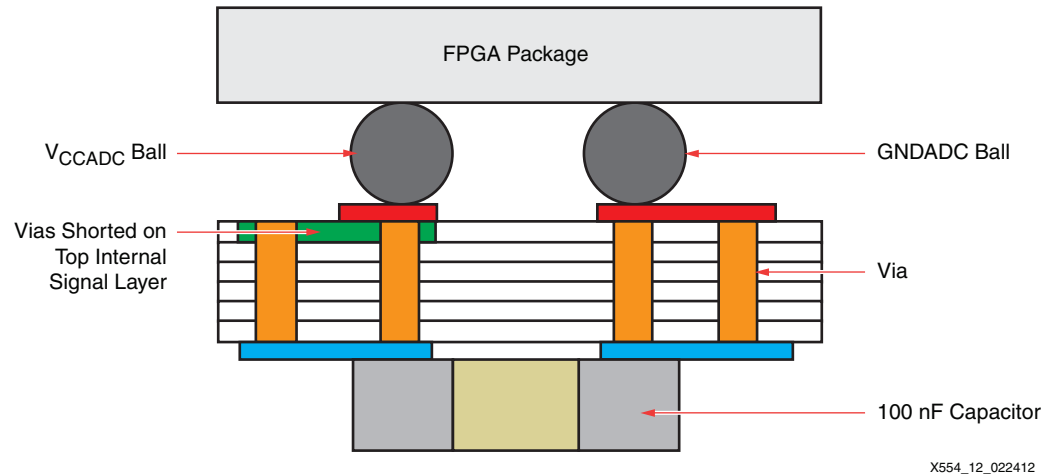

Figure 12:   **Power Supply Decoupling Layout for the KC705 Board**

Conclusion

This application note discusses guidelines to maximize the probability of achieving excellent XADC results on the first board iteration. The via associated with each BGA ball should first be staggered to maximize the routing space for differential signals and shields. Then:
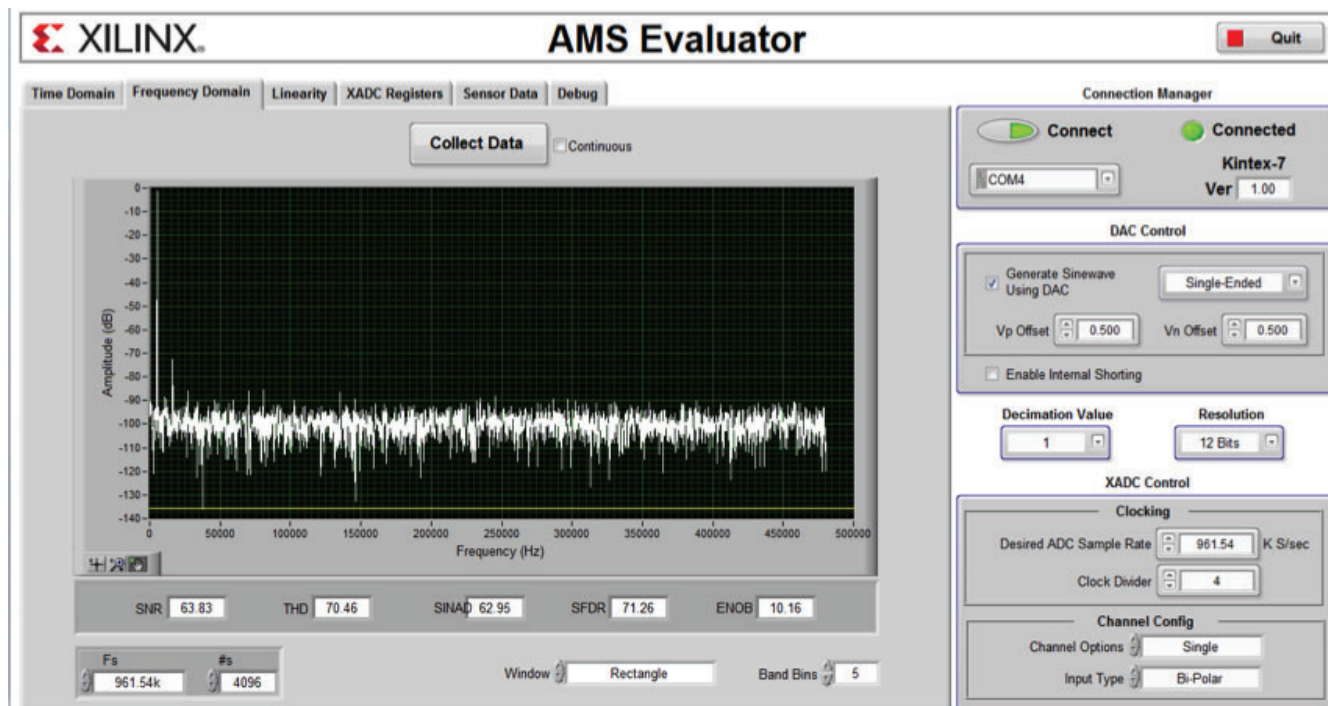
- The N and P lines should be routed together at the minimum PCB spacing where possible to maximize the benefits of differential sampling that the XADC offers.
- All decoupling and anti-aliasing capacitors should be placed as close as possible to the FPGA pins.
- The impedance on the power supply and ground lines should be minimized.
- Any common impedance between the RefN line and the GNDADC of the XADC should be minimized. Using a star connection is recommended.

To measure the expected performance of the XADC in the lab, the AMS evaluation platform provided in the KC705 evaluation kit can be used.

Appendix

XADC Performance on the KC705 Board

Figure 13 shows a fast Fourier transform of XADC data captured using the AMS evaluation card on a KC705 board. It shows a signal to noise ratio (SNR) of 63.8 dB for the KC705 board. The data sheet SNR specification for the XADC is 60 dB.

Figure 13: **Fourier Transform of XADC Data**

References

This application note uses the following references:

1. Kintex-7 FPGA KC705 Evaluation Kit
   http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm

2. DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics*

3. UG480, *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide*

4. Texas Instruments, *High Speed Analog Design and Application Seminar*
   http://www.ti.com/lit/ml/slyp169/slyp169.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
05/25/12	1.0	Initial Xilinx release.
02/13/13	1.1	Updated capacitances from mF to µF in Figure 2.

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