Measured Boot of Zynq UltraScale+ Devices

XAPP1342 (v1.0) April 18, 2019

Summary

The Zynq® UltraScale+™ devices secure boot functionality provides the capability to authenticate all partitions loaded at boot using RSA-4096 authentication. It also supports advanced encryption standard (AES) encryption of partitions that need confidentiality. The Zynq UltraScale+ devices provide a hardware root of trust (HROT) to protect against early load attacks.

Measured boot allows a remote client in a connected environment to measure its software and provide those measurements to a server. The term *measured boot* is used because the client returns a value, typically a secure hash algorithm (SHA2) digest, of each of the partitions loaded. In remote attestation, the server compares the measured logs with known good measurements. The server examines these measurements and provides remote attestation over the network that the remote client is running trusted software. This method uses a trusted platform module (TPM) to store the measurements and perform the cryptographic operations required to ensure that measured boot operates securely.

This application note combines the secure boot process of the Zynq UltraScale+ devices with measured boot to provide a secure solution where remote attestation measurements extend all the way down to the configuration security unit (CSU) ROM and first stage boot loader (FSBL). This solution offers security advantages over other measured boot solutions because the software performing the initial measurement is authenticated. The user is shown how to modify the FSBL to provide measurements of the CSU ROM, FSBL, and all subsequent partitions. RSA authentication from the Zynq UltraScale+ device's secure boot process authenticates the FSBL, ensuring that the FSBL has not been modified and is performing the measurements correctly.

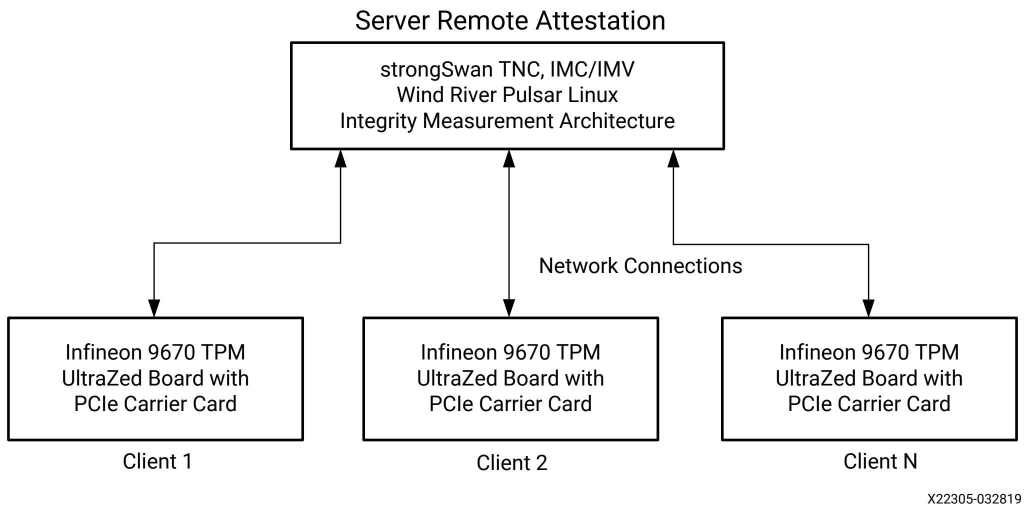
Download the reference design files for this application note from the Xilinx website. For detailed information about the design files, see Reference Design.

Introduction

Many applications require a method to add or change functionality over the life of the embedded system using field updates. However, field updates of software and firmware often leave a system vulnerable to attacks by anyone with network access.

Measured boot and network security are critical in firmware updates. The following figure shows an example system environment that uses measured boot. A server manages the software load, update, and validation of fielded, embedded systems based on the Zynq UltraScale+ devices. The embedded systems connect to the server over a network. In addition to updating software on the embedded systems, the server verifies that the correct, trusted software is loaded. This verification by the server, done at boot and run time, is called remote attestation.

Figure 1: **Measured Boot of Zynq UltraScale+ Device Embedded Systems**



Remote attestation capability has been in Linux starting with 2.6.3, and is generally known as integrity measurement architecture (IMA). The Linux extended verification module (EVM) is used with IMA. In remote attestation, the server compares the measured logs with known good measurements. The attestation server knows the characteristics (measurements) of the partitions loaded on the embedded systems. As each embedded system boots, it sends log files to the server containing partition measurements. The server verifies the measurement, and if a client loads software that is different than what is expected, the server executes a policy set up by the server administrator. A policy is a set of actions taken by the server based on measurement results.

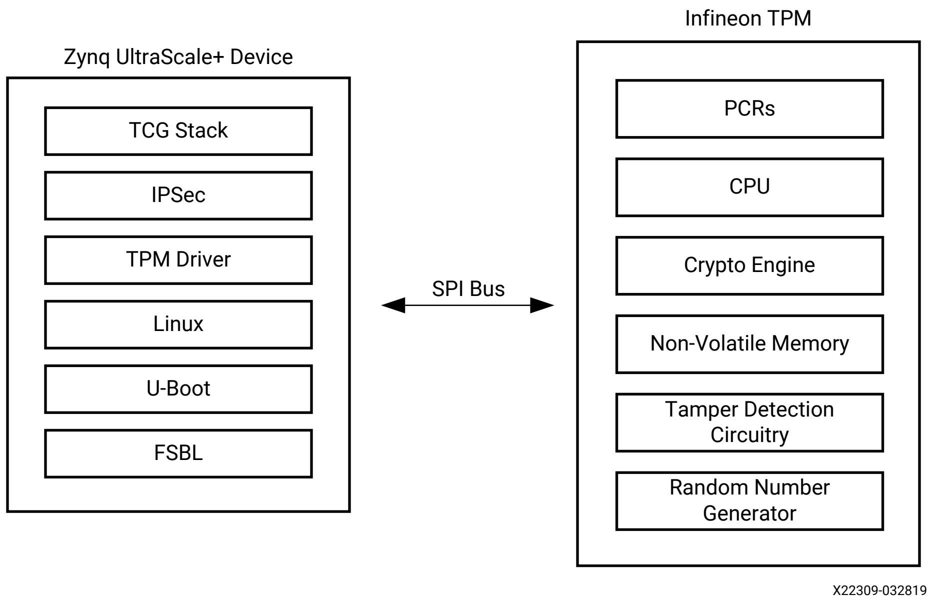
Examples of policies are keeping the embedded system off the network, updating the embedded system's software, re-running remote attestation, or disallowing access to network services. Isolating a corrupted embedded system from the network limits its ability to corrupt other embedded systems, perform incorrect operations, and cause other harm. This is a typical policy of a server in remote attestation, but not the only policy. Policy is generally defined by the application.

Measured boot is done in addition to, not in place of, secure boot. Measured boot by itself does not prevent malicious software from being loaded. The TPM enhances the HROT and increases the security of the software load/update process. The TPM provides cryptographic functions used in measure boot. The HROT is enhanced with the TPM because an adversary has to defeat both the Zynq UltraScale+ device secure boot and the tamper-resistant TPM for a successful attack. The TPM is placed on the same board as the Zynq UltraScale+ device.

The following figure shows functional components of a system that uses the Zynq UltraScale+ devices and the Infineon OPTIGA SLB 9670 TPM to create a client system that supports measured boot.

Note: This application note only demonstrates the FSBL changes required to communicate with the Infineon TPM, perform the measurements of the CSU ROM, FSBL, and other software partitions, and update the platform configuration registers (PCRs) with the measurements.

Figure 2: **Functional Diagram of Client Platform Based on the Zynq UltraScale+ Devices**



***Note*:** In the figure above, TCG is Trusted Computing Group.

At power-up, the Zynq UltraScale+ device CSU ROM code loads the FSBL. The FSBL loads U-Boot, and U-Boot loads the Linux kernel, root file system, device tree, and Linux application software. In one approach to booting with a chain of trust, the following steps occur:

1. The device hardware measures the BootROM.
2. The BootROM authenticates the FSBL.
3. The FSBL pushes the BootROM measurement to the TPM.
4. The authenticated FSBL measures itself.
5. The FSBL pushes all measurements made so far to the TPM.
6. The FSBL authenticates/measures U-Boot and the programmable logic (PL) using the TPM.
7. U-Boot authenticates/measures the Linux partitions using the TPM.

As per the TPM 2.0 specification, measurements are created by calculating a SHA2 hash of event data. Rather than treating the entire partition as the event data, which would require sending all of that data to the TPM, a SHA3 digest of the software image is used as the event data. An SHA3 digest of the partition is selected as the event data as that is readily available in the Zynq UltraScale+ architecture. The SHA3 digest is sent to the TPM, and the TPM creates an SHA2 measurement of that event data. The SHA2 measurement logs are stored in the TPM PCRs. Measurements of the BootROM and the FSBL are done by the FSBL and placed in the PCRs using a serial peripheral interface (SPI) connection. These measurements can be later transmitted to the server by the user application for remote attestation. The TPM cryptographically signs the SHA2 values in PCRs so that partition measurements are not transmitted from the embedded system in plain text.

For remote attestation of firmware updates, the network connection between the attestation server and clients must be secure. The firmware updates take place at the application level. IPSec functionality, including a privacy certificate authority (CA) that generates X.509 certificates, implements the transport layer security (TLS) handshake between the server and client(s).

The reference design does not demonstrate the IPSec and TLS handshaking application layer protocols because many diverse solutions exist. However, all solutions rely on the FSBL. The reference design shows how to modify the FSBL to use secure boot, extend that chain of trust up through the TPM measurements, and measure all of the partitions loaded by the FSBL. This reference design ends with the FSBL handoff. *Measured Boot of Zynq-7000 SoCs* (XAPP1309) demonstrates how this process can be continued from U-Boot onward. It uses strongSwan and TrouSerS as part of a TPM 1.2 solution.

Hardware and Software Requirements

The hardware and software requirements for the reference system include the following:

- Avnet UltraZed PCIe® Carrier Card
- Avnet UltraZed-EG System-on-Module (SOM)
- Infineon OPTIGA TPM 2.0 SLB 9670 peripheral module (Pmod)
- One micro USB cable (for UART communications)
- Micro Secure Digital (microSD) memory card (1 GB or greater and less than 64 GB)
- TeraTerm or equivalent communication software
- Xilinx Vivado® Design Suite 2018.3
- Xilinx Software Development Kit (SDK) 2018.3

Reference Design

Download the reference design files for this application note from the Xilinx website.

Reference Design Matrix

The following checklist indicates the procedures used for the provided reference design.

Table 1: **Reference Design Matrix**

Parameter	Description
General	
Developer name	Xilinx
Target devices	Zynq UltraScale+ devices
Source code provided?	Yes
Source code format (if provided)	C
Design uses code or IP from existing reference design, application note, third party or Vivado software? If yes, list.	Yes, Xilinx FSBL

Table 1: **Reference Design Matrix** *(cont'd)*

Parameter	Description
Simulation	
Functional simulation performed	N/A
Timing simulation performed?	N/A
Test bench provided for functional and timing simulation?	N/A
Test bench format	N/A
Simulator software and version	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/versions used	Vivado synthesis
Implementation software tool(s) and version	Vivado implementation
Static timing analysis performed?	N/A
Hardware Verification	
Hardware verified?	Yes
Platform used for verification	Avnet UltraZed-EG SOM with PCIe carrier card and Infineon OPTIGA SLB 9670 TPM

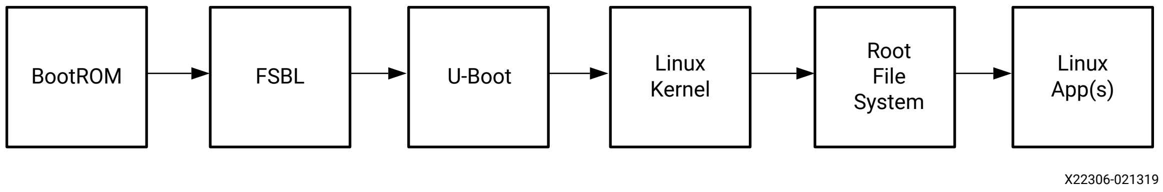
Hardware Root of Trust

In Zynq UltraScale+ devices, the HROT is based on the first code executed by the CSU at power-on. The code is stored in on-chip, metal-masked ROM and is referred to as CSU BootROM. The CSU BootROM code is immutable, and its principal function is to perform device initialization and load the FSBL into on-chip memory (OCM). Neither the CSU BootROM nor the OCM are directly accessible from device pins when secure boot mode is used. (In non-secure boot modes, the OCM is accessible from JTAG.) Refer to the Boot and Configuration chapter in *Zynq UltraScale+ Device Technical Reference Manual* (UG1085). If secure boot is specified, the BootROM authenticates the FSBL using the RSA-4096 standard prior to execution of the FSBL. The Zynq UltraScale+ device HROT is enhanced by adding a TPM to the embedded platform. The TPM provides partition measurements, cryptographic functions, and secure key storage for keys used by the Zynq UltraScale+ devices.

In Zynq UltraScale+ devices, during *secure boot* the PL bitstream can also be authenticated prior to being loaded into on-chip configuration memory. Software partitions stored in non-volatile memory (NVM) are also generally authenticated and copied to DDR memory. These partitions can also be optionally encrypted in addition to being authenticated.

As shown in the following figure, the RSA-4096 authentication uses a chain of trust sequentially on each partition loaded. Each partition can use its own private/public key pair. In its simplest form, all partitions loaded by the FSBL are authenticated using RSA-4096. In an alternative boot flow, U-Boot can also authenticate software that it loads. In secure boot, if RSA authentication fails, the Zynq UltraScale+ device searches the NVM for the next valid boot image. When no valid boot images are found, the Zynq UltraScale+ device transitions to a secure lockdown state. A malicious actor would need access to the RSA private key to load their own data onto the device. This RSA private key is not stored in the device. It resides at the customer's secure facility.

Figure 3: **Zynq UltraScale+ Device Chain of Trust Boot**



Measured Boot

Measured boot is recommended when embedded systems are connected to a network. Connecting embedded systems to a network provides a method for firmware and application updates. Yet, embedded systems connected to a network have a wider attack surface than closed systems, and hackers with network access are a common security threat. Remote attestation addresses this vulnerability during boot and run time. In secure and measured boot, all files/partitions are authenticated and measured. Secure boot should still be used in systems using measured boot because secure boot and measured boot are complementary.

The measured boot in the reference design uses a TPM for added security. Secure boot and measured boot do not use PL resources, so the Zynq UltraScale+ device unit cost is not affected when measured boot is used. For each image measured, an SHA3 digest is calculated over the image contents. This SHA3 digest is then sent to the TPM as a PCR event. The TPM uses the SHA2 to log the event into the PCR register. The PCR register maintains a history of all the events that have happened against that PCR. Only a PCR that has received the appropriate events will have the correct SHA2 digest. The remote attestation server can request the PCR digests from the client. The TPM uses RSA signatures in its responses so that the attestation server knows that these responses are coming from the client in question. Using measurements, an attestation server can periodically execute run-time integrity checks on clients and execute a policy based on the results.

Measurements Performed by the Modified FSBL

The CSU ROM measurement is based on the SHA3 digest created by the CSU during boot. It is stored in registers. The FSBL sends this SHA3 digest to the TPM as a PCR event.

The FSBL measurement is performed by the FSBL (only an authenticated FSBL can be loaded) after it has already started executing. The OCM address range over which to calculate the SHA3 digest is taken from the boot image's partition header table. Because the FSBL is already executing, some of the data structures in this memory range will have been modified. One of these data structures is the partition header table. The FSBL measurement is therefore also measuring the partition header table, and the measurement will be different if the partition header is altered. Thus, the FSBL measurement is actually a measurement of both the FSBL and the partition header table. The SHA3 digest of the OCM memory range specified is sent to the TPM as a PCR event.

All non-PL partitions are measured from the memory location into which the partition header table specifies them to be loaded. The measurement happens after authentication and decryption if either of those operations were specified in the partition header table. The SHA3 digest of the memory range specified is sent to the TPM as a PCR event.

Measurements of PL images are dependent on whether the PL image has been authenticated and/or encrypted. Authenticated PL images reuse the SHA3 digest from the authentication process and send that SHA3 digest to the TPM as a PCR event. Unauthenticated images calculate an SHA3 digest of data as it is sent to the PCAP port over the secure stream switch. This SHA3 digest is then sent to the TPM as a PCR event.

FSBL Changes to Support Measured Boot

By default the Xilinx FSBL does not support measured boot or communication with a TPM. This reference design demonstrates additional software and modifications to the FSBL that enable TPM measurements.

The source code for the modified FSBL includes a TPM directory. This TPM directory contains a small driver that allows the Zynq UltraScale+ device to communicate with the Infineon OPTIGA 2.0 SLB 9670 TPM. This driver is provided as a reference and is not discussed in additional detail.

Additionally, six new files are added to the FSBL. These files are as follows:

- `Fsbl_measured_boot.c`: Includes subroutines to startup/test the TPM and perform measurements on the CSU ROM, FSBL and all non-PL partitions.
- `Fsbl_measured_boot.h`: Include file for `fsbl_measured_boot.c`.
- `Fsbl_measured_pl.c`: Includes subroutines to measure the PL partitions.
- `Fsbl_measured_pl.h`: Include file for `fsbl_measured_pl.h`.
- `Fsbl_measured_utils.c`: Includes lower level subroutines required to perform measurements such as Tpm_ReadPcr, Tpm_Event, and SHA3 subroutines.
- `Fsbl_measured_utils.h`: Include file for `fsbl_measured_utils.h`.

The `fsbl_measured_boot.c` file contains a data structure that defines to which PCRs the various measurements for each partition should go. The reference design supports up to 32 partitions and up to 24 PCRs. A partition is not measured if the PCR number specified in the data structure is greater than 24. The data structure also specifies to which PCR the CSU ROM measurement and the FSBL measurement should go. The structure definition used below is arbitrary. An application can modify the data structure to suit whichever PCR definitions are required. The data structure used is as follows.

```
typedef struct {
    uint32_t ROM_PCR;
    uint32_t FSBL_PCR;
    uint32_t PARTITION_PCR[32];
} t_Partition_PCR_Map;

const t_Partition_PCR_Map Partition_PCR_Map = {
        0,            // ROM should be extended into PCR0
        4,            // FSBL should be extended into PCR4
        {   6,   7, 255, 255,   // Extend to PCR #6 and #7
          255, 255, 255, 255,   // All others aren't measured
          255, 255, 255, 255,
          255, 255, 255, 255,
          255, 255, 255, 255,
          255, 255, 255, 255,
          255, 255, 255, 255,
          255, 255, 255, 255
        }
};
```

Based on this definition, the following PCR measurements occur:

1. The CSU ROM measurement goes to PCR 0.
2. The FSBL measurement goes to PCR 4.
3. The partition 1 measurement, the PL bitstream in this example, goes to PCR 6.
4. The partition 2 measurement, hello_world in this example, goes to PCR 7.
5. This reference design does not have additional partitions so all other partitions are specified as not measured by using any number greater than 24 (for example, 255).

Changes in the Xilinx FSBL code can be found by searching for MEASURED BOOT in the comments or by searching for the macro SUPPORT_TPM_SLB9670. The following list shows the modified files and what was changed in them:

- `Xfsbl_config.h`: The SUPPORT_TPM_SLB9670 macro is defined. Detailed debug is used so the SHA3 digests and PCR events can be observed.
- `Xfsbl_initialization.c`: A global variable, Iv, is renamed to Global_FsblIv to prevent collisions with a global variable in the xilsecure library. The TPM initialization, startup, selftest, and CSU ROM measurement are all added early in the initialization process. The FSBL measurement is added after the partition header table has been loaded.
- `Xfsbl_partition_load.c`: The global variable, Iv, is renamed to Global_FsblIv again. Calls to measure all non-PL partitions and to measure all unauthenticated PL partitions are inserted here. The partition number is added to the PL parameter structure for use in measuring authenticated partitions.

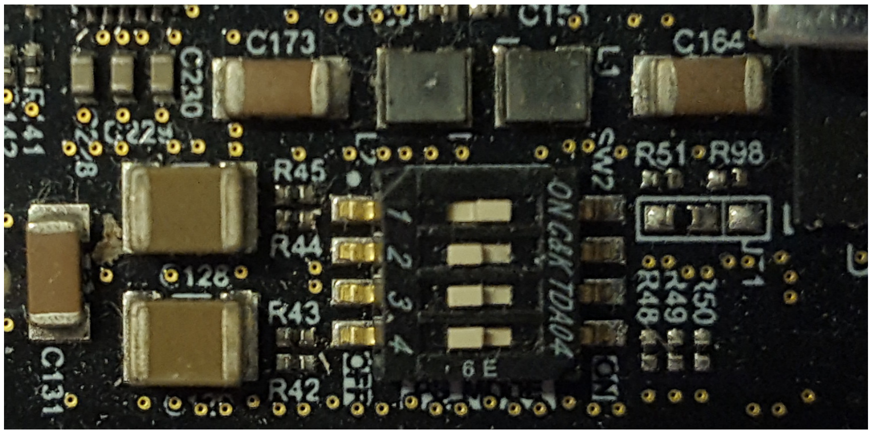
- `Xfsbl_plpartition_valid.c`: Measurements for authenticated PL partitions are inserted in this file.
- `Xfsbl_plpartition_valid.h`: The partition number is added to the PL parameter data structure.

Building the Secure and Measured Boot Image

The reference design includes a Boot Image Format (BIF) file that specifies that all partitions are authenticated. This is the minimum recommended setting so that the security from the HROT can be extended to measured boot. Optionally, encryption can be added to the BIF file to provide confidentiality of some or all of the partitions. The boot image can be built by running the BAT file `build_authenticated.bat`. It contains a single command to run bootgen using the `authenticated.bif`.

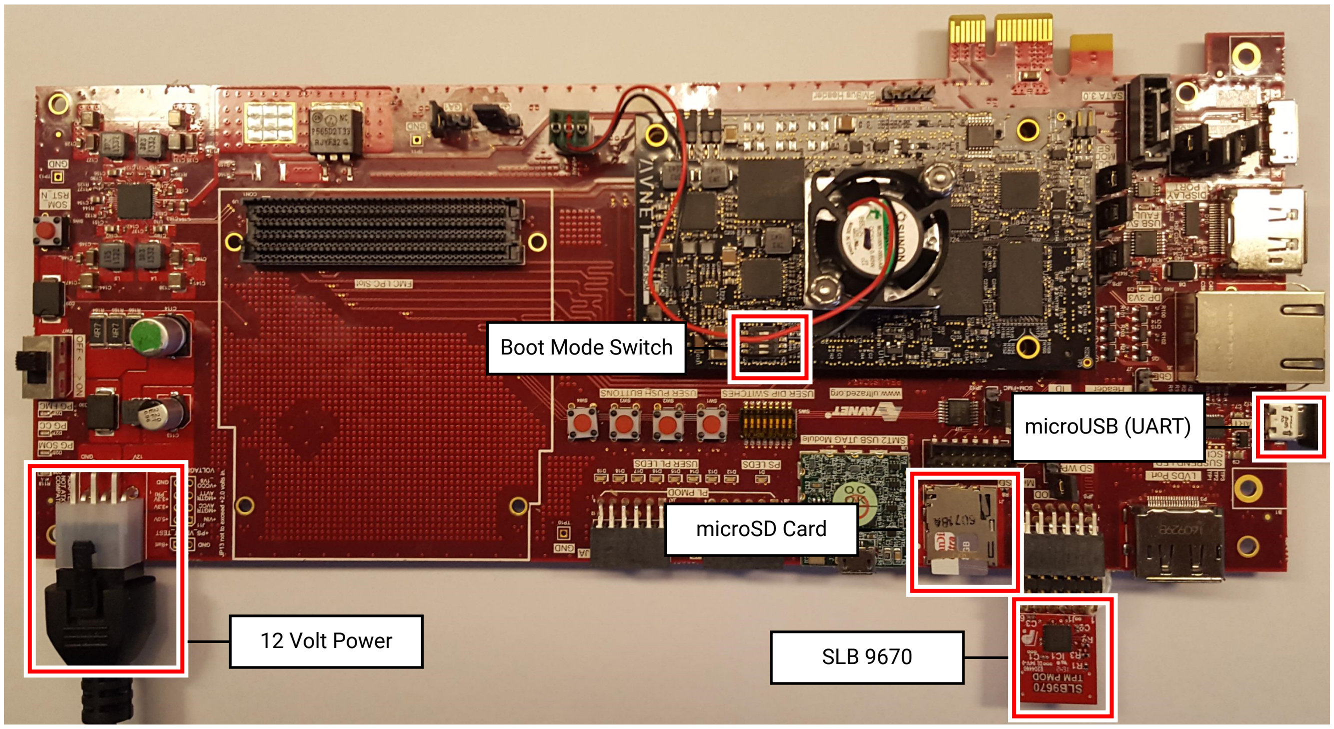
After the `BOOT.BIN` image is built, it can be placed on a microSD card. The microSD card is then inserted into the Avnet UltraZed PCIe carrier card. The BOOT mode pins are then set to boot from the microSD card, as shown in the following figure.

Figure 4: **Boot Mode Switch Settings for SD Card**



A microUSB cable can be connected from the UART connector to a PC running a terminal communication program such as Tera Term, as shown in the following figure. The settings for the UART are 115200,8,N,1.

Figure 5: **Hardware Connections**



After the board is turned on, the following output should appear on the terminal. Some additional FSBL output has been trimmed to focus on only the measured boot log statements. Most notably, these were debug printouts related to authentication.

```
Xilinx Zynq MP First Stage Boot Loader
Release 2018.3   Jan 21 2019  -  10:29:49
Reset Mode       :         System Reset
Platform: Silicon (4.0), Cluster ID 0x80000000
Running on A53-0 (64-bit) Processor, Device Name: XCZU3EG
SLB9670: Sending startup command
SLB9670: Sending selftest command
SLB670: Selftest passed
SLB9670: Sending PCR_Event to PCR #0

PCR VALUE BEFORE PCR_EVENT START
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

PCR VALUE BEFORE PCR_EVENT END

EVENT SHA256 DIGEST START
A8 2F ED 36 F7 73 51 92 57 59 25 14 A9 A3 5F 1F
77 E5 2E 40 EF 29 2F 26 F5 3B E6 00 D9 36 CC B7

EVENT SHA256 DIGEST END

PCR VALUE AFTER PCR_EVENT START
53 EE 7F 3F 42 0B CD 5C F9 79 A0 B7 76 2A 7A DF
4F A4 1A 41 4B 9B 47 1C 55 29 32 D2 F2 CC 7E 0C

PCR VALUE AFTER PCR_EVENT END

Processor Initialization Done
================= In Stage 2 ============
SD1 with level shifter Boot Mode
SD: rc= 0
File name is 1:/BOOT.BIN
Multiboot Reg : 0x0
Image Header Table Offset 0x8C0
Authentication Enabled

< REMOVE AUTHENTICATION DEBUG STATEMENTS >

Partition Verification done
*****Image Header Table Details********
Boot Gen Ver: 0x1020000
No of Partitions: 0x3
Partition Header Address: 0x440
Partition Present Device: 0x0
FSBL LOAD ADDRESS = FFFC0000
FSBL Size = 115472 bytes
FSBL SHA3-384 DIGEST START
DD DF F9 E7 02 08 9B 3E 9E 61 1A 09 0D B0 91 34
ED 64 91 B3 7D 6E 66 BD 49 BF 7E 96 07 A6 BB 97
B5 1D 70 C2 23 F8 AD 8B 68 FE C8 B1 5D 06 80 DB

FSBL SHA3-384 DIGEST END
SLB9670: Sending PCR_Event to PCR #4

PCR VALUE BEFORE PCR_EVENT START
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

PCR VALUE BEFORE PCR_EVENT END

EVENT SHA256 DIGEST START
B5 AB CB 3E C3 9E 5D 83 8E F8 84 E7 6B 07 E7 1C
A5 63 9F 9E 00 ED 87 AA 6C B5 2F 1C 8A 99 25 FB

EVENT SHA256 DIGEST END

PCR VALUE AFTER PCR_EVENT START
27 DB 07 29 6D C7 74 08 BD EF 2C 16 B4 FD C2 BD
5B 81 EA 45 02 22 A8 A3 12 D3 9C 6A 66 2C 5D 30

PCR VALUE AFTER PCR_EVENT END

Initialization Success
======= In Stage 3, Partition No:1 =======
UnEncrypted data Length: 0x153E27
Data word offset: 0x153E27
Total Data word length: 0x1541E0
Destination Load Address: 0xFFFFFFFF
Execution Address: 0x0
Data word offset: 0x7E80
Partition Attributes: 0x208026
Destination Device is PL, changing LoadAddress
Authentication Enabled

< REMOVE AUTHENTICATION DEBUG STATEMENTS >

PL SHA3-384 DIGEST START
08 F8 60 B4 8B 39 AA 10 5C E8 F3 21 BF 05 33 81
F3 A1 E2 41 CC 84 AC 6E 7B B3 70 65 81 F0 F7 DE
4B EF 24 AF 7B AE 62 6D 5D AB 7C 44 95 3C 5F D1

PL SHA3-384 DIGEST END
SLB9670: Sending PCR_Event to PCR #6

PCR VALUE BEFORE PCR_EVENT START
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

```
PCR VALUE BEFORE PCR_EVENT END

EVENT SHA256 DIGEST START
30 CE 3B 6A 8D 51 8E 1E 95 EF 87 8C BC 01 89 91
34 80 E2 3A C1 3C 8E 97 62 89 71 F2 59 B7 77 87

EVENT SHA256 DIGEST END

PCR VALUE AFTER PCR_EVENT START
AA 5B 21 A8 2D B5 AA D5 7F E6 BC E0 76 42 CD F5
CE 08 33 70 2B AB AD AA 12 C5 E3 6C F3 AE 0E C0

PCR VALUE AFTER PCR_EVENT END

PL Configuration done successfully
Partition 1 Load Success
======= In Stage 3, Partition No:2 =======
UnEncrypted data Length: 0x2412
Data word offset: 0x2412
Total Data word length: 0x27D0
Destination Load Address: 0x0
Execution Address: 0x0
Data word offset: 0x15C060
Partition Attributes: 0x8116
Authentication Enabled

< REMOVE AUTHENTICATION DEBUG STATEMENTS >

Partition Verification done
PARTITION 2 LOAD ADDRESS = 00000000
PARTITION 2 Size = 36936 bytes
PARTITION SHA3-384 DIGEST START
30 AD 08 39 92 96 E3 89 DD 5D 70 EC 03 54 00 34
08 6D 44 27 E5 1F C3 A6 4B 0E A3 61 D7 2C 8A 1A
30 D6 4B 42 38 A8 AF 9C DF D1 23 E4 E4 2E FC F5

PARTITION SHA3-384 DIGEST END
SLB9670: Sending PCR_Event to PCR #7

PCR VALUE BEFORE PCR_EVENT START
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

PCR VALUE BEFORE PCR_EVENT END

EVENT SHA256 DIGEST START
0A 52 73 C3 8E 55 58 A4 26 48 F4 36 2D 1F 37 0D
64 8A AA 70 F8 B7 D4 63 58 20 18 9F EB 36 F5 28

EVENT SHA256 DIGEST END

PCR VALUE AFTER PCR_EVENT START
5A FF 2A E5 27 78 F1 A3 DF 6E B9 0B C6 BE F2 68
DF 9C 59 CF 90 D7 95 65 5E 39 D5 80 EF 55 5A 6D

PCR VALUE AFTER PCR_EVENT END

Partition 2 Load Success
All Partitions Loaded
================= In Stage 4 ============
PMU-FW is not running, certain applications may not be supported.
Protection configuration applied
Running Cpu Handoff address: 0x0, Exec State: 0
Exit from FSBL
Hello World
```

Conclusion

Zynq UltraScale+ devices provide significant advantages in their ability to program both hardware and software on the same device. Cost-effective firmware updates are a key component to increasing an embedded system's capability and providing maintenance. Remote firmware updates rely on using the Internet, which opens the embedded system to attacks. The secure boot features of the Zynq UltraScale+ devices coupled with measured boot features enabled by a TPM provide a secure means of attesting the software and firmware being executed on a client system. A remote server is able to set policy for such client systems enabling detection, isolation, and correction of compromised client systems.

References

1. *Measured Boot of Zynq-7000 SoCs* (XAPP1309)
2. *Zynq UltraScale+ Device Technical Reference Manual* (UG1085)
3. TPM Main Specification
4. TCG PC Client Specific TPM Interface Specification

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
04/18/2019 Version 1.0	
Initial release.	N/A

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