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All Digital VCXO Replacement for Gigabit Transceiver Applications (UltraScale FPGAs)

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Summary

This application note delivers a system that is designed to replace external voltage-controlled crystal oscillator (VCXO) circuits by utilizing functionality within each serial gigabit transceiver.

Note: In this application note, *transceiver* refers to these types of transceivers:

Device Family	Transceiver Type
Kintex® UltraScale™ FPGAs	GTH transceiver
Virtex® UltraScale FPGAs	GTH and GTY transceivers

A common design requirement is to frequency or phase lock a transceiver output to an input source (known as loop, recovered, or slave timing). Traditionally, an external clock cleaning device or VCXO and PLL components are used to provide a high-quality clock reference for the transceiver, since FPGA logic-based clocks are generally too noisy. While effective, external clock components carry a power and cost penalty that is additive as each individual clock channel is generated. When using many channels or in low-cost systems, the cost can be significant. Additionally, adding many external clock sources provides more opportunity for crosstalk and interference at the board level.

The system described in this application note provides a method to effectively replace these external clock components using a combination of unique Xilinx transceiver features in conjunction with a high-performance FPGA logic-based digital PLL (DPLL). Each transceiver has a phase interpolator (PI) circuit in the high-speed analog PLL output circuits that provides, on an individual transceiver channel basis, the ability to phase and frequency modulate the transmit clock operating the transceiver. Using a fully digital interface, the phase interpolator can be phase and frequency controlled from the FPGA logic resources under control of a high-resolution programmable DPLL. In conjunction with the FPGA logic DPLL, the phase interpolator provides the ability to phase or frequency modulate the transceiver data output directly locking to an input reference pulse or clock while providing a built-in clock cleaning filter function. Unlike conventional solutions, a high-quality system results because the clocking components are contained within the transceiver.

The reference design circuit provides a fully integrated DPLL and transceiver phase interpolator system which can be instantiated for each transceiver channel used. The transceiver can phase or frequency lock to an input reference signal. The DPLL enables generation of a synchronous transceiver data output with run-time configurable parameters (e.g., gain, cutoff frequency, and clock divider values) to enable you to set up the operation specifically for the end application. This allows flexibility of the reference input signal and DPLL cleaning bandwidth.

The reference design circuit can lock an individual transceiver greater than ±1000 ppm[1] from the reference oscillator and programmatically provide jitter cleaning bandwidths in the range from 0.1 Hz to 1 KHz. In the UltraScale FPGAs, the transceiver can operate at up to 30.5 Gb/s[2]. Typical applications for this circuit include video SD/HD/3G/UHD-SDI, Sync E, IEEE1588, SDH, SONET, and OTN.

The system applications and operational theory are equivalent to the PICXO 7 series application note, *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)* (XAPP589) [Ref 1].

You can download the reference design files for this application note from the Xilinx website. For detailed information about the design files, see Reference Design.

PICXO DPLL

The phase interpolator controlled crystal or Xtal oscillator (PICXO) parameters must be set appropriately to generate a transceiver channel locked to a reference signal. The DPLL can be analyzed using standard methods from a derivation of the transfer function outlined in this section.

The PICXO DPLL circuit, for analysis purposes, is considered to have three functional blocks:

1. Phase frequency detector (PFD)

   The phase frequency detector measures the phase difference between the reference (R) and the PICXO (V) clocks and produces an error output. As the DPLL is second order when locked, this error output is driven to zero. It has a transfer function that is defined in units of radian^{-1} and gain, G_{PD}.

2. Second-order loop filter

   The second-order loop filter consists of proportional and integral paths with digital gains defined by the terms G_1 and G_2. The output represents the required tune value for the oscillator.

3. Numerically controlled oscillator

   The numerically controlled oscillator function is performed by the transmit phase transceiver's interpolator block, the phase accumulator, and the sigma-delta modulator. This has units of radians/s and gain G_{PICXO}.

1. PICXO frequency pull range depends on settings. Lowest jitter performance is achieved with <±200 ppm maximum pull range.
2. PICXO maximum operating bit rate is 16.4 Gb/s with GTY transceiver.

These blocks are shown in a standard DPLL configuration in Figure 1.

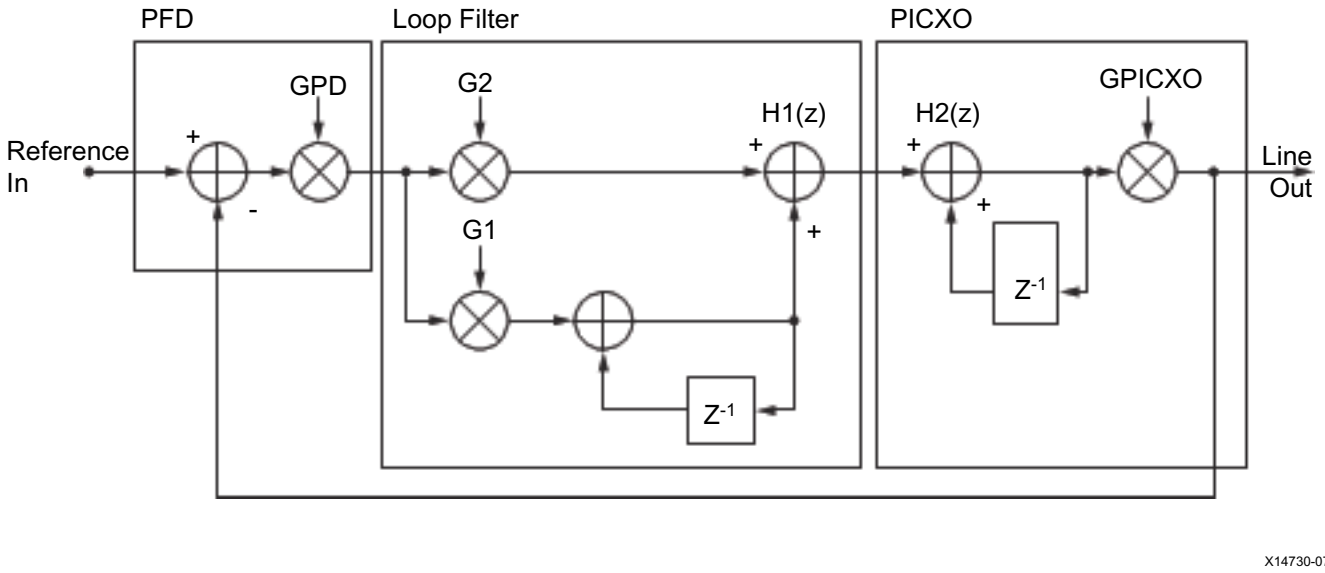


Figure 1: **PICXO DPLL Digital Equivalent**

The transfer of the reference input clock to the line output data is represented by the function in Equation 1. This allows the clock cleaning and tracking of the all-digital VCXO replacement to be exactly controlled by your application.

$$H(z) = \frac{H1(z)H2(z)G_{PD}}{1 + H1(z)H2(z)G_{PD}} \quad \textit{Equation 1}$$

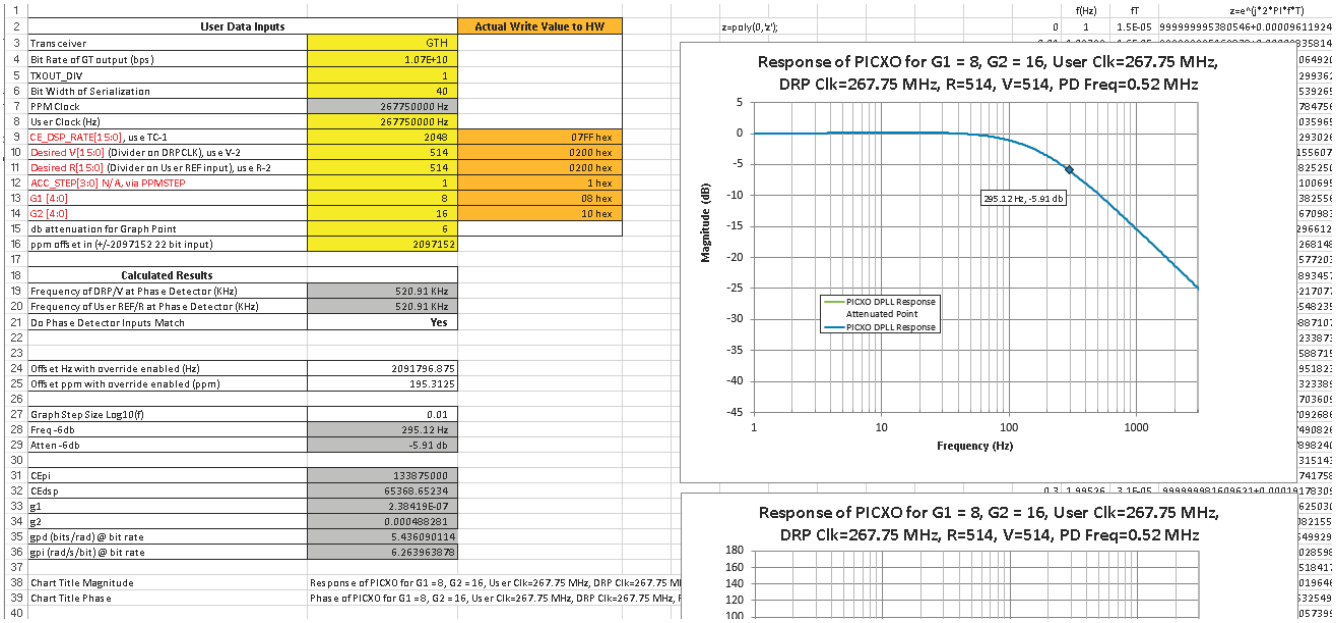
with:

$$H1(z) = \frac{(g1 + g2)z - g2}{(z - 1)} \quad \textit{Equation 2}$$

and:

$$H2(z) = \frac{Z(G_{PICXO})}{(z - 1)} \quad \textit{Equation 3}$$

The Excel spreadsheet tool included in the PICXO design file package (shown in Figure 2) allows you to estimate the PICXO response when setting the configurable parameters listed above. The PICXO DPLL allows complete flexibility with settings. Therefore, it is advisable to understand the performance trade-offs of the PLL in the end system.



User Data Inputs		Actual Write Value to HW
Transceiver	GTH	
Bit Rate of GT output (bps)	1.07E+10	
TXOUT_DIV	1	
Bit Width of Serialization	40	
PPM Clock	267750000 Hz	
User Clock (Hz)	267750000 Hz	
CE_DSP_RATE[15:0], use TC-1	2048	07FF hex
Desired V[15:0] (Divider on DRPCLK), use V-2	514	0200 hex
Desired R[15:0] (Divider on User REF input), use R-2	514	0200 hex
ACC_STEP[3:0] N/A, via PPMSTEP	1	1 hex
G1 [4:0]	8	08 hex
G2 [4:0]	16	10 hex
db attenuation for Graph Point	6	
ppm offset in (+/-2097152 22 bit input)	2097152	
Calculated Results		
Frequency of DRP/V at Phase Detector (KHz)	520.91 KHz	
Frequency of User REF/R at Phase Detector (KHz)	520.91 KHz	
Do Phase Detector Inputs Match	Yes	
Offset Hz with override enabled (Hz)	2091796.875	
Offset ppm with override enabled (ppm)	195.3125	
Graph Step Size Log10(f)	0.01	
Freq -6db	295.12 Hz	
Atten -6db	-5.91 db	
CEpi	133875000	
CEdsp	65368.65234	
g1	2.38419E-07	
g2	0.000488281	
gpd (bits/rad) @ bit rate	5.436090114	
gpi (rad/s/bit) @ bit rate	6.263963878	
Chart Title Magnitude	Response of PICXO for G1 = 8, G2 = 16, User Clk=267.75 MHz, DRP Clk=267.75 MI	
Chart Title Phase	Phase of PICXO for G1 = 8, G2 = 16, User Clk=267.75 MHz, DRP Clk=267.75 MHz, F	

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Figure 2: **PICXO DPLL Spreadsheet Example Calculation**

For optimum jitter and cleaning performance, it is recommended that the PICXO DPLL bandwidth be less than 300 Hz. Higher tracking bandwidths can be achieved, however, with some increase in jitter. It might be desirable to have a high bandwidth to acquire lock, then switching subsequently to a lower cleaning bandwidth. This is known as fast acquisition for the DPLL.

The DPLL architecture allows operational changes to the G1 and G2 values to support this while not losing phase lock. Changes can be supported in user logic by applying variable G1 and G2 values. It can be appropriate to monitor the error output from the DPLL as one method to ascertain a suitable point at which to switch gain values.

PICXO Measurements and Performance

This section includes sample measurements of the example PICXO design implemented on the KCU105 board where the system has been configured as a nominal 10 Gb/s loop-timed design. That is, the data is received on the transceiver input and re-transmitted with the PICXO generated line clock which tracks and jitter-cleans the received recovered clock from the input line data. For flexibility, an external clock source is used to drive the transceiver and PICXO system. For the measurements taken, the system is operated at 10.71 Gb/s with a reference clock of 267.7 MHz, which is the effective line rate /40.

The connections are shown in Figure 3.

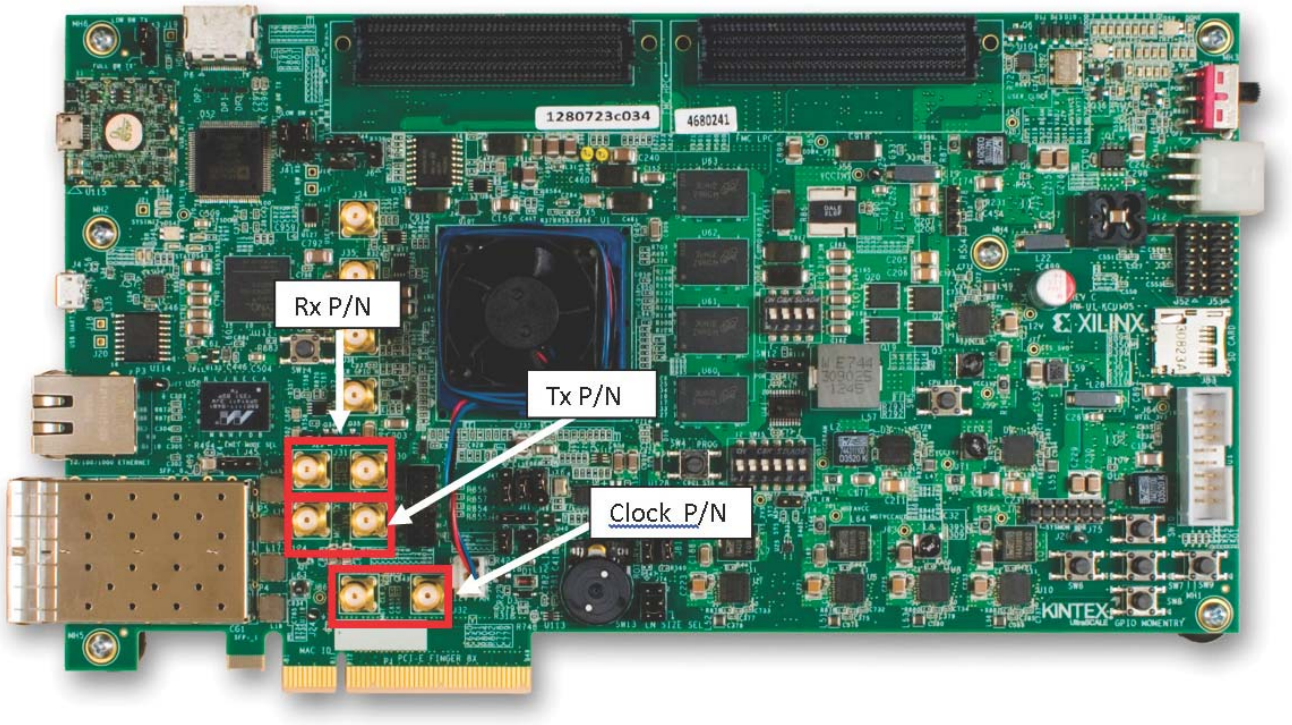

Figure 3: **KCU105 Board Connections**

Once loaded from Vivado Hardware Manager, the interface in Figure 4 is available with access to the PICXO configurable parameters and the transceiver driver outputs. The default virtual input/output (VIO) configuration should enable the PICXO to lock and loop the data through the device. For additional debug information, an integrated logic analyzer (ILA) is incorporated where the PICXO operation can be observed (i.e., ERROR and VOLT traces).

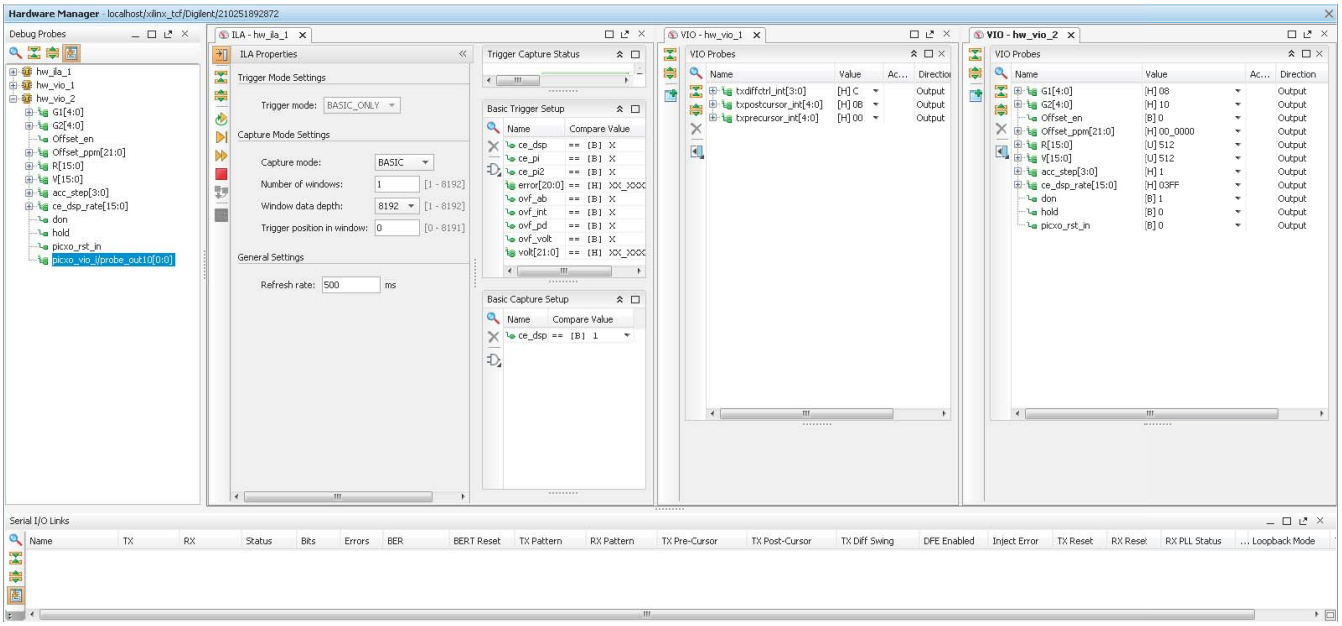

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Figure 4: **Vivado Hardware Manager Console**

Figure 5 through Figure 7 show the output waveforms and jitter decomposition of the output data when the PICXO and GTH are generating 0, 20, and 100 ppm offsets from the nominal system reference clock frequency.

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Figure 5: **Output 10.71 Gb/s 0 ppm Offset**

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Figure 6: **Output 10.71 Gb/s 20 ppm Offset**

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Figure 7: **Output 10.71 Gb/s 100 ppm Offset**

The jitter performance of the PICXO is dominated by two components:

- TXPI - The discrete phase steps on the interpolator and phase rotation introduce an incremental amount of jitter. With modest offsets (<100 ppm), this will likely have a negligible effect on the system. The amount of jitter added can be mitigated with reduced ppm tuning range.
- PICXO DPLL - The DPLL is a high-performance logic-based system utilizing a high accuracy phase detector to deliver lowest in bandwidth jitter. To reduce quantization effects, the PICXO has incorporated an optional dither circuit that can reduce the DPLL in band jitter. This is controlled by the active-High DON port.

Figure 8 shows a possible PICXO locked condition. The ERROR output has an average value around 0. This indicates the DPLL has converged and is locked and the PICXO phase detector has nominally the same phase and frequency on its inputs. The VOLT output has a value that represents the difference in frequency between the local XO and the PICXO frequency-locked output. The greater the value from 0, the further in frequency the PICXO is tracking.

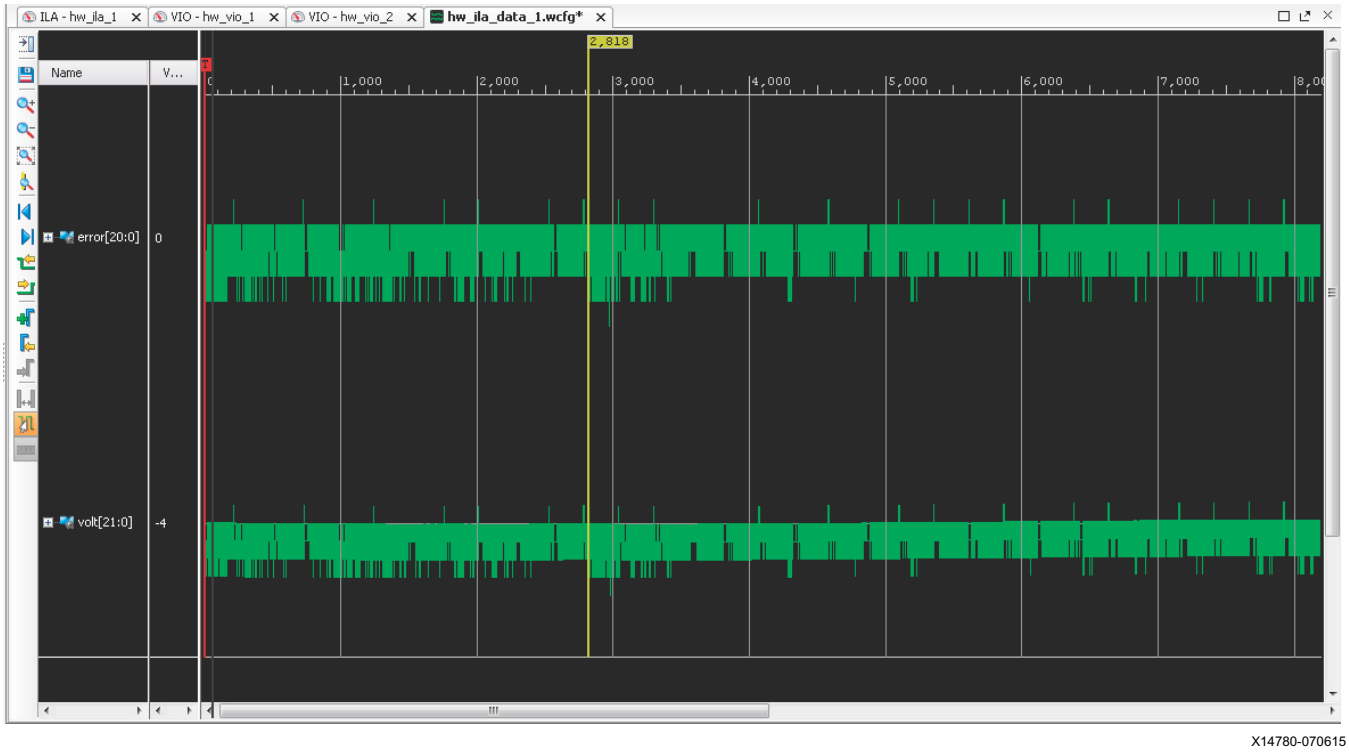

Figure 8: **PICXO VOLT_O and ERROR_O using CE_{DSP} as Storage Qualification**

PICXO Architecture Overview

Instead of using an external VCXO, as described in *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)* (XAPP589) [Ref 1], a complete digital PLL and clock cleaner can be created using the phase interpolator in the transmit serial/deserializer as a phase interpolator controlled crystal or Xtal oscillator (PICXO). The PICXO macro operation for GTH/GTY transceivers is shown in the functional block diagram in Figure 9.

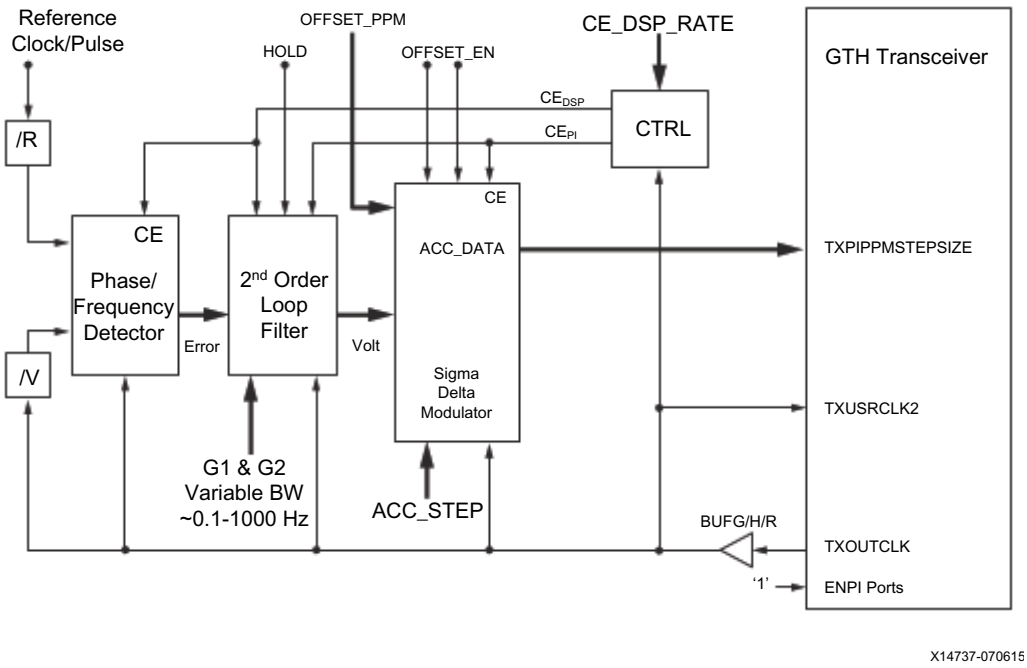

Figure 9: **PICXO Macro Functional Block Diagram for GTH and GTY Transceivers**

The phase accumulator tracks the current phase of the phase interpolator and increments or decrements the phase based on input from the sigma delta modulator block. Incrementing or decrementing phases directly results in a negative or positive frequency offset.

The required fine frequency control is achieved by the sigma delta modulation block driven by a second order DPLL consisting of filter and phase detector with user-configurable loop parameters and comparison frequencies for maximum flexibility.

The maximum phase interpolator update rate is the clock enable rate for the sigma delta modulator and accumulator CE_{PI}, shown in Figure 9. The DPLL runs at a sub-rate CE_{DSP}, the clock enable rate for the phase/frequency detector and second-order loop filter (in Figure 9). This allows the sigma delta modulator to run with high resolution and allows usable DPLL coefficients for low-frequency clock cleaning. The CE_{PI} and CE_{DSP} clock rate information is available within the spreadsheet tool shown in Figure 2 for the configuration selected.

The reference design circuit uses one BUFG/BUFH/BUFR per line rate generated. When locked, this clock is synchronous with the reference clock and can be used for other user downstream logic.

The PICXO macro provides phase increment information directly to the GTH/GTY transceiver TXPPMSTEPSIZE input ports. This bus applies phase increment or decrement information to the internal transceiver TXPI phase accumulator.

Designing with PICXO

Physical Interface

Table 1 through Table 5 list port definitions.

Table 1: **Clocks, Reset, and Interface to the Transceiver Ports**

Signal Name	Direction	Description
RESET_I	Input	Synchronous reset. Active-High. Needs 8 clock cycles to reset correctly.
REF_CLK_I	Input	Reference signal. Can be any clock (local, BUFG, pulse, etc.).
TXOUTCLK_I	Input	Connect to TXOUTCLK of the serial transceiver via a BUFG/BUFH/BUFR.
DRPEN_O	Output	Unused. Leave floating.
DRPWEN_O	Output	Unused. Leave floating.
DRPDO_I[15:0]	Input	Unused. Connect to 0 or 1.
DRPDATA_O[15:0]	Output	Unused. Leave floating.
DRPADDR_O[8:0]	Output	Unused. Leave floating.
DRPRDY_I	Input	Unused. Connect to 0 or 1.

Table 2: **DRP User Port (Unused)**

Signal Name	Direction	Description
DRP_USER_REQ_I	Input	Unused. Connect to 0.
DRP_USER_DONE_I	Input	Unused. Connect to 0.
DRPEN_USER_I	Input	Unused. Connect to 0.
DRPWEN_USER_I	Input	Unused. Connect to 0.
DRPADDR_USER_I[8:0]	Input	Unused. Connect to 0.
DRPDATA_USER_I[15:0]	Input	Unused. Connect to 0.
DRPRDY_USER_O	Output	Unused. Leave floating.
DRPDATA_USER_O[15:0]	Output	Unused. Leave floating.
DRPBUSY_O	Output	Unused. Leave floating.

Table 3: **TXPI Port**

Signal Name	Direction	Description
ACC_DATA[4:0]	Output	Connect to TXPIPPMSTEPSIZE[4:0] of the transceiver.

Table 4: **Debug Ports**

Signal Name	Direction	Description
ERROR_O[20:0]	Output	Output of phase detector. Signed number.
VOLT_O[21:0]	Output	Output of low-pass filter. Signed number.
DRPDATA_SHORT_O[7:0]	Output	Unused. Leave floating.
CE_PI_O	Output	Clock enable for accumulator.
CE_PI2_O	Output	Clock enable for low pass filter and DAC.
CE_DSP_O	Output	Reset phase detector counters, load phase detector error into the low-pass filter.
OVF_PD	Output	Overflow in the phase detector.
OVF_AB	Output	Saturation of the low-pass filter inputs.
OVF_INT	Output	Saturation of the low-pass filter integrator.
OVF_VOLT	Output	Saturation of the low-pass filter output.

Table 5: **PICXO Loop Parameters**

Signal Name	Direction	Description
G1[4:0]	Input	Filter linear path gain: range `0` to `x12h`.
G2[4:0]	Input	Filter integrator path gain: range `0` to `x14h`.
R[15:0]	Input	Reference divider: range `0` to `65535`. Divides by R+2.
V[15:0]	Input	TXOUTCLK_I divider: range `0` to `65535`. Divides by V+2.
ACC_STEP[3:0]	Input	PICXO step size: range `1` to `15` (`0` = no step).
CE_DSP_RATE[15:0]	Input	DSP divider: default `07FF`. Control CE_DSP rate.
VSIGCE_I	Input	Clock enable of the TXOUTCLK_I divider. Connects to 1 for normal operation.
VSIGCE_O	Output	Reserved: Floating.
RSIGCE_I	Input	Clock enable of Reference divider. Connects to 1 for normal operation.
C_I[7:0]	Input	Reserved: Connect to `0`.
P_I[9:0]	Input	Reserved: Connect to `0`.
N_I[9:0]	Input	Reserved: Connect to `0`.
OFFSET_PPM[21:0]	Input	Direct frequency offset control. Signed number. OFFSET_PPM overwrites the output of the low-pass filter (VOLT_O) when OFFSET_EN is High.
OFFSET_EN	Input	Enable direct frequency offset control input. Active-High: Enables OFFSET_PPM input to overwrite output of low-pass filter (Volt).
HOLD	Input	Hold low-pass filter output value (Volt). Clock enable of Volt that stops Volt to the latest known ppm.
DON_I	Input	Dither On. Potential jitter reduction. Active-High.

Interface Operation

General Operation

The PICXO parameters (V, R, ACC_STEP, CE_DSP_RATE) can affect the PICXO lock if changed, therefore they are considered pseudo-static inputs. The gains G1 and G2 can be changed without loss of lock. All input and output signals to/from the PICXO are synchronous to TXOUTCLK_I except REF_CLK_I and R. Figure 10 shows the timing dependency between TXOUTCLK_I and the main debug outputs.

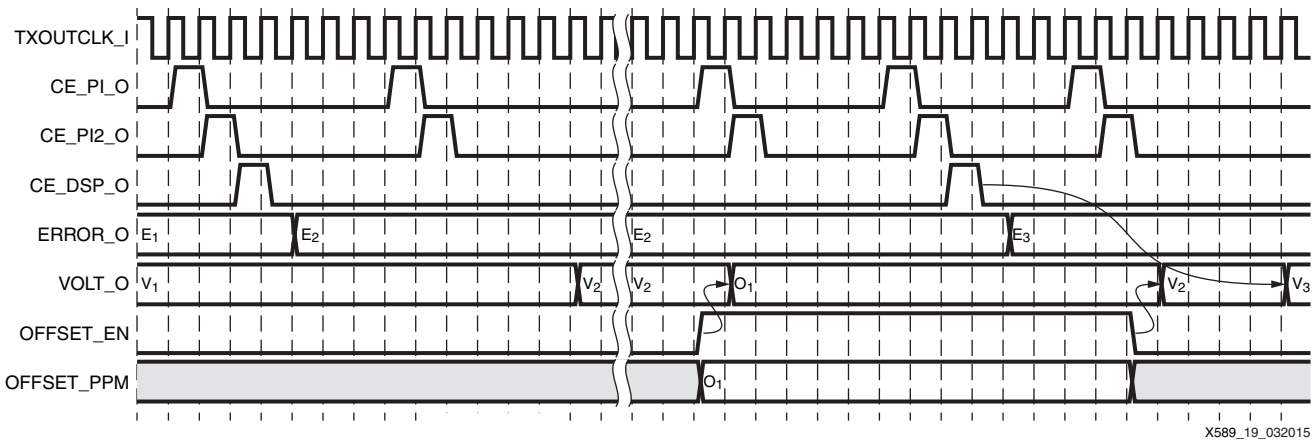

Figure 10: **Timing Waveforms of Main Debug Outputs**

Reset Considerations

The PICXO main reset RESET_I requires a minimum of eight TXOUTCLK_I cycles to reset the PICXO correctly. When applied, RESET_I resets all blocks, including the phase detector and low-pass filter. When releasing RESET_I, the first phase detector output (ERROR_O) is zero, and the first word written in the transceiver phase interpolator is zero.

The transceiver TX PMA reset sequence must be completed before the PICXO reset is released for operation.

UltraScale FPGA Transceiver Clocking

The primary clocking scheme is detailed in Figure 11. The transceiver TXOUTCLK connects to a BUFG/R/H that drives the PICXO inputs clocks TXOUTCLK_I.

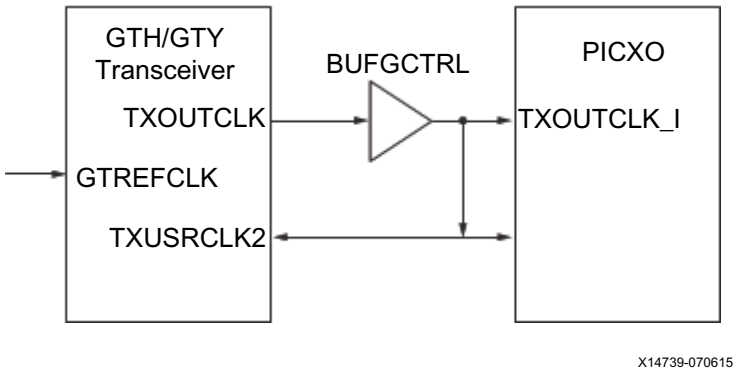

Figure 11: **7 Series FPGA Primary PICXO Clocking Scheme**

Notes relevant to Figure 11:

1. TXOUTCLK_I must be the same clock as TXUSRCLK2.

HOLD Input Operation

The HOLD input is a clock enable to the low-pass filter integrator and output (VOLT_O). While HOLD is High, the phase detector continues to operate as normal. When HOLD returns to Low, the low-pass filter output is not synchronized anymore with the phase detector. Figure 12 illustrates this behavior.

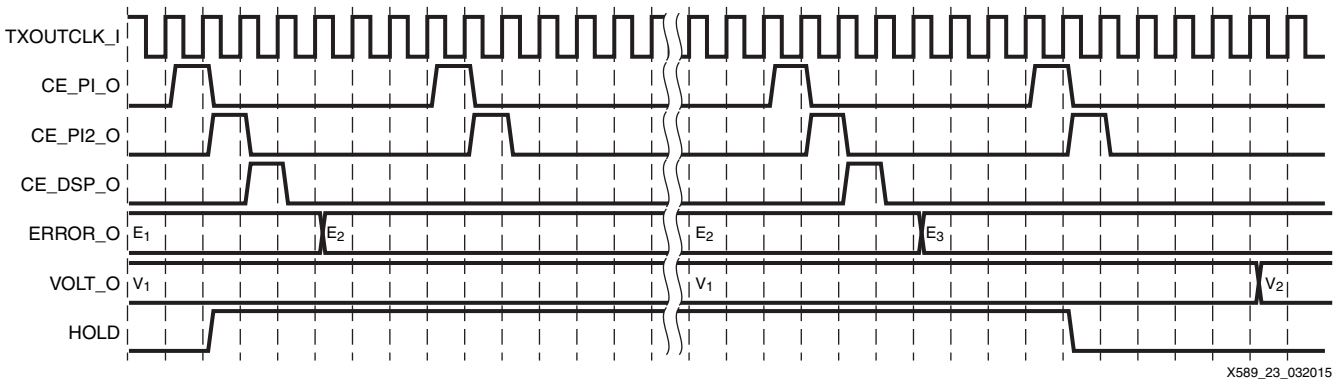

Figure 12: **HOLD Input Operation**

Direct Offset Control

OFFSET_PPM and OFFSET_EN allow direct control of the frequency offset. When OFFSET_EN is High, the output of the low-pass filter (VOLT_O) takes the OFFSET_PPM value. During this time, the phase detector and low-pass filter integrator operate normally. When OFFSET_EN returns to Low, the output of the low-pass filter (VOLT_O) takes the current value calculated by the phase detector and low-pass filter. Figure 13 illustrates this behavior.

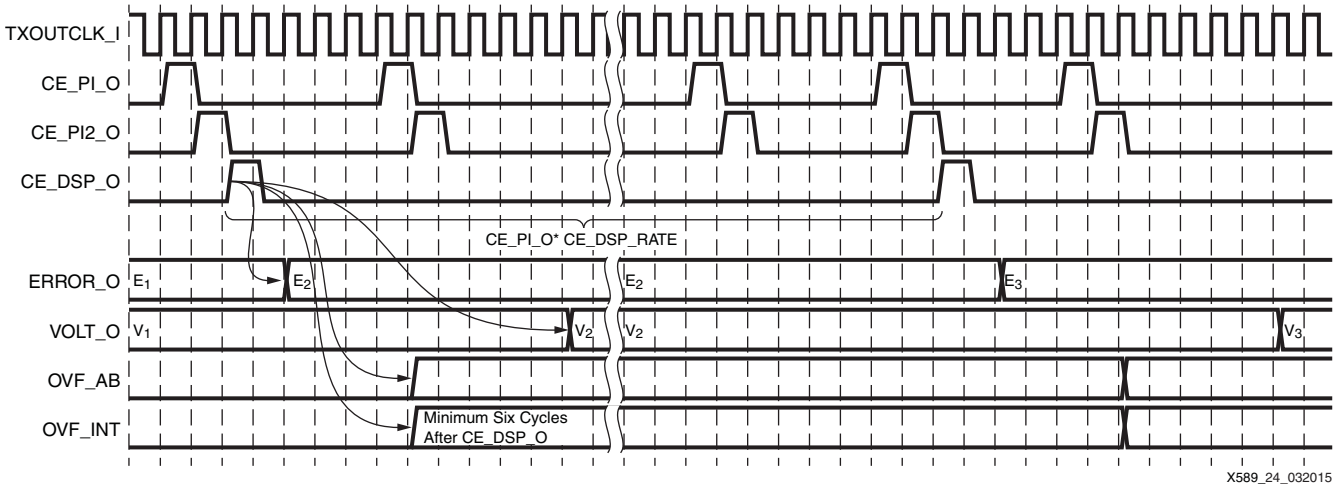

Figure 13: **Direct Offset Control**

Implementation

Vivado Tools Implementation

The PICXO design is delivered as a custom IP. To add the design to a project:

1. Unzip the file in a location.
2. Add the IP repository to the project: **Tools > Project Options**, select **IP** on the left pane, click **Add Repository**, and select the **XAPP589_XAPP1241_picxo** folder (see Figure 14).

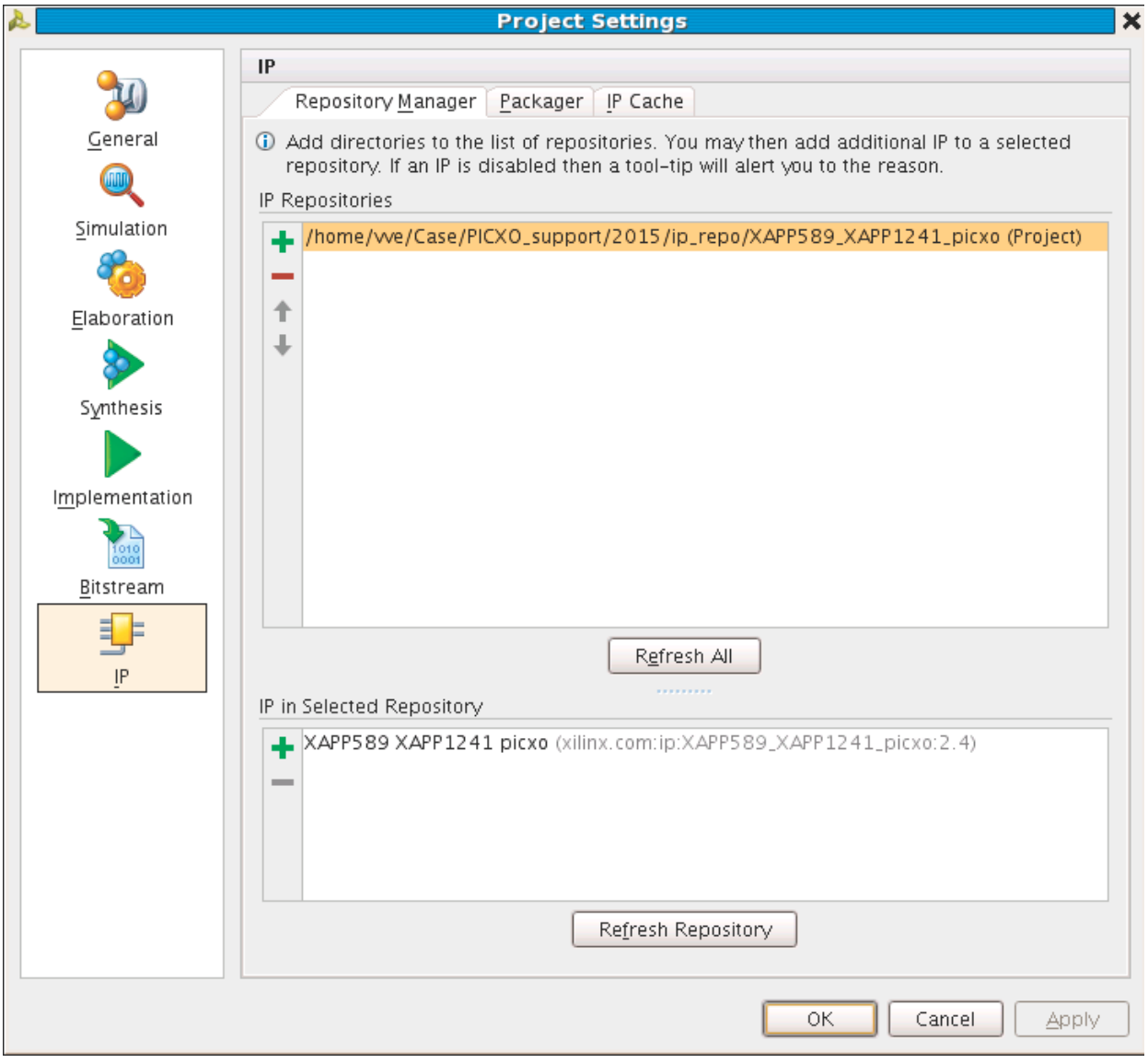

Figure 14: **Adding the IP Respository**

3. Select the IP catalog. The PICXO IP is under **FPGA Features and Design > IO Interfaces** (see Figure 15).

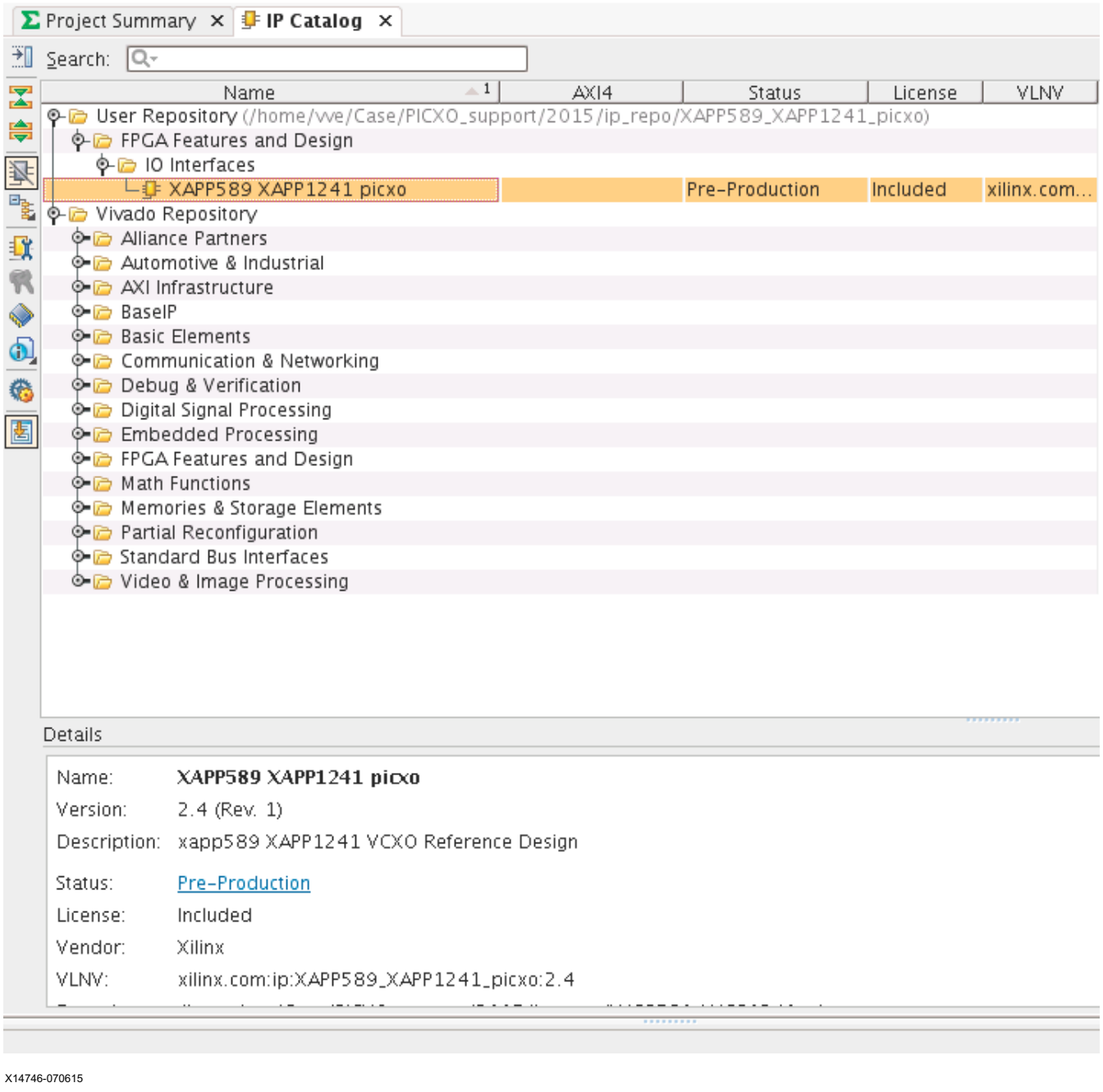

Figure 15: **PICXO IP Location**

4. Right-click **XAPP589_XAPP1241_picxo** and select **Customize IP**.

5. Select the IP module name and the type of GT (see Figure 16). Click **OK.**

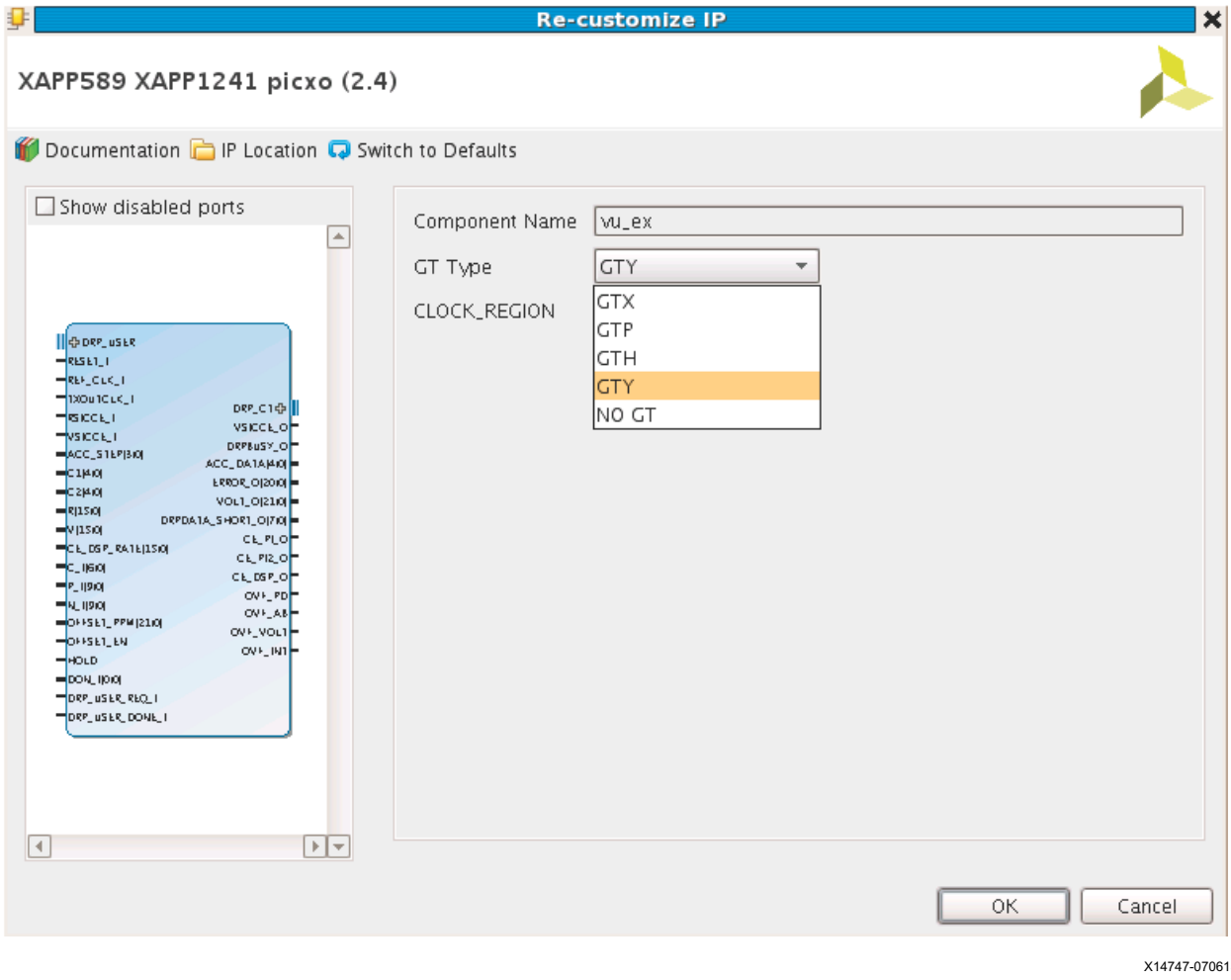

Figure 16: **GT Transceiver Selection**

6. The example design can be generated by selecting the IP source, right-click, and **generate example design.**

Mandatory Conditions and Limitations

UltraScale FPGA GTH and GTY Transceivers

- Transmit buffer bypass is not supported.
- GTH/GTY port TXPIPPMEN must be connected to 1.
- GTH/GTY port TXPIPPMSEL must be connected to 1.
- GTH/GTY attribute TXPI_SYNFREQ_PPM must be set to 001.
- TXOUTCLK and TXUSRCLK2 must be the same clock. If TX_PROGCLK_SEL is set to 00, TXOUTCLKSEL must be set to 101. In all other cases, TXOUTCLKSEL must be set to 010 or 001.
- The transceiver associated with the PICXO must be constrained to a specific location.
- Period constraints are necessary on TXOUTCLK_I and REFCLK_I.
- GTY maximum line rate is 16.4 Gb/s.

Note: A DRC check is performed during opt_design and critical warnings are generated if the conditions above are not respected.

Reference Design

The reference design files are based on the UltraScale FPGA transceiver wrapper v1.0 (see *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 2]. The designs target the KCU105 and VCU108 development platforms. They loopback the receive data to the transmitter. The PICXO instance locks the transmitter to the recovered clock RXRECLK.

The output error_o of the phase/frequency detector can be captured when CE_DSP_O is High to monitor the PICXO response. When locked, ERROR_O should oscillate around 0 (see Figure 8).

Simulation of the example design is not supported.

Download the reference design files for this application note from the Xilinx website.

Table 6 shows the reference design matrix.

Table 6: **Reference Design Matrix**

Parameter	Description
General	
Developer names	David Taylor, Matt Klein, and Vincent Vendramini
Target devices	Kintex® UltraScale™ XCKU040-2FFVA1156E Virtex® UltraScale™ XCVU095-2FFVA2104E
Source code provided	Yes
Source code format	VHDL
Design uses code/IP from existing Xilinx application note/reference designs, or third party?	Yes. Vivado ILA and VIO
Simulation	
Functional simulation performed	No
Timing simulation performed	No
Test bench used for functional and timing simulations	No
Test bench format	N/A
Simulator software tools/version used	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/version used	Vivado® Design Suite 2015.1
Implementation software tools/version used	Vivado Design Suite 2015.1
Static timing analysis performed	Yes
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	KU105 and VCU108 boards

Table 7 shows the device utilization table for the reference design.

Table 7: **Device Utilization and Performance for Reference Design (Vivado Design Suite 2015.1)**

	Kintex UltraScale (One GTH Transceiver) Full Design	Virtex UltraScale (One GTY Transceiver) Full Design
CLB LUTs	3,384	3401
CLB registers	4,504	4504
Occupied CLBs(1)	774	811
Block RAM	13.5	13.5
BUFG/BUFHCE	3	3
GTH/GTY	1	1
MMCM	0	0

Notes:

1. The number of occupied CLBs can vary depending on packing results.

Table 8 shows the statistics and performance expectations for a standalone PICXO.

Table 8: **Statistics and Performance Expectations for a Standalone PICXO (Vivado Design Suite 2015.1)**

Target Devices	Kintex UltraScale GTH Transceiver	Virtex UltraScale GTY Transceiver
LUTs	928	933
Registers	962	962
SRLs	33	33
Maximum PICXO clock rate	Speed grade dependent, matches TXUSRCLK2 maximum frequency.	Speed grade dependent, TXUSRCLK2 maximum frequency

References

1. *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)* (XAPP589)
2. *UltraScale Architecture GTH Transceivers User Guide* (UG576)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/14/2015	1.0	Initial Xilinx release.
10/22/2021	1.0.1	Editorial updates only. No technical content changes.

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