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Using Tandem Configuration for PCIe in the Kintex-7 Connectivity TRD

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Summary

This application note describes the use of the *Tandem PROM* and the *Tandem PCIe* configuration methods with the Kintex®-7 Connectivity Targeted Reference Design (TRD) running on the KC705 evaluation board with a Kintex-7 XC7K325T FPGA.

The PCI Express® specification requires the PCIe® link to be ready to link train with a peer within 120 ms after power is stable. Meeting this requirement is a challenge for large FPGAs using flash memory for configuration due to the size of the programming bitstream and the configuration rates available. One approach to meet this need is to use one of the Tandem Configuration methodologies supported by Xilinx® 7 Series FPGAs to ensure the PCIe Endpoint block in the FPGA is ready to link train in less than 120 ms.

FPGA Configuration

The PCI Express specification states that fundamental reset must remain asserted for at least 100 ms after power becomes valid. It also states that a device must enter the detect state (be ready for link training) 20 ms after release of the fundamental reset. Therefore, PCI Express cores must be ready to start link training 120 ms after the power good signal. Due to legacy reasons with PCI Express specification, this time is often referred to as the *100 ms boot time* requirement for PCI Express. In reality, the time that a PCIe core has to get ready for link training is actually 120 ms.

FPGAs are configured by loading application-specific data (known as a bitstream) into internal FPGA memory. A comprehensive discussion of configuration is available in the *7 Series FPGAs Configuration User Guide* (UG470) [Ref 1].

FPGA configuration times are a function of the bandwidth of the programming method. Data width and programming clock frequency are the limiting factors. Refer to the *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054) [Ref 2] for device programming time calculations and design power considerations.

As the capacity of FPGA devices increases, meeting the 120 ms requirement of the PCIe specification becomes more difficult. Traditionally, configuration time is reduced by using faster and wider BPI flash memories. However, this approach can raise the hardware BOM cost and increase the system complexity. Even when using wider flash memory, higher clock rates are needed to comply with the 120 ms requirement.

For example, the Kintex-7 XC7K325T FPGA configuration bitstream length is 91,548,896 bits (87.3 Mb), and has a T_{POR} of 50 ms (worst case). If the FPGA is configured from a16-bit-wide BPI flash memory and is running in Master BPI configuration mode with synchronous read, even an EMCCLK frequency of 50 MHz the FPGA will enter the detect state in 160 ms, which is not fast enough to configure the FPGA within the 120 ms requirement.

As an alternative to the traditional method, Xilinx provides two fast configuration methods—the Tandem PROM and Tandem PCIe methods.

Tandem Methodology

Tandem methodology facilitates fast configuration capable of meeting the PCIe 120 ms link training requirement by splitting the configuration into two stages:

Stage 1: The minimum PCIe functionality needed to ensure device discovery is configured. This stage requires a very small bitstream that can be configured in much less than 120 ms and is capable of handling all transactions during enumeration time.

Stage 2: The rest of the FPGA is configured with the user design after the PCIe block becomes active.

Tandem methodology is not partial reconfiguration. Unlike partial reconfiguration, the tandem approach never reconfigures a frame. Every frame in the device is configured only once. If dynamic updates to the user application are required, traditional partial reconfiguration should be used.

Two variations of the tandem methodology can be used: Tandem PROM, and Tandem PCIe.

Tandem PROM

Figure 1 shows the Tandem PROM method. The stage 1 and stage 2 bitstream segments are packed back-to-back in the same PROM in the form of a single bitstream.

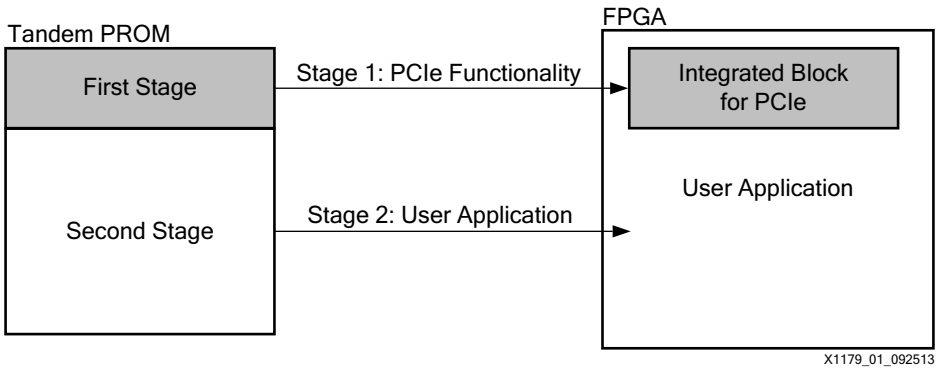

Figure 1: **Tandem PROM Method**

Tandem PROM flow is similar to standard flow. A single bitstream is generated at the end of implementation and the corresponding flash memory can be programmed. Both the PROM file and bitstream are self-contained. The PCIe block becomes active at the end of the stage 1 bitstream programming. Device programming continues with the stage 2 bitstream using the same programming path while PCIe enumeration is in progress.

Note: Dual-mode configuration pins must be reserved for Tandem PROM configuration use by setting the PERSIST property. These IO are therefore not available for the user design.

Tandem PCIe

Figure 2 shows the Tandem PCIe solution. Tandem PCIe is similar to Tandem PROM—the first stage bitstream programs the FPGA from a memory device to allow the PCIe functionality to be available quickly. However, with Tandem PCIe, the second stage BIN file is downloaded over the PCIe link and uses the Internal Configuration Access Port (ICAP) hardware in the FPGA for configuration through logic provided by the *7 Series Integrated Block for PCI Express* IP. This requires a software driver which loads the second stage BIN file over the PCIe link. Note that Tandem PCIe uses a BIN file for second stage instead of a BIT file. The BIN file is properly aligned for use with ICAP.

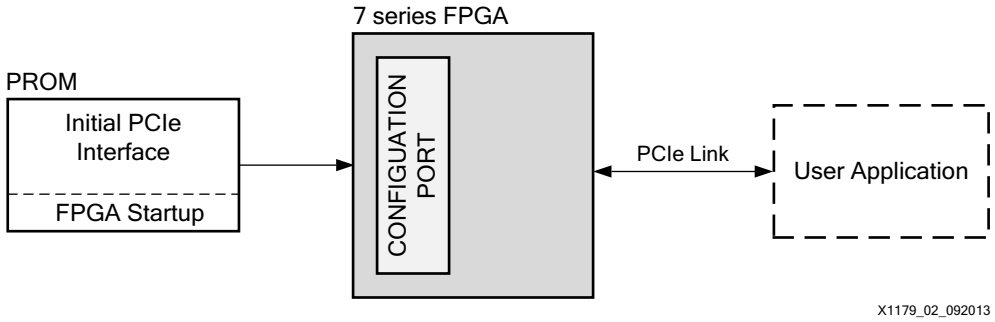

Figure 2: **Tandem PCIe Method**

The *7 Series Integrated Block for PCI Express* IP provides additional logic required for Tandem Configuration:

- Multiplexing for critical PCIe block inputs to disable them during the second stage configuration process.
- Tandem completer to handle additional memory reads and vendor defined messages possibly received during enumeration. These transaction layer packets (TLPs) are not processed within the *7 Series Integrated Block for PCI Express* IP.
- User handshake logic to indicate completion of stage 2 configuration. The handshake passes on the control of PCIe block ports to the user application residing in the second stage.

Descriptions of these logic blocks can be found in *7 Series FPGAs Integrated Block for PCI Express User Guide* (PG054) [Ref 2].

Enabling Tandem Configuration in the Kintex-7 Connectivity TRD

This section describes the modifications needed to support Tandem Configuration flow in the Kintex-7 Connectivity TRD.

Figure 3 shows the TRD with Tandem Configuration. The *7 Series Integrated Block for PCI Express* IP is generated for each configuration method (Tandem PROM and Tandem PCIe) and the IP internally adds the required logic listed here for Tandem Configuration:

- **Tandem PROM:** Includes isolation multiplexers, tandem completer, and handshake logic to establish completion of stage 2 configuration.
- **Tandem PCIe:** Includes ICAP for configuring the second stage, isolation multiplexers, tandem completer, and handshake logic to establish completion of stage 2 configuration. Tandem PCIe additionally requires a driver to download the second stage BIN file over PCIe link.

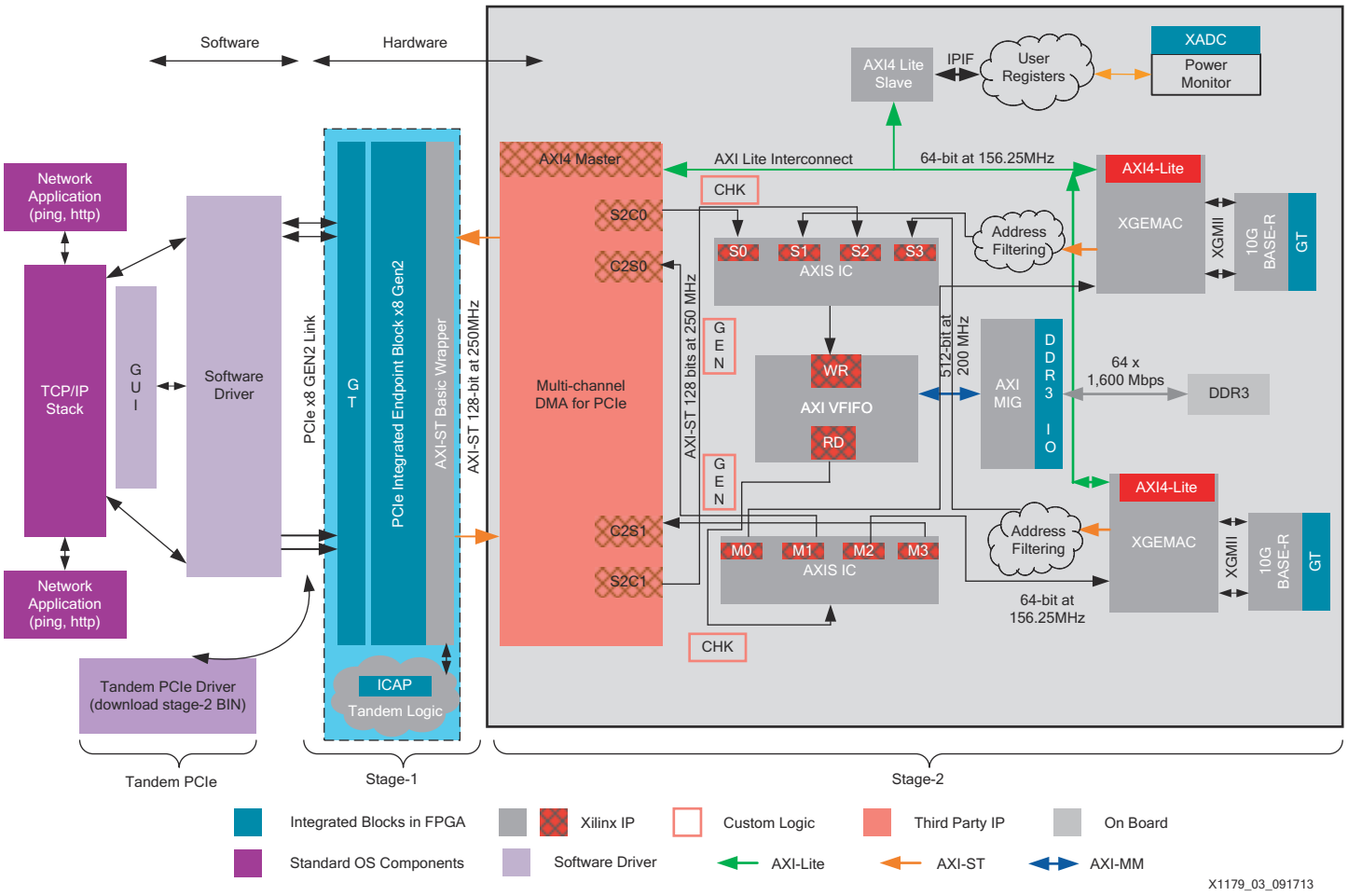

Figure 3: **Kintex-7 Connectivity TRD using Tandem Configuration**

The design associated with this application note has a macro named USE_TANDEM_FLOW to identify the changes needed for tandem flow.

For Tandem PCIe flow, an additional BUFG is included to provide a clock for ICAP. This is included under the USE_TANDEM_PCIE macro in the design top level file (`k7_connectivity_trd.v`). In addition, these adjustments have been made to the TRD to accommodate Tandem Configuration:

- **Design Updates:** For the tandem flow, the entire I/O bank where PERST# (a system-provided reset from the PCIe slot) resides is configured as part of the first stage bitstream. In the top-level, non-tandem design, user application blocks like MIG, 10G Ethernet MAC and 10GBASE-R, etc., are reset using PERST#. Using PERST# this way implies that all that logic should be part of the first stage bitstream. However, this would increase the size of the first stage bitstream as more logic gets added due to reset propagation. Increasing the size of the first stage bitstream defeats the purpose of Tandem Configuration. To keep the first stage bitstream small, the reset logic for the user application blocks is changed to use an inverted version of registered user_lnk_up signal from the PCIe block. This is identified by use of USE_TANDEM_FLOW macro at various places in the top-level file (`k7_connectivity_trd.v`).
- **IP Generation Updates:** *7 Series Integrated Block for PCI Express* IP generation for the TRD is changed to enable the Tandem PROM and Tandem PCIe flows. Relevant XCI files are available under the `ip_catalog` directory). The rest of the IP configuration remains the same as a non-tandem flow.

- **Constraint Updates:** Includes two constraint updates:
  1. The `k7_conn_pcie.xdc` file is modified to include the tandem-specific constraints that are provided by the *7 Series Integrated Block for PCI Express* IP. These are chosen from the example design XDC file provided in the IP.

     Note: In the tandem flow, the IP-provided constraints for Tandem PROM and the Tandem PCIe are the same.
  2. `k7_conn_pcie_tandem.xdc` includes tandem-specific constraints for PCIe. `k7_conn_trd_tpcie.xdc and k7_conn_trd_tprom.xdc` include additional constraints to target BPI flash for each of the Tandem Configuration flows.

The rest of the flow remains the same as running a non-tandem design through the Vivado GUI. The *7 Series Integrated Block for PCI Express* IP provides tcl files (`build_stage1.tcl` and `create_bitstreams.tcl`) that take care of setting up the tool flow for the appropriate tandem option. The XDC file shipped with the design (`k7_conn_trd_tpcie.xdc` or `k7_conn_trd_tprom.xdc`) by default sets up bitstream generation options for BPI flash memory.

Bitstream compression has been enabled by default by setting this property:

set_property bitstream.general.compress true [current_design]

To generate separate bitstreams for Tandem PROM (for testing purposes), set this property:

set_property bitstream.config.tandem_writebitstream separate [current_design]
write_bitstream -force separate.bit

This generates separate stage 1 and stage 2 bitstreams for Tandem PROM. By default, the Tandem PROM flow generates a single BIT file which includes both stages. The Tandem PCIe flow by default generates separate BIT and BIN files for stage 1 and stage 2, respectively.

Note: The bitstream configuration Tcl commands provided above can be made part of the design TCL file or can be executed on the Vivado Design Suite Tcl console.

Finally, **promgen** is used to generate the MCS file from the BIT file thus obtained.

Testing the Tandem Solution

The setup procedures described in Chapter 2 of the *Kintex-7 FPGA Connectivity Targeted Reference Design User Guide* (UG927) [Ref 3] must be performed before testing the Tandem solution described in Tandem PROM Testing and Tandem PCIe Testing.

Tandem PROM Testing

To test the Tandem PROM solution:

1. Program the BPI flash memory on the KC705 evaluation board with the MCS file generated from the unified BIT file from the Tandem PROM flow.
2. Program the FPGA through the BPI flash memory.
3. Boot the host PC and the with the KC705 board plugged into a PCIe slot.
4. Verify the Kintex-7 Connectivity TRD is recognized by confirming the **`lspci`** command output returns device ID 7082.
5. Test the Connectivity TRD and driver functionality as described in chapter 2 of the *Kintex-7 FPGA Connectivity Targeted Reference Design User Guide* (UG927) [Ref 3].

To confirm that the Tandem PROM flow is working, testing can be performed using a separate BIT file as described here:

1. The BIT file size for stage 1 will be much smaller than the BIT file size for stage 2.
2. Separate stage testing via JTAG:
   a. Download only the stage 1 BIT file using the Chipscope or iMPACT tool.

b. Let the system boot and check if the Xilinx endpoint card is recognized (`device ID = 7082` for TRD) through **`lspci`** command.

Note: Do not try to run the TRD GUI at this point. It will cause DMA engine discovery to fail because the second stage has not been configured yet.

c. When the FPGA is recognized, download the stage 2 bitstream while the system remains booted.

d. Continue further testing with the TRD application without rebooting system.

Tandem PCIe Testing

1. Program the BPI flash memory on the KC705 evaluation board with the stage 1 BIT file.
2. Program the FPGA through the BPI flash memory.
3. Boot the host PC and the with the KC705 board plugged into a PCIe slot.
4. Verify the Kintex-7 Connectivity TRD is recognized by confirming the **`lspci`** command output returns device ID 7082.

   Note: Do not try to run the TRD GUI at this point, it will cause the DMA engine discovery to fail as the second stage has not been configured yet.
5. Use the Tandem PCIe driver and application available from AR#51950 to load the second stage BIN file (note that second stage should use the BIN file and not the BIT file):
   a. Modify the `tpcieSwRelease/common/Xilinx_fpc_constants.h` file to match the design device ID (7082 for this TRD).
   b. Follow instructions provided as part of the answer record.

   Note: The Tandem PCIe driver is shipped as part of the design ZIP file with changes to the device ID to target the TRD stage 1 bitstream.
6. Verify that the device is still recognized. Remove this driver and continue further testing with TRD drivers.

Bit File Size and Programming Time Estimate

The exact bitstream size is reported in the log when **`write_bitstream`** is run.

The size of the stage 1 bitstream will vary based on a number of factors, including device, design density, tandem variant, reset pin location, and compression. The typical size range is 15–20% of the full bitstream size.

Table 1 shows the programming time estimate and bitstream sizes for Tandem PROM, Tandem PCIe, and flat (non-tandem) configuration methods.

Table 1: **Bitstream Sizes and Programming Time Estimates**

Configuration Method	Bitstream Compression	Bitstream Size (Mb)			Programming Time (ms)[1]		
		Total (Mb)	Stage One (Mb)	Stage Two (Mb)	Quad SPI Memory at 66 MHz	BPI x 16 Flash Memory at 50 MHz	BPI x 16 Flash Memory at 33 MHz[2]
Tandem PROM	No	91.2	17.6	73.6	66.9	22.1	33.4
	Yes	63.4	13.5	49.9	51.2	16.9	25.6
Tandem PCIe	No	N/A	23.3	67.7	88.1	29.1	44.1
	Yes	N/A	18.2	43.7	68.9	22.7	34.4
Flat (non-tandem)	No	87.3	N/A	N/A	330.7	109.1	165.3
	Yes	59.0	N/A	N/A	223.4	73.7	111.7

Notes:
1. Does not include T_{POR}.
2. Supported on the KC705 evaluation board.

Assuming T_{POR} = 50 ms, it can be seen in Table 1 that for programming from the Quad SPI memory at 66 MHz, Tandem PROM and Tandem PCIe meet the 120 ms requirement. Note that compression improvements will vary from design to design, so additional overhead should be considered when planning bitstream storage and configuration time needs. Configuration using BPI flash memory with a 33 MHz clock is enabled by default in the design for the KC705 board.

Conclusion

The Tandem Configuration approach from Xilinx is a practical solution to reduce FPGA configuration time to meet the 120 ms PCIe link training requirement. This design demonstrates use of tandem methodology in the Kintex-7 Connectivity TRD and describes the adjustments made to the TRD to accommodate Tandem Configuration. Using the this approach, the base bitstream size, and therefore the initial configuration time, is reduced by more than 85% when using Tandem PROM, and more than 80% when using Tandem PCIe. With these reduced bitstream sizes, the fast configuration requirements for PCI Express enumeration can be met using Quad SPI flash memory or BPI flash memory with a 16-bit datapath. Tandem PCIe usage also allows designers to move to smaller boot flash devices, lowering BOM costs.

Using the Tandem Configuration methods, the time duration between power good (V_{ADJ}) and stage 1 DONE assertion was measured on the KC705 evaluation board using an oscilloscope. The measured configuration time when using Tandem PROM and BPI Flash memory with a16-bit datapath at 33 MHz was 52 ms, which included 27 ms of T_{POR} and 25 ms of configuration time. The measured configuration time when using Tandem PCIe under the same conditions was 62 ms, which included 28 ms of T_{POR} and 34 ms of configuration time. These measurements confirm that using Master BPI configuration mode with synchronous read at 33 MHz with Tandem Configuration meets the 120 ms time requirement for PCIe endpoints.

References

The documents listed here are referenced in this application note:

1. *7 Series FPGAs Configuration User Guide* (UG470)
2. *7 Series FPGAs Integrated Block for PCI Express User Guide* (PG054)
3. *Kintex-7 Connectivity Targeted Reference Design User Guide* (UG927)

Reference Design

The design ZIP file can be downloaded at:

https://secure.xilinx.com/webreg/clickthrough.do?cid=351633

Note: The readme file provided with the design ZIP file details the contents of the design ZIP file.

Table 2 shows the reference design checklist.

Table 2: **Reference Design Checklist**

Parameter	Description
General	
Developer Name	Xilinx
Target Devices	Kintex-7 FPGA XC7K325T-2FFG900
Source code provided	Yes
Source code format	Verilog, C
Design uses code and IP from existing Xilinx	
application note and reference designs,	
CORE Generator software, or third party	Yes

Table 2: **Reference Design Checklist *(Cont'd)***

Parameter	Description
Simulation	
Functional Simulation Performed	No
Timing simulation performed	No
Test bench used for functional and timing	
simulations	No
Test bench format	N/A
Simulator software/version used	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/version used	Vivado Design Suite version 2013.3
Implementation software tools/versions used	Vivado Design Suite version 2013.3
Static timing analysis performed	No
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	KC705 Evaluation Board

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
10/25/13	1.0	Initial Xilinx release.

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