2021 Xilinx Security Working Group (XSWG) EMEA

Day 1

Monday, December 6, 2021	
All times in Central Europe Time (CET)	
Topic	**Time**
Welcome and Introductions	1:00pm - 1:15
Versal Security Features	1:15 -2:15
Break	2:15 - 2:30
Versal Asymmetric HWRoT Secure Boot	2:30 - 3:30
Versal Symmetric HWRoT Secure Boot	3:30 - 4:30
Break	4:30 - 4:45
Versal External Secure Storage	4:45 - 5:15
Versal Isolation/Access Controls	5:15 - 6:00

2021 Xilinx Security Working Group (XSWG) EMEA

Day 2

Tuesday, December 7, 2021	
All times in Central Europe Time (CET)	
Topic	**Time**
Versal Glitch Detector Characterization	1:00pm - 1:45
Versal Secure HW Characterization	1:45 - 2:45
Break	2:45 - 3:00
Versal Readiness and Roadmap	3:00 - 4:00
Versal AHWRoT Lab Demo	4:00 - 5:00
Break	5:00 - 5:15
Versal SHWRoT Lab Demo	5:15 - 6:15

2021 Xilinx Security Working Group (XSWG) EMEA

Day 3

Wednesday, December 8, 2021	
All times in Central Europe Time (CET)	
Topic	**Time**
Versal Authenticated JTAG Lab Demo	1:00pm - 1:45
Versal eFUSE-Enabled Fault Mitigation Features Lab Demo	1:45 - 2:30
Break	2:30 - 2:45
Zynq UltraScale+	2:45 - 3:45
Future Products Roadmap	3:45 - 4:45
Break	4:45 - 5:00
Attacking Semiconductor Devices	5:00 - 6:00

2021 Xilinx Security Working Group (XSWG) EMEA

Day 4

Thursday, December 9, 2021	
All times in Central Europe Time (CET)	
Topic	**Time**
Automotive Security (ISO21434 and J3101)	1:00pm - 2:00
Zynq UltraScale+ HSM IP	2:00 - 2:45
Break	2:45 - 3:00
Industrial/SOM Security	3:00 - 3:45
DataCenter Security	3:45 - 4:45
Break	4:45 - 5:00
Guidance on Essential Security Resources / Information	5:00 - 6:15