2021 Xilinx Security Working Group (XSWG) North America

Day 1

Monday, November 8, 2021	
All times in Mountain Standard Time	
Topic	**Time**
Welcome and Introductions	8:00am - 8:15
Versal Security Features	8:15 - 9:15
Break	9:15 - 9:30
Versal Asymmetric HWRoT Secure Boot	9:30 - 10:30
Versal Symmetric HWRoT Secure Boot	10:30 - 11:30
Lunch	11:30 - 12:30
Versal External Secure Storage	12:30pm - 1:00
Versal Isolation/Access Controls	1:00 - 1:45
Break	1:45 - 2:00
Versal Glitch Detector Characterization	2:00 - 2:45
Versal Secure HW Characterization	2:45 - 3:45

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Day 2

Tuesday, November 9, 2021	
All times in Mountain Standard Time	
Topic	**Time**
Versal Readiness and Roadmap	8:00am - 9:00
Versal AHWRoT Lab Demo	9:00 - 10:00
Break	10:00 - 10:15
Versal SHWRoT Lab Demo	10:15 - 11:15
Versal Authenticated JTAG Lab Demo	11:15 - 12:00
Lunch	12:00pm - 1:00
Versal eFUSE-Enabled Fault Mitigation Features Lab Demo	1:00 - 1:45
Zynq UltraScale+	1:45 - 2:45
Break	2:45 - 3:00
Future Products Roadmap	3:00 - 4:00

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Day 3

Wednesday, November 10, 2021	
All times in Mountain Standard Time	
Topic	**Time**
Attacking Semiconductor Devices	8:00am - 9:00
Supply Chain Security	9:00 - 10:00
Break	10:00 - 10:15
Automotive Security (ISO21434 and J3101)	10:15 - 11:15
Zynq UltraScale+ HSM IP	11:15 - 12:00
Lunch	12:00pm - 1:00
Industrial/SOM Security	1:00 - 1:45
DataCenter Security	1:45 - 2:45
Break	2:45 - 3:00
Guidance on Essential Security Resources / Information	3:00 - 4:15