SOLUTION BRIEF

ACCELERATING FINITE ELEMENT METHOD WITH THE ALVEO™ U55C CARD

INTRODUCTION

The finite element method (FEM), like all sparse matrix computation requires a great deal of data access. This requirement makes CPU memory architectures less than optimal for sparse matrix solving.

CPU caches are small and matrix queries often lack enough relevant results to maintain throughput. This results in wasted clock cycles accessing data from system memory, and causes under-utilization of CPU cores leading to performance degradation.

Xilinx Alveo U55C accelerator cards allow developers to design data pipelines where every data manipulation necessary to maintain momentum when moving from one function or block to another is accounted for, and data movement is limited. Data can flow without constant reads and writes to onboard memory. This functionally results in more work per clock cycle in an Alveo pipeline in contrast to smaller jobs across many cores in CPU (and GPU) architectures.

CPU Inefficiencies for Sparse Matrix

- x86 architectures aren't equipped to provide the high I/O and bandwidth required
- CPU memory hierarchies are inflexible and create unnecessary overhead
- x86 architectures are inherently inefficient at handling data movement

THE ALVEO U55C CARD ADVANTAGE

Built from the ground up to deliver the best performance-per-watt for HPC and Big Data workloads, the Alveo™ U55C accelerator card delivers the efficiency and scalability called for by the most demanding applications. The U55C delivers:

- High-performance, low power HBM
- Lowest performance per watt
- Fast and easy clustering

The U55C harnesses the power of Xilinx Adaptive Computing to deliver extraordinary performance unmatched by competing architectures, with:

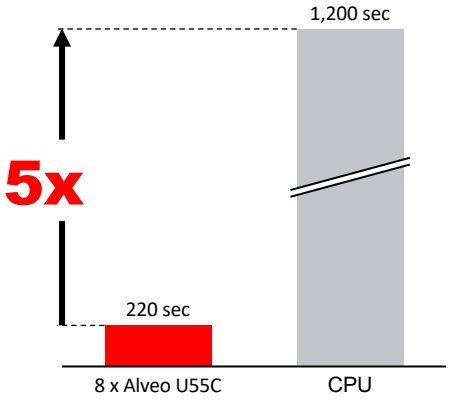
- Data pipeline hyperparallelism
- Superior memory management
- Optimized data movement

U55C HYPERPARALLEL DATA PIPELINING FOR LS-DYNA

LS-DYNA from ANSYS is a general-purpose finite element program capable of simulating complex real-world problems. LS-DYNA allows designers and engineers the ability to create simulations with an infinite amount of complexity.

LS-DYNA solvers underpinning simulation represent 90% of LS-DYNA run times. Ansys tapped into Xilinx's scale-out fabric and non-hierarchical memory structure to partition workloads across multiple Alveo U55C cards to achieve 5x better performance vs. CPU.

LS-DYNA Workload Partitioned Across Multiple Alveo U55C Cards in a Large Scale Simulation Test



Dimensions of matrix -> 12M
nnzs: *No of non-zero elements -900M*
Time in secs*: JPCG solver equation runtime*
CPU model: *Intel Xeon CPU E5-2665 @2.4GHz, 8C/16T, single thread, 32GB memory*
One U55C card *-> 1.5M equations*

- Data is pipelined to simply stream between functions
- Data is prepared in transit to achieve maximum throughput
- Highly composable memory hierarchies
  - HBM2 memory, 32 HBM channels @ 460GB/s

TAKE THE NEXT STEP

Learn more about the Alveo U55C data center accelerator card > www.xilinx.com/AlveoU55C

Corporate Headquarters
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Europe
Xilinx Europe
Bianconi Avenue
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan
Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.
Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

India
Xilinx India Technology
Services Pvt. Ltd.
Block A, B & C, 8th, 12th and 13th Floors,
Meenakshi Tech Park, Survey No. 39,
Gachibowli (V), Serilingampally (M),
Hyderabad – 500 084 India
Tel: +91-40-6721-4747
www.xilinx.com

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