PRODUCT BRIEF

Virtex UltraScale+ VU23P FPGA

OVERVIEW

The Virtex® UltraScale+™ VU23P FPGA brings a new optimization point to the UltraScale+ FPGA portfolio, delivering breakthrough performance for networking and storage applications. The Virtex UltraScale+ VU23P FPGA offers the highest ratio of look-up tables[1] (LUTs) and block RAM to DSP slices in an UltraScale+ FPGA along with package options as small as 35mmx35mm. This unique mix of resources enables efficient packet processing and scalable data bandwidth to deliver unparalleled performance for networking and storage applications.

The Virtex UltraScale+ VU23P FPGA is also the first UltraScale+ FPGA to provide both 58G PAM4 transceivers and PCIe® Gen4 combined. These high-performance interfaces provide scalable connectivity and high I/O bandwidth in a device that's right-sized for server deployment.

Built on the proven UltraScale™ architecture, the Virtex UltraScale+ VU23P FPGA allows users to move quickly to production. With mature development tools and frameworks, system designers reduce the development cycle, and deliver new solutions to the marketer faster than ever.

HIGHLIGHTS

Optimized Resources for Adaptable Networking and Storage Acceleration

- Highest ratio of LUTs[1] and block RAM to DSP slices in Virtex UltraScale+ FPGAs
- Maximize packet processing throughput per port with adaptability
- Scale data bandwidth within a fixed power envelope

Unique Mix of 58G PAM4 SerDes and PCIe Gen4

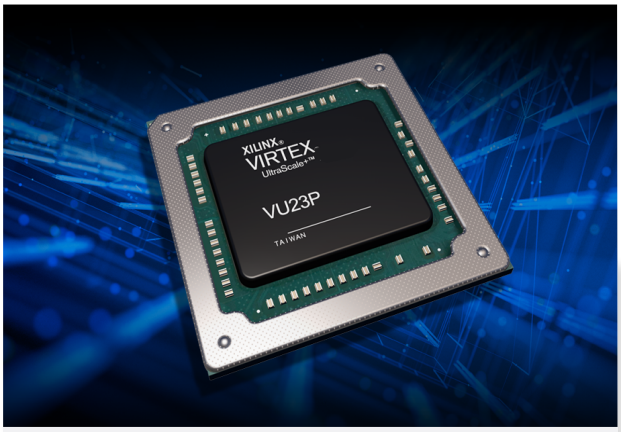
- Integrated blocks for PCIe Gen4 for maximum bandwidth with low latency
- 58Gb/s PAM4 transceivers for up to 200G SmartNIC and edge network systems
- 34 transceivers operating at 32.75Gb/s for 10/25G interoperability
- Integrated 100G Ethernet MAC with KR4-FEC for built-in error correction

Right-Sized Packaging for Server Deployment

- Compact package options as small as 35mmx35mm
- Flexibility to support a broad range of standard server form factors

Proven HW/SW Platform to Accelerate Time to Market

- Co-optimized with Vivado® Design Suite with IP integration
- Comprehensive solution stacks enabled by Vitis™ unified software platform



TARGET APPLICATIONS

Network Acceleration

- Full OVS Offload Acceleration
- Network Security Acceleration
- SmartNIC

Storage Acceleration

- NVMe-oF Acceleration
- Flash Storage Controller
- Bare-metal Cloud Storage Acceleration

Wired Communications

- Converged Access Fronthaul
- Fronthaul Gateway Acceleration
- PON Access

Adaptable. Intelligent.

1. Highest ratio of LUT and BRAM to DSP slices in the Virtex UltraScale+ Portfolio, excluding the Virtex UltraScale+ VU19P FPGA

FEATURE	DESCRIPTION
16nm low power FinFET+ process technologyfrom TSMC	> Industry-leading process from the #1 service foundry delivers a step function increase in performance-per-watt > The same scalable architecture and tools as 20nm UltraScale™ FPGAs
Broad Range of SerDes Rates	> 28G and 58G backplane support > 32.75G and 58G chip-to-chip and chip-to-optics support > High-density I/O for smaller area and greater power efficiency per pin
Integrated 100G Ethernet MAC with KP4-FEC	> Saves 60K–100K system logic cells per port > Up to 90% dynamic power savings vs. soft implementation > Built-in KR4-FEC (Ethernet MAC) for optics error correction > Optional built-in KP4-FEC for PAM4 optics and backplanes
Integrated blocks for PCI Express® with cache coherent CCIX ports	> Complete end-to-end solution to support multiple 100G ports > PCIe Gen4 x8 and Gen3 x16 for up to 16GB/s bandwidth > Expanded virtualization for data center applications > Acceleration for cache coherent compute using CCIX ports
On-Chip Memory for deep memory buffering	> 79Mb Block RAM for deep FIFO and granular memory usage > 99Mb on-chip UltraRAM for SRAM device integration
Massive memory interface bandwidth	> DDR4 support of up to 2,666Mb/s > Support for server-class DIMMs
UltraScale architecture enhanced clocking and routing	> Lower skew, faster performing clock networks > Up to one speed grade advantage vs. comparable solutions > Efficient CLB use and placement for reduced interconnect delay

TAKE THE NEXT STEP

For more information about the Xilinx Virtex UltraScale+ VU23P FPGA, visit www.xilinx.com/vu23p

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