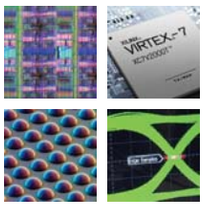


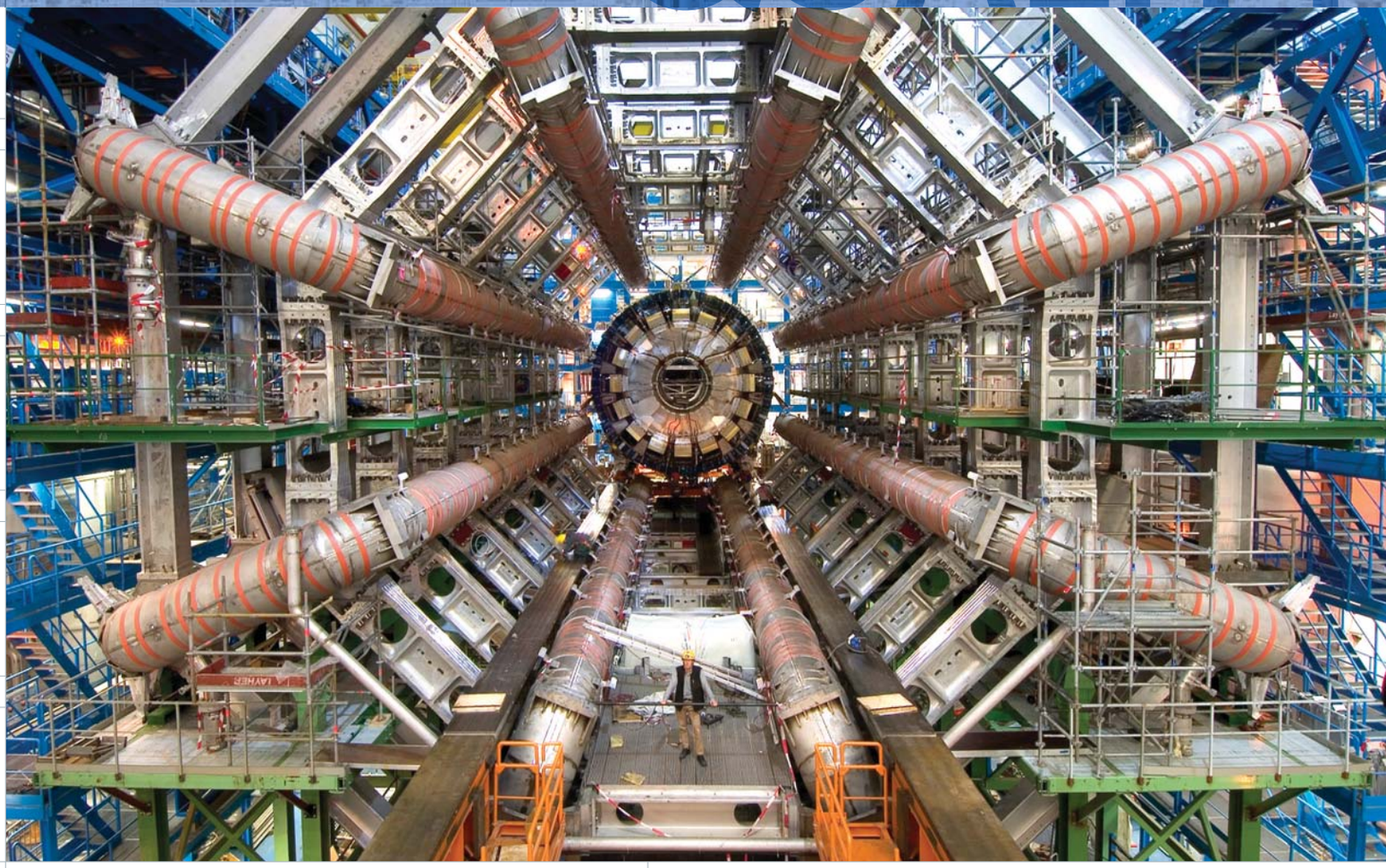




2011 QUALITY REPORT

ENGINEERING QUALITY



XILINX®

ABOUT OUR COVER:

FIELD-PROGRAMMABLE GATE ARRAYS HAVE COME A LONG WAY—TODAY THEY HELP ENGINEERS TACKLE SOME OF THE WORLD'S BIGGEST CHALLENGES. THE COVER DESIGN SHOWS JUST ONE EXAMPLE OF FPGA-POWERED ENGINEERING, THE LARGE HADRON COLLIDER, A PARTICLE ACCELERATOR BUILT AND OPERATED BY CERN, THE EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH. ONE OF THE MOST RESPECTED CENTERS FOR SCIENTIFIC STUDY, CERN RELIES ON THE QUALITY AND TECHNOLOGY OF XILINX SOLUTIONS TO EXPLORE THE PHYSICAL BEHAVIOR OF FUNDAMENTAL PARTICLES THAT MAKE UP ALL MATTER.

Engineering Quality

Engineering quality—it is what we create and how we create it. In the field of physics, the law of entropy explains how energy tends towards chaos. We believe that quality will similarly deteriorate without ongoing effort. So we invest our time, energy, and knowledge to engineer continuous quality advancements. We also drive breakthroughs by listening to our customers and using real-world needs and feedback to adjust ongoing strategies, guide execution, and achieve results our customers have come to expect.

Each year we share the results of our most recent efforts.

In 2011, more than any other year, we saw our investments pay off in the form of milestone achievements like the Xilinx® Virtex®-7 2000T and Zynq™-7000 families. We have transformed ourselves from a supplier of FPGAs to a programmable solutions provider, giving customers a new level of value. Our Targeted Design Platforms are coming to life—making FPGA solutions easier to use, powerful enough for the biggest engineering challenges, and truly ubiquitous in the industry. Xilinx quality has contributed to these achievements with programs that are focused on the following areas:

- **Foundations.** Greater predictability and standardization using a scalable optimized architecture and 28nm foundry process have resulted in accelerated product development.
- **Complexity.** Repeatable development processes, improved over three product generations, have allowed us to pioneer and ship the world's first stacked-silicon interconnect devices and ARM-based processing platform.
- **Solutions.** Consistent, corporate-wide quality methodologies are elevating next-generation design tools and simultaneously improving current tool releases.
- **Innovation.** Rigorous verification and industry standards are enabling plug-and-play, innovation-accelerating IP from Xilinx and third parties.
- **Processes.** Customer feedback and multilevel collaboration with our ecosystem partners are elevating the value we deliver to systems and businesses.
- **Overall quality.** Tools that increase visibility and reduce human error allow us to meet customer expectations and address issues sooner.

We are proud of what we have achieved and look forward to sharing with you the innovation and product leadership that are the direct results of engineering quality.

Moshe Gavrielov
President & CEO
Xilinx, Inc.

Vincent Tong
Senior Vice President, Quality & New Product Introductions
Xilinx, Inc.
Board of Directors, Global Semiconductor Alliance

LESS IS MORE—an adage that is reflected in the latest generation of Xilinx programmable devices. A single architecture has harmonized the 7 series FPGA families and created a roadmap that fosters design reuse, solution portability, and increased developer productivity. Along with a single 28nm process, the scalable optimized architecture streamlines product development and allows more predictable product results and shorter time to market.

ENGINEERING Foundations

ARCHITECTURE AND FABRICATION

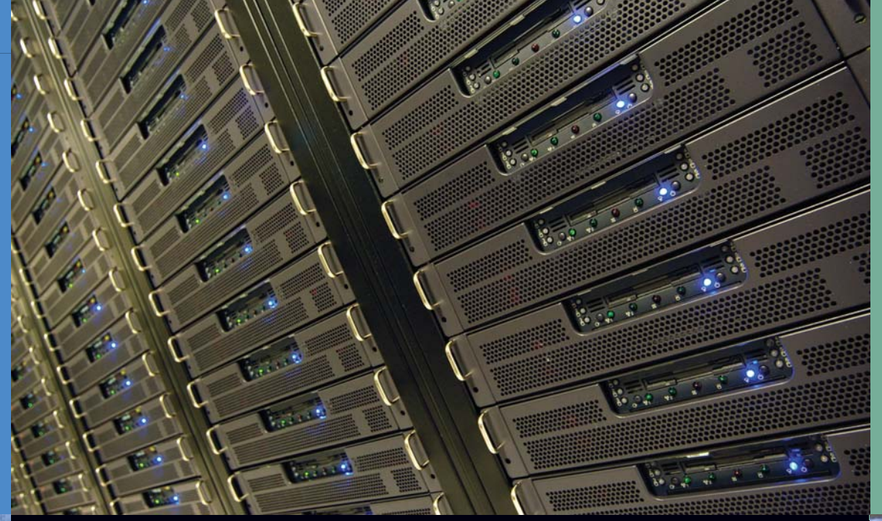
Scalable Optimized Architecture: One Vision, One Organization

Xilinx's use of a scalable optimized architecture allowed a single merged engineering team to launch all three 7 series families (28nm). With 90% of the fabric, logic, and I/O in common, Xilinx brought to market a broad range of silicon features in just 15 months (down from 18 months for the complete rollout of 6 series devices). The scalable optimized architecture allows for parallel product learning during engineering sampling, avoids late-in-cycle product adjustments, and lets Xilinx—and our customers—respond quickly to dynamic market opportunities.

The Scalable optimized architecture has simplified development and learning, and is leveraged across multiple families for higher-quality products. The common architecture facilitates development of silicon, design tools, and intellectual property (IP) for stronger Targeted Design Platforms and promoting the growth of a healthy ecosystem.

28nm: One Partner, One Process

The High-Performance Low-power (HPL) process at TSMC was pioneered in partnership with Xilinx and allowed Xilinx to ship the industry's first 28nm devices in 2011. Long before customers saw a single 28nm device, Xilinx invested years of effort using Process and Performance Learning Vehicles (PPLVs) to improve the quality of processes, materials, and techniques. Besides leveraged learning, Xilinx introduced tighter controls and improved alignment with a single foundry and process. As a result, we achieved robust wafer-level reliability (WLR) and lower defect densities for reduced excursion rates. Currently, the Xilinx 28nm yield results have exceeded 40nm benchmarks, met production milestones, and achieved power reductions of greater than 50% compared with previous generations.



> ZTE has achieved enviable revenue growth in the extremely competitive telecommunications and networking market by taking a leading role in standardization and partnering with vendors that align with our focus on ultra-high-speed wired and wireless products. Xilinx (2011 Best Comprehensive Award winner) has continued to score above nine on ZTE's performance scorecard and is providing a 98 percent on-time first commitment delivery.
>
> LESLIE ZHONG
> *Director of Strategic Supplier Management*
> ZTE CORP.

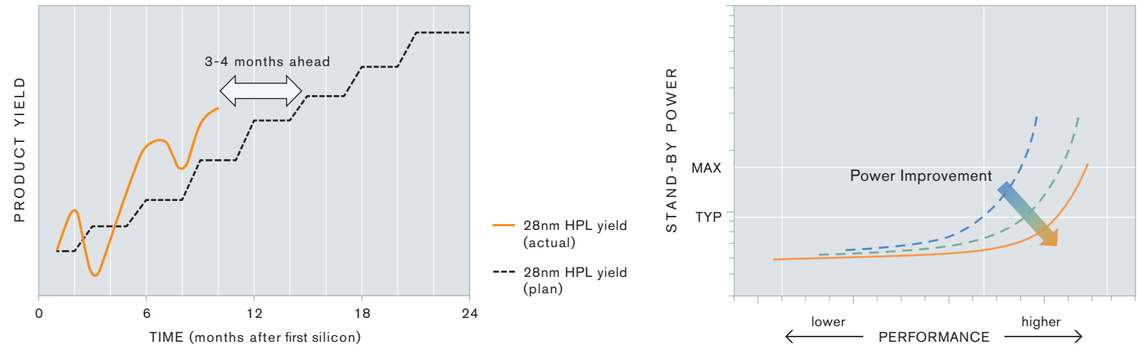
WIRED: ENGINEERING HIGHER BANDWIDTH

In the field of wired communications, designers are pushing the limits on the road to higher-bandwidth networks. Xilinx is smoothing the way with a 100G OTN platform that addresses faster market implementations of 100G line cards, and **leverages a scalable optimized architecture to let developers get started on 400G designs today.**

The Virtex-6 HXT FPGA ML630 Evaluation Kit for OTN was included in the *EDN Hot 100 Products of 2011* list. Based on the industry's first optically compliant device, the kit enables next-generation transponder, muxponder, and ODU switching applications.

Last year's launch of the Xilinx OTN platform illustrates the envisioned benefits that drove Xilinx to adopt a scalable optimized architecture. By letting engineers get started with one device family, and later move to another when it becomes available, Xilinx makes it possible to have a design ready when the silicon ships.

DRIVING TSMC PROCESS IMPROVEMENT



In 2011, Xilinx was the first in the industry to tape out 28nm. Since then, the 7 series devices have exemplified the resulting HPL process benefits for customers, including lower power and higher yields.

SEMICONDUCTOR QUALITY starts and ends with excursion prevention. In 2011, Xilinx New Product Evaluation (NPE) and New Product Introduction (NPI) advancements brought to market much more complex devices without wavering in the quest for Zero Defects. The improvements allow more rapid delivery of devices that perform to specifications, give customers early access to higher-density packaging (stacked-silicon interconnect devices), and provide a roadmap to embedded processor platforms.

> We continually push ourselves to increase our value-add while maintaining high quality for fast-moving markets like wireless communications. This segment sets a high bar due to insatiable demand for bandwidth, the programmable imperative, and multiple evolving standards. Our 28nm leadership and design win momentum in wireless is the result of our leadership performance, power, and cost and our ability to improve quality even in the face of greater design and technology complexity.
>
> VICTOR PENG
> *SVP, Programmable Platforms Development*
> XILINX, INC.

ENGINEERING Complexity

SILICON DEVICES

Zero Defect Mindset

At Xilinx, excursion prevention is treated as more than a "wafer fabrication issue." It begins with design. Xilinx quality is driven by the next wave of innovations through efforts such as design for test (DFT), design for reliability (DFR), design for manufacturing (DFM), mitigations for single-event upset (SEU), and the consistency provided by a scalable optimized architecture. This drive has resulted in a "shift to the left" such that risks are reduced by earlier verification.

The scalable optimized architecture efficiencies, a single 28nm process, and related NPE/NPI enhancements add up to faster customer access to 7 series devices that perform to specifications. For example, the first Virtex-7 X485T devices showed 12.5-Gbps transmit performance within 36 hours of first silicon, without any optimization—which puts the 7 series on track for delivering 28G.

Quality Integration

Predictable integration is resulting in Xilinx NPE/NPI methodology breakthroughs. An example of this is Xilinx achieving "more than Moore's Law" with its launch of the world's first FPGA based on stacked-silicon interconnect technology. The Virtex-7 2000T effectively delivers 20nm logic density, and shatters the industry record for programmable device density by 2X (6.8 billion transistors). The devices have passed all reliability conditions and began shipping in December 2011.

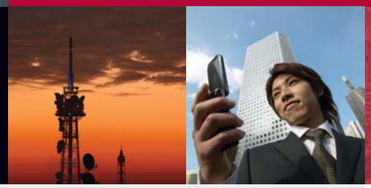
Xilinx has also announced the Zynq-7000 Embedded Processing Platform family, representing a new FPGA device class that combines FPGA and ARM in a single chip.

Because of the larger and more complex devices, Xilinx has also been extending board-level reliability methodologies, increasing testing, and expanding its 3D equipment capabilities.

7 Series Quality Milestones:

- Improved NPI sequencing, to bring the most complex verification and characterization work into the first silicon cycle, leading to higher product confidence and simpler closure prior to General Engineering Sample (ES)
- Earlier access to first silicon with over 2,000 dice, allowing extended characterization rigor whereby almost all designs were verified on first silicon
- New PPLV discoveries
- Many new tests and faster completion of test pattern development—2X corner material and 10X testing compared with the previous generation
- 3X more automated testing
- Early BRAM circuit and process verification (all patterns are functional, with solid performance margins) to extended operating specifications
- Improved generational test coverage

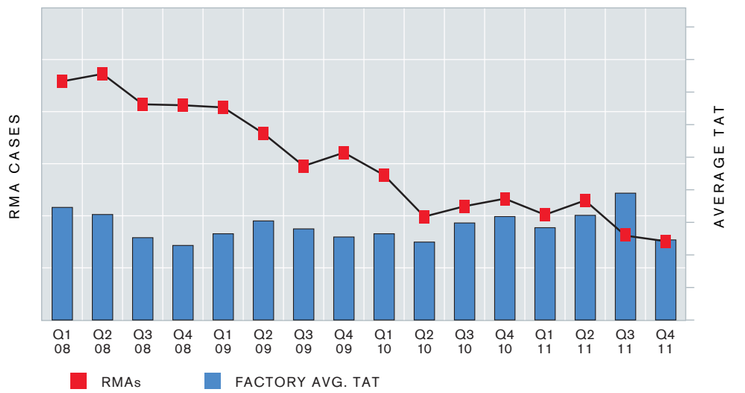
WIRELESS: ENGINEERING LOW POWER & HIGH PERFORMANCE



Wireless system integrators and solution suppliers choose Xilinx for complete platforms including silicon devices that help them reduce CapEx and OpEx while meeting the throughput and low-latency demands for high-performance networks. Xilinx quality advancements of particular interest in the wireless market in 2011 included the following:

- **Zynq** drives up integration levels, allowing applications to be designed with fewer devices and lower power for a lower overall cost. For example, an LTE radio head that required a Spartan®-6 and seven other devices (10.2W) can be implemented with a Kintex™-7 and just two other devices (6.4W) or a Zynq-7030 and a memory device (5.3W) for less than half the cost of the Spartan-6 design.
- Advancing improvements in the IP development process—validation, interoperability testing, test coverage—drive up ease of use and shorten FGPA design tasks from weeks to days.
- Xilinx acquired AutoESL, to expand its design suite with high-level synthesis that can drive up designer productivity and innovation for Xilinx silicon devices.

RMA TRENDS ARE DOWN



Xilinx RMA rates reached an all-time low in 2011 as a result of a company-wide Zero Defect mindset.

Spartan FPGA		
Product	Technology Node	PPM
Spartan-2/2E	.22µm / .18µm	0.42
Spartan-3	90nm	0.59
Spartan-3E	90nm	0.09
Spartan-3A/AN	90nm	0.96
Spartan-6	45nm	0.73

Virtex FPGA		
Product	Technology Node	PPM
Virtex/E	.25µm / .18µm	0.00
Virtex-2/2Pro	.15µm / .13µm	0.51
Virtex-4	90nm	2.08
Virtex-5	65nm	7.62
Virtex-6	40nm	2.31

Products PPM Trend CY2011

QUALITY GOES BEYOND SILICON—Xilinx design tools boost productivity by simplifying the entire design experience. Developers of the next-generation Xilinx design suite are leveraging lessons learned from silicon quality methodologies, a scalable optimized architecture, and 28nm process readiness through PPLV. As a result, Xilinx has evolved a more holistic development process that encompasses both silicon and design tools and includes more rigorous release criteria across devices and tools. Customer solutions are more thoroughly vetted, with tighter collaboration between silicon, design tools, and IP teams at every stage of development.

ENGINEERING Solutions

DESIGN TOOLS

Unifying Proven Processes

Development of the next-generation Xilinx design suite created an opportunity—and a need —for major advancements in tool quality methodologies. Armed with a new development model vision, the design and quality teams expanded beta testing, formalized more metrics, and adopted more internal tools for automating various design stages.

These quality innovations include greatly accelerated time-to-milestone sign-offs and earlier identification and resolution of issues. The improvements were made even as complexity increased, and have allowed Xilinx to introduce 4X the number of devices in roughly the same time compared with the previous generation.

Earlier Discovery

Just as the scalable optimized architecture is helping elevate silicon quality, the common logic blocks help design tool engineering and quality teams focus their efforts and streamline evaluations. The efficiencies gained are being translated into more test development, test patterns, and debugging. Test result and analysis cycles have been greatly reduced—with daily instead of bi-weekly builds multiplying the iterative cycles. Next- generation modules are reaching quality milestones earlier, with staged release for early vetting as part of the current design environment.

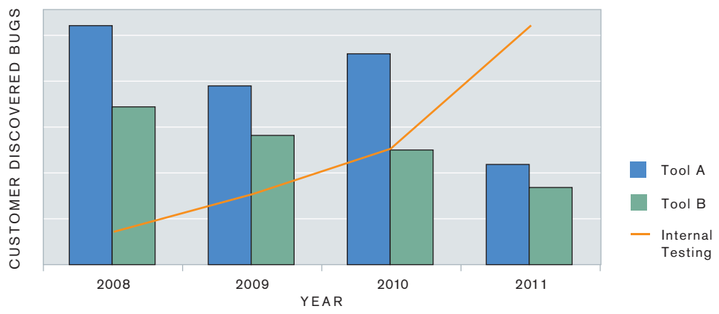
Leveraging Tools Proven to Improve Designer Experiences

- Formal verification for XST Synthesis
- Verific Parser, for maximizing language coverage
- Coverity, for static code analysis and bug reporting
- Perforce, for source control and versioning

Process Advancements that Further Boost Design Tool Quality

- Automation advancements, with best-in-class compute cloud:
  - — Massively parallel builds
  - — Capability to perform thousands of regressions per hour
  - — Faster iterative cycles, to accommodate testing of more configurations
- Stringent exit criteria for design tools, based on Zero Defect mindset
- Extensive and dynamic database of test designs (spanning a broad testing range, from individual functions to subsystems to large customer-like designs)

EARLIER DISCOVERY MINIMIZES CUSTOMER IMPACT



> Our vision was to significantly reduce the time to market for innovative embedded systems. From the start of our long-term relationship, Xilinx and NI have been extremely well aligned. Our common mindset around innovation has allowed us to do extraordinary things. We aimed to help solve amazingly difficult problems, and our customers' accomplishments are the testimony to our joint success.
>
> KEITH ODOM
> *R&D Fellow*
> NATIONAL INSTRUMENTS

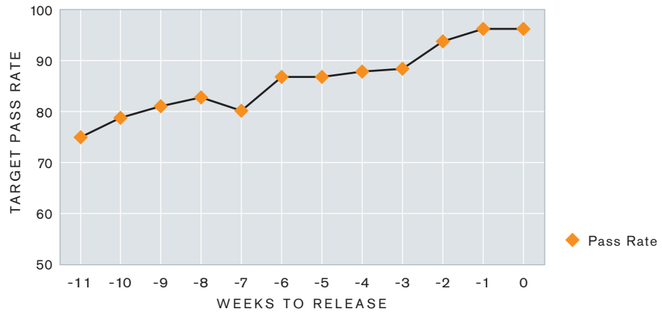
AUTOMOTIVE: ENGINEERING SAFETY AND AWARENESS

In the automotive market, quality saves lives. Auto manufacturers continue to incorporate more safety-related functions relating to driver assistance, and OEMs have consequently heightened their focus on standards for device functional safety and reliability.

Besides aligning Xilinx quality initiatives with the essential automotive industry standards and guidelines, Xilinx has pioneered Targeted Design Platforms to accelerate automotive innovations and quality design methodologies. The platforms help OEMs develop flexible designs that can be tailored to multiple automakers and quickly adjusted to track changing connectivity standards.

In 2011, the portfolio was expanded with the Xilinx Automotive platform for four-camera surround view. **Improvements in the Xilinx ISE® Design Suite gives automotive designers the tools they need and a productive environment that lets them focus on the 20% of the design that represents their differentiating value.** Besides reducing risk, Xilinx platforms simplify development and allow even first-time FPGA adopters to successfully deliver solutions to market.

CUSTOMERS EXPERIENCE FEWER DESIGN HALTS



Earlier and more stringent testing and vetting are outweighing the risks stemming from increased complexity. More issues are identified during development, to avoid impact on customers and to accelerate design cycles for higher-quality products and an improved customer experience.

CUSTOMER INNOVATION IS ACCELERATED by high-quality IP, making it a fundamental success factor. In 2011, Xilinx made it much easier for our customers to benefit from IP. The Xilinx IP development team implemented processes (the Open Verification Methodology) and adopted standards (AXI-4, IP-XACT) that allow customers easier evaluation of IP and simplified integration of IP, leading to a more predictable development environment. Targeted reference designs and Targeted Design Platforms are also speeding the development and validation of IP, helping to ensure higher-quality IP.

> By providing standards for IP interfaces, verification and certification standards and services, protection and security standards based on industry standards, and distribution standards, Xilinx is approaching an infrastructure that would enable the 'app store' model for IP.
>
> KEVIN MORRIS
> *"One for All: Does a Standards-Based IP Strategy Hurt Competition?"*
> *ELECTRONIC ENGINEERING JOURNAL*
> July 12, 2011

ENGINEERING Innovations

INTELLECTUAL PROPERTY (IP)

Process-Driven Results

One key Xilinx IP quality initiative for Plug and Play has led to the adoption of industry standards for developing and releasing IP. The initiative makes it easier for customers to incorporate Xilinx IP into systems and leverage the efficiencies gained from a scalable optimized architecture and a single set of IP interfaces. The IP team has also standardized on the Open Verification Methodology and best practices, with four well-defined levels of compliance and plans for evolving all Xilinx IP to the highest level. Through the Premier Program, Xilinx is promoting the same standards within its third-party IP ecosystem. The customer benefits of these initiatives include ease of IP integration and higher-quality IP, which lead to faster time to market.

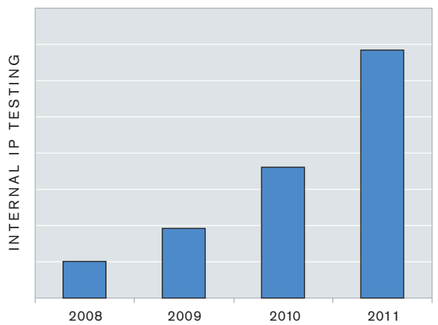
Customer-Focused Testing

In addition to the new verification methodology and practices, new quality metrics include testing and validation of Xilinx IP against more stringent criteria. Tools for tracking and reporting streamline the oversight of progress against an extensive IP development checklist. The more challenging release criteria, coupled with the automated tracking, help facilitate a 3X increase in test coverage.

Standardized, Easy-to-Use, Feature-Rich IP

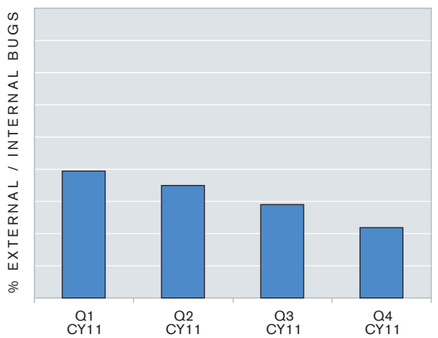
- Industry-standard interconnect: AXI-4 interface
- IP-XACT, for expressing data consistently; single IP repository
- Encryption: IEEE-1735
- Adoption of Open Verification Methodology
- More stringent release criteria
- Simulation environment improvements (C models, testbenches, example designs)

INCREASED TESTING PREVENTS CUSTOMER ISSUE DISCOVERY



Xilinx IP verification methodology tracks industry design trends. Standardization and increased testing maximize issue identification and resolution prior to application by a customer.

DRIVING FEWER PRODUCT BUGS



Even with the increase in the breadth of the IP offerings and the increased complexity of the IP, customers are encountering a lower percentage of bugs. The vast majority of issues have been discovered and resolved earlier by Xilinx teams.

BROADCAST: ENGINEERING HIGHER BANDWIDTH

The power of FPGAs is driving innovation at every point in the broadcasting landscape. **To simplify the integration of productivity-enhancing Xilinx video and imaging IP cores and third-party IP, Xilinx launched an IP plug-and-play initiative in 2011.** Xilinx quality is also helping drive down power and increase throughput:

- At the cable headend, with comprehensive testing and validation of the Xilinx EdgeQAM platform. **The integrated IP speeds the development of single-chip solutions that can simultaneously process the full upstream and downstream broadcast spectrum.**
- In the studio and at the delivery points, with platforms that are preverified for fully supporting a variety of display interfaces (e.g., triple-rate SDI, DisplayPort). The integrated IP facilitates real-time video processing for scaling, deinterlacing, 3D, calibration, and waveform generation.

ENGINEERING IS A TEAM EFFORT. Even the most talented engineers need a standardized environment that simplifies knowledge sharing, enhances coordination, and drives out inefficiencies. Recognizing this, Xilinx actively promotes repeatable methods that create productive, high-quality, cross-functional collaboration. Industry and internal measures are used to gauge organizational success. Structured product development strengthens teamwork to improve quality through design, verification, and test, and also fosters consistent company-wide processes.

ENGINEERING Processes

COLLABORATION

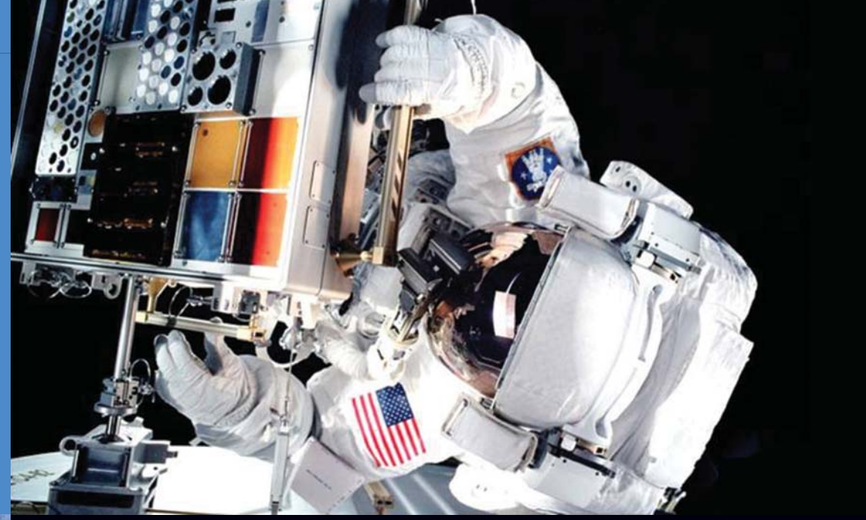
Strong Partnerships

Adoption of a scalable optimized architecture led to major organizational changes throughout Xilinx, and inherently improved collaboration by merging multiple teams. Next-generation design tools, currently under development, are also strengthening cross-functional collaboration by serving as a center of integration that spans all product families. As a result, Xilinx teams—hardware, design tools, IP, and quality—are collaborating sooner in the NPE/NPI process. In earlier stages, IP is being tested with tools, and tools tested with hardware. This shift, combined with more detailed specifications and documentation, is enhancing work flow and communication between teams.

Knowledge Management

New metrics and reporting are accelerating Xilinx collaborations by automating the transfer of learning from one group to another. To collaborate more effectively with customers and partners, Xilinx helps customer designs move forward through knowledge sharing that includes:

- **Quality Workshops—The launching of on-site workshops is helping customers apply best practices, debug more effectively, and solve issues to strengthen their understanding of Xilinx technology.**
- Premier Program—The newly formalized partner program includes a revised qualification process that categorizes partners based on their ability to streamline customers' product development cycles and reduce design risks. Premier Partners benefit from collaboration with Xilinx that ultimately drives up quality for ecosystem customers.
- Published IP Ratings—Xilinx publishes third-party IP quality and implementation metrics—a practice that leads the industry in terms of the level of transparency and promotion of quality.
- Technical Support Channels—Xilinx quality and support teams drive closed-loop learning with engineering that responds to the customers' needs. The knowledge gained through these interactions is systematically managed and used to drive online knowledge bases for customers (MySupport), technical support forums, and issue resolution.



"Tesat's customers' designs are onboard more than half of the satellites that circle Earth. This magnitude of an accomplishment requires collaboration with—and support from—a strong ecosystem of partners and suppliers. Xilinx is one of the vendors that we trust to contribute space-grade products and support to our customers' programs. In each instance, working with Xilinx has been excellent."

MARKUS KRAL
Project Manager, Parts Projects
TESAT-SPACECOM GMBH & CO. KG

SPACE:
ENGINEERING A HERITAGE OF MISSION RELIABILITY

For more than two decades, Xilinx has been contributing a broad portfolio of radiation-tolerant and radiation-hardened devices. Xilinx collaboration within the space market not only helps space agencies and contractors carry out successful missions, it also benefits all Xilinx customers with the resulting quality advancements that ripple through the entire Xilinx portfolio of devices.

Xilinx radiation-hardened technology, such as the Virtex-5QV device, has in fact been a game changer by fostering standard architectures that are more competitive and versatile. **Since testing and certifying these and other space-grade devices is complex, Xilinx formed the Xilinx Radiation Testing Consortium (XRTC). Today more than 100 members work together to produce trusted certifications.**

In February 2012, the XRTC celebrated its 10th anniversary at its annual meeting. Attendees had three days of seminars on radiation studies and demonstrations from the third-party suppliers of products that complement Xilinx hardened products.

AVIONICS:
QUALITY ADVANCEMENTS IN 2011

- DO-254 and DO-178 focus: Partnered with industry and ecosystem to provide guidance and support for certifiable SoC solutions
- Industry-leading SEU support: Regularly published SEU FIT rate data; first release of SEU failure rate calculator; SEU mitigation IP enhancement enabling >60% increase in system uptime
- Isolation Design Flow: Pioneering reusable and reliable design flows for high-reliability applications and expanding our heritage in information assurance to streamline avionics certifications

A CUSTOMER'S DESIGN and product quality is the truest measure of Xilinx quality, and does not stem from the work of a single group. At Xilinx, quality is everyone's business and the full-time focus for more than 300 employees that make up the quality teams. To harness this organizational powerhouse requires clear quality goals, objectives, and customer focus. From the board of directors to the engineering labs, Xilinx uses its performance management system to drive accountability and ownership for quality results. Customer-reported scorecards and problem resolution are studied diligently to drive world-class results.

ENGINEERING Quality

ACCOUNTABILITY

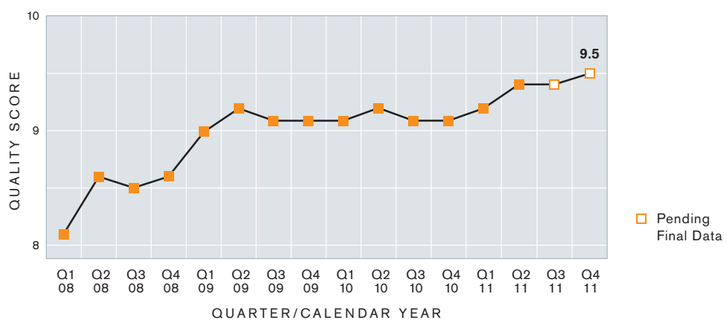
Driving Ownership

Well-understood responsibilities and goals form the beginnings of success for individuals, teams, and Xilinx as a whole. When met, these goals produce all of the components of Xilinx quality that benefit customers. In 2011, we made including more fine-grained tracking of deliverables, checklists, and schedules. **Related status reports along with clearly attached ownership resulted in improved communications and greater efficiency.**

Managing Quality

The Xilinx quality dashboard has been instrumental in taking NPE/NPI implementation to the next level. The tracking data for design tools and IP releases is organized and accessible in real time using a comprehensive dashboard. The visually intuitive displays highlight critical data for developers and quality teams, and allow rapid identification of issues. Checklists and testing information are centralized and provide easy access to authorized users any time, anywhere. The automated delivery of at-a-glance current information keeps quality front and center throughout Xilinx.

CONSISTENT TOP-TIER CUSTOMER SATISFACTION



Xilinx aligns strategies and processes with feedback from customers, to achieve and sustain improved satisfaction levels.

"For several years, hundreds of Xilinx engineers have been working behind the scenes to change the way we do business, and to make it easier for our customers to deliver world-changing innovations based on programmable silicon. In 2011, the results of their vision and efforts have grabbed the attention of industry watchers and our customers. A relentless commitment to quality has allowed Xilinx to be first to market with 28nm, stacked-silicon interconnect, and other advancements that now make it possible to solve the world's biggest problems with the help of FPGAs."

JACK ELWARD
Vice President, Worldwide Quality Systems and Customer Support
XILINX, INC.

DATASHEET COLOR KEY

- **INNOVATION**
- **QUALITY**
- **CASE STUDIES**

"We have worked closely with Xilinx and its leading engineers for over a decade. Without the high-speed performance of the Virtex-4 devices and their active dynamic reconfiguration capability, combined with low-latency serial links and high-speed LVDS interconnectivity, this project would not have been possible."

VOLKER LINDENSTRUTH
Professor
UNIVERSITY OF HEIDELBERG
CERN, ALICE (A Large Ion Collider Experiment)

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Printed in the U.S.A. PN 2503