Value Multiplier Summary

Packet Processing | Waveform Processing | Video Processing | High Performance Computing

- System Integration and BOM Cost Reduction
- System Performance
- Total Power
- Design Productivity

UltraSCALE™

Multiplying the Value of 20nm - *Doing More for Less*

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XILINX
ALL PROGRAMMABLE™

UltraScale Value Multiplier Summary

Migration Path	Device Migration (Equivalent Logic Capacity)	System Integration (Multiple to Fewer Devices)
VIRTEX-7 TO▶ KINTEX UltraSCALE	• 2-3X Logic Cell Throughput*/$ • 2-4X DSP Bandwidth/$ • 1.5-3X Serial Bandwidth/$ • 2X DDR Memory Bandwidth/$ • 25-45% Lower Power at Same Performance	• Up to 3.5X System Performance/$ • Up to 2X Greater System Performance/Watt • Up to 40% System Power Reduction • Up to 60% BOM Cost Reduction
KINTEX-7 TO▶ KINTEX UltraSCALE	• 15-30% Greater Logic Cell Throughput*/$ • 25-120% Greater DSP Bandwidth/$ • 1.5-2X Greater Serial Bandwidth/$ • 2-4X DDR Memory Bandwidth/$ • 25-45% Lower Power at Same Performance	• Up to 2.5X System Performance/$ • Up to 2.5X Greater System Performance/Watt • Up to 50% System Power Reduction • Up to 60% BOM Cost Reduction
VIRTEX-7 TO▶ VIRTEX UltraSCALE	• 20-40% Greater Logic Cell Throughput*/$ • 10-30% Greater Serial Bandwidth/$ • 25-45% Lower Power at Same Performance • Up to 33% Smaller Devices through Integrated Blocks	• Up to 3X System Performance/$ • Up to 2.5X Greater System Performance/watt • Up to 50% System Power Reduction • Up to 50% BOM Cost Reduction • 28G-LR Drives 2X Port Density/$
UltraScale architecture and Vivado® Design Suite are co-optimized to enable a device utilization target of 90%, which can result in up to a 30% effective cost advantage relative to the nearest competitor.		

* Logic cell throughput = logic capacity × average realizable speed of logic cells

Xilinx is multiplying the value of 20nm with the UltraScale architecture and associated family of FPGAs and 3D ICs. Whether viewed from almost every attribute at the chip level or viewed when integrating multiple chips into one or fewer chips at the system level, designers will find compelling value metrics as they migrate to an UltraScale solution.

The table above shows the potential chip and system level value multipliers associated with 3 different migration paths.

When migrating from Virtex-7 to Kintex UltraScale devices, designers will see 1.5-3X chip level performance-per-dollar improvements across all performance areas, with 25-45% power reductions. For those doing multi-chip integration, up to 60% BOM cost reduction and 2-3.5X higher system level values are enabled. The 20nm process, UltraScale architecture, DSP block-level enhancements, and higher bandwidth interfaces have paved the way for customers to utilize the Kintex UltraScale "mid-range" in applications where only a high-end Virtex class product was feasible before.

When migrating to 20nm Kintex UltraScale devices from Kintex 7, UltraScale enables 25-120% more DSP and 1.5-4X more serial bandwidth and memory bandwidth-per-dollar improvements, with 25-45% power reductions. Again, for those integrating multiple chips into one, up to 60% cost reductions and >2X higher system level values are enabled. In addition to leveraging of the UltraScale architecture and DSP block level enhancements and higher bandwidth interfaces, the Kintex UltraScale devices were optimized with a resource mix to maximize the value when migrating DSP and memory intensive applications from Kintex-7 to Kintex UltraScale.

Applications that migrate from Virtex-7 to Virtex UltraScale FPGAs will typically leverage the full capacity of UltraScale devices for programmable systems integration, and the ability to double system level performance, reduce power and BOM cost by up to 50%, while still enjoying significant chip-level value enhancements. With greater performance-per-dollar in nearly every category when compared to Virtex-7 devices, 4X the logic capacity and 60% greater serial bandwidth than the nearest competitor, Virtex UltraScale FPGAs represent the leading edge in performance and value. ■

The breadth of Xilinx's 20nm solutions is both compelling and complementary to its 28nm portfolio. Through the UltraScale architecture and associated family of FPGAs and 3D ICs, Xilinx is multiplying the value of 20nm for the next generation of smarter, high performance systems.

The Value of UltraScale in Packet Processing and Transport

Delivering the Fastest Path to Multi-Hundred Gigabit Throughput with a Target of 90% Device Utilization and 3D IC Enhanced System Integration

Packet Processing	Value Multipliers	Key Applications
Domain Optimized Integrated Blocks • Integrated 150G Interlaken Interface • Integrated 100G Ethernet MAC Interface • VCXO for External Clock Clean Up • Enhanced DSP for Efficient FEC & CRC	**Device Migration Multipliers** • 2.2X Logic Cell Throughput/$ • Up to 25% Smaller Devices Through Integrated IP • 1.6X Serial Bandwidth/$ • 1.65X DDR Memory Bandwidth/$ • 30% Lower Power at Same Performance	**Wired Comms** • 2x100G Muxponder • 4x100G Transponder • 4x100G MAC to Interlaken Bridge • 4x100G MuxSAR • 100G Traffic Manager NIC • OTU5 Muxponder • 100G, 200G, MAC-to-Interlaken Bridge • 200G FIC
Domain Optimized Capabilities • Block RAM Cascading for Deep Buffers • Wide Bus-Optimized Interconnect • ASIC-like Low Skew Clocking • TX Phase Interpolator & Fractional PLL	**System Integration Multipliers** • Up to 3X System Performance/$ • Up to 2.5X System Performance/Watt • Up to 60% System Power Reduction • Up to 50% BOM Cost Reduction	**Data Center** • 100G SDN NIC • SSD Controller • PEX Devices
Key I/O and Connectivity Interfaces • DDR4 Memory Support up to 2400 Mb/s • Up to 33G Transceiver Support • Increased Independent DDR Memory Channels • Increased Independent Transceiver Clocking (X2/bank) • 28G Backplane Support • 12.5G Transceiver in Slowest Speed Grade • Low Cost CFP4 and CFP2 Interfacing		

Xilinx UltraScale™ architecture delivers 3X higher system performance and integration for next generation packet processing and transport applications, and provides an ASIC-class advantage for engineers. UltraScale devices are optimized to address packet processing applications based on a detailed, holistic understanding of the system-level requirements, constraints, and bottlenecks associated with next-generation wired communications and data center applications. The thoughtful mix of system-optimized features and architecture delivers ASIC-class performance capable of supporting multi-hundred gigabit-per-second throughput at line rates scaling from100s of gigabits to terabits-per-second. UltraScale devices address the performance demands within an economic power envelope that is a non-negotiable prerequisite for success, while also delivering an extra node of realizable system value through advanced integration technologies that include 3D ICs.

UltraScale FPGAs and 3D ICs combine the right system-level functions for next-generation applications. This includes massive I/O and memory bandwidth, optimized critical paths, efficient hardened functions, scalable integration with ASIC-like clocking, advanced power management, and a next generation routing structure for extremely high device utilization without degradation in performance. The combination of these elements enables 3X higher system performance and integration in a fully programmable architecture that can be tailored to match the exact needs of the most demanding packet processing applications.

The combination of UltraScale devices, the Vivado® Design Suite, and the UltraFast™ Design Methodology removes system-level design and productivity bottlenecks for next-generation packet processing applications. Only the UltraScale architecture can support datapaths that exceed 2048 bits at device utilization with a target of 90% without any degradation in performance.

UltraScale is the only architecture that scales from monolithic to extremely high capacity 2nd-generation 3D ICs. Enhancements and critical-path optimizations across DSP blocks and Block RAM lead to greatly improved system-level performance for CRC & FEC calculations, a typical bottleneck for most packet-based operations. Embedded Interlaken and 100G Ethernet MAC interfaces enable unmatched levels of integration, cost, and power efficiencies. DDR4 memory interfacing at 2400 Mb/s and backplane connectivity at 28 Gb/s hold the potential for a tectonic shift in system level capabilities and a re-think of an overall system architecture. The Vivado Design Suite and UltraFast Design Methodology enable the ASIC-strength design capabilities and the fastest time to differentiation, integration, and implementation for both monolithic and highly integrated 3D ICs.

Taken as a collective, only Xilinx delivers the fastest path to multi-hundred gigabit throughput with a target of 90% device utilization and 3D IC enhanced system integration.

The Value of UltraScale in Waveform Processing

Delivering the Fastest Path to Cost and Power Optimized Multi-TeraMAC Throughput with a Target of 90% Device Utilization and 3D IC Enhanced System Integration

Waveform Processing	Value Multipliers	Key Applications
Domain Optimized Capabilities • High DSP Count Devices • DSP 491 MHz Critical Path in Slow Speed Grade • Block RAM Cascading for Deep Buffers • Enhanced DSP for Resource Reduction • Enhanced DSP for Complex Functions **Key I/O and Connectivity Interfaces** • DDR4 Memory Support up to 2400 Mb/s • CPRI 16G Capable Transceivers over Industrial Temperature Grade • 9.8G CPRI in Slowest Speed Grade • 12.5G Transceiver in Slowest Speed Grade • JESD204B Support in Slowest Speed Grade • 12G SDI Support • Highest Performance Industrial Temperature Grade Support	**Device Migration Multipliers** • 2.7X DSP Bandwidth/$ • 2.2X Serial Bandwidth/$ • 3X DDR Bandwidth/$ • 30% Lower Power at Same Performance **System Integration Multipliers** • Up to 3X System Performance/$ • Up to 2.6X System Performance/Watt • Up to 50% System Power Reduction • Up to 50% BOM Cost Reduction	**Wireless** • 4X4 60 MHz and Above Radio • BTS (CPRI) Switching • HD-BTS/CRAN Switching • Mwave/Eband MIMO+ **Medical Imaging** • Ultrasound **Aerospace and Defense** • Radar • Milcom

Xilinx UltraScale™ architecture delivers TeraMACs of DSP performance in a cost-optimized footprint that requires only half the power and area to address next-generation waveform-processing applications and provide an ASIC-class advantage for engineers. Through a focus on next-generation system-level performance, power, and cost requirements, the UltraScale architecture delivers the right mix of DSP performance with the right blend of features, optimized connectivity, and memory. Wireless carriers keenly focused on both OPEX and CAPEX demand cost-optimized and power-optimized solutions for next-generation Hi-Density Macrocell Basestations and Cloud RANs. Radar and Milcom applications, notorious for their Size, Weight, Power, and Cost (SWAP-C) constraints, continue to demand 2X and beyond improvements across all elements of SWAP-C. To address these mandates, UltraScale devices address the massive waveform processing performance demands within an economic power envelope that is clearly a non-negotiable prerequisite for success, while also delivering an extra node of realizable system value through advanced integration technologies that include 3D ICs.

UltraScale FPGAs and 3D ICs combine the right system and device level functions for next-generation applications: cost / performance optimized I/O connectivity (CPRI and JESD 204B), high-performance memory interfacing (DDR3-1866 and DDR4-2400), optimized and enhanced DSP processing critical paths (491 MHz LTE optimized, enhanced for double precision multiplication and more), hardened interfacing functions (PCIe® Gen 3 and more), scalable integration with ASIC-like clocking, advanced power management, and a next-generation routing structure that delivers extremely high device utilization without degradation in performance. The combination of these elements enables scalability to TeraMACs of performance in a fully programmable architecture that can be tailored to match the exact needs of the most demanding application with up to 50% reduction in power.

The combination of UltraScale FPGAs, the Vivado® Design Suite, and the UltraFast™ Design Methodology removes the system-level design and productivity bottlenecks for next-generation waveform processing applications. Only the UltraScale architecture can support wide, parallel processing at device utilization with a target of 90% without any degradation in performance. The addition of greatly enhanced and optimized Block RAM and DSP blocks enable a massive jump in fixed-point and complex arithmetic performance and efficiency, a typical bottleneck for most waveform applications. The Vivado Design Suite and UltraFast Design Methodology enable the ASIC-strength design capabilities and the fastest time to differentiation, integration, and implementation for both monolithic and highly integrated 3D ICs. ■

Taken as a collective, only Xilinx enables the fastest path to cost and power optimized multi-teraMAC throughput with a target of 90% device utilization and 3D IC enhanced system integration.

The Value of UltraScale in Image and Video Processing

Delivering the Fastest Path to 8K/4K Image and Video Processing and Transport with a Target of 90% Device Utilization and 3D IC Enhanced System Integration

Video and Image Processing	Value Multipliers	Key Applications
Domain Optimized Capabilities • High DSP Count Devices • Enhanced DSP - FIR Filtering • Integrated VCXO **Key I/O and Connectivity Interfaces** • MIPI Connectivity • 12G SDI Support in Slowest Speed Grade • 4K/2K @ 120Hz (51 Gb/s) Sensor Interface in Small Footprint • DDR4 Memory Support up to 2400 Mb/s • 12.5G Transceiver in Slowest Speed Grade	**Device Migration Multipliers** • 3.2X Logic Cell Throughput/$ • 1.6X Serial Bandwidth/$ • 1.5X DSP Bandwidth/$ • 1.4X DDR Bandwidth/$ • 25% Lower Power at Same Performance **System Integration Multipliers** • Up to 3.5X System Performance/$ • Up to 2.1X System Performance/Watt • Up to 30% System Power Reduction • Up to 60% BOM Cost Reduction	**Audio, Video, and Broadcast (AVB)** • 8K/4K Image Processing **Aerospace and Defense** • 4K/2K Surveillance

Xilinx UltraScale™ architecture delivers another 2X system performance and integration for next-generation 8K and 4K Video Processing applications, providing an ASIC-class engineering advantage with much faster time to market and lower system-level BOM costs. The UltraScale family was optimized to address video-processing application requirements based on a detailed, holistic understanding of system-level needs, constraints, and bottlenecks associated with capturing, encoding, recording, transmitting, decoding, and displaying high-quality 8K and 4K video at high frame rates. The thoughtful mix of system optimized features and architecture delivers ASIC-class performance capable of supporting system-level throughputs measured in gigapixels and terabits per second. UltraScale devices address peak performance demands within economic power envelopes that are non-negotiable prerequisites for system-level success in all video applications and markets, while delivering an extra node of system value through advanced integration technologies including 3D ICs.

UltraScale FPGAs and 3D ICs combine the right system-level functions for next-generation applications. This includes massive I/O and memory bandwidth, optimized critical paths, efficient hardened functions, scalable integration with ASIC-like clocking, advanced power management, and a next-generation routing structure for extremely high device utilization without degradation in performance. The combination of these elements enables 2X higher system performance and integration in a fully programmable architecture that can be tailored to match the exact needs of the most demanding video-processing applications.

The combination of UltraScale devices, the Vivado® Design Suite, and the UltraFast™ Design Methodology removes system-level design and productivity bottlenecks for next-generation video-processing applications. Only the UltraScale architecture can support datapaths that exceed 2048 bits at device utilization with a target of 90% without any performance degradation. UltraScale is the only architecture that scales from monolithic to extremely high capacity 2nd-generation 3D ICs. Enhancements and critical-path optimizations across DSP blocks and Block RAM lead to greatly improved system-level performance, such as a 50% reduction in required multiplications for symmetric FIR filters that doubles maximum sample rates. Independent, programmable digital PLLs integrated into each UltraScale transceiver eliminate the need for costly external VCXOs or clock cleaners, resulting in massive system-level BOM cost reductions. Additional UltraScale device features such as direct, high-speed DDR4-2400 memory interfacing and native 12G and 6G UHD-SDI connectivity hasten tectonic shifts in system-level capabilities, performance, and power consumption by enabling the development of new, innovative, and streamlined system architectures. The Vivado Design Suite and UltraFast Design Methodology enable the ASIC-strength design capabilities and the fastest time to differentiation, integration, and implementation for both monolithic and highly integrated 3D ICs. ■

Taken as a collective, only Xilinx delivers the fastest path to 8K/4K Image and Video Processing Systems with a target of 90% device utilization and 3D IC enhanced system integration.

The Value of UltraScale in High Performance Computing

Delivering the Fastest Path to Cost and Power Optimized Multi-Teraflop Throughput with a Target of 90% Device Utilization and 3D IC Enhanced System Integration

High Performance Computing	Value Multipliers	Key Applications
Domain Optimized Capabilities • DSP Cascading for Improved F_{MAX} • Integrated 100G Ethernet MAC • Block RAM Cascading for Deep Buffers	**Device Migration Multipliers** • 2.2X Logic Cell Throughput/$ • 1.6X Serial Bandwidth/$ • 1.8X DSP Bandwidth/$ • 1.65X DDR Bandwidth/$ • 35% Lower Power at Same Performance	**Test and Measurement** • ASIC Emulation
Key I/O and Connectivity Interfaces • DDR4 Memory Support up to 2400 Mb/s • HMC Capable Transceivers up to 15G • Enhanced Integrated PCIe® Gen 3 • PCIe Gen 4 Compliant Transceivers • 33G Transceiver Support • Extended QPI Support • 12.5G Transceivers in Slowest Speed Grade	**System Integration Multipliers** • Up to 4X System Performance/$ • Up to 3.4X System Performance/Watt • Up to 35% System Power Reduction • Up to 70% BOM Cost Reduction	**Data Center** • Low Latency Switches • QPI Accelerators • PCIe Accelerators

Xilinx UltraScale™ architecture delivers 2X higher system performance and 35% reduction in power for next-generation high performance computing applications, and provides an ASIC-class advantage for engineers. The UltraScale FPGAs are optimized to address high performance computing applications based on a detailed, holistic understanding of the system-level requirements, constraints, and bottlenecks associated with next-generation high performance computing applications. The thoughtful mix of system-optimized features and architecture delivers ASIC-class performance with logic capacities capable of encompassing large algorithms. This includes support for massive multi-threaded concurrent execution threads with the extreme compute performance and memory throughput to deliver full line-rate complex processing with single-digit microsecond turnarounds. UltraScale devices address the extreme low-latency compute performance demands within an economic power envelope that is a non-negotiable prerequisite for success, while also delivering an extra node of realizable system value through advanced integration technologies that include 3D ICs.

UltraScale FPGAs and 3D ICs combine the right system-level functions for next generation applications. This includes massive I/O and memory bandwidth, optimized critical paths, efficient hardened functions, scalable integration with ASIC-like clocking, advanced power management, and a next-generation routing structure for extremely high device utilization without degradation in performance. Whether the task requires accelerated processing of large datasets, computing investment value and risk in real time, or responding to financial market events in nanoseconds, the UltraScale FPGAs and 3D ICs combine the right system-level functions and capabilities to deliver 2X higher system performance and integration in a fully programmable architecture that can be tailored to the exact needs of the most demanding high performance computing applications.

The combination of UltraScale FPGAs, the Vivado® Design Suite, and the UltraFast™ Design Methodology removes system-level design and productivity bottlenecks for next-generation high performance computing applications. Only the UltraScale architecture can support teraflop compute performance at device utilization with a target of 90% without any degradation in performance. UltraScale is the only architecture that scales from monolithic to extremely high capacity 2nd-generation 3D ICs. Significant enhancements and critical-path optimizations across DSP and BRAM blocks address key performance bottlenecks. Extended support for double-precision floating point leading to1.5X to 2X improved system-level performance for complex data flow machines at power levels that set new standards for GMACs/watt. Embedded 100G Ethernet MAC and PCI Gen 3 interfaces enable unmatched levels of integration, cost, and power efficiencies. DDR4 memory interfacing at 2400 Mb/s, extended QPI connectivity and 32 Gb/s serial connectivity hold the potential for a tectonic shift in system-level capabilities and a re-think of an overall system architecture. The Vivado Design Suite and UltraFast Design Methodology enable the ASIC-strength design capabilities and the fastest time to differentiation, integration, and implementation for both monolithic and highly integrated 3D ICs. ■

Taken as a collective, only Xilinx delivers the fastest path to cost-optimized and power-optimized multi-teraflop throughput with a target of 90% device utilization and 3D IC enhanced system integration.

UltraScale: System Integration and BOM Cost Reduction

Key System Integration and BOM Cost Reduction Enablers	
Device Utilization	• Greater than 30% utilization advantage vs. the competition
High Transceiver Count	• Up to 120 transceivers enable up to 4-to-1 device count reduction for Nx100G applications
DSP Bandwidth	• Over 8 TeraMACs of DSP bandwidth enable up to 3-to-1 device count reductions
Integrated, High Bandwidth Cores	• 100G Ethernet MAC and 150G Interlaken cores enable resource savings for additional functionality
Device Capacity	• 2nd generation 3D IC devices enable breakthrough device capacity—4X the nearest competitor

Xilinx has moved well beyond its programmable logic origins to enable the next-generation of flexible, programmable, and 'smarter' systems. Key to delivering value to system designers is integrating complex, multi-chip functionality into a single device, thereby removing chip-to-chip performance bottlenecks, reducing system-level power, BOM cost, footprint, and simplifying board and system development. Building on the foundation of the All Programmable device portfolio of the Xilinx 7 series, UltraScale™ FPGAs and 3D IC devices take system integration to the next level through architectural advancements and breakthrough capacity.

Fundamental to system integration is device utilization—optimally leveraging the device to absorb as much system functionality as possible. UltraScale devices feature a massive re-architecture of the routing, clocking, and logic infrastructure, allowing developers to integrate IP and subsystems that span clock domains while targeting a 90% utilization of the device without performance degradation. The ability to fit more functionality into a device—while meeting performance requirements—translates into system-level cost savings by allowing the designer to select the smallest possible device for a given design.

To enable integration of IP and subsystems, and to reduce chip counts from 2-chips-to-1 or even 4-chips-to-1, the right mix of specialized resources is also essential.

Transceiver resources are key enablers of high bandwidth systems. UltraScale devices deliver not only the highest quality transceivers with the lowest jitter, but the highest transceiver count in their class. With up to 120 transceivers in a single device, 60 of which operate at 32 Gb/s, the Virtex® UltraScale devices integrate 400G and 500G networking applications into a single chip. In addition to enabling high bandwidth, UltraScale transceivers reduce system-level BOM cost, power, and form factor, given their ability to interface to the latest 28 Gb/s-enabled CFP4 optical modules. In a 4x100G OTN switching application, for example, a single Virtex UltraScale device can integrate 400G throughput and complex processing functions capacity that would previously have required four FPGAs.

Resource mix also includes complex, integrated IP cores. The UltraScale architecture includes integrated 100G Ethernet MAC and 150G Interlaken blocks for Nx100G networking applications. These cores provide power, latency, and logic capacity benefits, and also allow more functionality to be integrated on-chip. With UltraScale devices, MAC-to-Interlaken bridges, for example, can now integrate other functionality, such as packet processing and time stamping.

With the need for massive signal processing for wireless communications and smart vision applications, the UltraScale devices include re-architected DSP blocks for efficiency of fixed-point and IEEE Std 754 floating-point arithmetic functions as well as complex multiply-accumulate operations, among other optimizations. The DSP-optimized Kintex® UltraScale family in particular addresses massive signal processing demands—delivering up to 8.2 TeraMACs of compute bandwidth.

As an example, an 8x8 100 MHz TD-LTE remote radio head unit requires two Kintex-7 devices due to extreme compute performance requirements (for functions such as up-conversion, down-conversion, crest factor reduction, and pre-distortion). With nearly 3X the signal processing bandwidth of its mid-range predecessor due to its high DSP-to-logic ratio and architectural enhancements, Kintex UltraScale devices enable 2-to-1 device integration, putting complex functionality into a small device, and providing the critical power, cost, and footprint advantages needed for distributed base station design.

Beyond architectural advancements and processing bandwidth, a key enabler to integration is sheer device capacity. With the breakthrough 3D IC technology introduced in the 7 series, UltraScale devices are based on the only architecture that scales from monolithic to extremely high capacity 2nd-generation 3D ICs—leveraging Xilinx's Stacked Silicon Interconnect technology that is both cost-efficient and production-proven. Both Kintex UltraScale and Virtex UltraScale families take advantage of the 3D IC architecture to expand the mid-range and extend the high-end—leveraging 2X greater inter-die connections for a seamless design experience and maximum system integration. The Virtex UltraScale VU440 devices for example, doubles the industry's highest capacity 28nm device to 4.4 million logic cells, enabling the highest system integration for next-generation test and measurement and prototyping applications. ■

In summary, system integration drives key care-abouts in system-level design: performance, power, cost, productivity, and footprint, among others. Xilinx All Programmable devices have been at the heart of complex systems for multiple generations, and the UltraScale architecture builds on the experience and technological breakthroughs of its predecessor to target designs that can only scale by integrating as much functionality into the fewest devices.

UltraScale: Scaling System Performance

Key System Performance Enablers	
Logic Architecture	• Next-generation routing capacity, creating up to a two speed grade performance improvement • ASIC-like clocking for minimum skew • Enhanced CLB logic infrastructure enables a target of 90% device utilization
Data Processing	• Hardened cascading of block RAM arrays for greater performance • 8.2 TeraMACs of DSP bandwidth; up to 2X more efficient complex MAC functions
Expanded I/O Capabilities	• ~6 Tb/s of overall peak serial bandwidth; 28G backplane support • DDR4 and HMC memory support • Integrated 100G EMAC, 150G Interlaken, and PCIe® Gen3 cores for savings in die size and power

Next-generation systems require multi-hundreds of gigabits per second with smart processing at full line rate, scaling to terabits and teraflops per second. The UltraScale™ architecture was uniquely developed with these performance requirements in mind, enabling systems to "scale" in design size and complexity while meeting next-generation bandwidth demand. Whether for intelligent packet processing and traffic management, mixed-mode radio design with smart beamforming, or high definition displays with smart image enhancement and recognition, the UltraScale architecture enables a massive leap in overall system performance for next-generation digital systems.

As a foundation, the UltraScale architecture was designed to enable massive data flow and processing. Data buses can commonly range from 512-bit to 2048-bit, putting strain on existing architectures to meet performance requirements and challenging routability of next-generation designs. To address these interconnect-related challenges, Xilinx took a unique approach to re-architecting the FPGA core by more than doubling the routing capacity, implementing an advanced ASIC-like clocking network, and enhancing the logic infrastructure for better utilization.

UltraScale devices feature a re-designed routing architecture that dramatically increases the number of routing tracks and point-to-point direct routes to logic cells, giving the software tools more options to connect logical resources in the fastest configuration. However, as interconnect performance increases due to routing enhancements, clock performance must also increase accordingly with minimum skew. The clock routing and buffers in the UltraScale architecture have been entirely redesigned to provide 20X more global clock buffers and thousands of placement options to enable clock network sources to be easily placed at the "center" of their respective networks—the same as an ASIC. This enables extremely low clock skew and high performance scalability. In addition to routing and clocking, every aspect of the existing configurable logic block (CLB) structure was analyzed to explore how the components can be used more efficiently. The resulting CLB enhancements collectively enable the Vivado® Design Suite to place many more, often unrelated, components in a logic block to achieve a more tightly packed design, allowing higher performance operation. Along with process derived performance gains, the routing, clocking, and logic infrastructure enhancements enable more "realizable performance"—up to a two speed-grade performance improvement with the highest utilization in the industry.

Enabling massive data bandwidth also requires data to be efficiently moved on- and off-chip. The UltraScale architecture vastly expands I/O capabilities for serial throughput and general-purpose parallel I/O. Translating multi-Gb/s serial data into wider data buses demands not only high line rates but robust signal quality.

The next-generation GTY serial transceivers in the Virtex® UltraScale FPGAs support serial system bandwidth of nearly 6 Tb/s, enabling up to 32.75 Gb/s for chip-to-chip and chip-to-optics applications, and the only 20nm FPGA to support 28.21 Gb/s backplane support. The optimized GTH transceivers in Kintex® UltraScale and Virtex UltraScale FPGAs provide 16.3 Gb/s backplane support and can meet today's serial protocol requirements such as 9.8 Gb/s CPRI and 12.5 Gb/s JESD204B. Robust backplane support in both GTH and GTY transceivers is made possible with the industry's only auto-adaptive equalization features, inherited from the Xilinx 7 series FPGAs, to directly drive high-speed, multi-gigahertz line rates across the toughest transmission channels.

With memory bandwidth becoming a major bottleneck to overall system performance, the UltraScale architecture takes parallel and serial memory interfacing to a new level. It enables more memory controllers as well as wider, faster memory ports to provide more than 1 Tb/s of DDR bandwidth. The Kintex UltraScale family represents the FPGA industry's first DDR4 memory interface, supporting rates up to 2400 Mb/s. For even greater bandwidth, UltraScale devices interface to serial memory technologies such as Micron's Hybrid Memory Cube (HMC), offering as much as 15X the memory throughput of a DDR3 module.

With a re-architected core, optimizations to embedded blocks were also included to resolve signal processing and packet processing bottlenecks. For example, the UltraScale architecture's new DSP block features wider 27x18 multipliers, allowing efficient implementation of key arithmetic functions and thereby enabling greater signal processing performance while consuming fewer routing or logic resources. This creates the foundational building block for key applications in wireless communications infrastructure, high performance computing, and image/video processing.

Critical-path optimization for packet processing includes CRC 32 checksum support in DSP blocks and the inclusion of integrated 100G Ethernet MACs and 150G Interlaken chip-to-chip interfaces. These serve as key enablers for networking and data center applications.

Critical to signal and packet processing is internal memory buffering. Multiple enhancements were made to the embedded memory architecture, including hardened cascading of block RAM arrays to create deep memories without consuming on-chip routing or logic resources, thereby improving performance. ■

In summary, these architectural breakthroughs boost data flow, open up I/O capabilities, and provide a leap in processing capacity, distinguishing the UltraScale devices from other programmable solutions. With the UltraScale architecture, system architects can take an "All Programmable" approach to scaling their designs for next-generation industry demands.

UltraScale: Innovations for Total Power Reduction

Key Power Reduction Enablers	
Static	• Static power reduction enabled by the 20SoC process • 30% static power reduction with power binning and voltage scaling
Dynamic	• 10% dynamic power reduction through flexible clock networks and intelligent clock gating • 60% block RAM power reduction through hardened cascading and granular power-gating • 20% DSP power reduction due to architectural efficiencies
I/O	• DDR4 interface support reduces I/O power by 20% vs. DDR3 • Serial memory interface support
Transceivers	• 30-50% power reduction through architectural improvements and low-power mode
Total Power	• 25-45% device level and up to 50% system level power reduction based on actual applications

Power consumption in programmable devices has become a primary factor for device selection and end system success. Whether the concern is total power consumption, usable performance, battery life, system cooling capacity, or reliability, power consumption is at the center of it all. The UltraScale™ architecture equips high-performance designs with innovative techniques to reduce power by 20-45% over Xilinx 7 series devices. In designing UltraScale devices, multiple strategies were explored and implemented to reduce static power, dynamic power, I/O power, and transceiver power.

TSMC's 20nm silicon process (20SoC) offers significant total power savings over its 28nm predecessor (28HPL) and operates at a core nominal voltage of 0.95V. Moreover, the headroom (the flexibility to trade-off performance for power reduction) of the process enables power binning and voltage scaling for further static power reduction. Xilinx screens for parts that can scale to a lower voltage—.9V—for ~30% static power reduction over the nominal core voltage of .95V. The lower voltage still delivers high performance but at lower power. Voltage scaling enables designers to choose the optimal power/performance trade-offs for their system on a design-by-design basis.

Because Xilinx focused on power efficiency from every angle, many architectural innovations were introduced to reduce dynamic power, starting with a new ASIC-like clocking network. With 20X increase in available global-capable clock buffers and the flexibility to place them anywhere on the die, the clock network runs only where it is needed—similar to an ASIC. This enables the network to consume only the power needed to get clock signals from source to destination. Another dynamic power reduction innovation includes enhancements to the block RAM. The UltraScale architecture enables granular gating by routing power only to the instantiated block RAM, and disabling power distribution to the unused block RAM. The block RAM also supports a high-speed, memory-hardened cascade feature utilizing dedicated routing and output multiplexing, which avoids use of external routing and configurable logic block (CLB) resources and enables dramatically lower dynamic power requirements.

To further reduce dynamic power, Xilinx has also significantly enhanced the DSP slice for greater efficiency per block while consuming fewer routing and logic resources. The slice improves multiplication and multiply-accumulate (MACC) operations by using as much as two-thirds fewer DSP blocks for common functions. Additionally, significant power reduction is achieved with new 96-bit XOR functionality to make efficient implementation of forward correction algorithms, CRC, and ECC blocks for wired communications designs.

Beyond the data flow and processing that takes place inside the device, I/O power has become a significant contributor to total power consumption of a device. One area where I/Os have historically consumed significant power is in memory interfaces. The UltraScale architecture enhances memory interfacing with support for DDR4 and serial-based memories. Designers will see a 20% reduction in I/O power when moving from DDR3 at 1866 Mb/s to DDR4 at 2400 Mb/s. In addition, interfacing with serial memories, such as Micron's Hybrid Memory Cube, offers 15X the bandwidth of DDR3 while consuming 70% less energy through the use of Xilinx industry leading serial transceivers.

The transceivers in the UltraScale architecture provide several low-power operating features, allowing users to explore performance and power trade-offs in a flexible and granular fashion. The UltraScale architecture's GTH (up to 16.3 Gb/s) transceiver has been redesigned to cut total power by 50% compared to the 7 series GTX (up to 12.5 Gb/s) and 7 series GTH (up to 13.1 Gb/s) transceivers. In addition, the UltraScale architecture's transceivers provide a 3rd-generation low-power mode that turns off decision feedback equalization (DFE) circuitry—a technology commonly used in backplane applications to compensate for signal degradation—to save power.

A key enabler to all these power saving features is the tool flow. The Vivado® Design Suite provides best-in-class tools for system power analysis and optimization. Starting at the architectural stage, designers can rely on the accuracy of the Xilinx Power Estimator (XPE) spreadsheet to determine system power consumption with the ability to fine tune settings and accurately model various scenarios. Through compilation and implementation, the Vivado Design Suite provides automatic power reduction and user controlled optimizations, such as fine-grained clock-gating to reduce power consumption across an entire system design or just portions of it. ■

In summary, Xilinx's power reduction strategies in the UltraScale architecture range from process enhancements, voltage scaling strategies, architectural innovations, and software optimization strategies. Dozens of options were evaluated on the percentage of static, dynamic, I/O, or transceiver power reductions that each could yield. With this, designers can safely scale performance and maximize system integration without breaking their power budgets.

UltraScale: Design Productivity for an ASIC-Class Advantage

Key Tools, Abstractions, and Methodology Enablers	
UltraScale Device Utilization and QoR	• Target of 90% device utilization with 20-30% better quality of results in complex designs.
Design Abstractions	• Up to 15X development cost reduction when using Vivado IPI in conjunction with Vivado HLS
UltraFast Design Methodology	• Proven 10X improvement in development time by using the UltraFast Design Methodology

Time-to-integration, time-to-implementation, and ultimately time-to-market become increasingly difficult to predict as design for next-generation systems becomes more sophisticated and complex. Productivity in the development process can be undermined if the tools, silicon architecture, and methodology do not scale with design complexity. The Vivado® Design Suite combined with the UltraScale™ architecture and UltraFast™ Design Methodology meets this need by ensuring the most productive path to delivering an ASIC-class advantage to designers.

It all begins with the design process itself—and this often means going beyond RTL. Accelerated time to IP and systems integration requires levels of design abstractions and automation. The Vivado Design Suite employs a combination of C and IP-based design environments to accelerate development by up to 15X over traditional RTL flows.

For example, Vivado High Level Synthesis (HLS) eases the evolution from C-based algorithms into reusable IP, while speeding verification time. Advanced, sophisticated algorithms used in wireless, medical, defense, and consumer applications demand system engineers to design in C/C++ or SystemC due to ease of algorithm development and sheer simulation performance over RTL based simulations. C-based IP generation with Vivado High-Level Synthesis (HLS) enables the C specification to be directly targeted into Xilinx All Programmable devices—automatically using Xilinx on-chip memories, DSP elements, and floating-point libraries—without the need to manually create RTL. The result is the fastest time to quality-of-results (QoR) that rivals hand-coded RTL.

To rapidly integrate C-based algorithmic IP or RTL IP into a design, Xilinx also added the Vivado IP Integrator (IPI) for IP packaging and integration. Vivado IPI is based on industry-standard interfaces and metadata such as the ARM® AXI interconnect and IP-XACT, abstracting the design process even further. Device- and platform-aware, Vivado IPI supports intelligent auto-connection of key IP interfaces, one-click IP subsystem generation, real-time DRCs, interface change propagation, and powerful debug, all through a graphical and TCL-based development flow. Design teams can rapidly assemble complex systems while ensuring designs and IP are configured correctly.

With the use of Vivado IPI, designers can seamlessly integrate from a vast library of IP cores from Xilinx or its Alliance Program members. Vivado Design Suite's broad offering of Plug-and-Play SmartCORE™ and LogiCORE™ IP accelerates productivity through fast and efficient reuse of proven cores. SmartCORE IP provides the technology foundation needed to create an extremely wide range of next-generation applications, ranging from data center security appliances to extremely efficient mobile backhaul modems, and smarter wired access equipment. It also supports an increasing number of third-party smart IP for a wide range of applications, including image and video processing and analytics for Smarter Vision applications.

After design integration and verification, implementation closure is the next productivity bottleneck. The Vivado Design Suite is co-optimized with UltraScale devices to ensure the fastest time-to-implementation for designs of highest complexity. A design tool's ability to fit more functions into the smallest possible device translates into system-level cost and power savings. The Vivado Design Suite achieves high device utilization because it employs advanced fitting algorithms and leverages the UltraScale architecture's truly independent look-up-tables (LUTs) within each configurable logic block (CLB).

Key to implementation closure, however, is achieving high utilization while simultaneously delivering high performance. At advanced silicon process nodes, the interconnect becomes the key limiter to performance. The Vivado Design Suite's analytical place-and-route algorithms break through this bottleneck by concurrently optimizing across multiple variables including timing, interconnect usage, and wire length. As designs double or even triple in capacity from one generation to the next and designers try to fit multiple chips into one, such breakthroughs are imperative to maximize iterations-per-day and deliver the shortest time to world-class QoR.

A design team can have access to the most advanced silicon and the greatest tools in the world, but if the group doesn't establish a solid methodology, it's difficult to deliver products at the right time for business success. Xilinx's UltraFast Design Methodology represents an authoritative set of best practices for board and device planning, design creation and IP integration, implementation and design closure, configuration, and hardware debug. With the Vivado Design Suite automating many aspects of the methodology, this series of guidelines and checklists enables developers to bring design closure to the front end of the design flow, where the impact on QoR is much greater. ■

In summary, the unique combination of tools, architecture, and methodology enables an ASIC-class advantage while leveraging an All Programmable approach. While designers of current generation designs have benefited from the co-optimization of the Xilinx 7 series FPGAs with the Vivado Design Suite and UltraFast Design Methodology, Xilinx has scaled this productivity and seamless design experience for next-generation systems that demand the performance, low power, and integration benefits of the UltraScale architecture.