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Heterogeneous Exascale Computing

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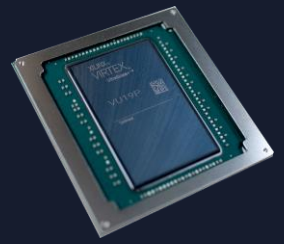
Towards Exascale Computing



SCALAR VECTOR MATRIX SPATIAL

Compute

EXA

PETA

TERA

ASIC

Democratize hardware design

RTL developers

Digitalization

Internet

Virtex

Accelerator

HW/SW co-design

Hardware savvy SW developers

Cloud

Mobile

Zynq

Alveo

Peer

Machine Learning

Data scientists

AI

Zen

Radeon

Versal

2000

2010

2020

cisco

illumina

Microsoft

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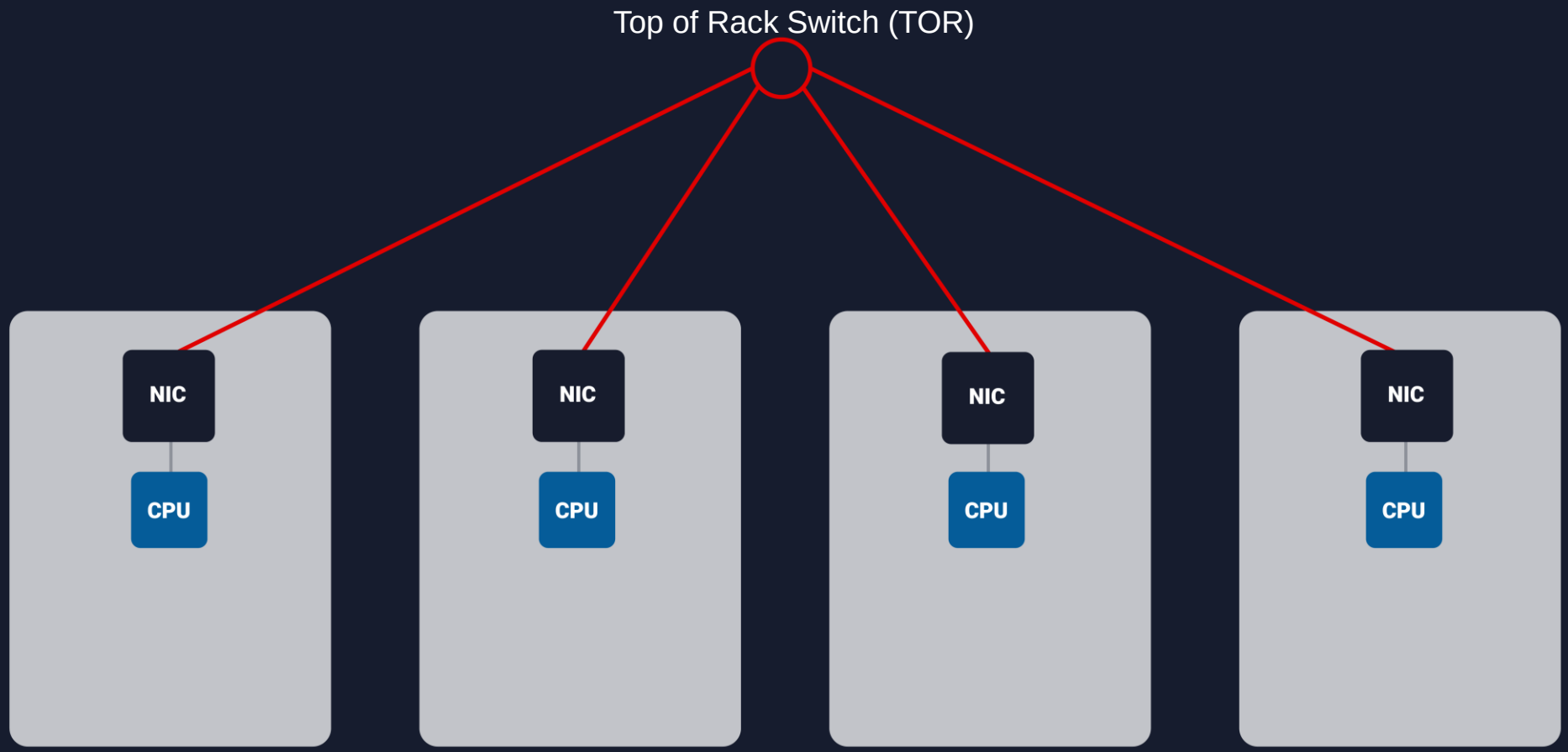
Historic: CPU Only



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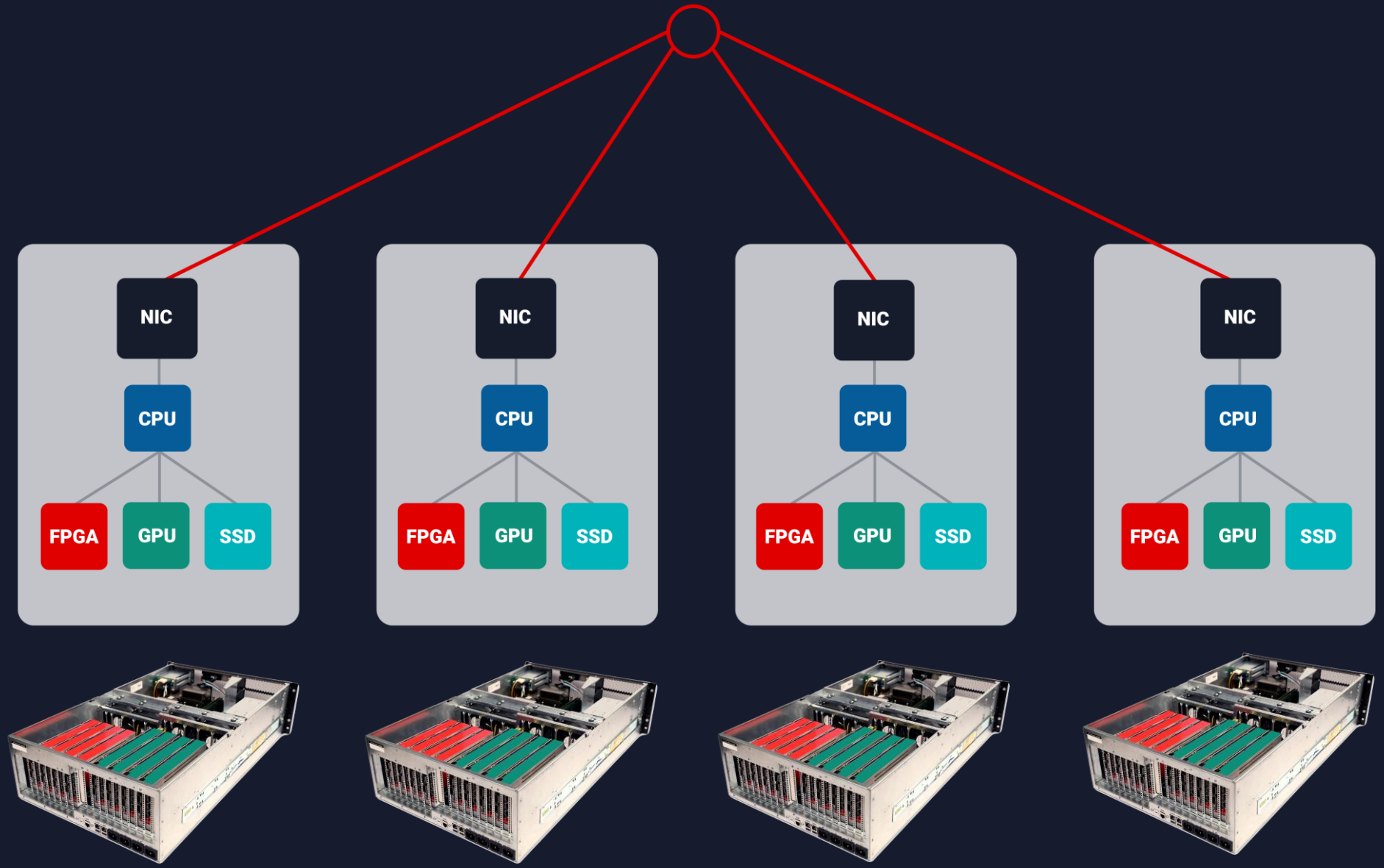
Scale-Up: CPU Host With GPU *and* FPGA Accelerators



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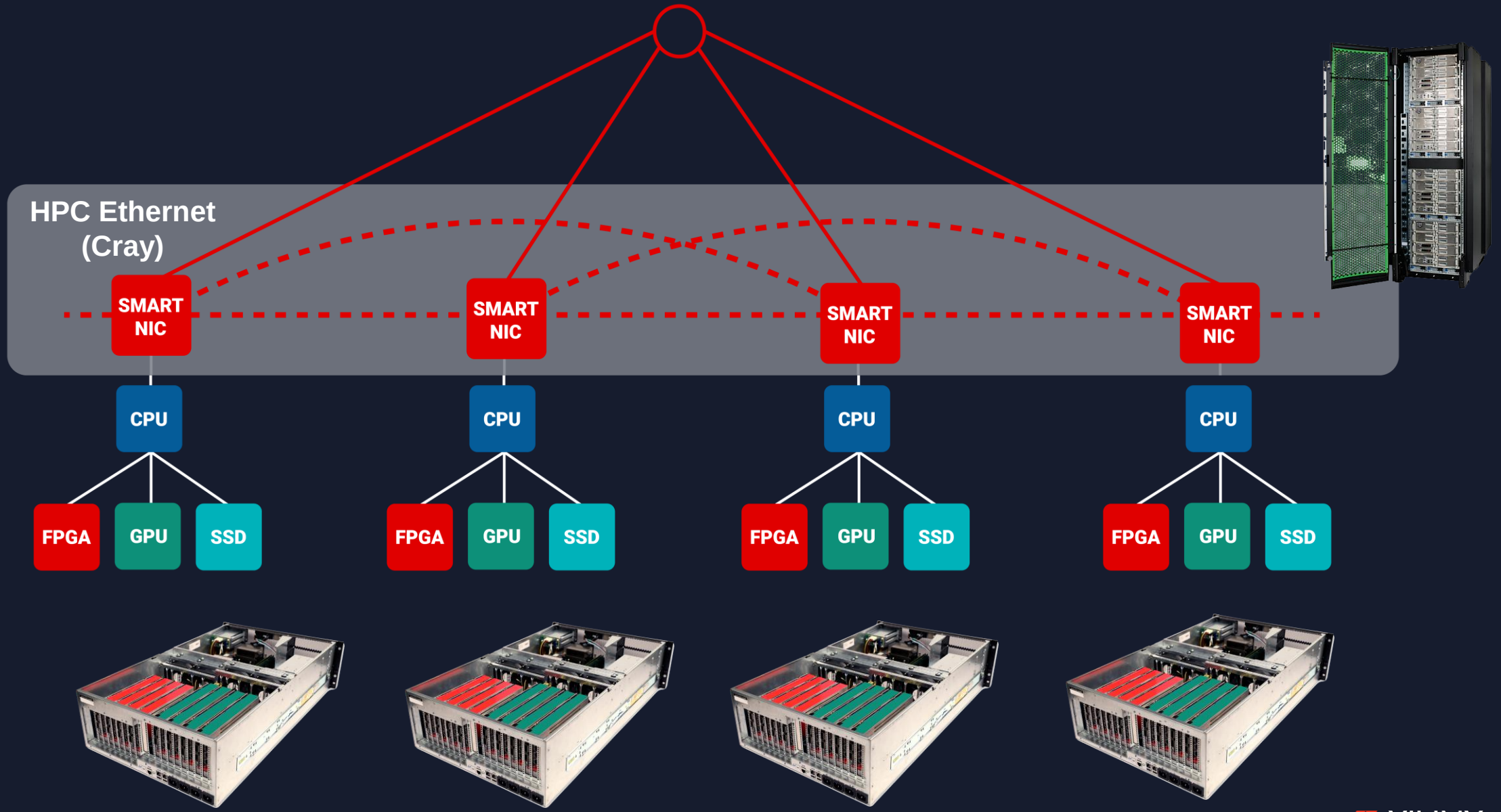
Scale-Out: CPU Host With GPU, FPGA and SmartNIC



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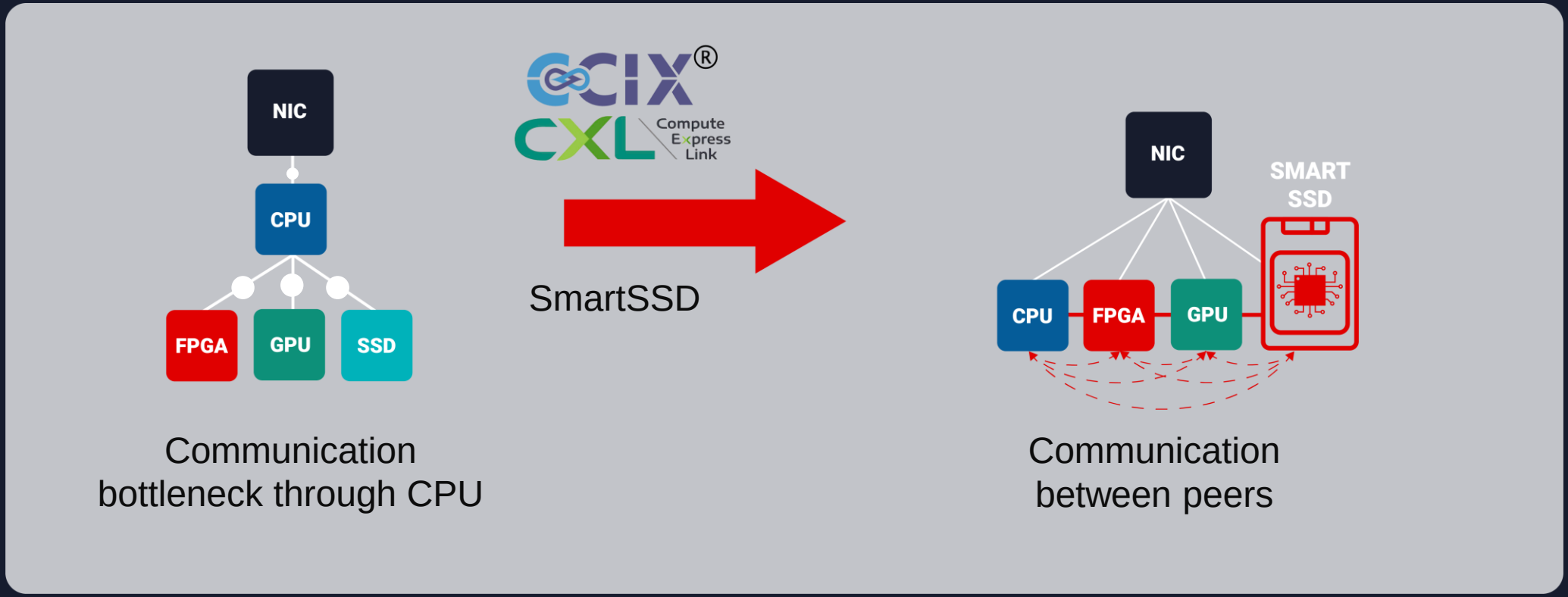
Scale-Up: Heterogeneous Fabric of Peers (CPU, GPU, FPGA, SSD)



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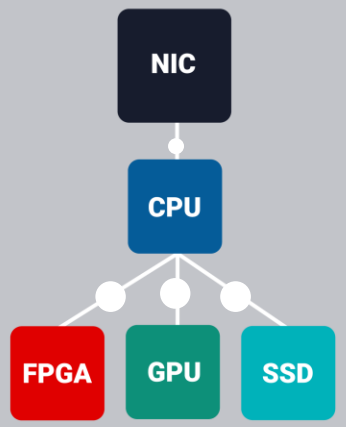
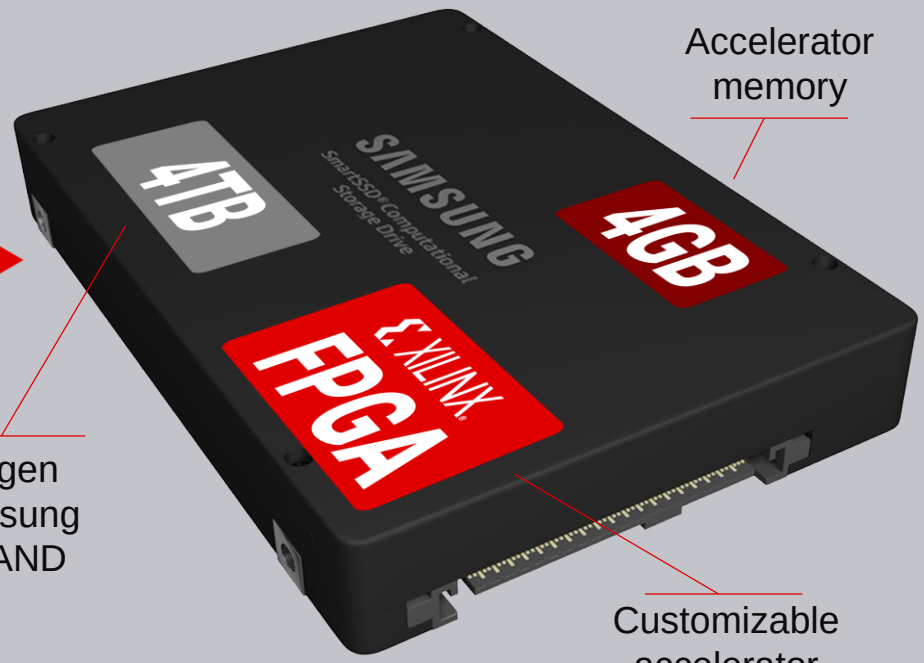
Scale-up: Heterogeneous fabric of Peers + Smart SSD



Communication bottleneck through CPU

CCIX®
CXL Compute Express Link



Accelerator memory

5th gen Samsung VNAND

Customizable accelerator

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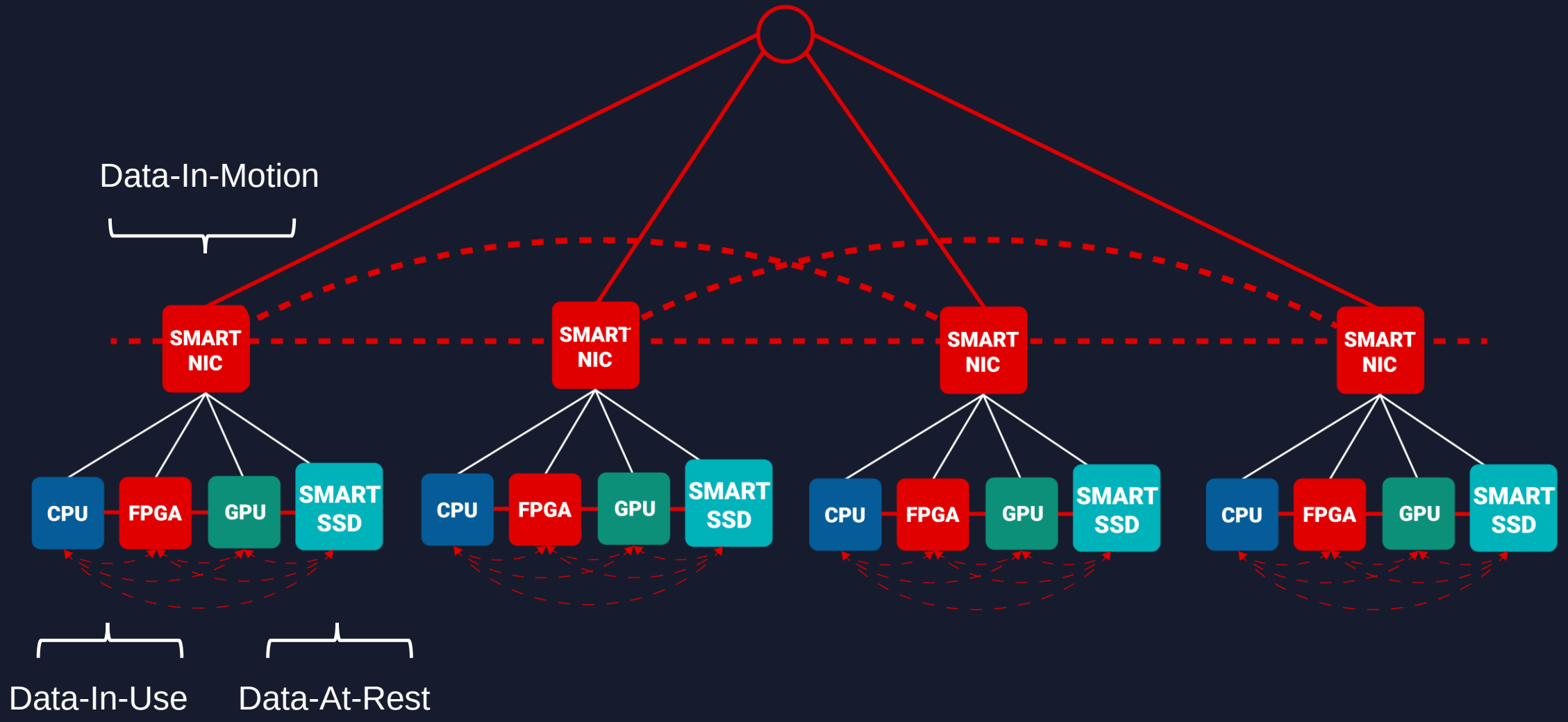
Scale-out : Compute On Data-In-Use, Data-In-Motion, Data-At-Rest



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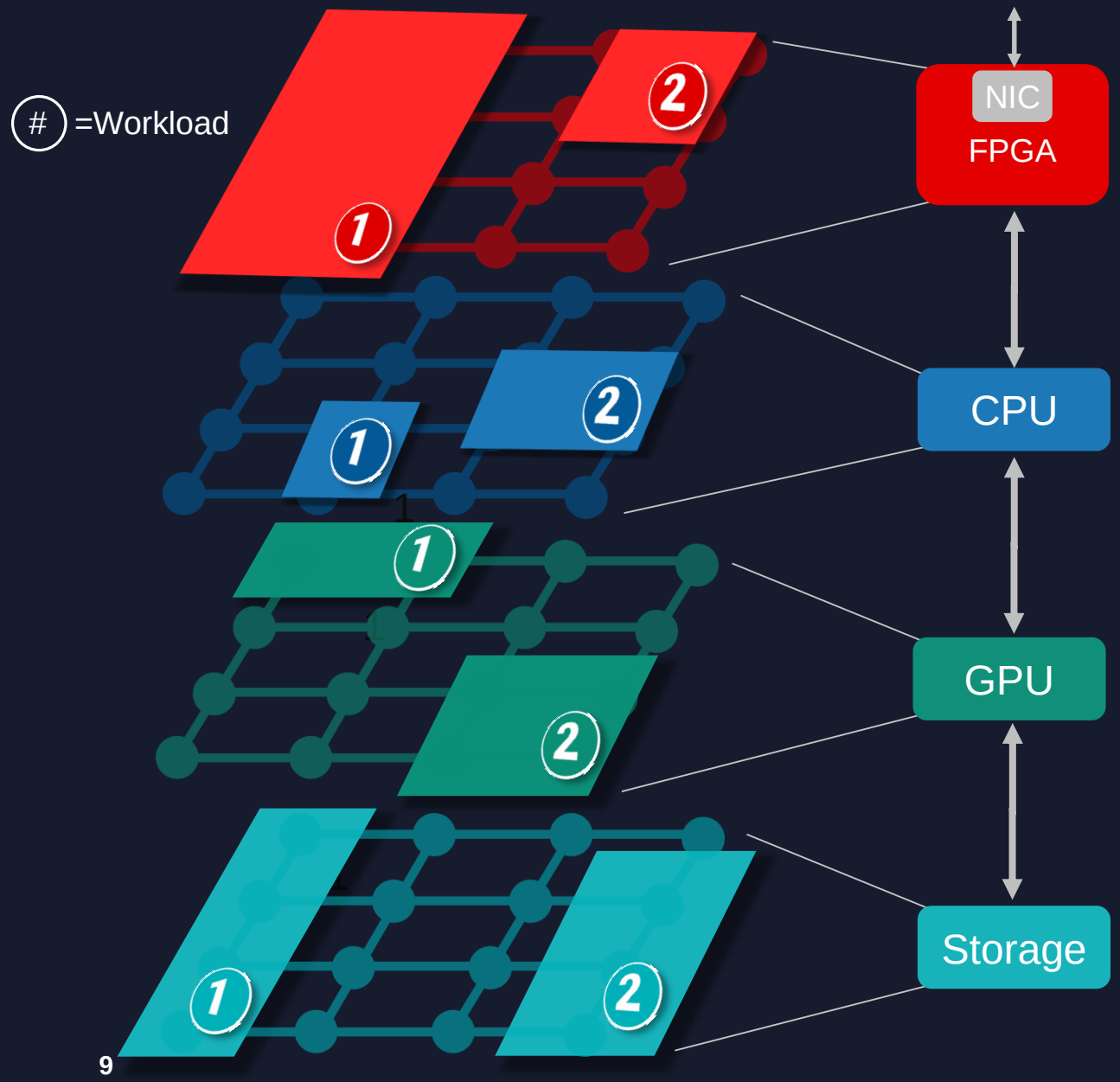
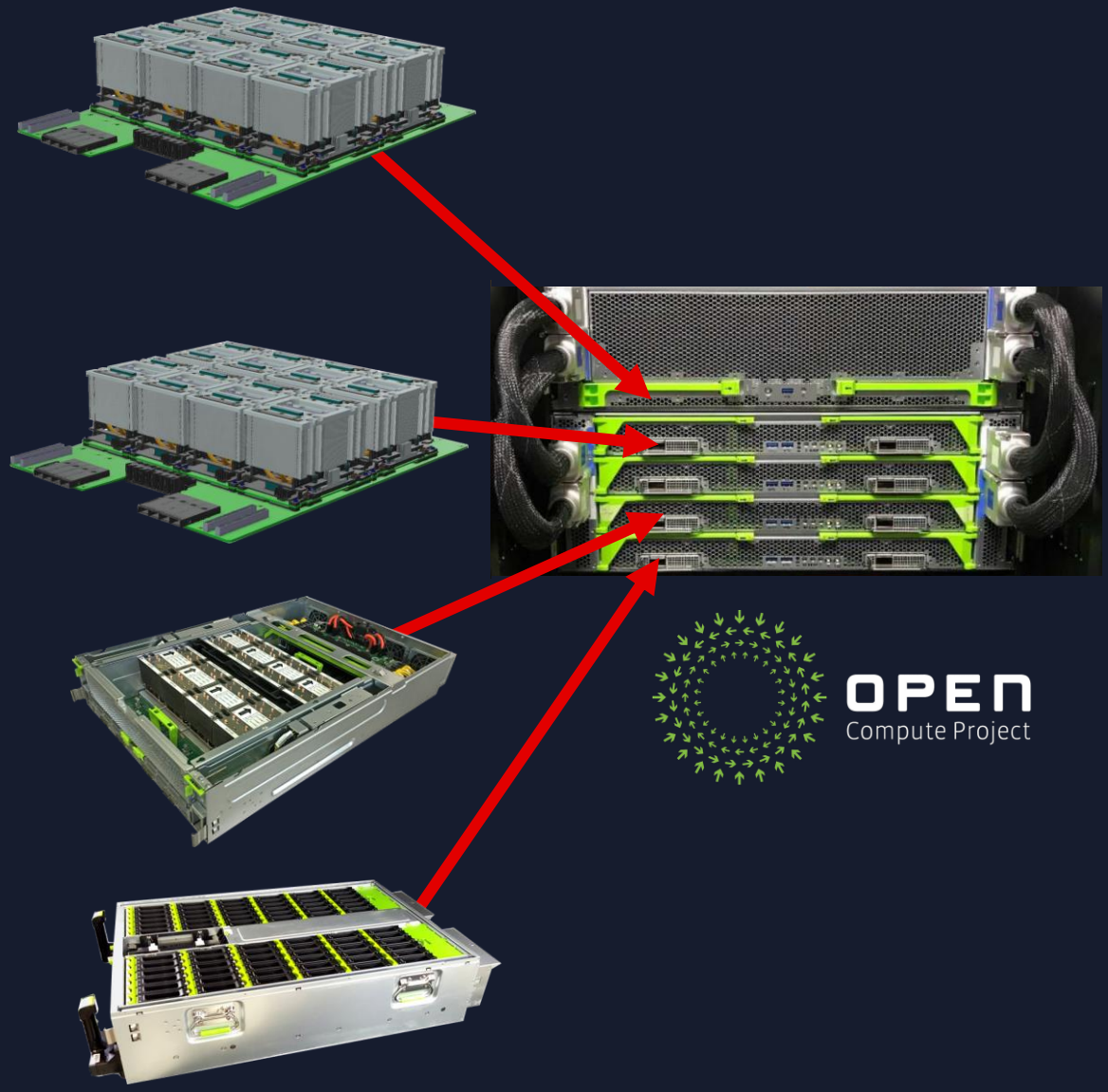
Scale-Out : Disaggregation of Compute And Storage





OPEN Compute Project

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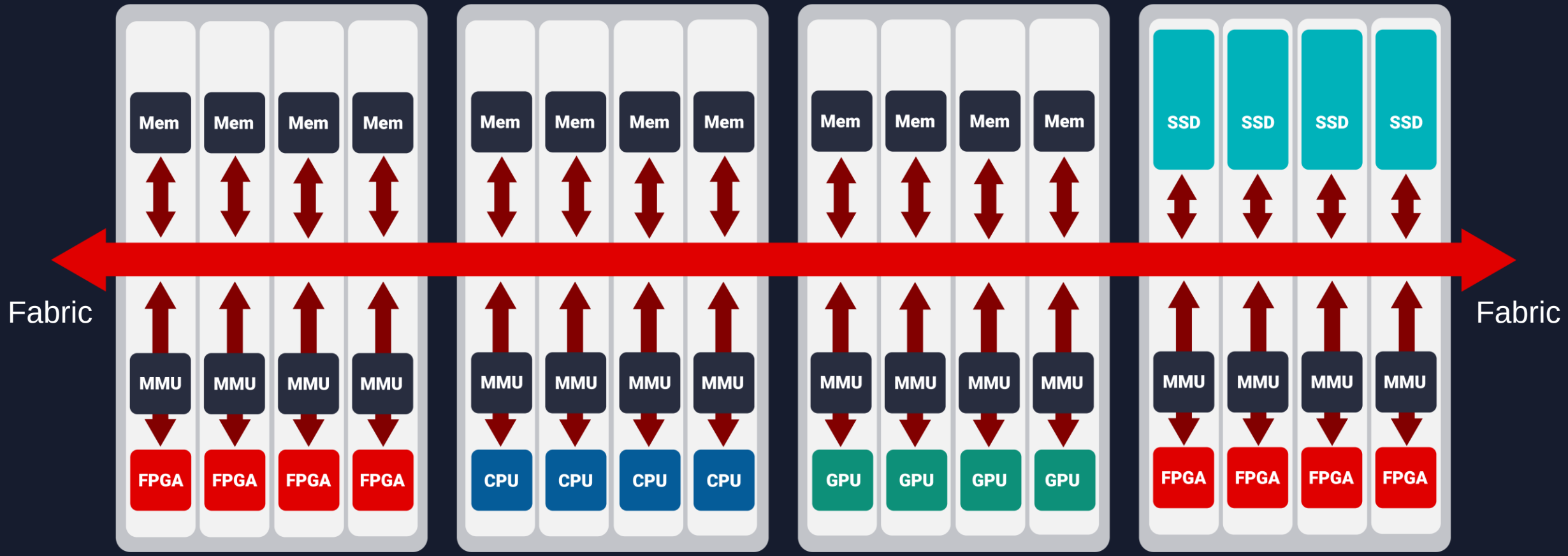
Data “In-Use” In Distributed Memory



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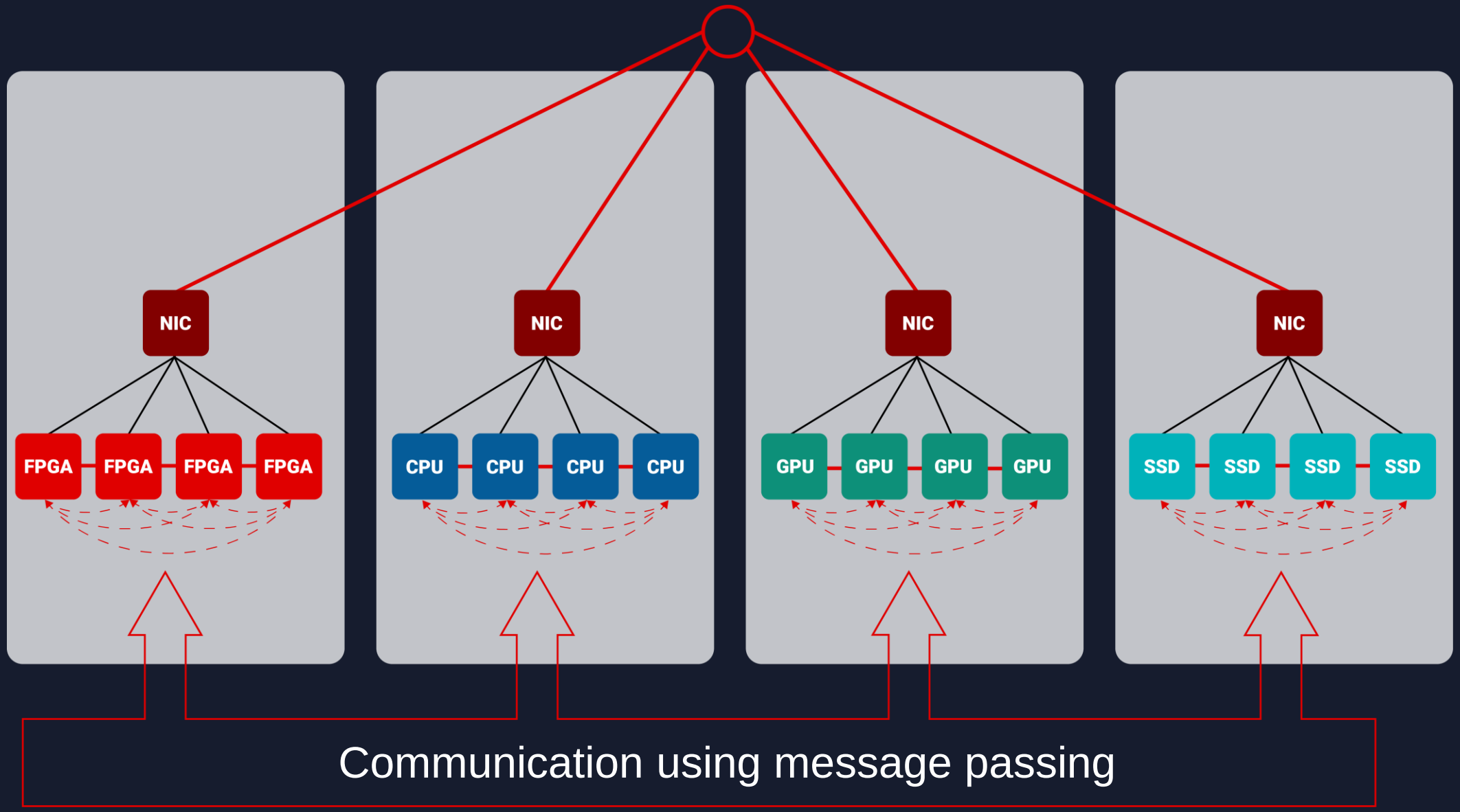
Software view : Local memory & message passing



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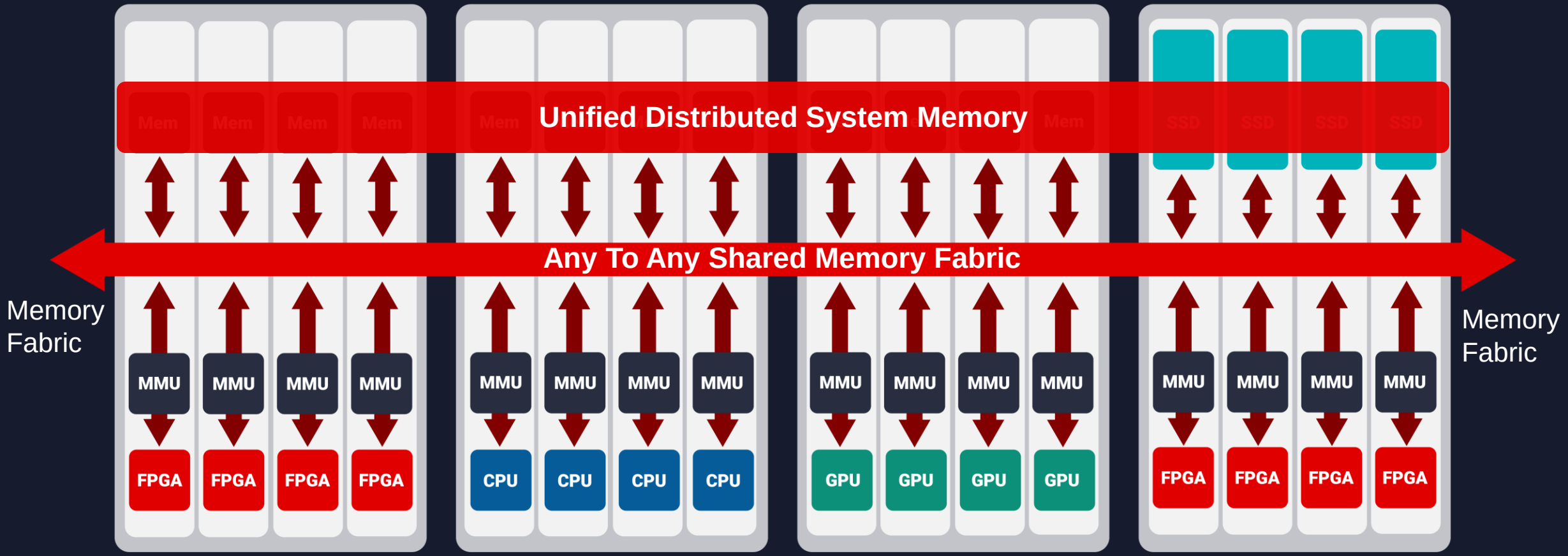
Future Programmer's View: Unified Memory



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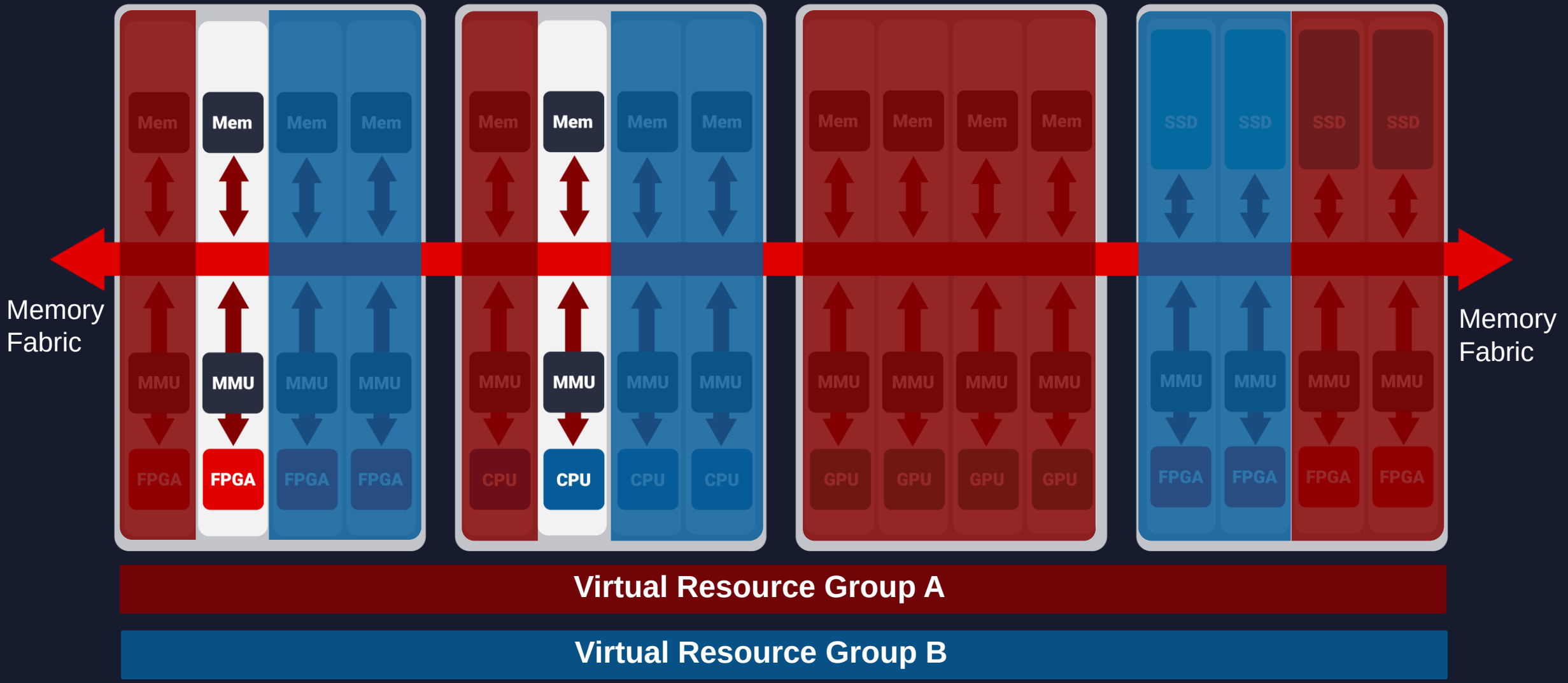
Future: Shared Virtual Address Spaces



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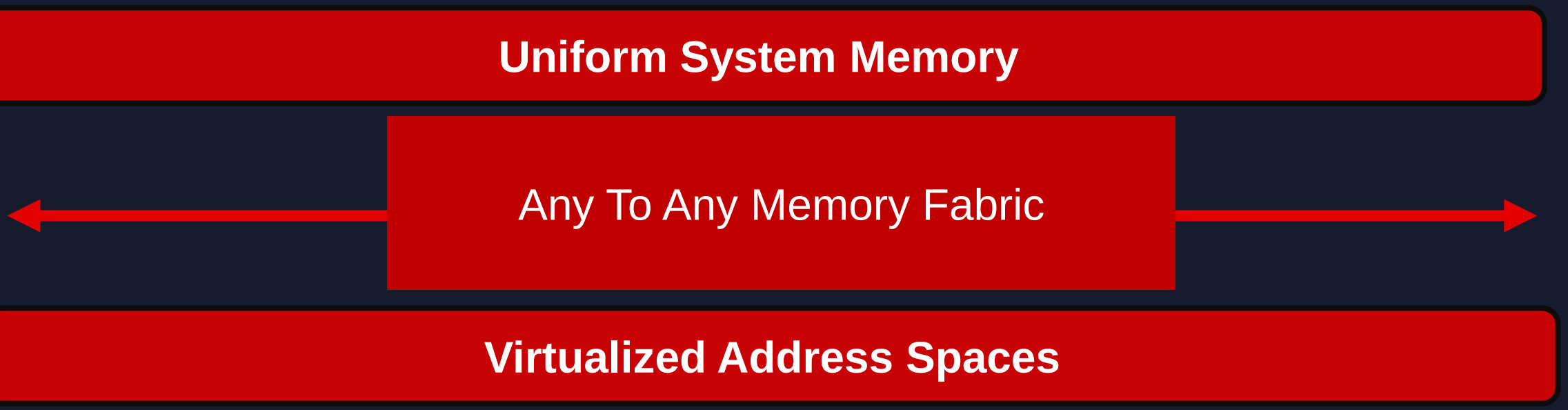
Software Abstraction for Exascale Compute



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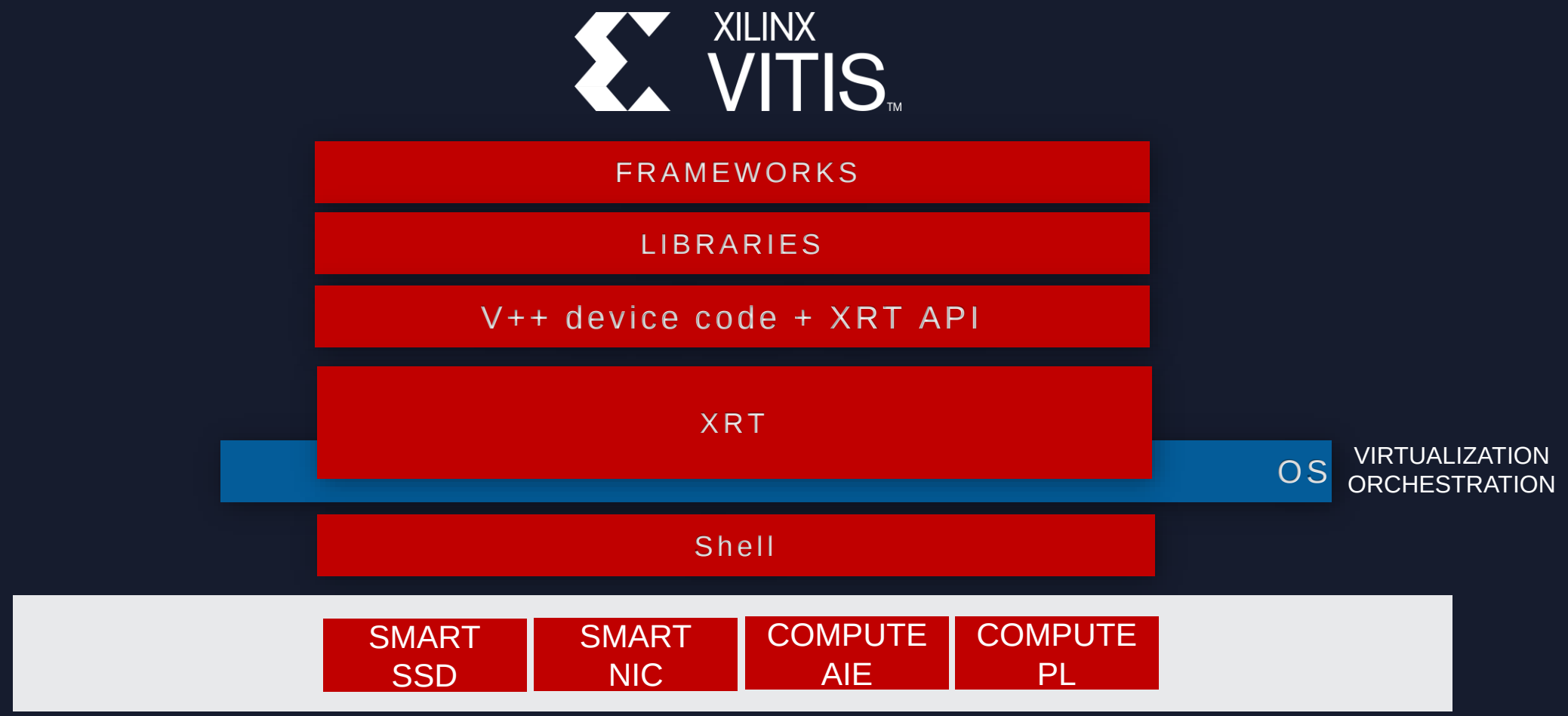
VITIS Software Stack

Enables Smart NIC|SSD + Heterogeneous Compute



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Conclusions

Future

- Exascale computing and data - driven by new workloads such as AI
- Increase compute power by
  - Scale-up of compute nodes
  - Scale-out of network
- Enabled by Accelerators, SmartNIC and SmartSSD
  - Compute on data-in-use
  - Compute on data-in-motion
  - Compute on data-at-rest
- Software stack :
  - Higher level of programming abstraction
  - Runtime enabling heterogeneous compute fabrics
  - Shared virtual address spaces

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Thank You