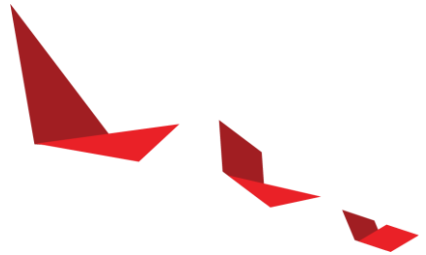
Agenda

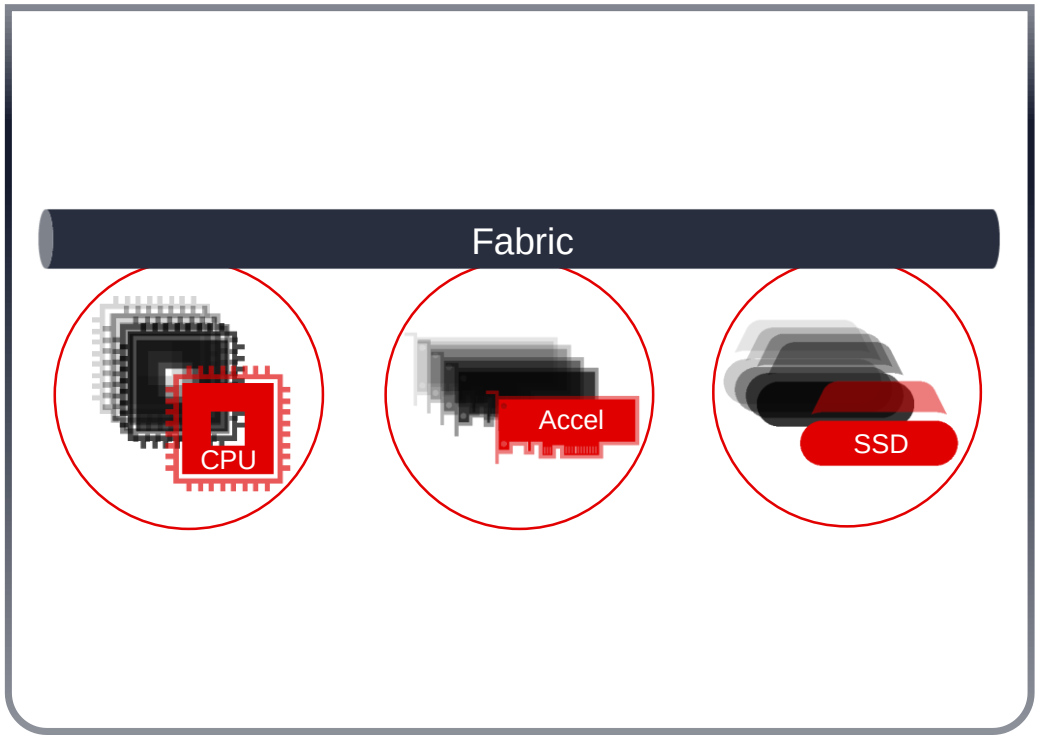


- SmartNIC Evolution and Industry Challenges
- Introducing the SN1000 Composable SmartNIC
- Architecture and Use Cases

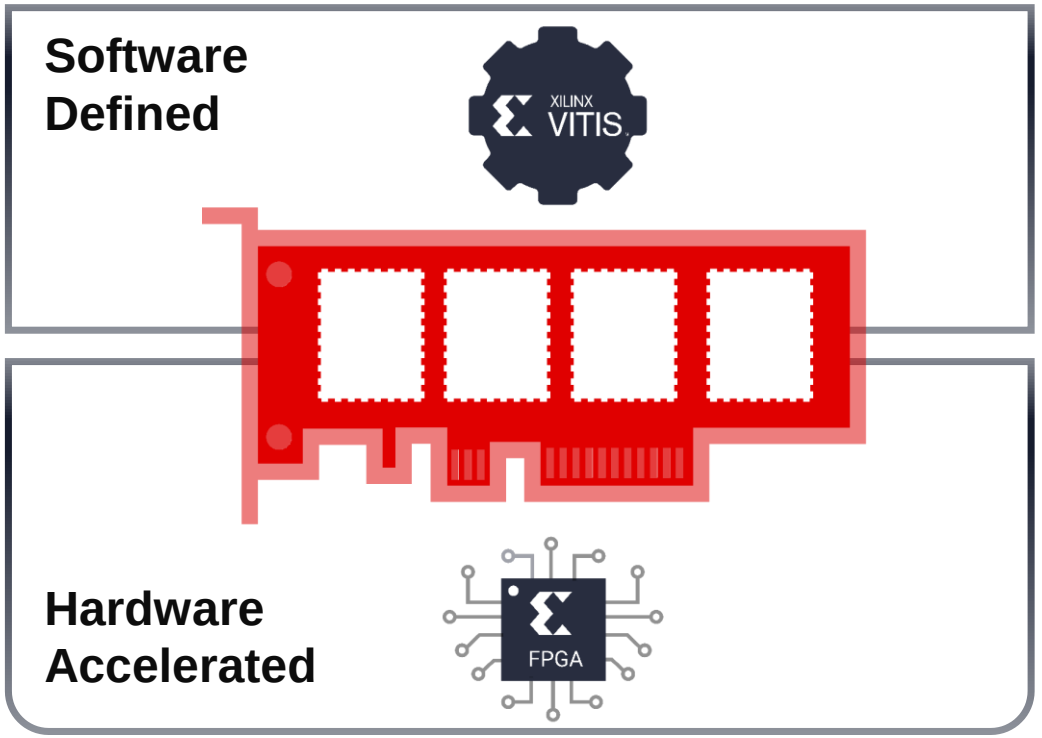
The Composable Datacenter

There Is No “Typical” Datacenter

Requires not just disaggregated compute, network, and storage…



…but composability of the *device* itself



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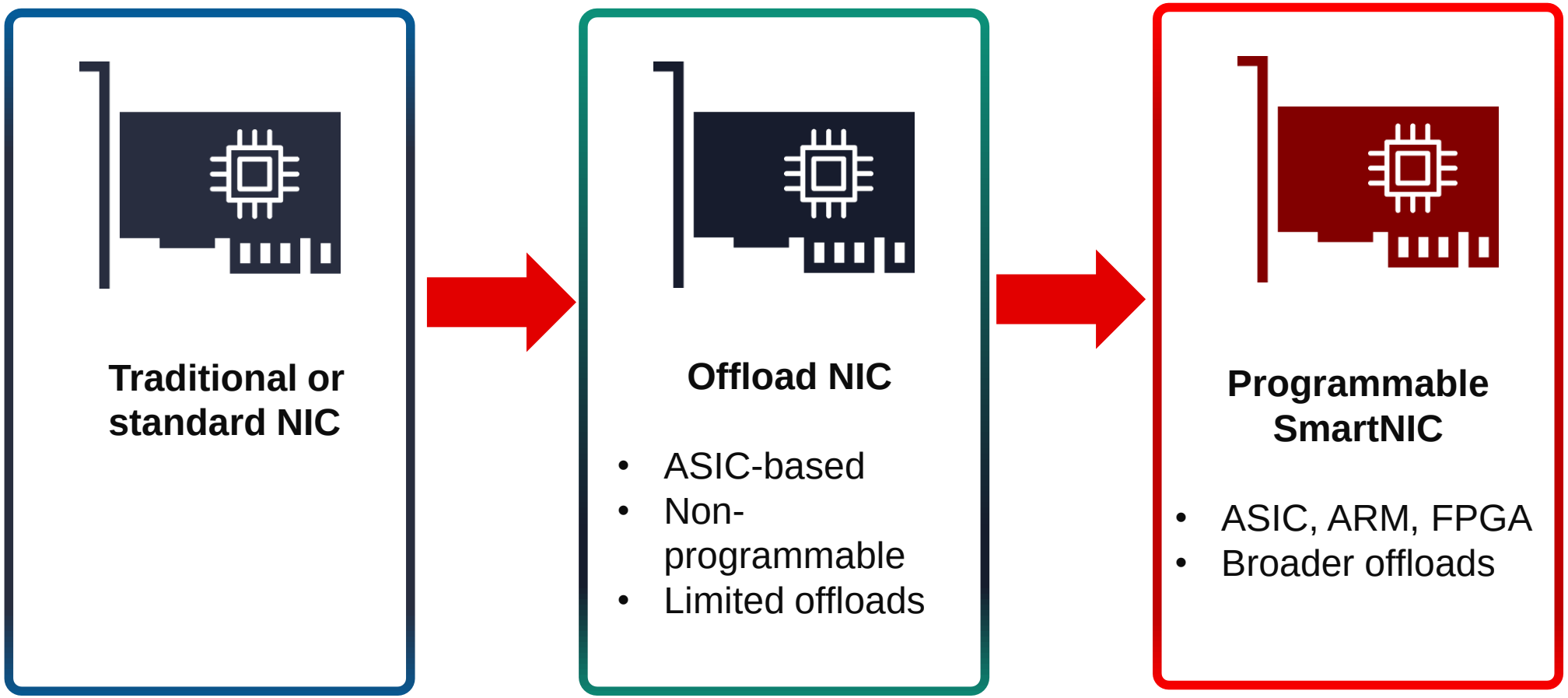
Evolution of the NIC



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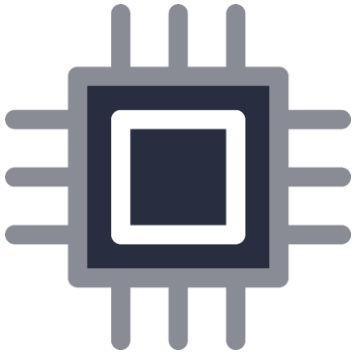
SmartNICs: Emerging Limitations

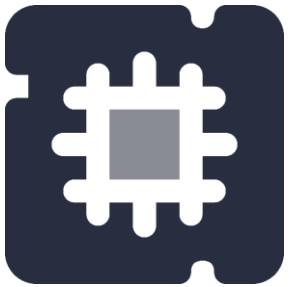
Cloud providers need both performance *and* adaptability

- Fast pace of change
- Wide variety of network functions
- Every Hyperscaler and CSP has different needs

BUT…



ASIC implementations lack customization capabilities



CPU/SOC implementations suffer performance hits at scale

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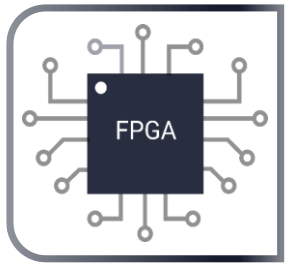
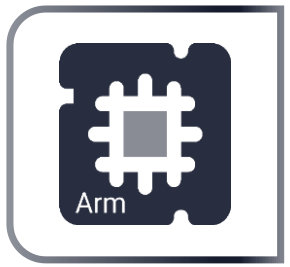
Introducing The Xilinx Alveo SN1000



The Adaptability of Xilinx FPGAs

+



Isolated Control and Data Planes

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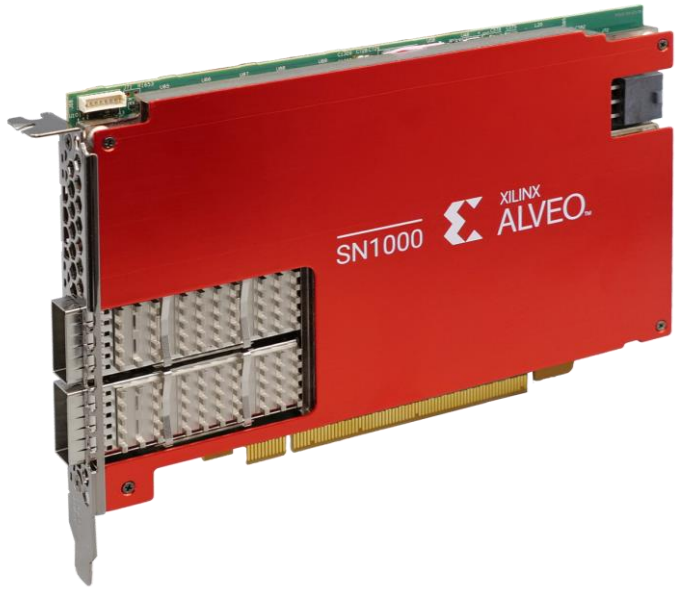
Vitis Networking:
P4, C, C++ Programming

=

The Industry's First SmartNIC with *Composable Hardware*



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SN1000 SmartNIC Summary

Hardware
- 100G
- PCIe Gen3 x16 or Gen 4 x8
- QSFP28 Direct Attach Copper | SR Optical
- 75W
- Form Factor: FHHL

Net. Offloads/Virtualization
- Stateless and Tunneling Offloads
- SR-IOV, Multiqueue
- VirtIO-net
- vDPA

Networking Acceleration
- Onload®
- DPDK Poll Mode Driver
- OVS

Storage Acceleration
- VirtIO-blk
- CEPH RBD Client Offload

FPGA
- 1M+ LUTs
- Memory: 2x 4GB x 72 (FPGA)

On board CPU
- Up to 16-core A72
- Memory: 1x 4GB x 72

FPGA Custom Acceleration Plugins
- Networking, Storage, Security, Compute
- P4 / RTL / HLS

OS Support
- Linux

Manageability and Pre-boot
- PXE, UEFI w/ HII
- MCTP SMbus, MCTP PCIe, and PLDM
- Secure Firmware Upgrade

XCU26
UltraScale+

LX2162A

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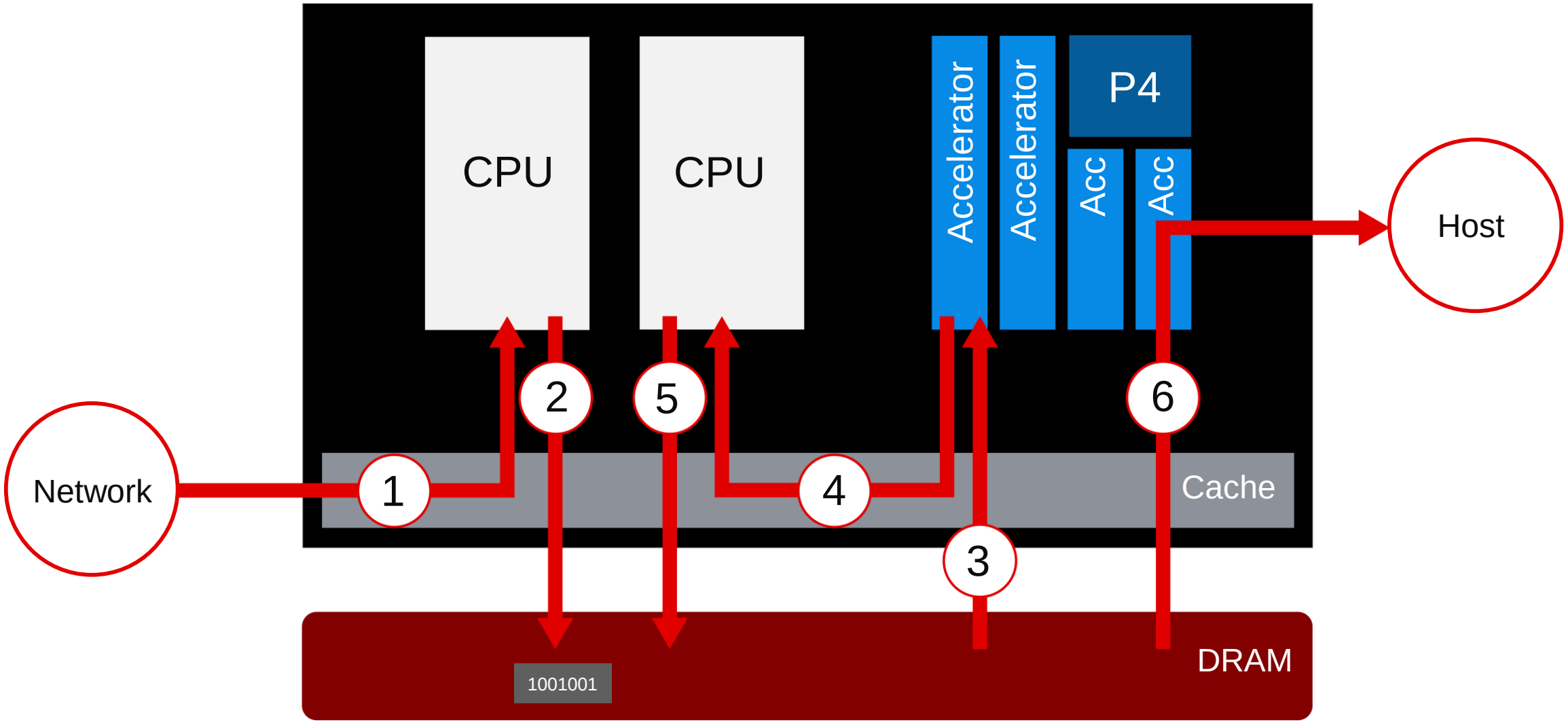
SN1000 Architecture

Rip Sohan

Conventional SmartNIC Bottlenecks



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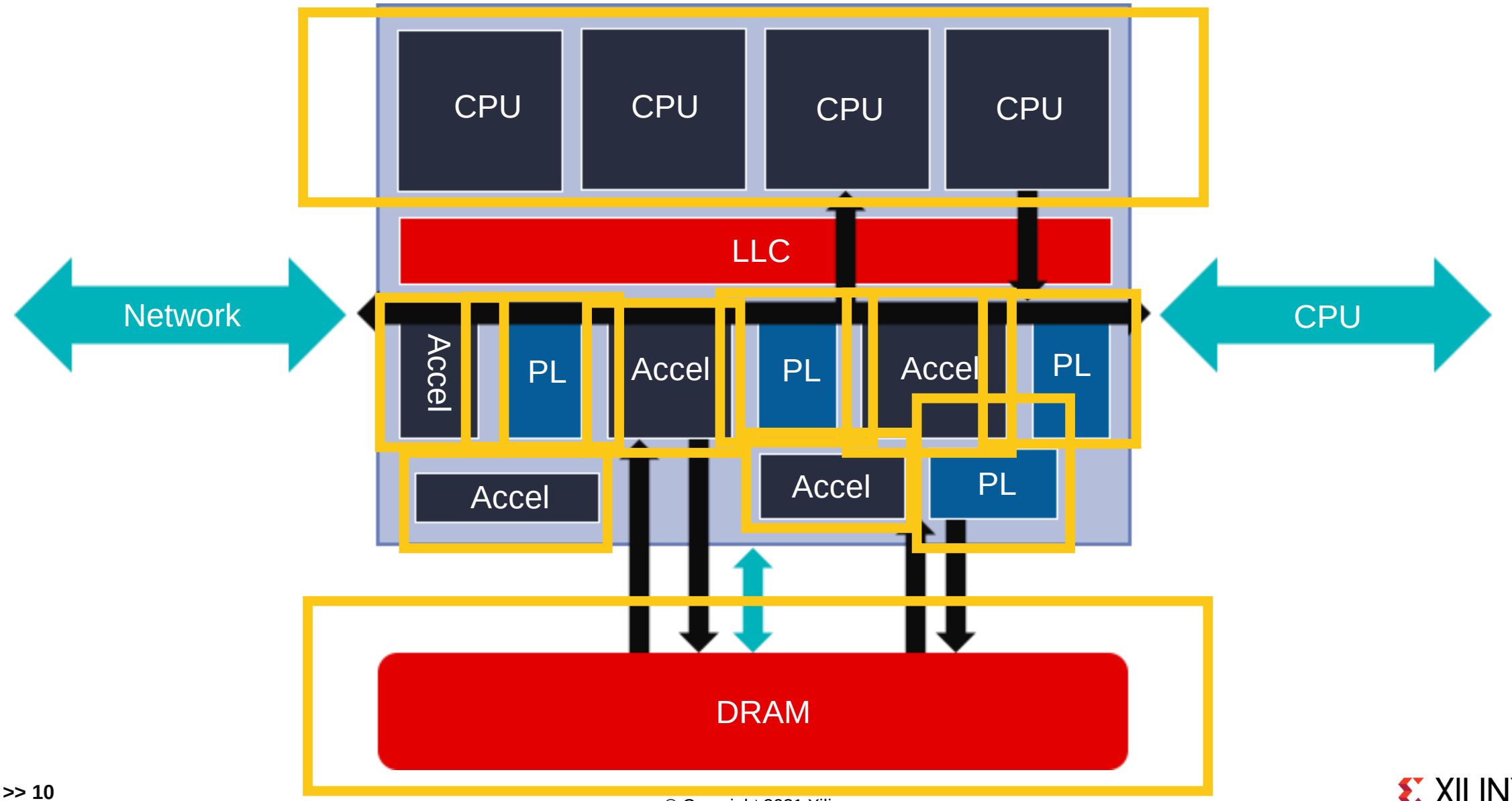
The Xilinx Composable SmartNIC Architecture



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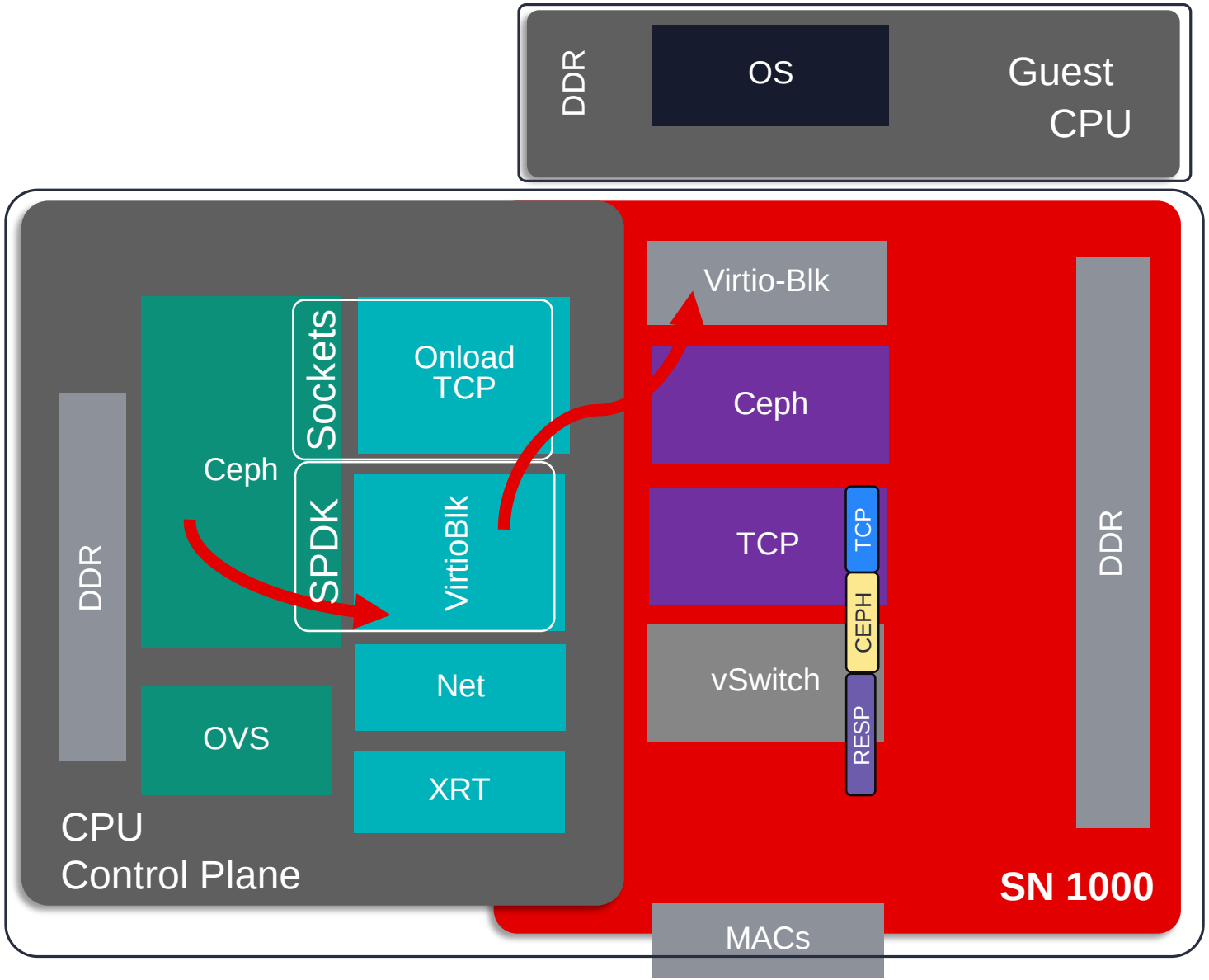
Support For Application-Specific Data Plane Accelerators

1. Can be composed of Standard and Application Specific Accelerators

2. Can be chained to perform L2-L7 processing without requiring control or data transfer to on-board CPUs

3. Native support for P4 and HLS C/C++

Example: Storage Virtualization on Composable NIC



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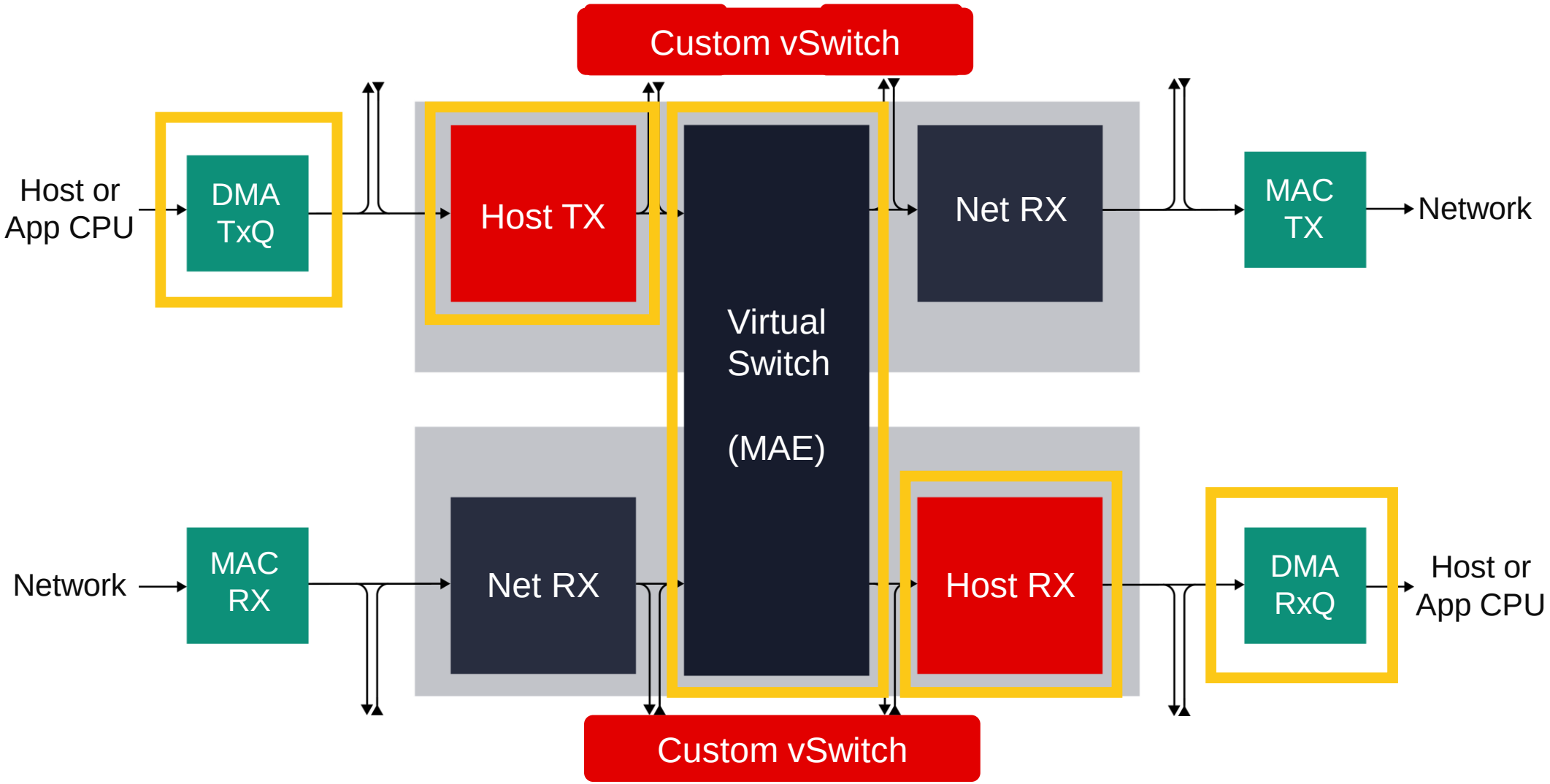
A Portable NIC Architecture



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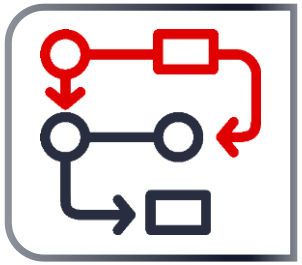
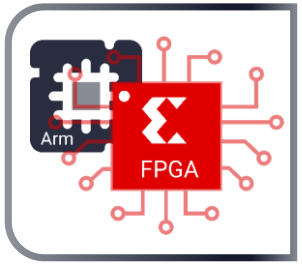
The SN1000 Difference

Software-defined hardware acceleration for all offloads



Application specific data paths at line-rate performance

P4 , C, C++ programming for fast, adaptable hardware acceleration



Heterogeneous architecture with control and data plane isolation

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Thank You

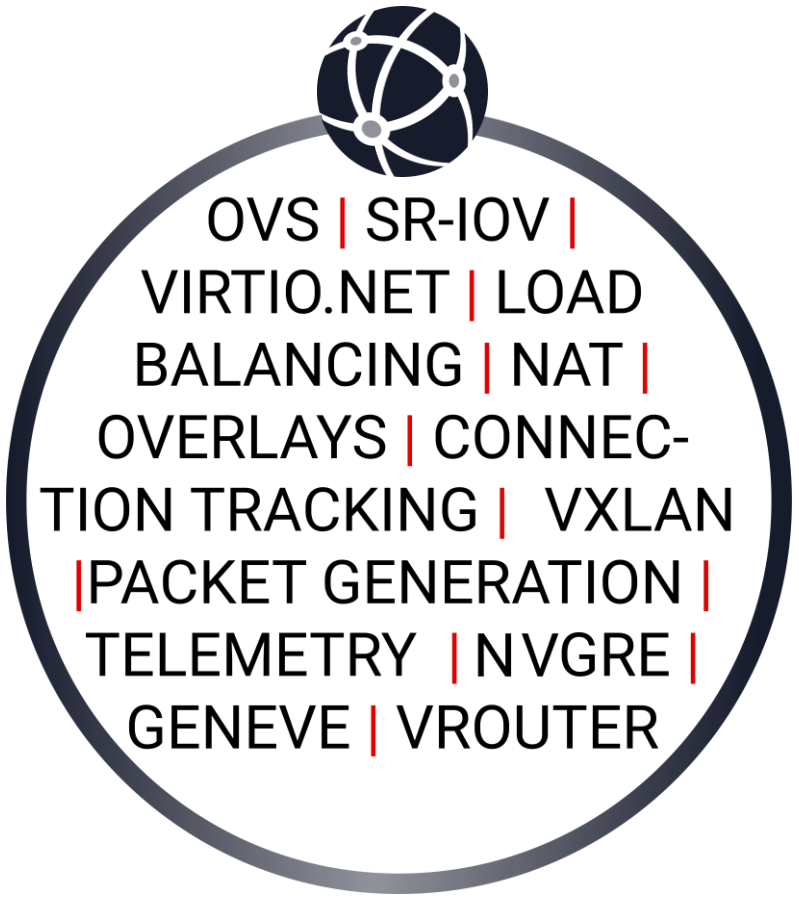
Common Offload Types

NETWORKING

SECURITY

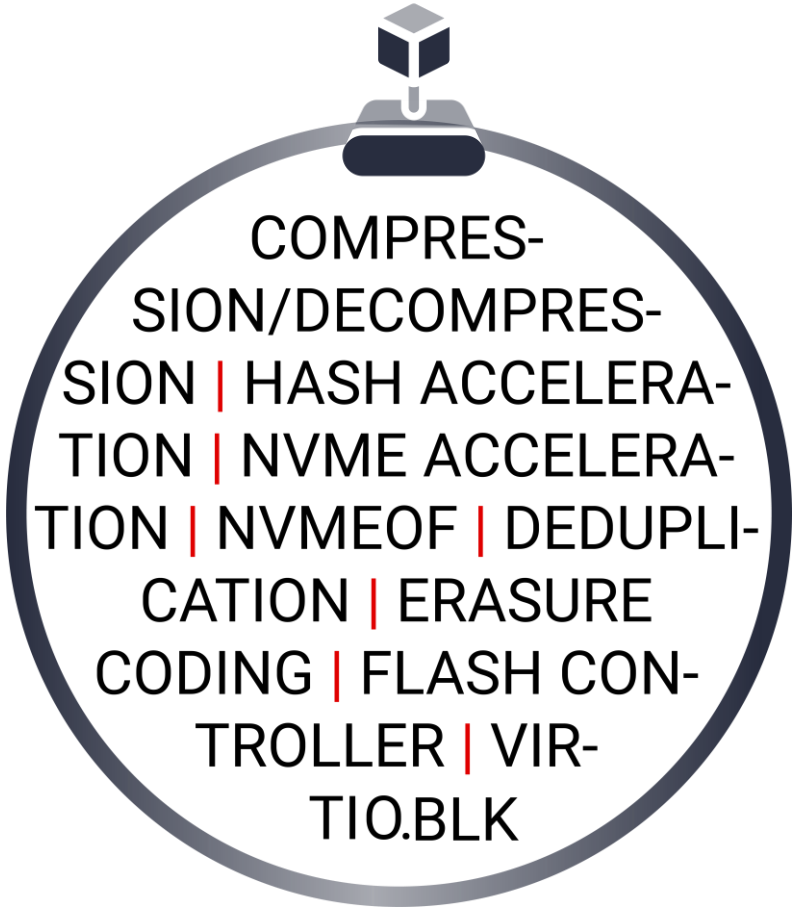
STORAGE

Common Offload Types



NETWORKING

SECURITY



STORAGE

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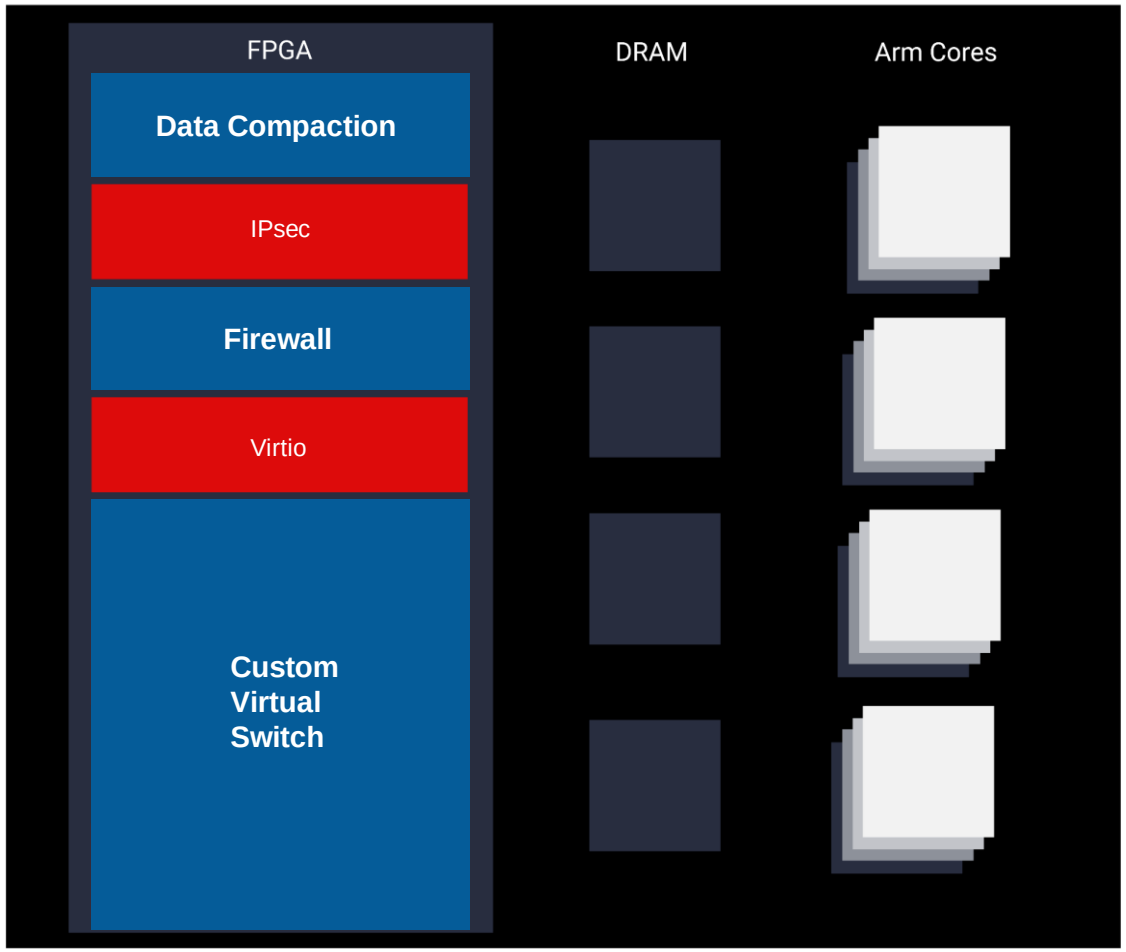
Introducing The Xilinx Alveo SN1000

- **Software-defined hardware acceleration**
- Application specific data paths
- Build **custom offloads** or **extend existing offloads** to handle new protocols and applications

Composability Example 2



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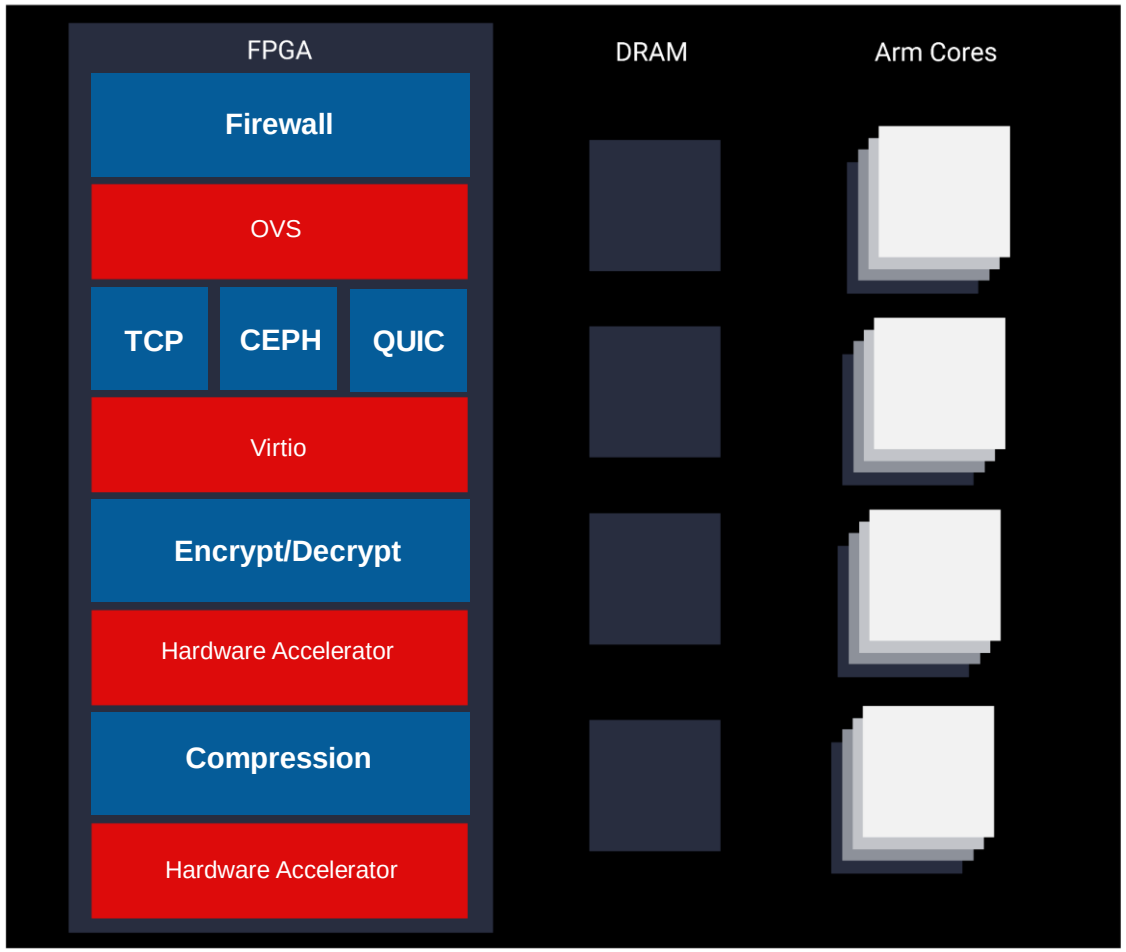
Example 1



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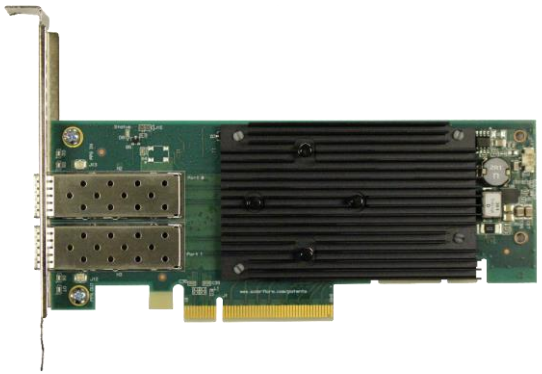
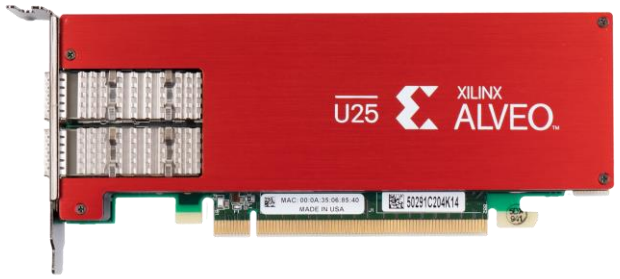
Xilinx NIC Family



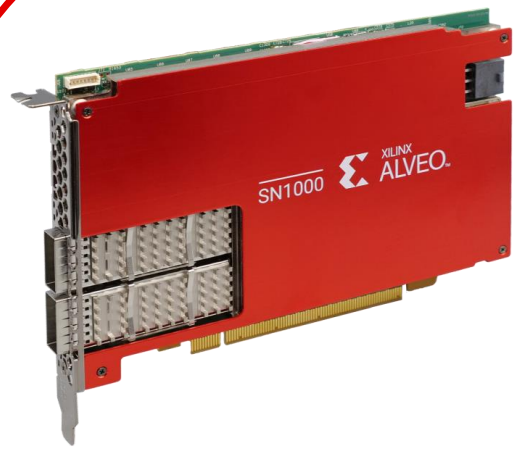
X2

10/25/100Gb Offload NIC



U25

25Gb SmartNIC



SN1000

100Gb SmartNIC

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Introducing The Xilinx Alveo SN1000

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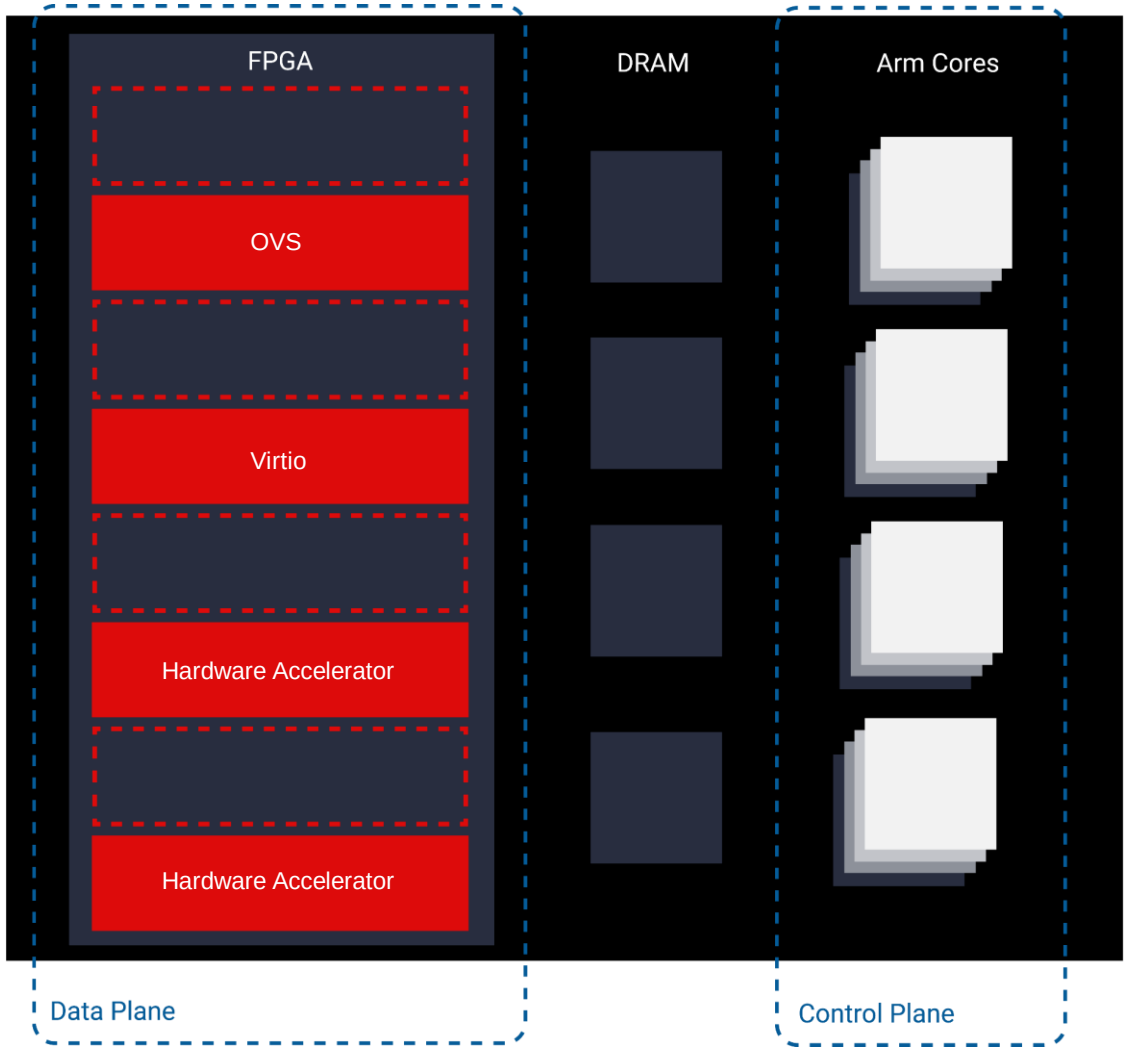
- Application specific data paths
- Build **custom offloads** or **extend existing offloads** to handle new protocols and applications

Composable Architecture



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Introducing The Xilinx Alveo SN1000

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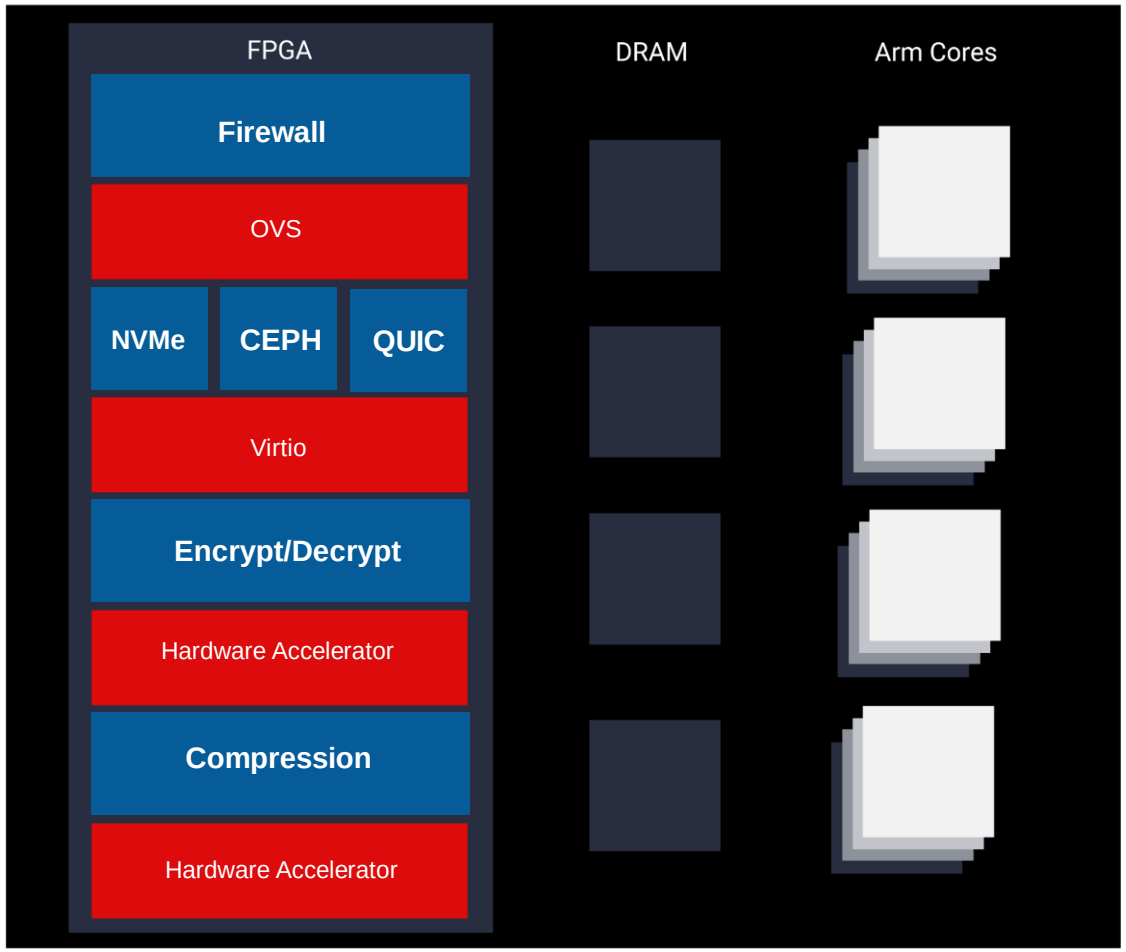

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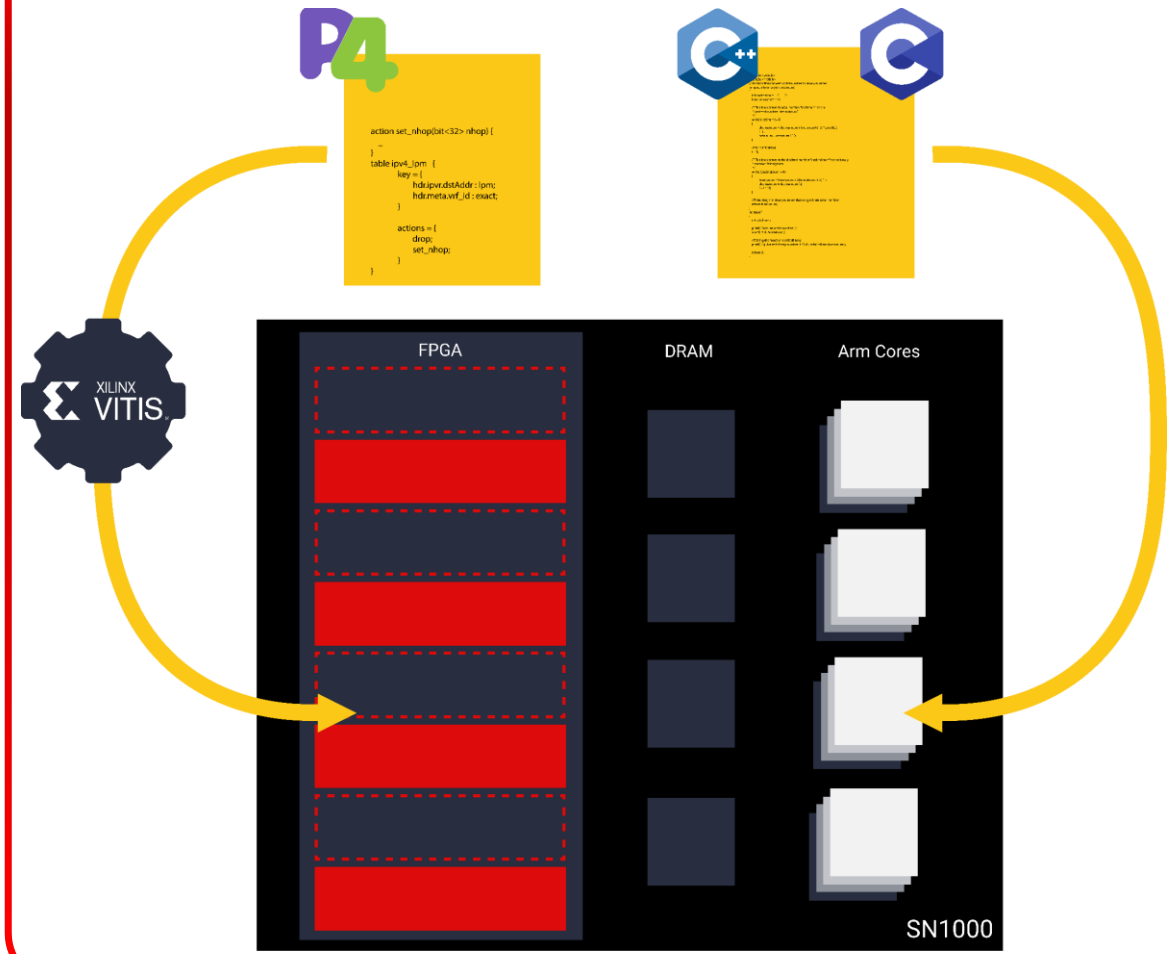
Vitis Networking

- **Customize with ease, without sacrificing performance**
- **P4: the perfect match for "Match-Action" processing**
  - Tailored for high-performance networking
  - Includes high performance algorithmic CAM technologies
- **Vitis RTL/HLS-** Mature developer tools for any compute or storage offloads at HW speeds with powerful high level language support
- **Xilinx SmartNIC Plug-In Framework**
  - Customizations can be easily embedded into the powerful SN1000 SmartNIC flow

Software-Defined Hardware Acceleration



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