Emeraude INSA Team Builds Low Latency Tech for Sound Synthesis and Acoustic Control

Audio DSP to FPGA Compilation Solution Powered by AMD Zynq™ SoCs and Vitis™ HLS

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INDUSTRY

Embedded Audio Programming Systems

CHALLENGES

Design a tool allowing audio DSP programmers to implement any audio DSP algorithm on an FPGA with a very low latency.

SOLUTION

Connect the output of an audio DSP language compiler (i.e., Faust) with an HLS tool: AMD Vitis™ HLS.

RESULTS

The result is a new compilation flow compiling any audio DSP program automatically onto an AMD Zynq™-based FPGA board.

AMD TECHNOLOGY AT A GLANCE

Zynq™ SoC

Existing real-time digital audio systems can hardly reach a latency below 1ms from audio input to output. 200µs is actually the best latency that was achieved up to now. The Emeraude research team at INSA (France) is developing the Syfala compiler which combines Faust, a domain specific language for real-time audio DSP, and AMD Vitis™ HLS, to provide a very high-level synthesis tool for audio DSP users.

Emeraude managed to reach a latency of 11µs on many simple DSP programs using an AMD Zynq™-based FPGA board, a low latency audio codec, and the Syfala compiler. This new technology is used for sound synthesis and active acoustic control.

CHALLENGE

Real-time audio Digital Signal Processing (DSP) has been implemented on a wide range of computer architectures: Von Neuman CPUs, multi-cores, GPUs, dedicated circuits, FPGAs, etc. However, the only way to achieve ultra-low latency (i.e., less than 1ms) is to use dedicated circuits such as ASICs or FPGAs. However, using FPGAs is almost impossible for DSP programmers as they do not have hardware design skills. Hence, the main challenge of this project was to design a tool allowing audio DSP programmers to implement any audio DSP algorithm on an FPGA with a very low latency (i.e., less than 100µs).

SOLUTION

The solution that was adopted connected the output of an audio DSP language compiler (i.e., Faust) with an HLS tool: Vitis HLS. The Faust compiler handles the hardware/software partitioning and isolates the kernel DSP algorithm to be implemented on the FPGA, as shown in Fig. 1.

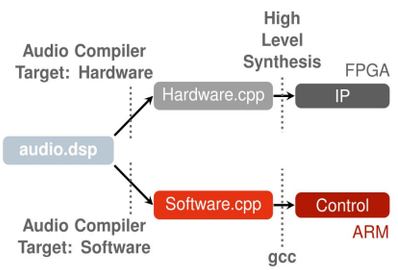

Figure 1: Syfala compilation flow from Faust programs to FPGA.

Vitis HLS is used to implement hardware for this kernel DSP, enabling access to external DDR memory as well as hardware controllers using the ARM Zynq processing system driver.

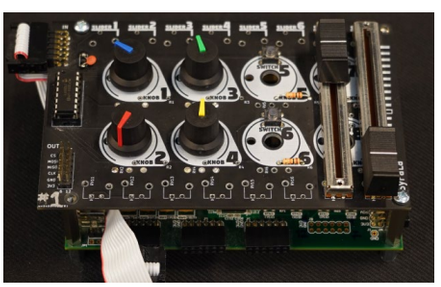

Figure 1: Hardware control for DSP implemented on a Digilent Zybo Board.

"Vitis HLS allows us to reuse directly the C++ code generated by the Faust compiler, hence no manual design process is needed from the Faust high-level specification down-to the FPGA bitstream," stated Tanguy Risset, research lead at INSA-LYON. "Moreover, Vitis HLS is very well integrated to the AMD design flow and allows us to perform hardware/software co-design."

RESULT

The result is a new compilation flow compiling any audio DSP program automatically onto AMD Zynq 7000-based FPGA boards such as Digilent Zybo or Genesys. The implemented programs can reach a latency of 11µs from analog input to analog output. Such a short latency has never been achieved before. The compiler is open-source and is currently used to implement active acoustic control algorithms and 3D audio coding and decoding processes.

"Vitis HLS allows us to precisely control the latency of the IP," Risset added. "In particular Vitis HLS was able to generate an IP that has a one sample delay latency. This was very important to achieve the latency that we reached from analog to analog."

Risset said the scheduler view of Vitis HLS IP was useful to understand how parallelization is guided by Vitis HLS and how memory access influences IP latency. "This pushed us to optimize memory accesses in the C++ code generated by Faust which was necessary step to reach low latency," he added.

WANT TO LEARN MORE?

About AMD's Zynq SoCs

About Emeraude INSA Research Team

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The Emeraude INSA research team is studying embedded audio programming systems and is also maintaining the Faust compiler.

About Syfala Compiler

The Syfala compiler is currently available on GitHub and can be used on any Zynq-based boards coupled with any I2S audio codecs. It is also used in the context of non-ultra-low latency audio: for multi-channel applications such as high order ambisonics, etc.

About AMD

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