



**(Preliminary Agenda) 2018 Functional Safety Working Group (FSWG)**

The Inn at St. John's, 44045 Five Mile Road, Plymouth, Michigan 48170

**Day 1 June 19, 2018**

<b>Topic</b>	<b>Presenter</b>	<b>Time</b>
<b>Check In 7:15 / Continental Breakfast</b>		7:15 - 8:00 AM
<b>Welcome/Intro: Xilinx Functional Safety Solutions</b>	<b>Xilinx</b>	8:00 - 8:30 AM
<b>Keynote</b>	<b>TBD</b>	8:30 - 9:30 AM
<b>Xilinx Functional Safety Solutions State of the Union</b>	<b>Xilinx</b>	9:30 - 10:30 AM
<b>Break</b>		10:30 - 11:00 AM
<b>Zynq UltraScale+ Overview</b>	<b>Xilinx</b>	11:00 - 12:00 PM
<b>Lunch</b>		12:00 - 1:00 PM
<b>Zynq UltraScale+ Common Cause Mitigation</b>	<b>Xilinx</b>	1:00 - 2:00 PM
<b>Zynq UltraScale+ Security Capabilities for Safety applications</b>	<b>Xilinx</b>	2:00 - 3:00 PM
<b>Break</b>		3:00 - 3:30 PM
<b>Zynq UltraScale+ Isolation Capabilities &amp; Implementation</b>	<b>Xilinx</b>	3:30 - 4:30 PM
<b>Day One Wrap Up</b>	<b>Xilinx</b>	4:30 - 4:45 PM
<b>June 19, 2018 : Day 1 Social</b>		
<b>Join us for light appetizers and cocktails</b>		4:45 - 7:30 PM



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### Day 2 June 20, 2018

Topic	Presenter	Time
Re-Check In 7:30 / Continental Breakfast		7:30 - 8:00 AM
Quality and Reliability	Xilinx	8:00 - 9:00 AM
Soft Error Mitigation in FPGA Memory	Xilinx	9:00 - 10:00 AM
Break		10:00 - 10:30 AM
Isolation & Partial Reconfiguration in FPGAs	Xilinx	10:30 - 11:30 AM
Xilinx IP Solutions for Functional Safety	Xilinx	11:30 - 12:15 PM
Lunch		12:15 - 1:15 PM
Functional Safety in FPGAs/Programmable Logic	Xilinx	1:15 - 2:15 PM
Zynq Safety Design Example	Xilinx	2:15 - 3:15 PM
Break		3:15 - 3:45 PM
Zynq-7000 Safety Design Example - Metrics Calculation	Xilinx	3:45 - 4:45 PM
FSWG Adjournment and Call to Action	Xilinx	4:45 - 5:00 PM