Characterization of DDR4 Receiver Sensitivity Impact on Post-equalization Eye

Yong Wang, Xilinx Inc.
Thomas To, Xilinx Inc.

Penglin, Xilinx Inc. , Fangyi Rao, Keysight Inc.,
Juan Wang Xilinx Inc., Sean Long Xilinx Inc.

SPEAKERS

Yong Wang

Sr. Director, Xilinx Inc.
yongw@xilinx.com

Thomas To

Technical Director, Xilinx Inc.
tto@xilinx.com

Outline

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  - Channel Signal Attenuation
  - Simple DDR Receiver and Input Mask
  - Jitter Measurement Point for Simple DDR Receiver
- **Problem Statement**
  - Traditional Simulation Approach with CTLE receiver
- **CTLE Receiver and Output Eye Mask**
  - Overview of CTLE in Signal Improvement
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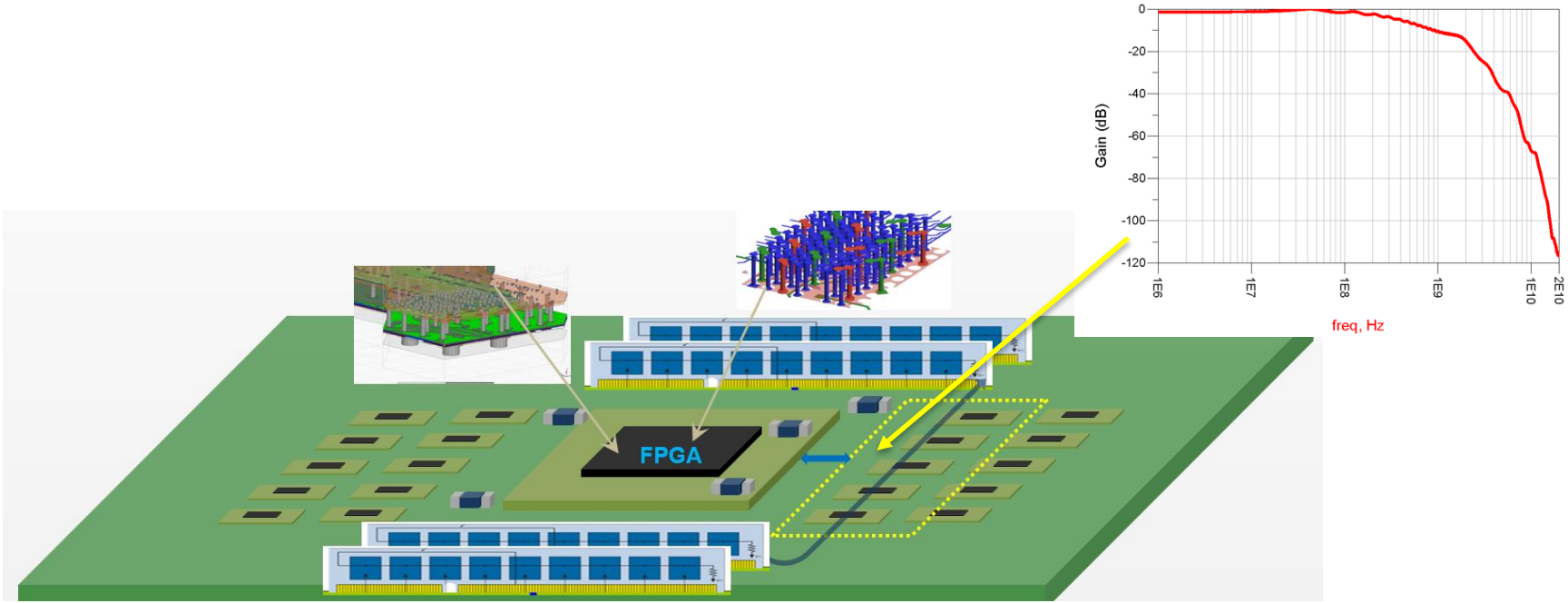
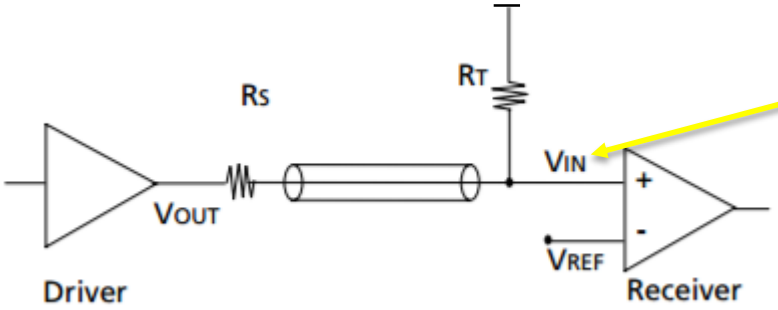
- **Channel Simulation in DDR4 system**
  - Traditional Simulation Approach with CTLE receiver
  - DJ Incorporation in Statistical Simulation approach
- **Conclusion**

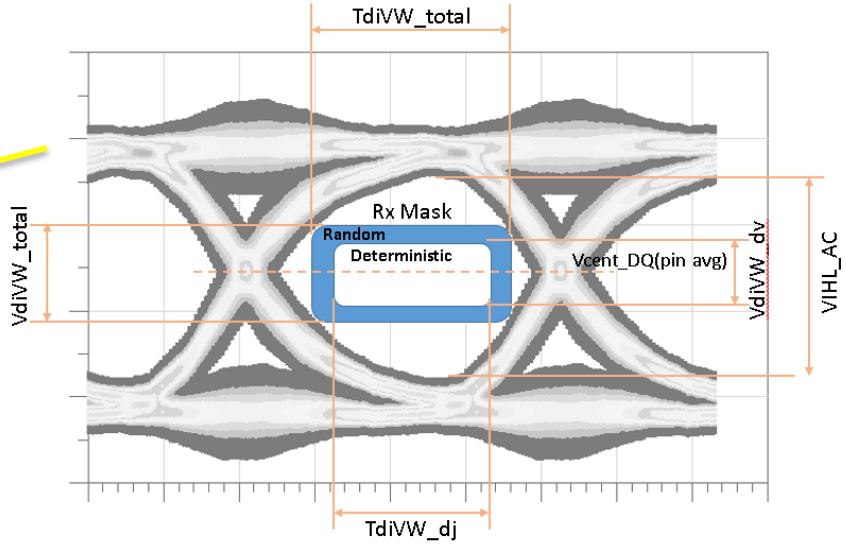
A Typical DDR System & Channel Attenuation



→ *DDR Channel Attenuation becomes more significant as data rate increases!*

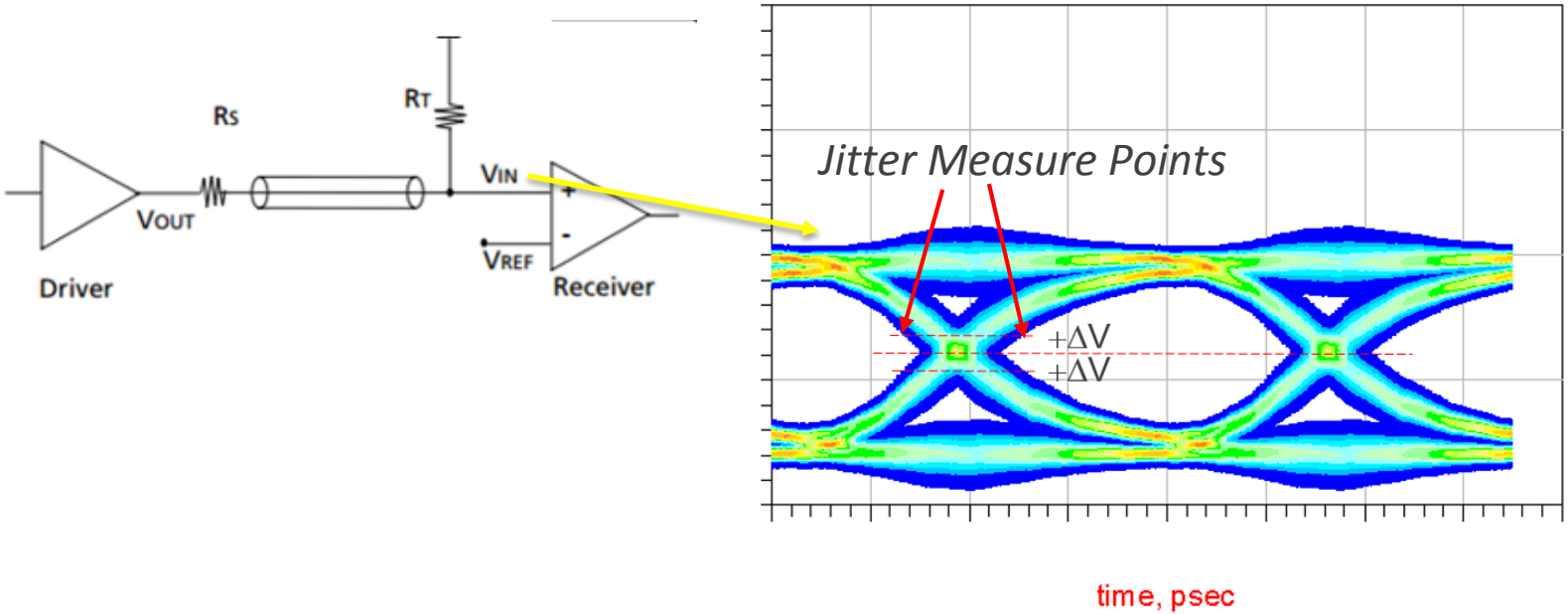
Simple DDR Receiver & Input Mask





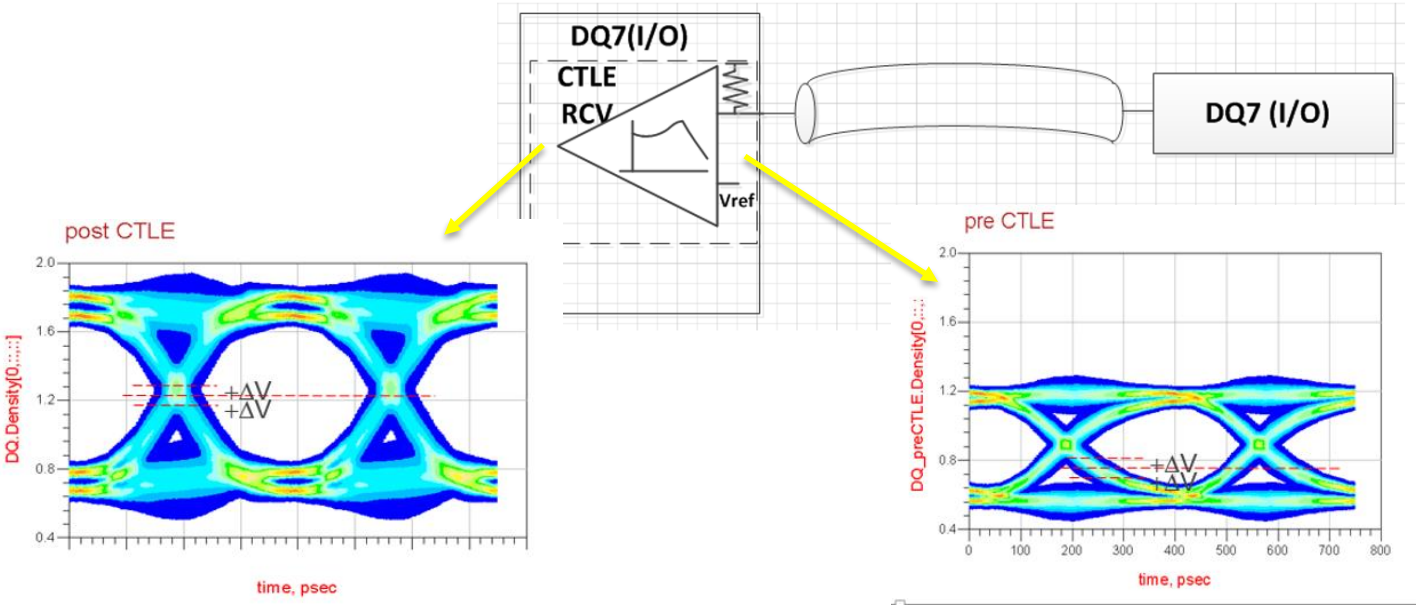
→ *Voltage and Timing Sensitivity (Rx Mask) is to guarantee Rx to capture correct signal state.*

Jitter Measurement Point for Simple DDR Receiver



→ *Timing jitter measurement at the Rx Mask defined threshold.*

Traditional Jitter Measurement Point in CLTE

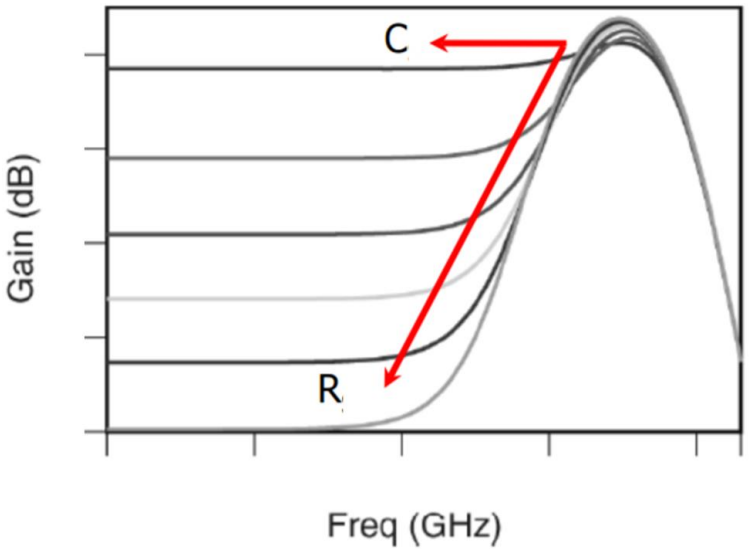


→ *CTLE improves incoming signal jitter.*

→ *One way is to impose Rx input threshold to the output of the CTLE Rx.*

→ *This leads to pessimistic jitter measurement !*

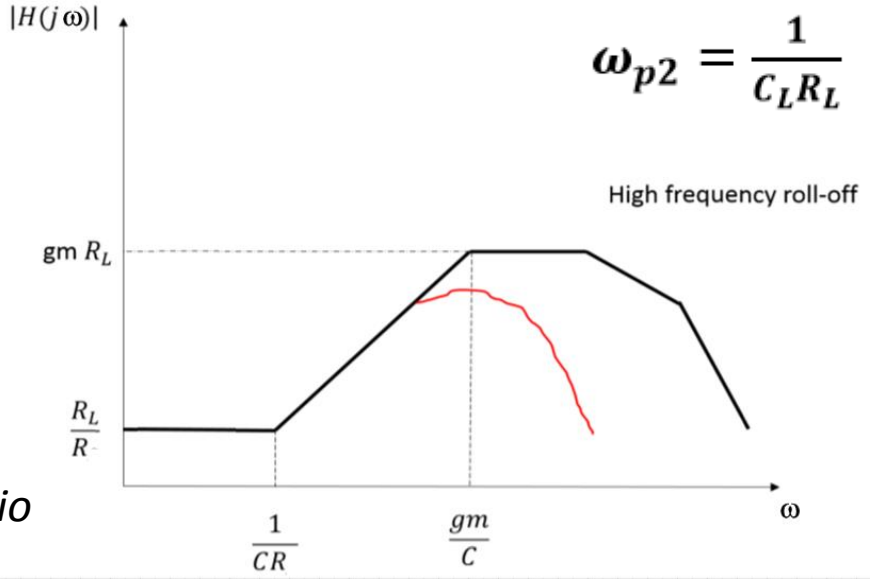
CTLE High Frequency Roll Off



$$\omega_z = \frac{1}{CR} \quad (1)$$

$$\omega_{p1} = \frac{1+g_m R/2}{CR} \quad (2)$$

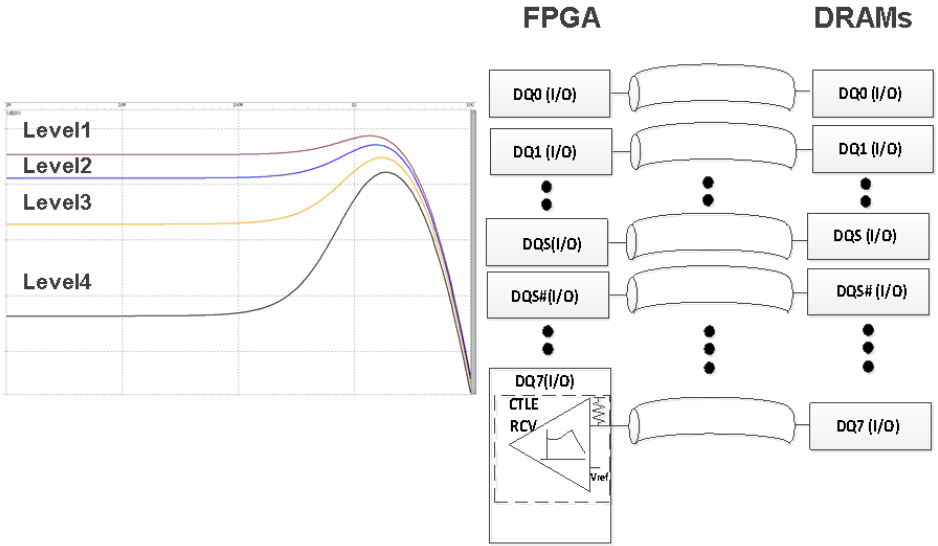
$$\omega_{p2} = \frac{1}{C_L R_L} \quad (3)$$



→ *CTLE has active gain stage.*

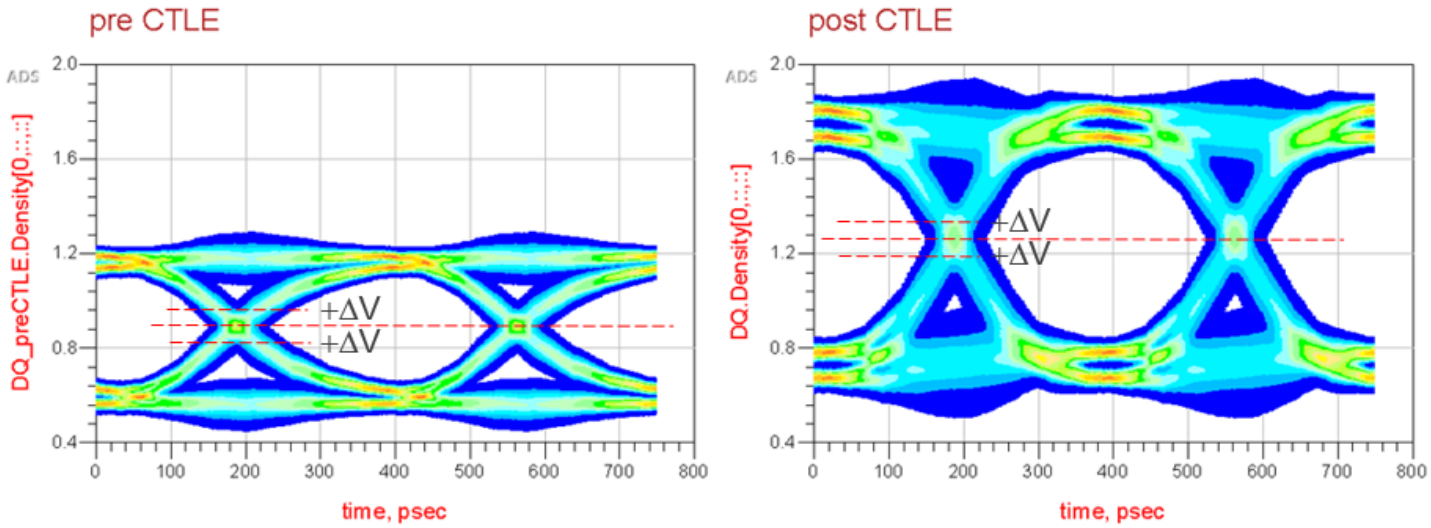
→ *CTLE uses degeneration resistor & capacitor to tune low to high freq. ratio*

CTLE in Memory System (One Byte)



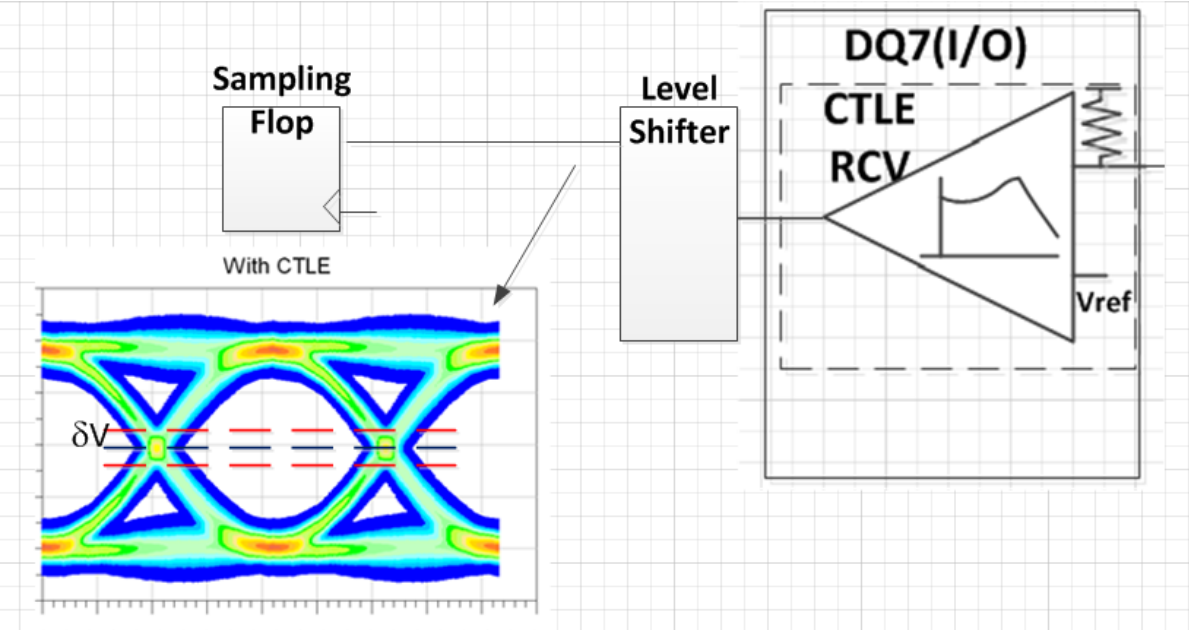
→ *CTLE implemented in a DDR System.*

CTLE in Memory System Improvement



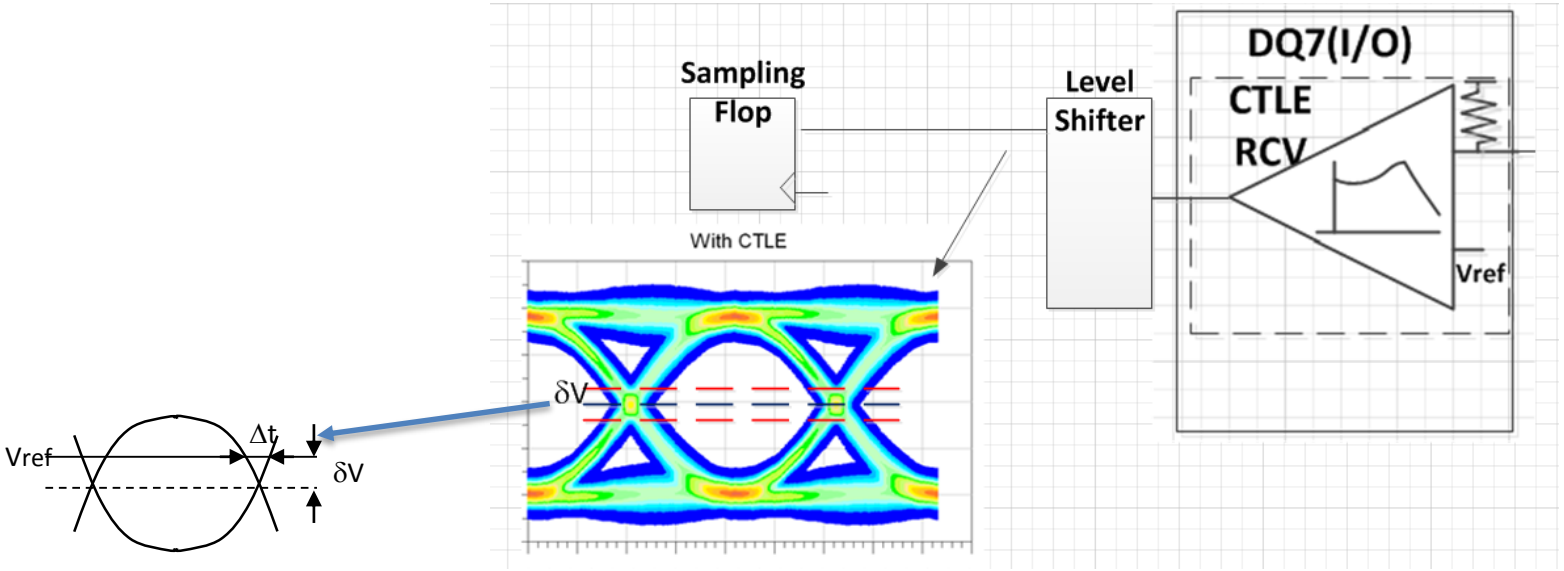
→ *CTLE improves incoming signal edge rate.*

Data Signal Eye Improvement after CTLE



→ *CTLE output will have common mode variation.*

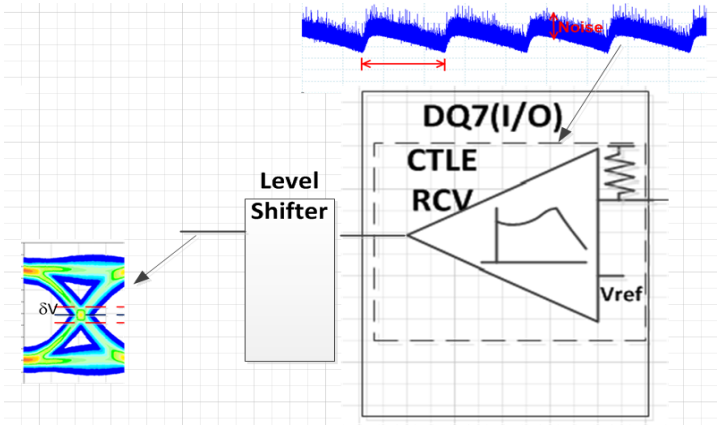
Channel Simulation in DDR4 System

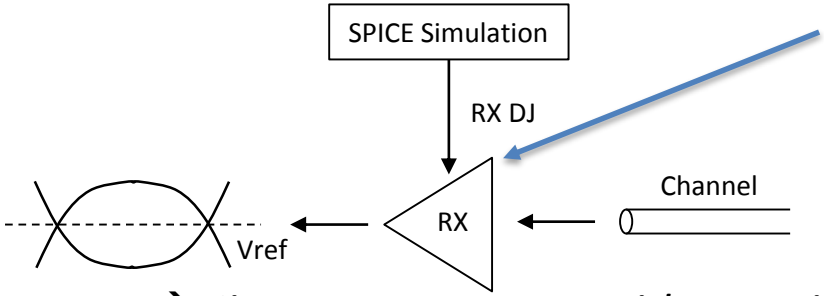


→ *Jitter should be considered with CLTE output common mode variation.*

→ *Sampling Flop Set up time reference to Vtrip of CMOS logic.*

Proposed Simulation Approach at Post Equalization Eye with Rx Sensitivity Impact

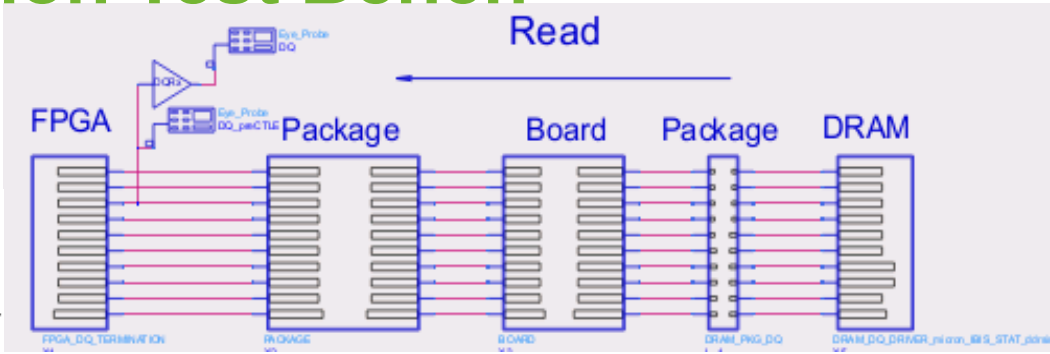


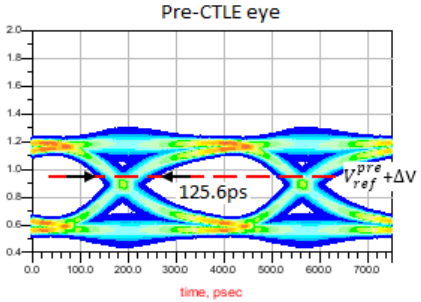


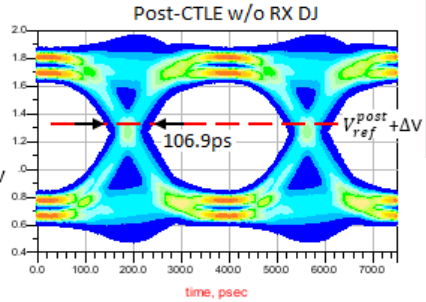
→ *Jitter measurement with mapping Rx DJ to Rx Vref.*

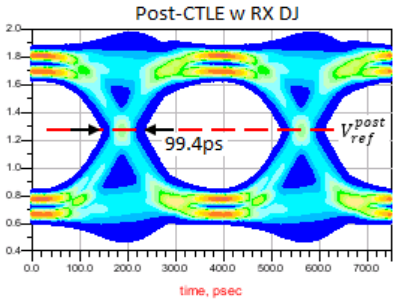
→ *Similar concept can apply to incorporate power supply noise induced DJ*

DDR4 Channel Simulation Test Bench



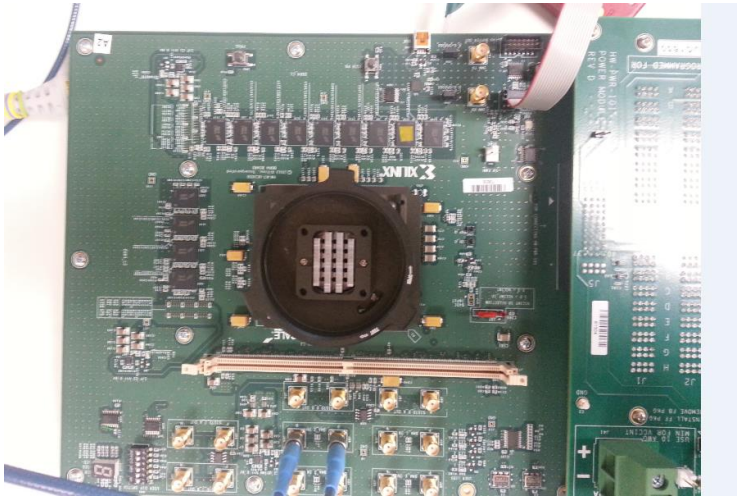


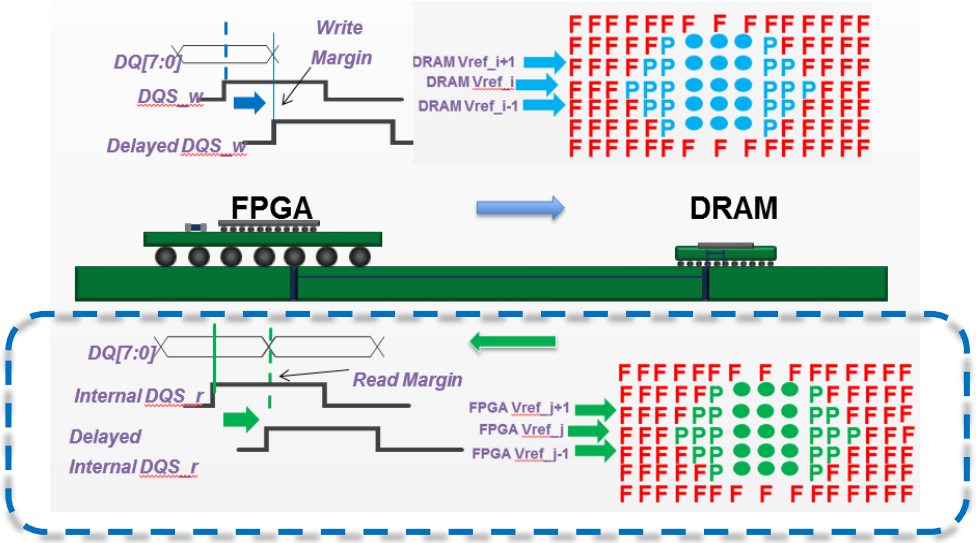




→ *Using Input threshold for post CTLE jitter measurement lead to pessimism .*

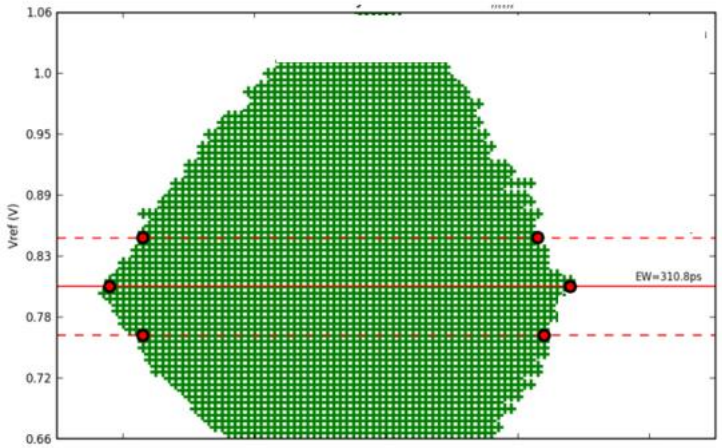
Validation Set Up

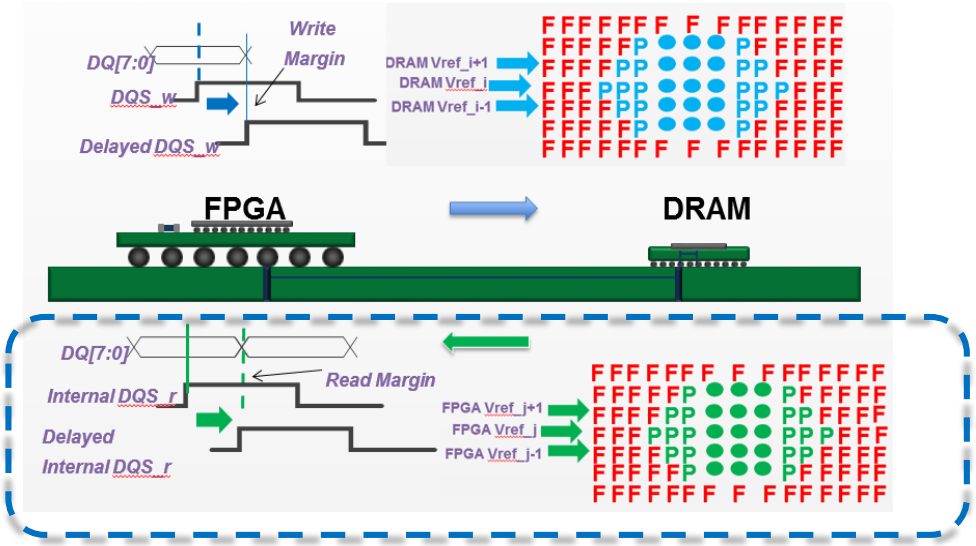




→ *Measure Functional Eye for sampling flop.*

Read Eye Diagram Measurement

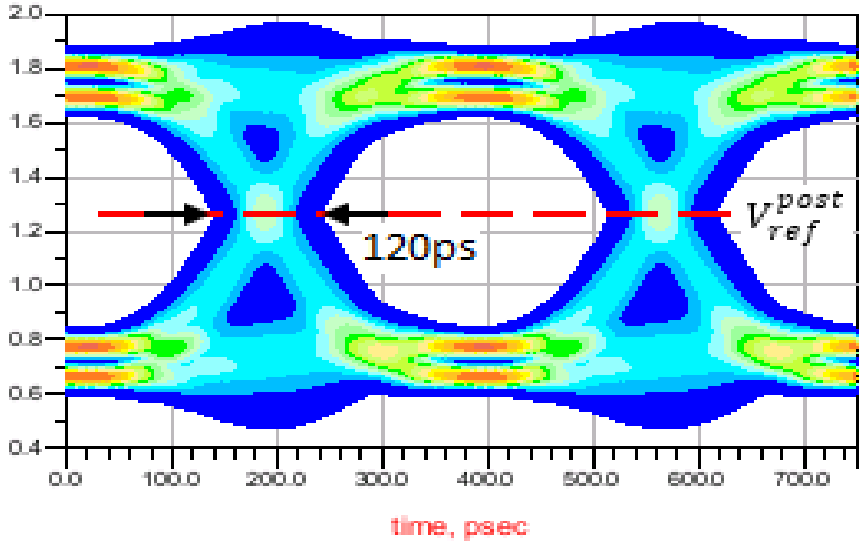




→ *Functional Eye measured at Vref is within 5% of prediction.*

→ *Relative Light Traffic Test Case.*

Post CTLE DQ Eye Jitter with Power Supply Noise



→ *Jitter measurement after mapping to Vtrip for sampling flop.*

Summary & Conclusions

- DDR Channel Attenuation becomes more significant as data rate increase.
- More precise system timing methodology is needed to accurate predict the timing analysis.
- New approach to analyze the system timing was presented using DJ to map the jitter measurement threshold voltage point to the Vtrip.
- New design features for jitter measurement was proposed as a critical design parameters.
- Receiver and Channel co-design is critical in future DDR interface design to enable robust channel timing.

Thank you!

QUESTIONS?