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Characterization of DDR4 Receiver Sensitivity Impact on Post-equalization Eye

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Abstract

The current DDR4 specification for the receiver (Rx) sensitivity defined at the Rx input does not account for equalization functionalities implemented in advanced Rx designs and may lead to over-design. In this paper we present a novel approach to characterize the Rx sensitivity impact on Rx post-equalization signal. We demonstrate that at the Rx output timing impairment is induced by common mode variation. The resulting jitter can be represented by a deterministic jitter model and incorporated in the statistical eye calculation. Timing margin and jitter in the post-equalization eye is measured at Vref to eliminate over-design.

Author(s) Biography

Yong Wang is currently a Sr. Director of Engineering at Xilinx leading Device Power and Signal Integrity Group since 2011. His team owns Xilinx product families' SI/PI methodology development, noise/timing/jitter analysis, interface timing such as DDR4/3, and corresponding verification/characterization. Prior to joining Xilinx, Mr. Yong Wang has been system design lead and SI/PI lead of several companies such as NVIDIA, MetaRAM, HP/Intel. He led the world first 16GB and 32GB R-DIMM design, validation and production with patented memory buffer ASIC design when he was system lead with MetaRAM. In NVIDIA/HP/Intel, he provided technical leadership in the areas such as but not limited to, IA-64 system front-side parallel bus channel timing, serial link channel analysis, system level power modeling, on-die power grid noise/timing analysis and timing/noise validation in the lab. Mr. Yong Wang received his M.S. degree in Electrical Engineering from Colorado State University and B.S. degree in Electrical Engineering from Peking University. Mr. Yong Wang has 21 US patents issued and several publications including best paper rewards in conferences like EPEP and ECTC.

Thomas To is a Technical Director in System Memory Signal Integrity & Device Power Group at Xilinx, Inc. Prior to joining Xilinx, Thomas was with NVIDIA Advanced Technology Group focused on high speed (32GTs) circuits & system channel designs and supported different test chips for different advanced process nodes such as 20nm SOC & 16nm FINFET process. Before NVIDIA, Thomas worked for Intel for more than 16 years covered and led many different types of system memory IO development such as Sandy Bridge Server DDR IO and covered many different system memory technology ranging from DDR1 to DDR4. Thomas received his PhD degree in Electrical Engineering from the Ohio State University in 1995 & he has over 37 patents in the fields of mixed signal IO circuits and system memory configurations as well as high speed clocking for high speed memory designs.

Penglin Niu is an engineer manager at Xilinx. Her team is responsible for SI/PI modeling methodology, and product SSN and PDN analysis. She was the signal integrity lead for memory interface in Xilinx before the management position. Prior to Xilinx, she worked for Intel as signal integrity lead and package design lead. She was deeply involved in high speed DDR3/DDR3L system design and high performance CPU package design. Penglin received her Ph.D. degree from University of Illinois Urbana-Champaign, and M.S. degree from University of Missouri-Rolla.

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Juan Wang is a Staff Signal Integrity engineer at Xilinx Inc. She has been focusing on memory interface timing analysis such as DDR4/DDR3/RLDRAM3 and corresponding lab verification. Prior to Xilinx, she worked for Juniper as signal integrity engineer for more than 5 years supporting system design 10GE/XFI/XLAUI/SFI/sGMII/rGMII/PCIE/DDR3 signal integrity modeling, simulation and measurements. Juan received her MSEE from University of Missouri-Rolla and Tsinghua University.

Xi (Sean) Long is a senior Signal Integrity engineer at Xilinx Inc. His work at Xilinx focus on timing analysis and lab validation of DDR memory interface. Prior to Xilinx, he was with Nvidia Corp as a Mixed Signal Design/Validation engineer working on circuit design and lab validation of analog blocks in DDR and SERDES interfaces such as LPDDR4/GDDR5/PCIE. He received his MSEE from University Delaware

1. Introduction

Traditionally, DDR Receiver sensitivity is defined by a threshold level from the reference voltage. For example, this threshold level in DDR4 is defined by the receiver compliance mask [1]. The voltage sensitivity parameter in the DRAM is called VdiVW_dv, as shown in Figure 1. The implication of this parameter is that once the incoming signal passes this threshold, the receiver will sense the signal to the correct state. Similarly in the controller side, the receiver sensitivity is also defined by a certain voltage sensitivity such that the signal will be guaranteed to latch to the correct state.

Figure 1 Simple DDR Receiver & Input Mask

However, when the DDR system memory speed scales up and together with the IO capacitance loading, the DDR channel often experiences considerable channel loss. Figure 2 below shows a typical DDR memory system and its channel loss over operating frequency.
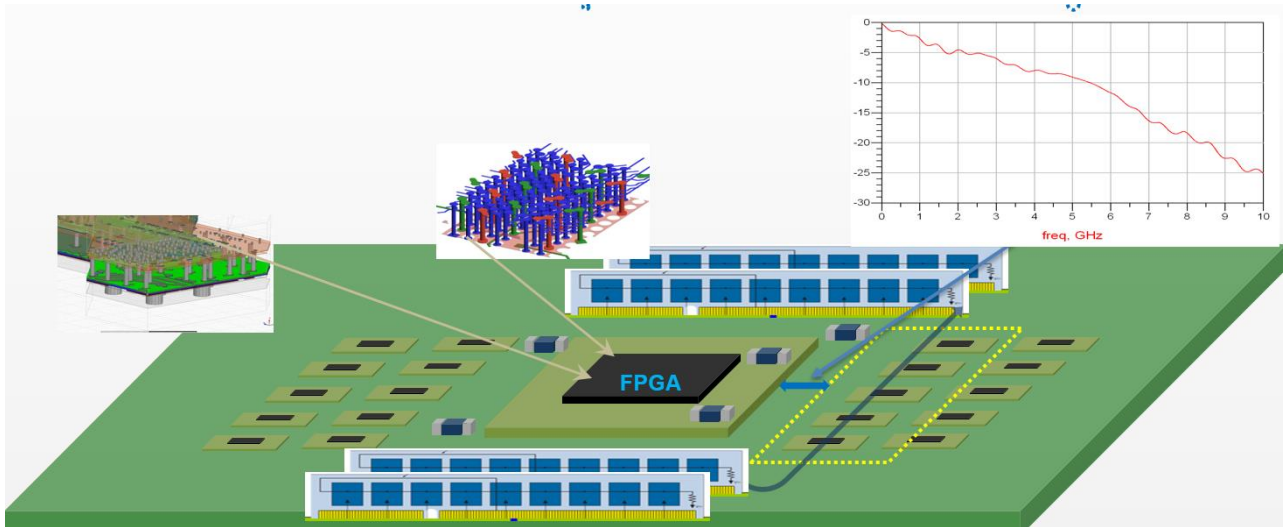
Figure 2 DDR System & Typical Channel Attenuation

In order to mitigate the channel loss problem, modern controller will implement receiver equalization at their receiver. Most common receiver equalizer is the CTLE (Continuous Time Linear Equalization).

Besides latching the incoming signal to the correct state, one must quantify the incoming jitter. Doing so enables the understanding of channel margin as well as comparing possible memory system channel timing trade-offs.

If there is no special equalization filter in the receiver, the channel jitter can be measured at the defined threshold levels of the input receiver, as shown in Figure 3. This measured jitter represents the timing variation to the input receiver requirement.
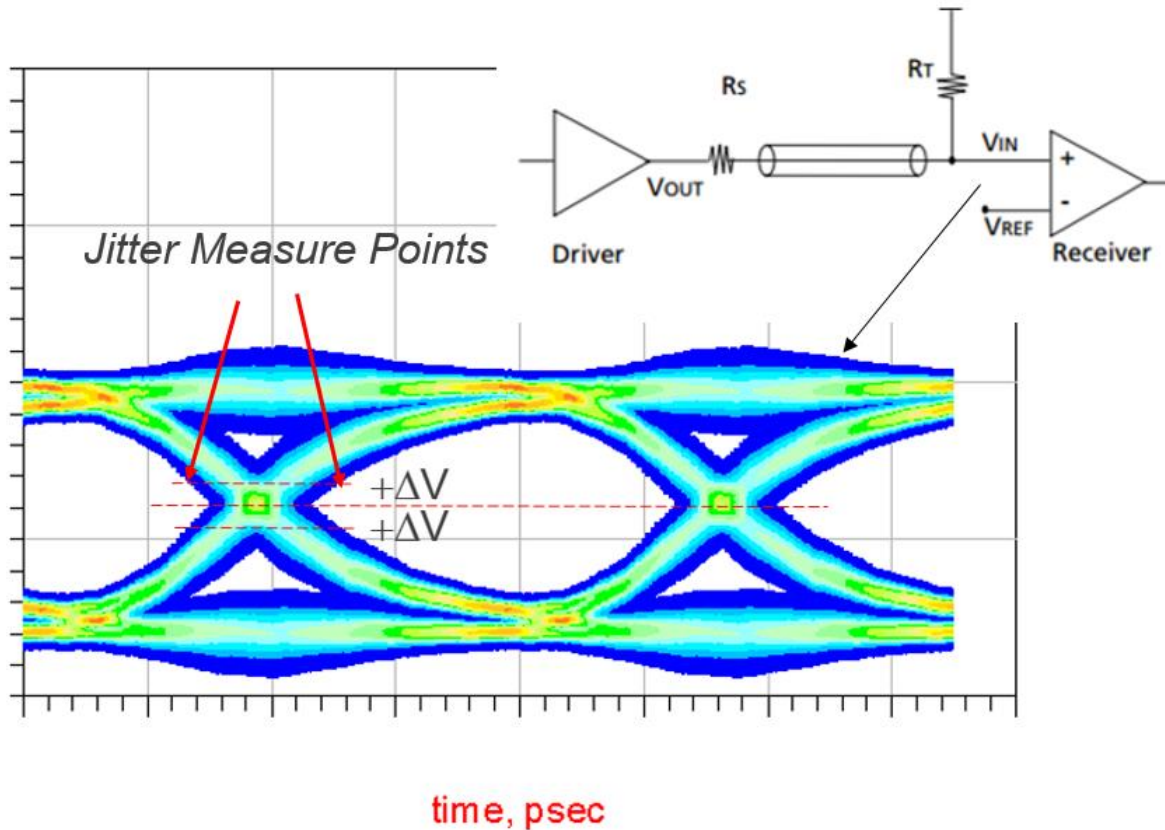
Figure 3 Jitter Measurement Point for Simple DDR Receiver

2. Problem Statement

When the channel jitter measurement is done using the input threshold defined for the receiver only, it does not capture the jitter improvement by the CTLE gain. One method is to impose the input threshold and apply the measurement after the CTLE. But it is pessimistic because the CTLE will amplify the signal at the output before the signal is sampled by the sampling flop, which will be implemented in CMOS logic. The measurement points should be defined more accurately and different from the input receiver threshold requirement.

3. Traditional Simulation Approach

Figure 4 below illustrates the receive data eye before and after the CTLE receiver. When the input receiver voltage requirement is ΔV, and when the jitter is measured at the input of the receiver, this jitter measurement represents the timing uncertainty that impacts the receiver data sensing. But this measured jitter does not represent the actual jitter to the

sampling flop. If the same input voltage threshold ΔV is applied after the CTLE, the measurement will be pessimistic.
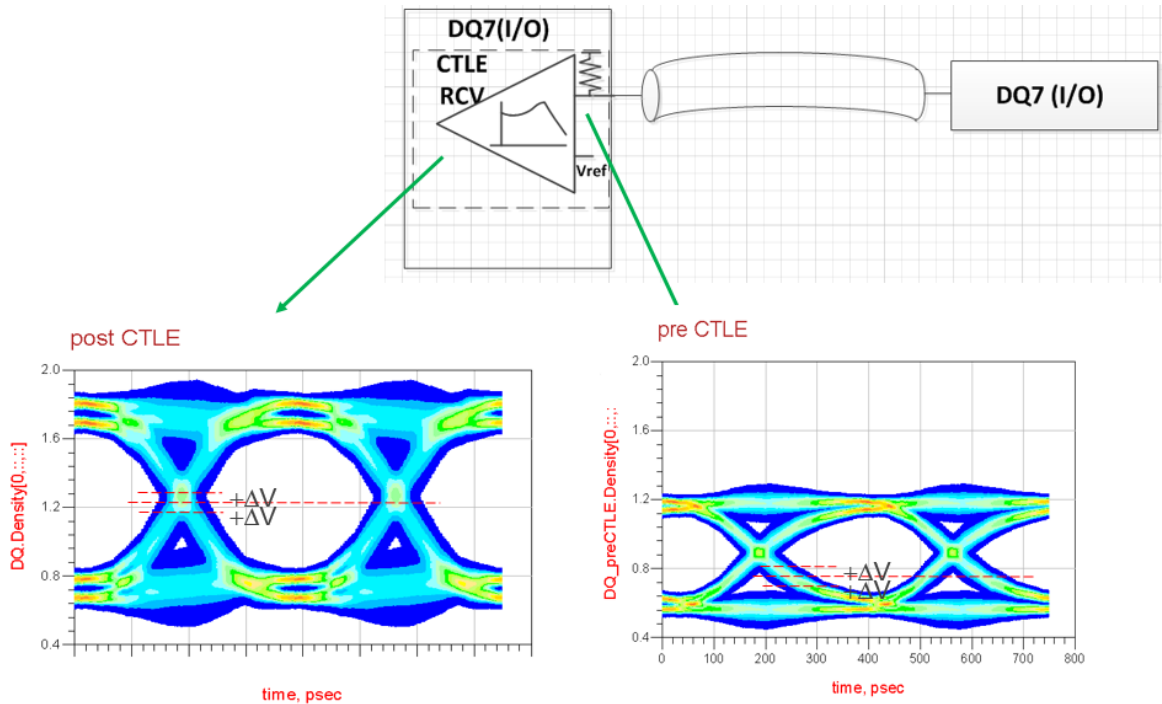

Figure 4 Traditional Jitter Measurement Point

4. CTLE Receiver and Output Eye Mask

As mentioned earlier, CTLE filter has been incorporated in modern memory system, usually on the controller, to mitigate channel loss. The loss attenuates the incoming signal. Part of the channel loss is from the PCB dielectric loss and part of the loss is due to the input capacitance of the IO. The CLTE filter adjusts the ratio of the low frequency to high frequency attenuation to equalize and to invert the low pass effect of the channel. A typical frequency response of a CTLE filter is shown in Figure 5 below.
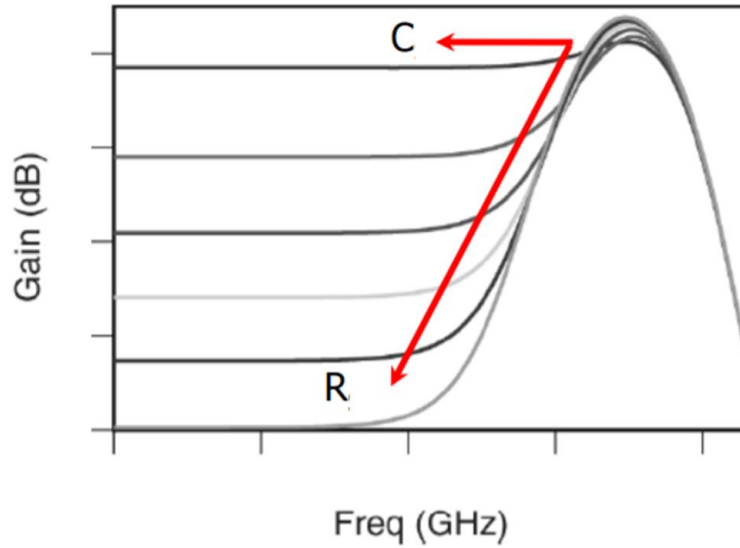
Figure 5 CTLE Low to High Frequency Peaking Ratio

Typically, the CTLE filter is implemented with an active gain stage together with the tuning degeneration resistor and capacitor. These degeneration resistors and capacitors are used to adjust the zero and poles frequencies so as to tune the low frequency to high frequency peaking ratio. A simplified breakdown Bode plot of the relative zero and poles for a one zero and two poles filter is illustrated in Figure 6. A more general form of the transfer function will be shown in the next section.
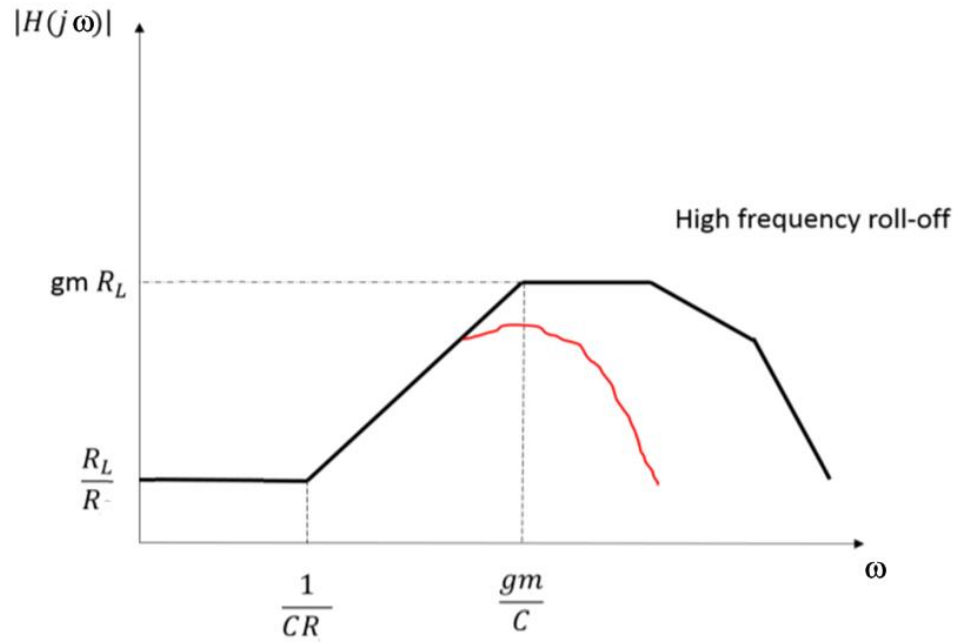
Figure 6 CTLE Zero and Poles Relative Position Breakdown

Mathematically, the zero and the poles are listed in equations below.

$$\omega_z = \frac{1}{CR} \quad (1)$$

$$\omega_{p1} = \frac{1+g_mR/2}{CR} \quad (2)$$

$$\omega_{p2} = \frac{1}{C_LR_L} \quad (3)$$

where gm is the active stage trans-conductance, R_L is the loading resistance, R and C are the degeneration resistance and capacitance, and C_L is the loading capacitance.

The solid black line represents the ideal transfer peaking and the red line shows the actual peaking behavior due to parasitic capacitances in the CTLE receiver circuit.

An incorporation example of the CTLE receiver is shown in Figure 7.
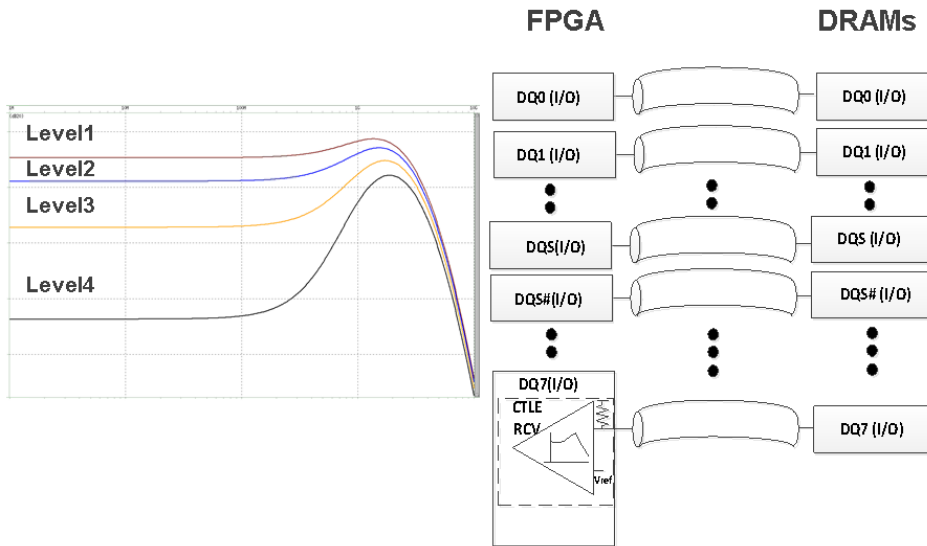
Figure 7 CTLE Receiver in Memory System

When the equalization is optimized, the equalized signal eye jitter will be improved. Figure 8 below is an example comparing a system with and without CTLE.
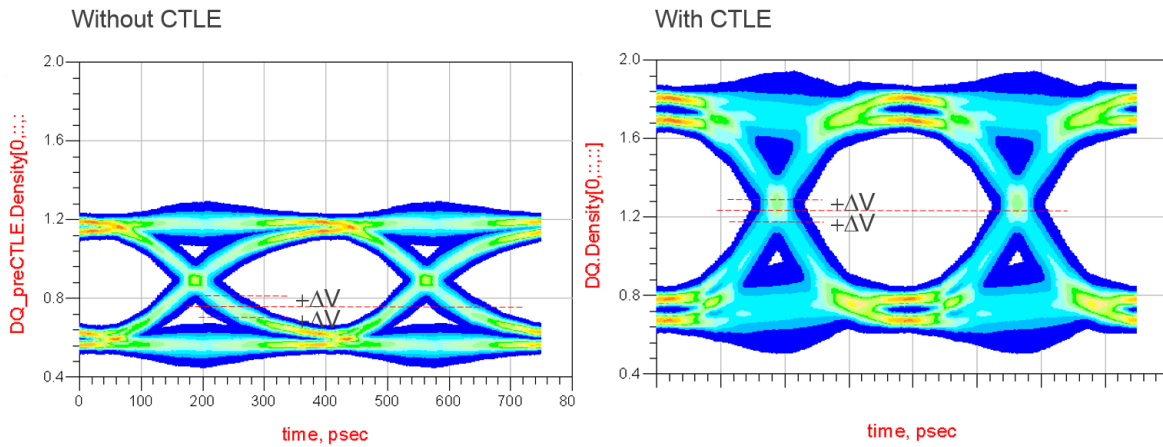

Figure 8 Signal Eye Improvement with and without CTLE

Because of the high frequency peaking with gain at the Nyquist frequency, the signal eye after the CTLE shows sharper transition edges. Hence, the receive eye jitter improves.

Unlike the SerDes system, the data signal is a single ended signal; for instance DDR4 uses PODL12. The incoming signal is referenced to a defined reference voltage, Vref. Normally, the sensitivity of the input receiver is defined as certain ΔV from the Vref signal. The set up

and hold time are then defined with this ΔV to guarantee the incoming signal is properly detected.

However, when the jitter of a system needed to be quantified together with the CLTE improvement, the CTLE output signal common mode variation should be considered and that variation should be used to measure the channel jitter before the signal is sampled by the internal sampling flop.

The jitter measurement mask should be at the output of the CTLE receiver as shown in Figure 9. The voltage threshold is denoted as δV. Besides the equalization and gain of the CTLE filter, the voltage threshold δV is also a design parameter across all Process, Voltage and Temperature (PVT) variations such that $\delta V < \Delta V$. In other words, the output of the CTLE filter will have a tighter threshold with respect to the internal sampling flop compared to the receiver input sensitivity threshold.
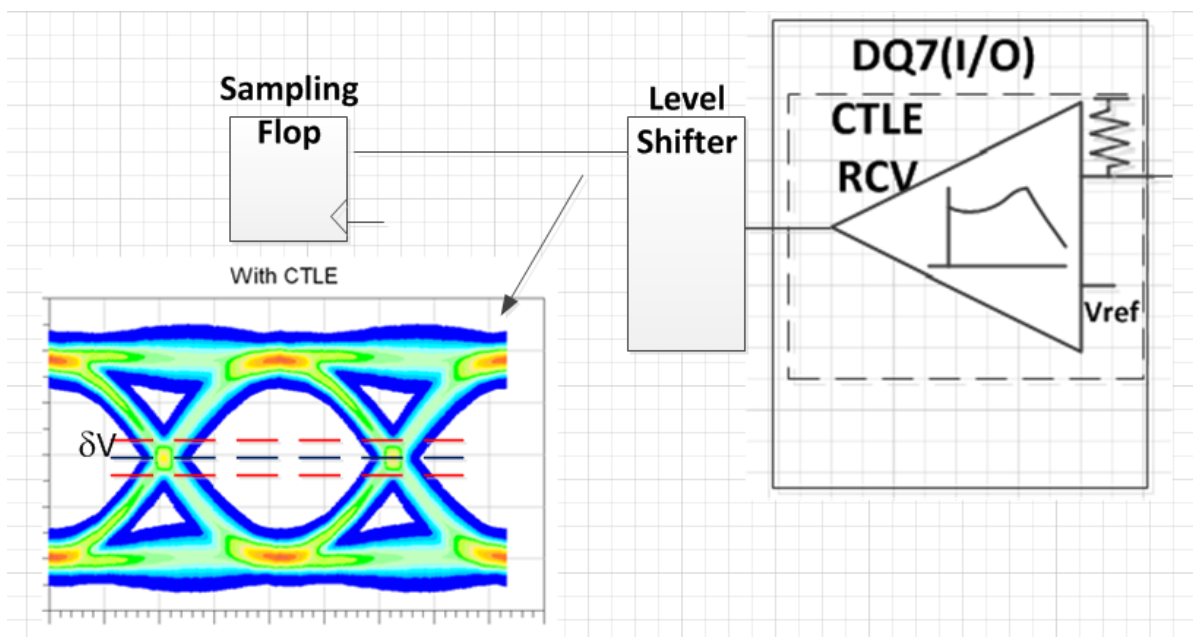

Figure 9 Signal Eye Improvement after CTLE

5. Channel Simulation

According to the JEDEG DDR4 specification [1], compliance of DQ eye mask must be verified at the 10^{-16} bit-error-rate (BER) level. For time domain simulations, such a low BER target requires an extremely long bit sequence to be processed, making the computation

impractically time-consuming. An alternative approach is the statistical BER simulation, which directly computes eye probability distributions and BER without running an actual bit sequence. The results are equivalent to those of simulating infinite number of random bits, allowing accurate BER prediction in a very short amount of time. As a result, the statistical method becomes the only feasible way to simulate DDR4 designs.

The statistical eye calculation is based on the channel step responses [2,3]. Under the linear time invariant condition, the Rx equalization can be included in the calculations by convolving the step responses with the equalizer's impulse response, which is the inverse Fourier transform of the transfer function. The general CTLE transfer function H(s) can be expressed in the pole-zero form.

$$H(s) = c\frac{\prod_i(s - z_i)}{\prod_k(s - p_k)} \tag{4}$$

In this paper the CTLE is characterized by a DC gain, a zero and two poles.

$$H(s) = G_{DC}\frac{\omega_{p1}\omega_{p2}}{\omega_z}\frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})} \tag{5}$$

where G_{DC}, ω_z, ω_{p1}, ω_{p2} are the DC gain, the zero and the poles, respectively.

As illustrated in Figure 10 , the common mode variation shifts the crossing level of the CTLE output eye away from the ideal Vref, causing timing impairment at Vref, which can be represented by a receiver deterministic jitter (DJ). The common mode variation impact on the timing margin can be accounted for in statistical calculations by convolving the CTLE output eye probability density function (PDF) with the receiver DJ PDF as

$$p(v, t) = \int p_{CTLE}(v, t - \tau)p_{DJ}(\tau)d\tau \tag{6}$$

where p_{CTLE} is the CTLE output eye PDF, and p_{DJ} the PDF of the common mode variation induced DJ. The peak-to-peak DJ amplitude can be extracted from SPICE simulations. Since the common mode offset effects are captured by the RX DJ, timing margin and jitter of the CTLE output eye are then measured at the Vref. The proposed approach is illustrated in Figure 11.
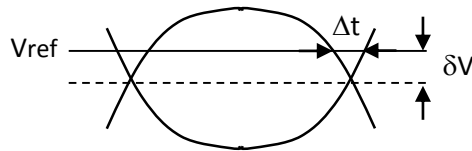

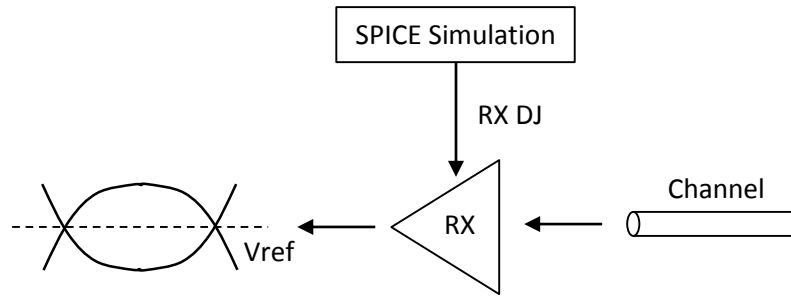**Figure 10 Common variation impact on CTLE output timing margin**

Figure 11 Proposed simulation approach for post-equalization eye with RX sensitivity impacts

Similar approach can also be applied to account for power supply noise induced jitter. Figure 12 shows the deterministic jitter induced in the CTLE receiver.
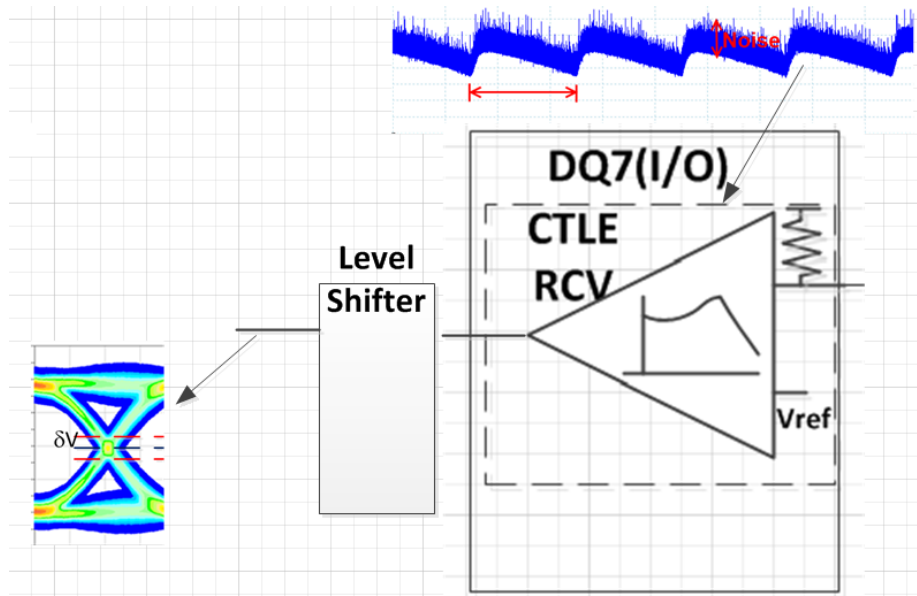

Figure 12 Receiver with power supply noise induced Deterministic Jitter

The proposed approach is applied to a DDR4 channel shown in Figure 13. The channel consists of eight DQ lines and one DQS differential pair. The common mode offset induced RX DJ is estimated to be 7.5ps according to SPICE simulation results. Pre-CTLE and post-CTLE eyes yielded by statistical channel simulations are shown in Figure 14. Post-CTLE eyes with and without the RX DJ are both shown in the plot.

As demonstrated in Figure 14, in the traditional approach, the pre-CTLE jitter at 10^{-16} BER is measured at pre-CTLE Vref + ΔV, and the value is 125.6ps. The post-CTLE jitter at 10^{-16} BER is measured without the RX DJ at post-CTLE Vref + ΔV, and the value is 106.9ps. In the proposed approach, the post-CTLE jitter at 10^{-16} BER is measured with the RX DJ at post-

CTLE Vref, and the value is 99.4ps, which is more optimistic than both pre- and post-CTLE jitters measured using the traditional approach, as discussed previously.
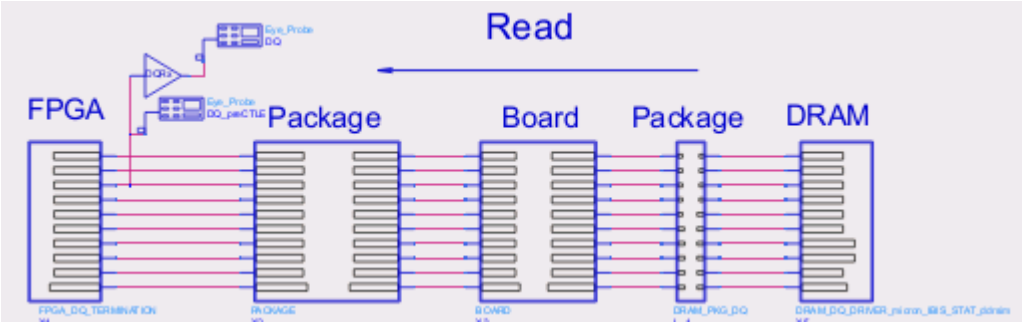

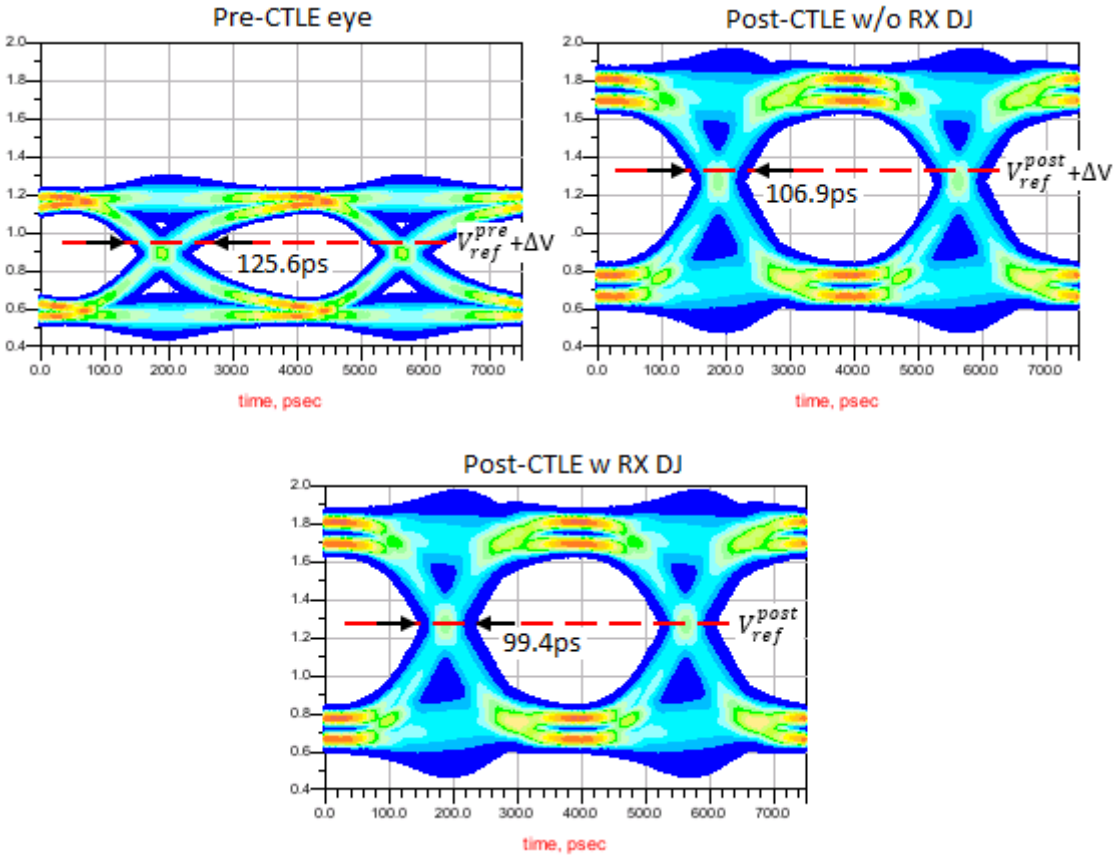**Figure 13. DDR4 channel simulation setup**

Figure 14. Pre-CTLE and post-CTLE DQ eyes and jitters at 10^-16 BER.

In the figure above, V_{ref}^{pre} and V_{ref}^{post} are pre- and post-CTLE Vref, respectively. ΔV is the input RX sensitivity. The RX DJ induced by the common mode variation is 7.5ps.

The proposed approach is also employed to investigate power supply noise effects. The power noise induced DJ is estimated to be 22ps from SPICE simulations. This DJ is combined with the previous common mode offset induced DJ in statistical calculations. The resulting post-CTLE eye and jitter at 10^{-16} BER are shown in Figure 15. As expected, the power supply noise causes additional timing impairments in the channel.
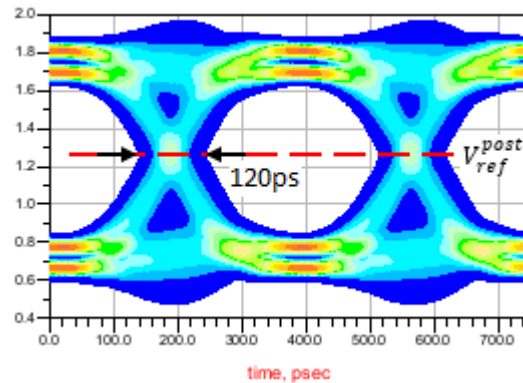

Figure 15. Post-CTLE DQ eye and jitter at 10^{-16} BER with RX DJ induced by both common mode offset and power supply noise.

6. Conclusion

DDR system speed keeps moving upwards to catch up with increasing data bandwidth requirement in the big data world. DDR4 is in 3-4 Gbps regime and DDR4 is on the horizon. System timing methodology and every part of system timing need to be revisited to more accurate predict timing impact for better system design trade-off in such low cost high bandwidth interface. This paper explores new approach to analyze channel jitter beyond traditional eye mask approach. Especially with new receiver design features for higher speed requirement, eye mask approach may not be accurate to assess channel jitter for system level timing closure. This paper presented detail approach and simulation result benchmark. Receiver and channel co-design is critical in future DDR interface design to enable robust channel timing with such co-design analysis.

REFERENCE

[1] JEDEC DDR4 Standard, Sept. 2012.

[2] Casper, M. Haycock, R. Mooney, "An accurate and efficient analysis method for multi-Gb/s chip-to-chip signaling schemes," *VLSI Circuit Symposium*, pp. 54-57, June 2002.
[3] F. Rao, V. Borich, H. Abebe and M. Yan, "Rigorous modeling of transmit jitter for accurate and efficient statistical eye simulation," IEC DesignCon, Feb. 2010.