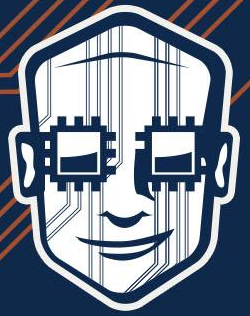
DesignCon® 2015



ULTRASCALE FPGA DDR4 2400 MBPS SYSTEM LEVEL DESIGN OPTIMIZATION AND VALIDATION

XILINX ALL PROGRAMMABLE™

UBM

FPGA High Speed High Bandwidth Unique Challenges

- Massive amount of High Performance IO can be used for DDR4

	KINTEX-7	KINTEX UltraSCALE	VIRTEX-7	VIRTEX UltraSCALE
Logic Cells (LC)	478	1,161	1,995	4,407
Block RAM (BRAM; Mbits)	34	76	68	115
DSP48	1,920	5,520	3,600	2,880
Peak DSP Performance (GMACs)	2,845	8,180	5,335	4,268
Transceiver Count	32	64	96	104
Peak Transceiver Line Rate (Gbps)	12.5	16.3	28.05	32.75
Peak Transceiver Bandwidth (Gbps)	800	2,086	2,784	5,101
PCI Express Blocks	1	6	4	6
100G Ethernet Blocks	-	1	-	7
150G Interlaken Blocks	-	2	-	9
Memory Interface Performance (Mbps)	1,866	2,400	1,866	2,400
I/O Pins	500	832	1,200	1,456

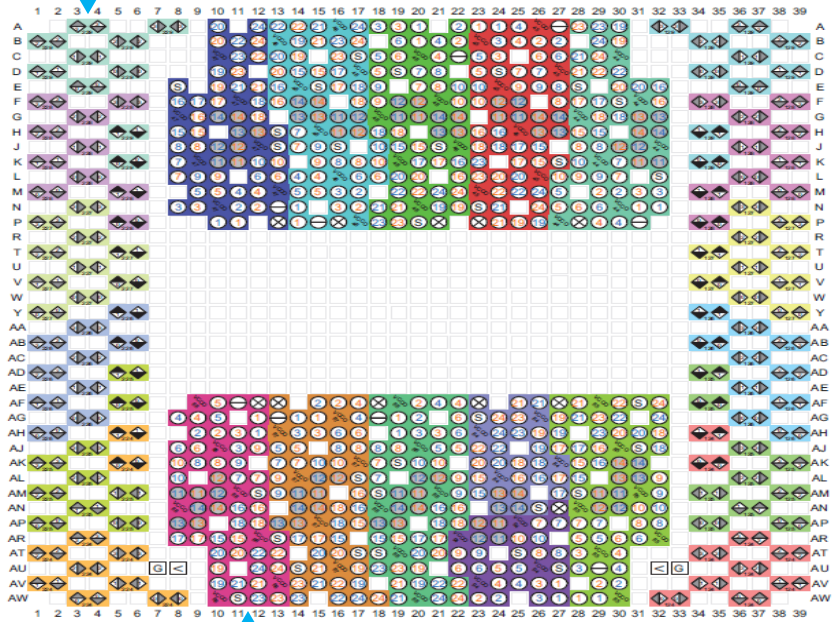
Multiple Supported for High Performance IO (HPIO) Standards

- High Speed High Performance IO supports many memory interface; hence, the IO capacitance is higher than in ASIC design.

	Memory IO Standards
DDR4	POD12
DDR3	SSTL15
DDR3L	SSTL135
LPDDR3	HSUL
RLDRAM3	SSTL12
QDR4	HSTL/SSTL:1.2V,1.25V POD:1.1V,1,2V
QDR2+	HSTL:1.2V,1.8V

FPGA HP IO location

- High Performance IOs are located at the center of the package, IO breakouts are more susceptible to cross talk



GTY Quad 131 X0Y28–X0Y31	Bank 51 HP I/O	PLL[14:15] CMT MMCM[07]	Bank 71 HP I/O	PLL[30:31] CMT MMCM[15]	GTH Quad 231 X1Y28–X1Y31
GTY Quad 130 X0Y24–X0Y27	Bank 50 HP I/O	PLL[12:13] CMT MMCM[06]	Bank 70 HP I/O	PLL[28:29] CMT MMCM[14]	GTH Quad 230 X1Y24–X1Y27
GTY Quad 129 X0Y20–X0Y23	Bank 49 HP I/O	PLL[10:11] CMT MMCM[05]	Bank 69 HP I/O	PLL[26:27] CMT MMCM[13]	GTH Quad 229 X1Y20–X1Y23
GTY Quad 128 X0Y16–X0Y19	Bank 48 HP I/O	PLL[08:09] CMT MMCM[04]	Bank 68 HP I/O	PLL[24:25] CMT MMCM[12]	GTH Quad 228 X1Y16–X1Y19
GTY Quad 127 X0Y12–X0Y15	Bank 47 HP I/O	PLL[06:07] CMT MMCM[03]	Bank 67 HP I/O	PLL[22:23] CMT MMCM[11]	GTH Quad 227 X1Y12–X1Y15
GTY Quad 126 X0Y8–X0Y11	Bank 46 HP I/O	PLL[04:05] CMT MMCM[02]	Bank 66 HP I/O	PLL[20:21] CMT MMCM[10]	GTH Quad 226 X1Y8–X1Y11
GTY Quad 125 X0Y4–X0Y7	Bank 45 HP I/O	PLL[02:03] CMT MMCM[01]	Bank 65 HP I/O	PLL[18:19] CMT MMCM[09]	GTH Quad 225 X1Y4–X1Y7
GTY Quad 124 X0Y0–X0Y3	Bank 44 HP I/O	PLL[00:01] CMT MMCM[00]	Bank 84/94 HR I/O	PLL[16:17] CMT MMCM[08]	GTH Quad 224 X1Y0–X1Y3

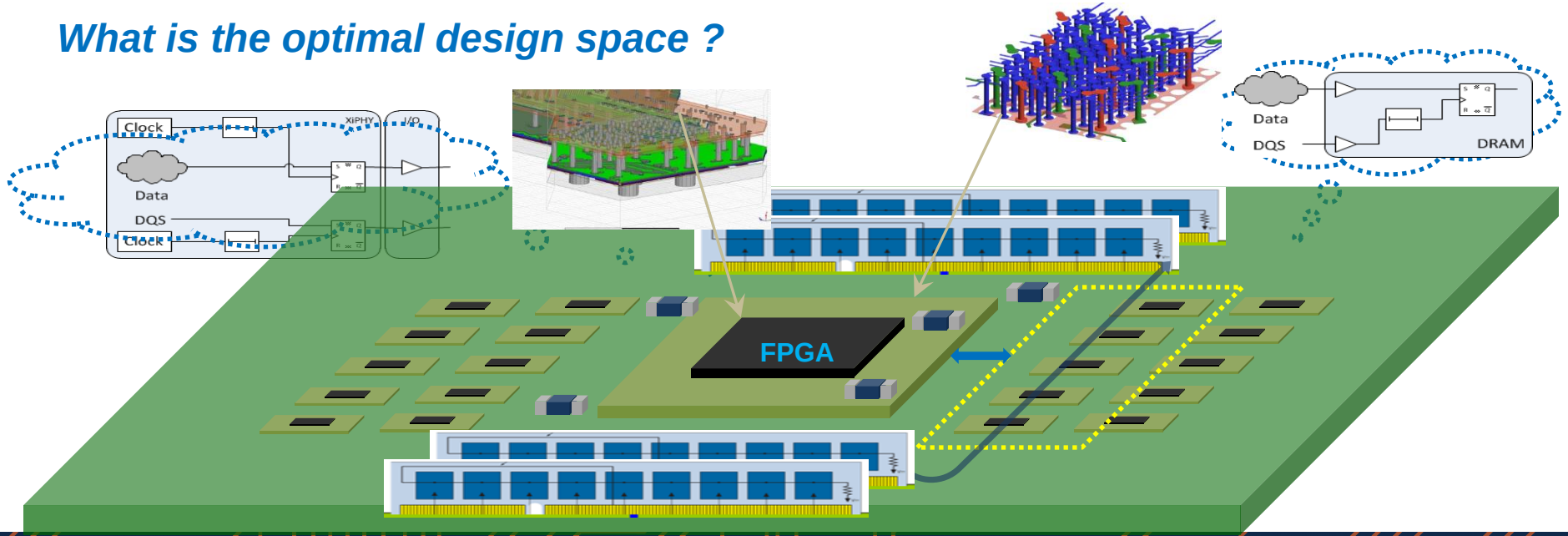
High Speed Parallel Bus System Considerations

What is the memory interface speed?

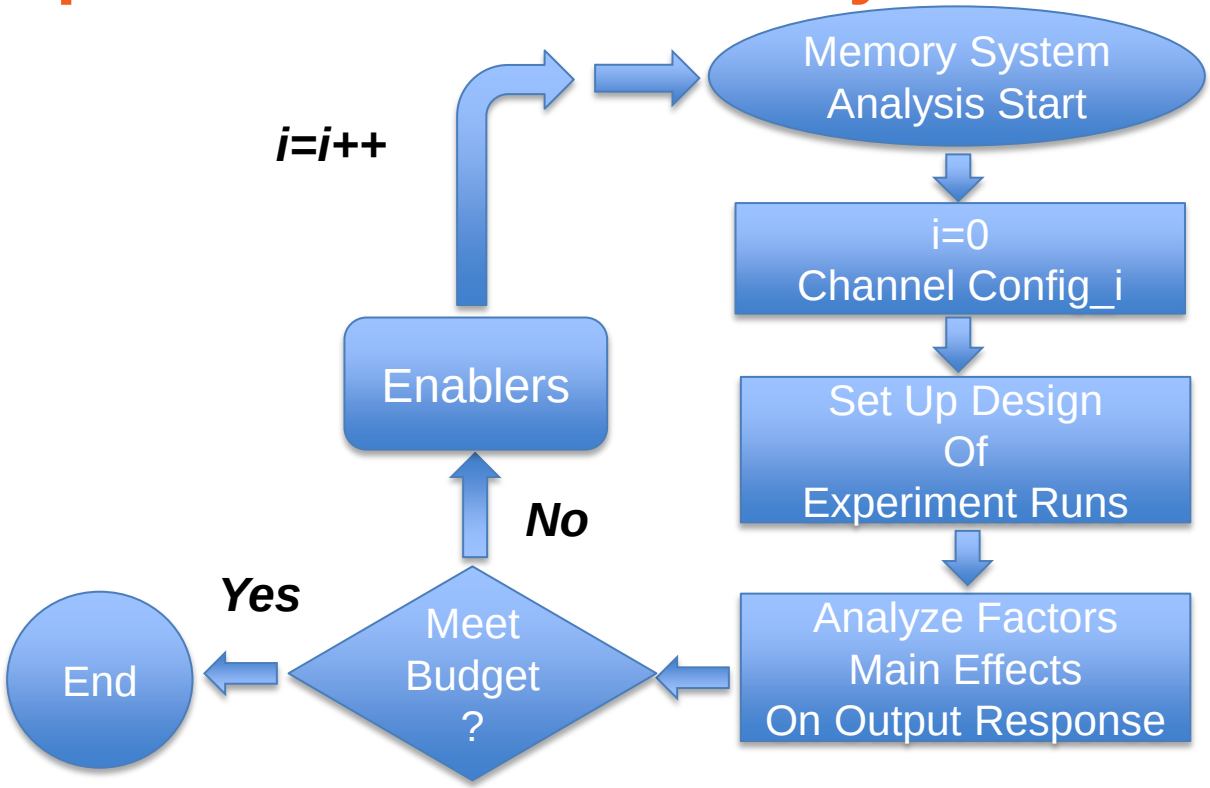
What is the memory devices variations & electrical limits?

What is the electrical channel characteristics ?

What is the optimal design space ?



High Speed Parallel IO Bus System Design Flow



Statistical Design Of Experiment Approach

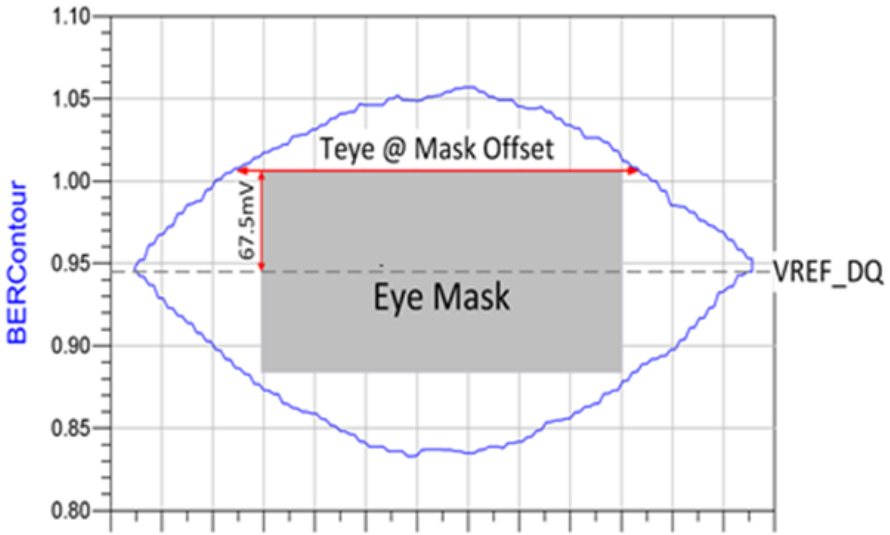
Identify the performance output (Response)

Identify the design factors (parameters) limits

Create design run table & simulate response(s)

Analyze response & Identify key design parameters from Prediction Profiles

Design Parameter Table & Design Data Eye Response

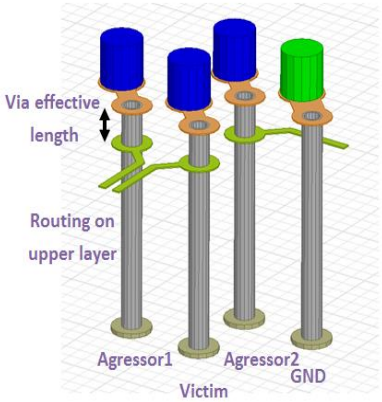


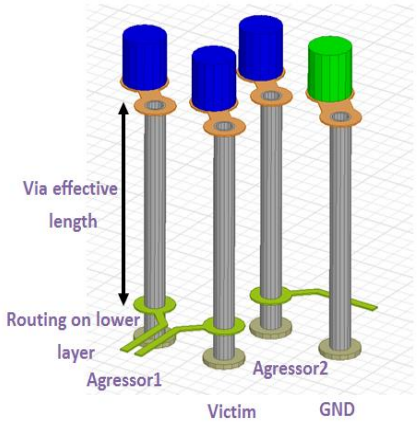
	Design Factors	Low Limits	Up Limit
FPGA	Drv Slew Rate (V/ns)	-1	+1
	Drv Impedance (Ω)	-1	+1
	Drv Supply (V)	-1	+1
Package	Impedance (Ω)	-1	+1
	: : :	: : :	: : :
	: : :	: : :	: : :
Board	Impedance (Ω)	-1	+1
	: : :	: : :	: : :
	: : :	: : :	: : :
DRAM	Dram Cap Load	-1	+1
	Rtt	-1	+1
	: : :	: : :	: : :

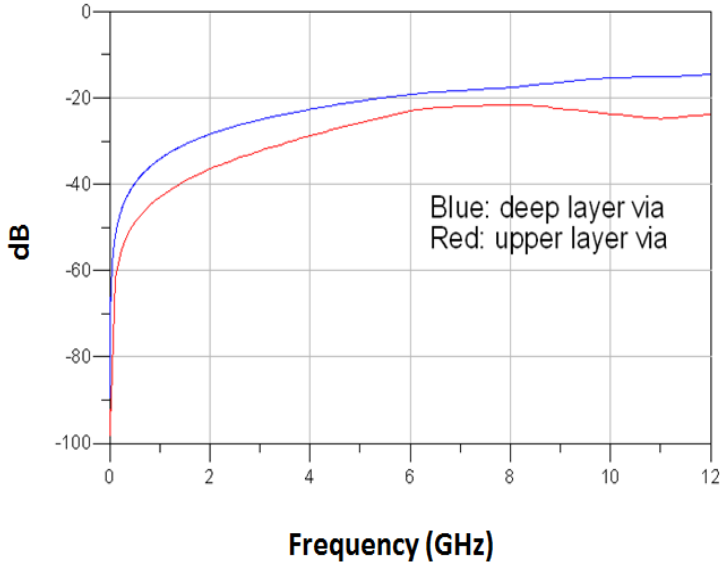
IO Key Features to Enable DDR4 Interface

- **Mother Board via Improvement Quantification**
  - Upper Routing vs Lower Routing improvement
- **Tx Feature**
  - POD12 Driver with De-emphasis Equalization
- **Rx Feature**
  - Continuous Time Linear Equalization
- **De-skew Feature**
  - Data (DQ) & Data Strobe (DQS) per bit de-skew

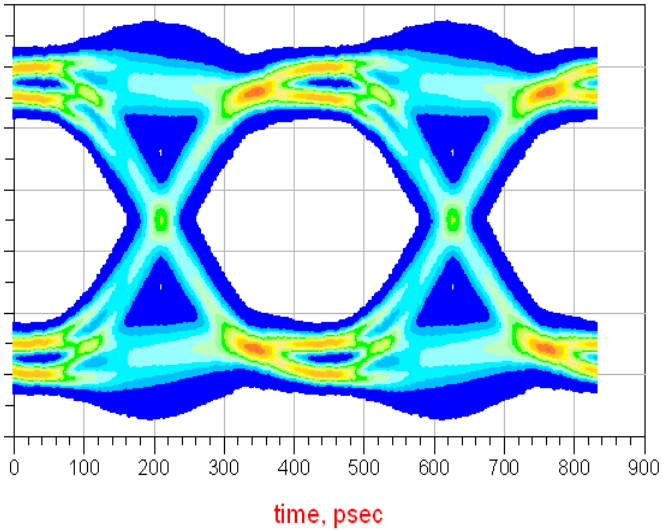
Mother Board Via Cross Talk Quantification



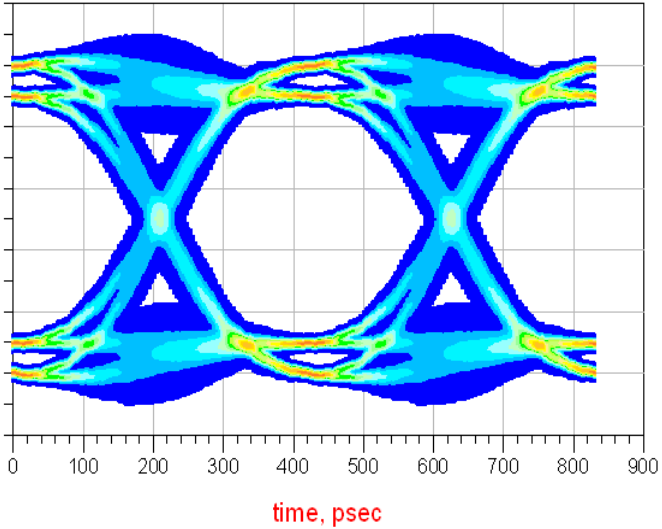




Upper and Lower Routing Eye Diagram Comparison



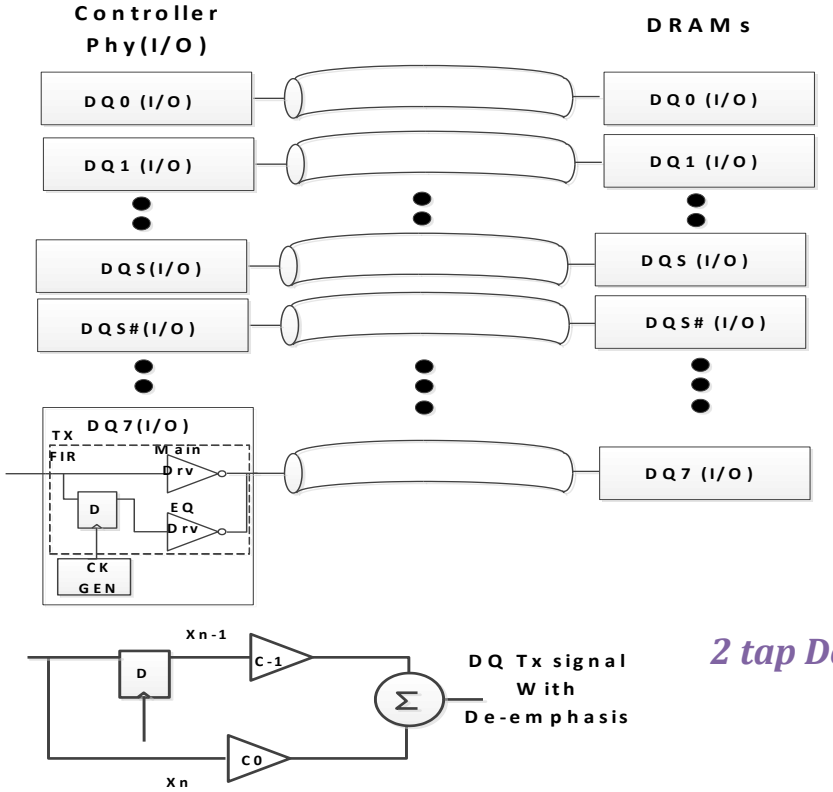
Lower Layer

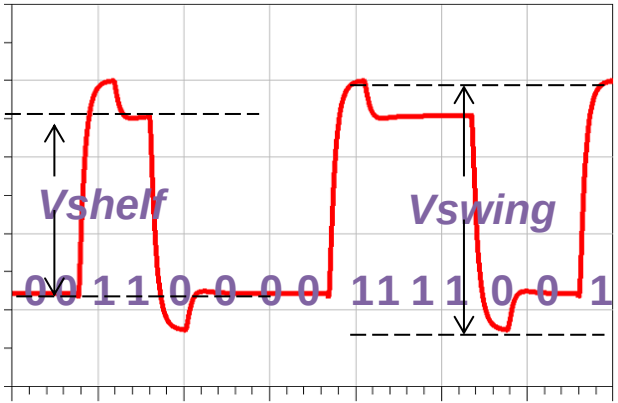


Upper Layer

~ 7.2% jitter improvement using upper layer

Tx De-emphasis Architecture



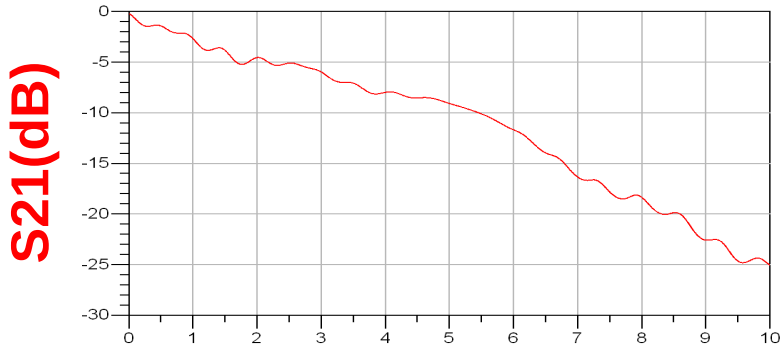


$$\sum_{k=0}^{k=-1} |ck| = 1$$

$$2\ tap\ De\text{-}emphasis\ Spec(dB) = -20\ log\left(\frac{Vshelf}{Vswing}\right)$$

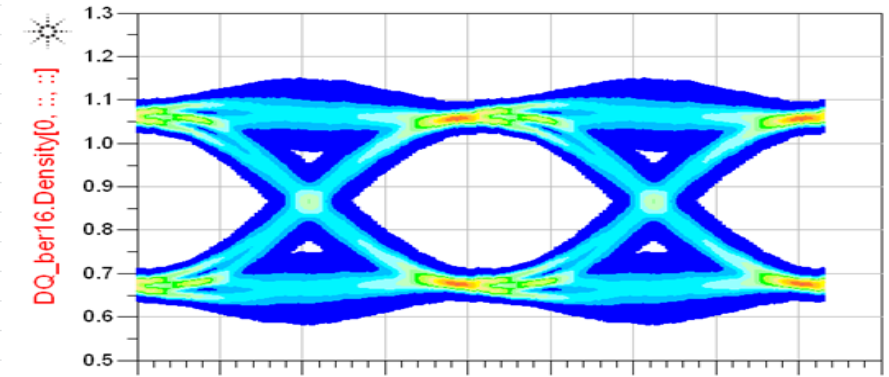
$$= -20\ log\left(\frac{(|c_0| - |c_{-1}|)/2}{(|c_0| + |c_{-1}|)/2}\right)$$

Write Data Eye Improvement with De-emphasis

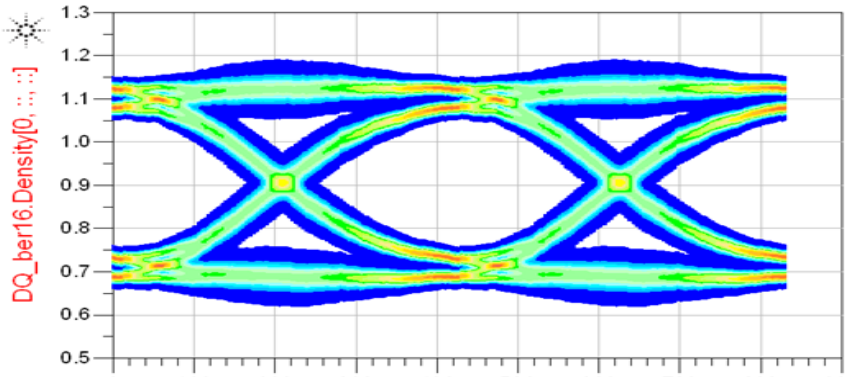


→ *With De-emphasis ~ 4% improvement*

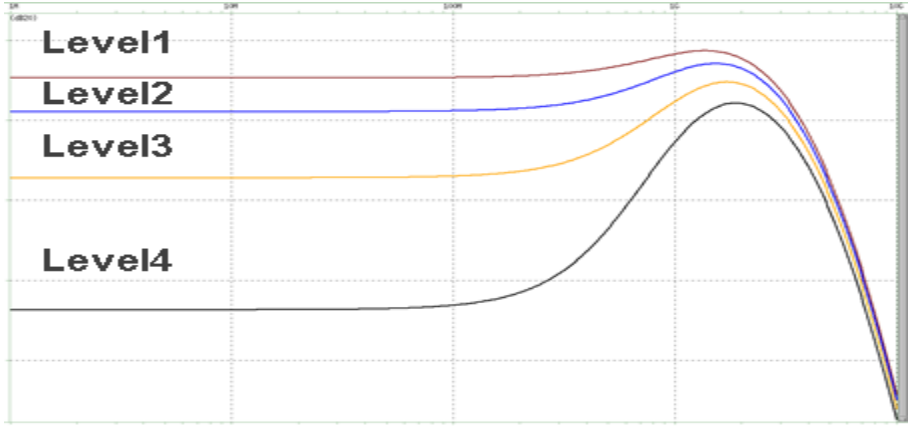
w de-emphasis

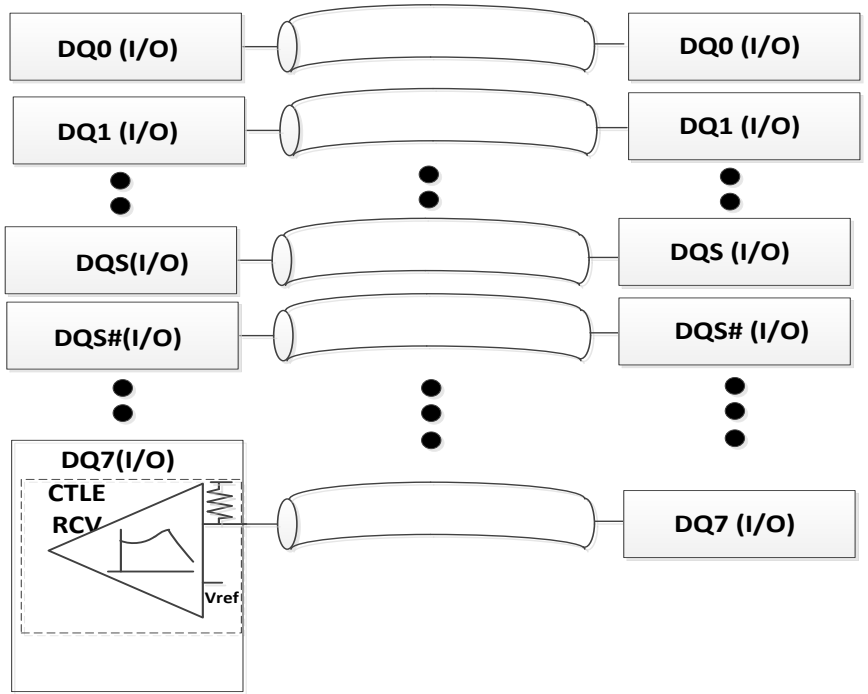


w/o de-emphasis

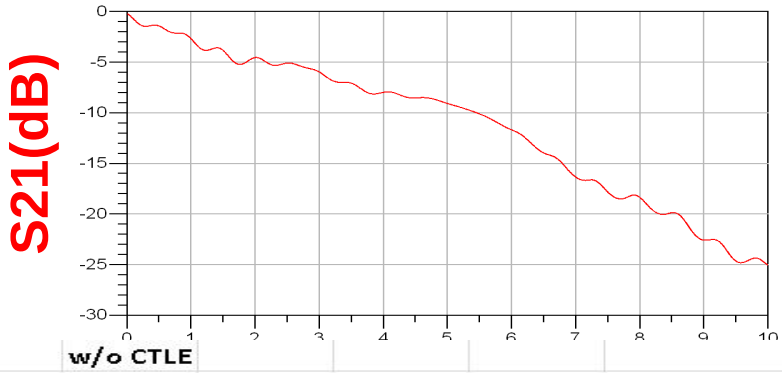


Receiver Continuous Time Linear Equalizer



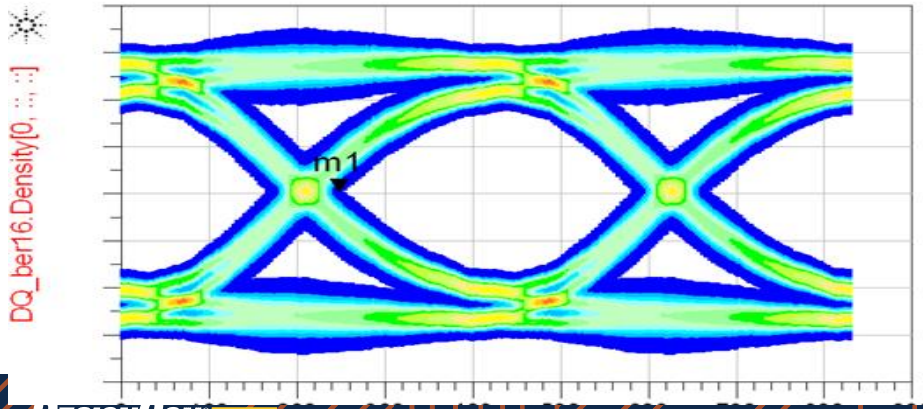


Read Data Eye Improvement with CTLE Improvement

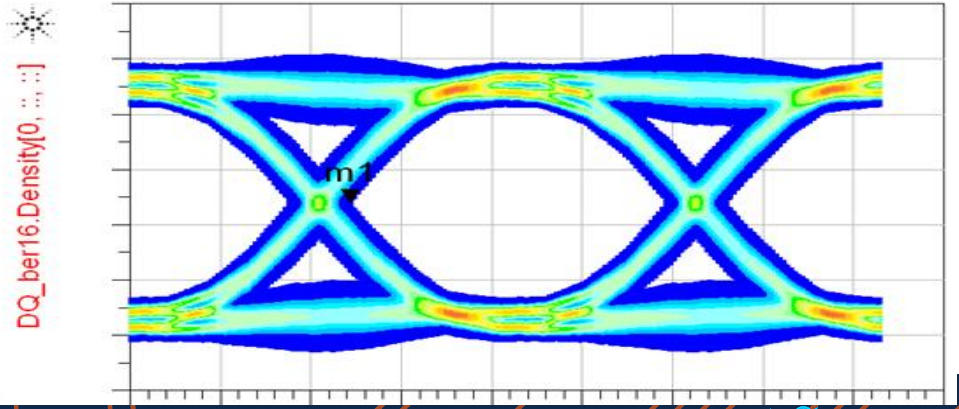


→ *With CTLE ~ 9.6% improvement*

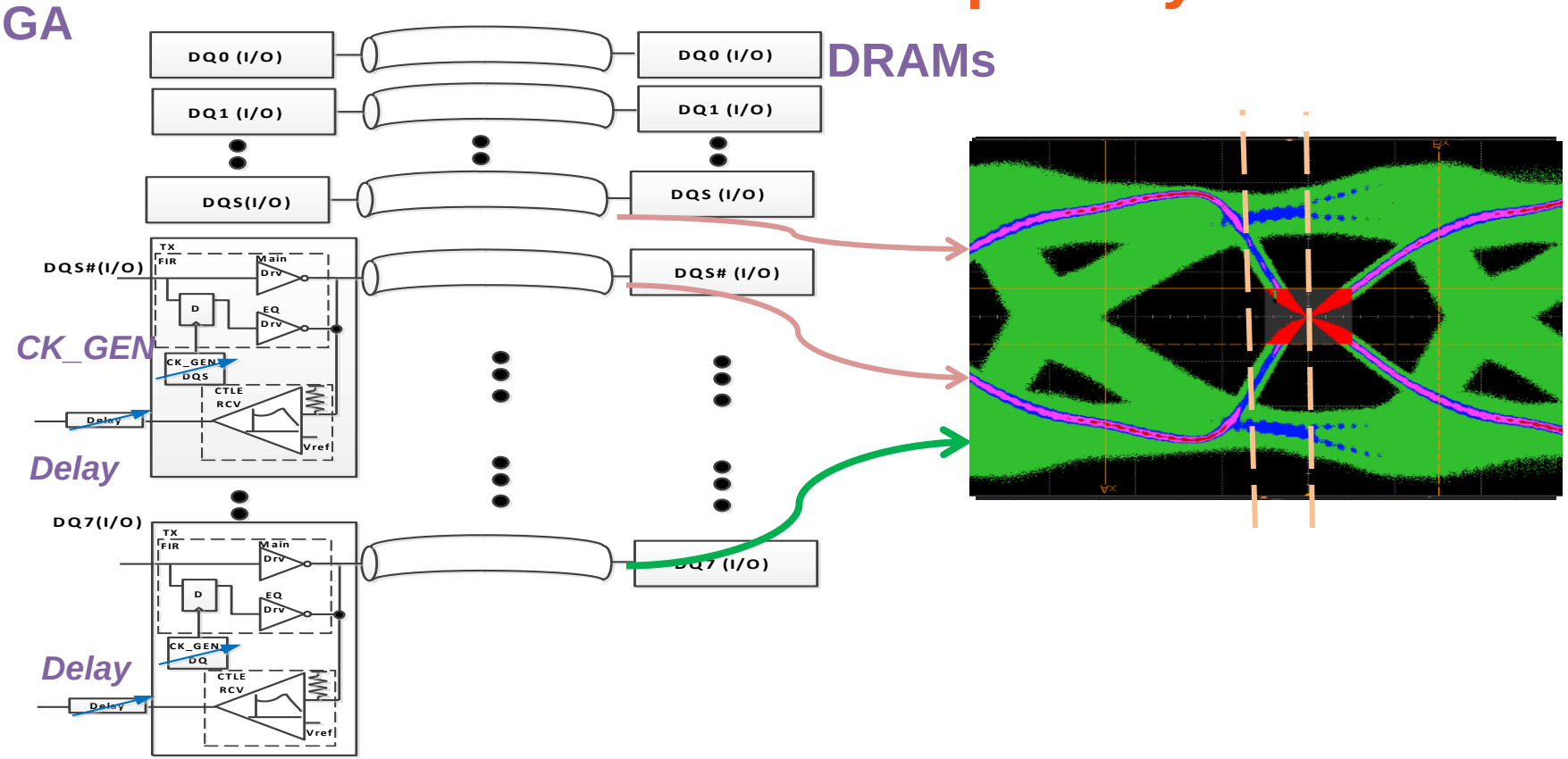
w/o CTLE



w CTLE



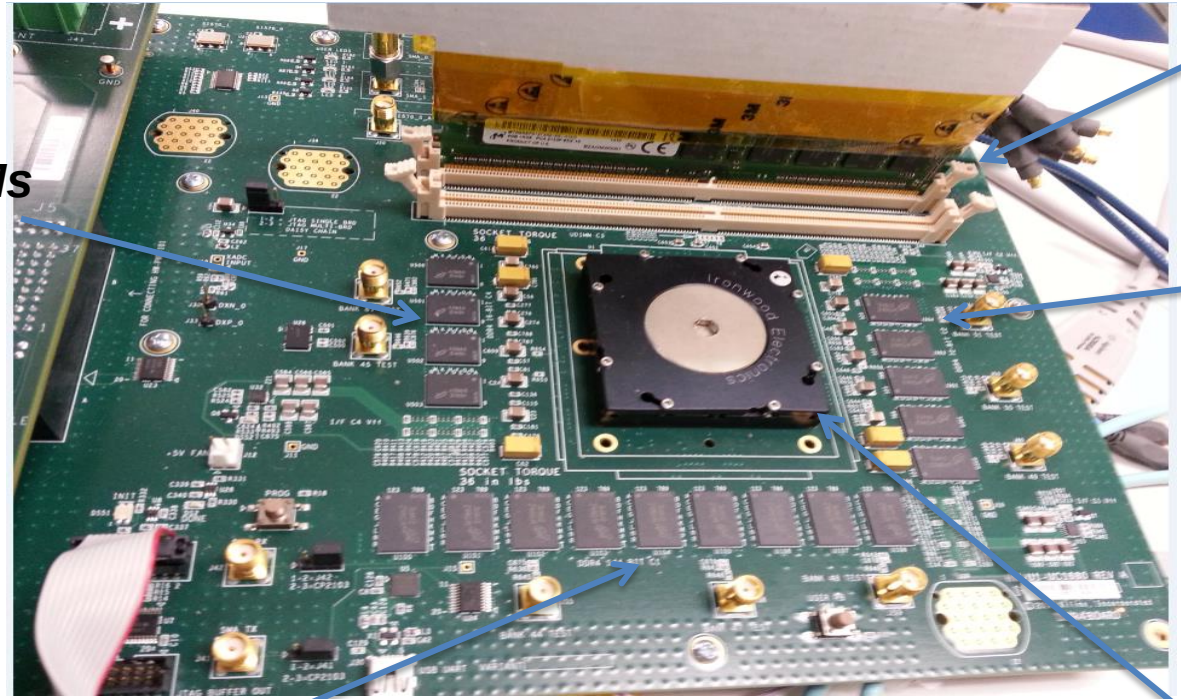
Per Bit De skew Capability



Experimental Data Validation

- Validation System Configuration
- Write Shmoo Procedure Overview
- Read Shmoo Procedure Overview
- Data Eye Scope Capture
- Over Clocking Results

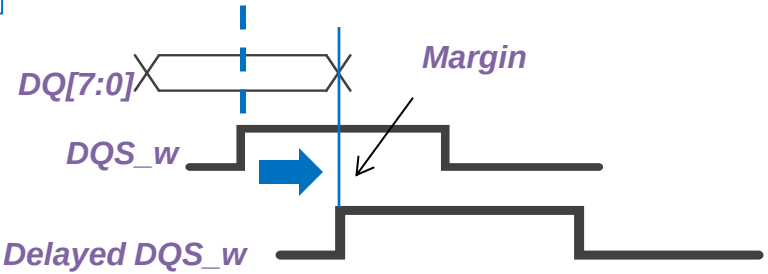
Validation System



Write Shmoo Margining Test Flow

FPGA

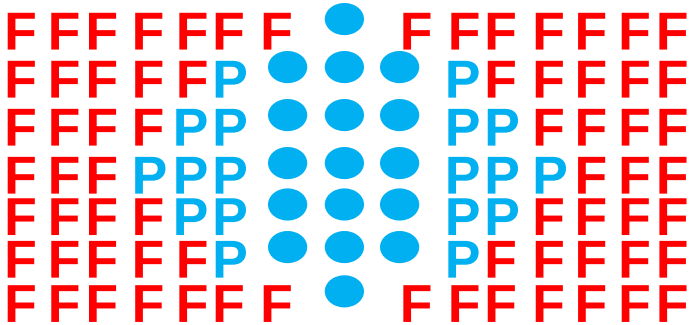
Margining Shmoo



Write DQS pushes to find the min. passing eye

DRAM @Vref_i

DRAM Vref_i+1
DRAM Vref_i
DRAM Vref_i-1



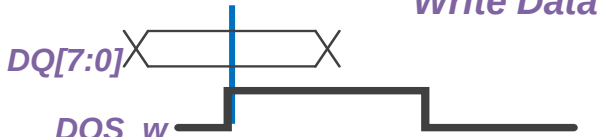
= Starting Pt After Calibration

= FPGA Internal Cal. Strobe position

Read Shmoo Margining Test Flow

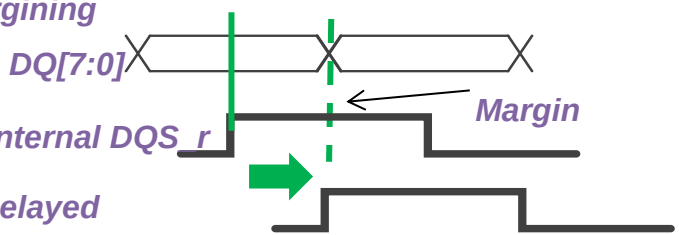
FPGA @Vref_ j

Write Data Send to DRAM (like regular Write)

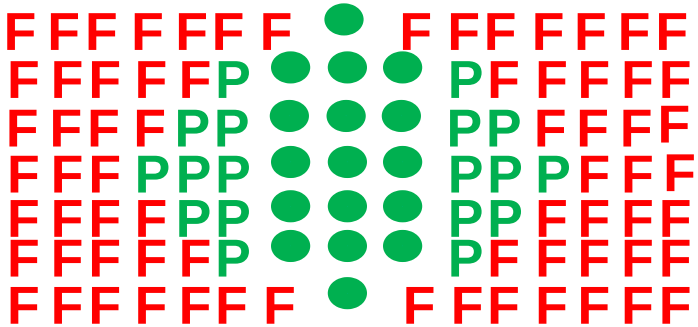


DRAM

Read Margining



FPGA Vref_ j+1
FPGA Vref_ j
FPGA Vref_ j-1

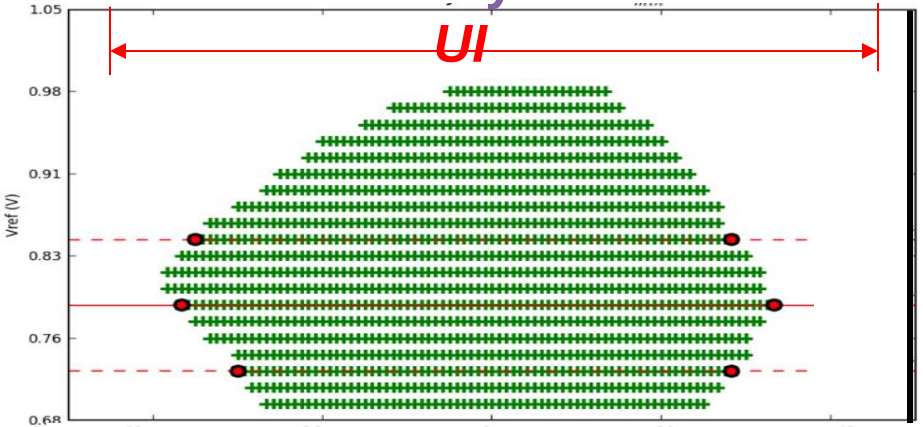


= Starting Pt After Calibration

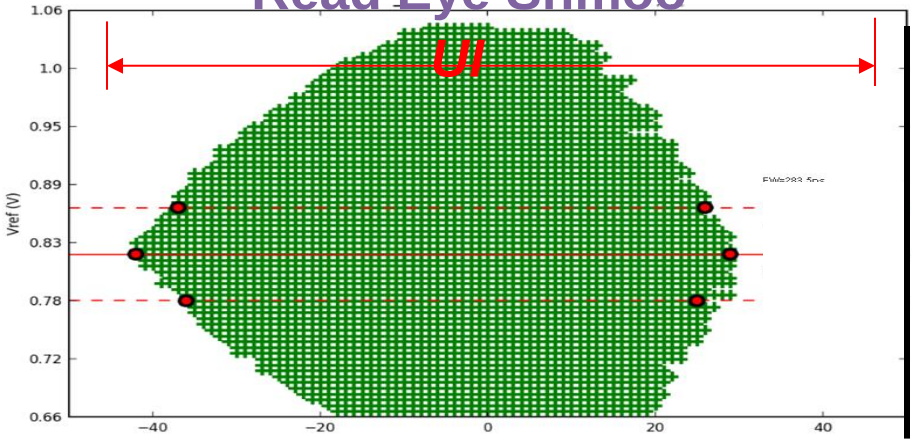
= FPGA Internal Cal. Strobe position

Write and Read Eye Shmoo at 2400MTs

Write Eye Shmoo



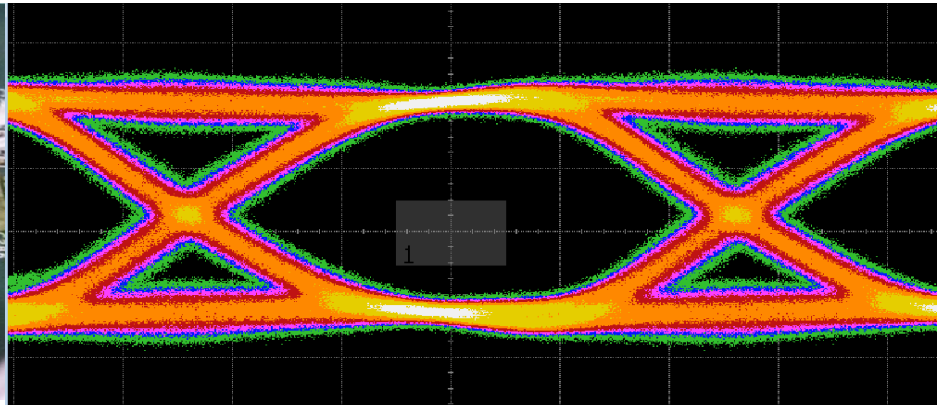
Read Eye Shmoo



DDR4 Memory Write Eye (Scope) Measurement
Write Eye Capture at 2400MTs

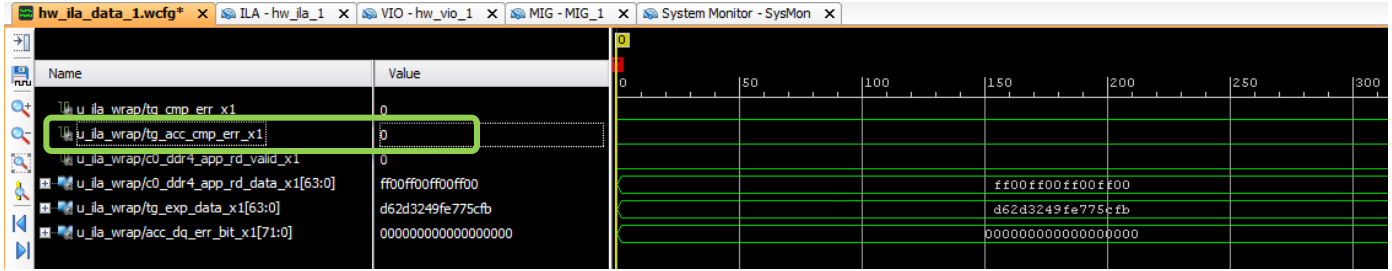
Probes Attachment

Write Data Eye Capture

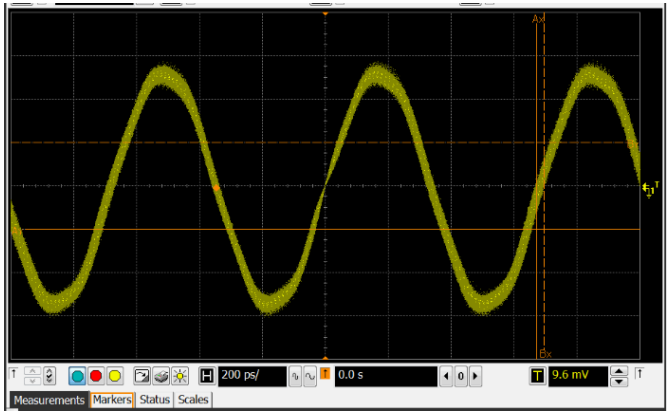


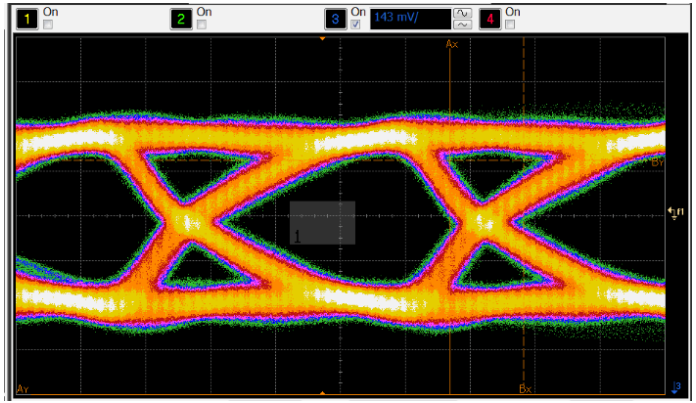
Over Clocking Results (at 2933MTs)

No Error



System Clock has low Jitter.





Data Eye has sufficient margin.

Summary & Conclusions

- A top down systematic approach using statistical DOE enabled an effective method to ensure design robustness.
- System enablers such as routing selection, IO equalization circuits improvement were quantified.
- Validation procedures and empirical data showed healthy margin for the DDR4 running at 2400MTs.
- Over clocking data indicated that the Interface is functioning at 2993MTs with lower system clock jitter and sufficient data eye margin.