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Model Extraction and Circuit Simulation Approaches for Successful SSO Analysis of Chip-Package-Board Systems

Brad Brim, Cadence Design Systems
bradb@cadence.com

Mike Kang, Cadence Design Systems
mkang@cadence.com

Chris Wyland, Xilinx Inc.
chris.wyland@xilinx.com

Romi Mayder, Xilinx, Inc
romi.mayder@xilinx.com

Abstract

This paper concerns guidelines to support successful SSO analysis for Chip-Package-Board systems. The procedures detailed address extraction and circuit simulation application of high node-count (N>100) frequency domain models. The focus of this paper is the low frequency portion, including DC, of the spectrum for broadband S-parameters. Frequency domain model extraction options and transient circuit simulation options were investigated and their interdependencies are discussed. These procedures apply to a broad class of extraction and transient circuit simulation tools typically applied to support SSO analysis. A high-speed digital board with 50 single-ended channels was applied as a test vehicle for guideline development.

Author(s) Biography

Brad Brim is a Senior Staff Product Engineer at Cadence Design Systems with over 20 years of experience in EDA tools for code/algorithm development, marketing, applications engineering, and product management. His present responsibilities are with package and board SI/PI extraction tools and chip/package/board system-level applications. His past experiences were in the area of RF/microwave/antenna modeling for components, circuits and systems with EM and circuit analyses.

Mike Kang has over 10 years of experience as an Applications Engineer for high-speed and high frequency applications in SI/PI, RF/microwave/antennas, circuit and system simulation, and other related areas. He is currently an Applications Engineering Director at Cadence Design Systems.

Chris Wyland is a Senior Staff Signal Integrity Engineer in the System Signal Integrity Group at Xilinx, Inc. He has over 20 years experience in package electrical modeling and signal integrity, working at such companies as Xilinx, Philips Semiconductors, and Integrated Device Technology. He has published over 10 papers in the area of package signal integrity and holds over 20 patents.

Romi Mayder is Manager of Transceivers and IOs at Xilinx, Inc. Previously, he was Senior Staff Signal and Power Integrity engineer at Xilinx, Inc. Prior to joining Xilinx, Mr. Mayder worked as a consultant specializing in silicon die level signal and power integrity. Mr. Mayder also has over 10 years experience in semiconductor process technologies. Mr. Mayder received his BS Degree in Electrical Engineering and Computer Science from the University of California at Berkeley in 1992. Additionally, Mr. Mayder has published 25 patent applications in the fields of signal and power integrity, as well as semiconductor process technologies.

Motivation

The application of time domain (TD) circuit simulation to characterize simultaneous switching output (SSO) behavior of chip-package-board systems can be a challenging task. The application of high node-count frequency domain (FD) data models, typically from numerical extraction, is the root cause of this difficulty. Broadband FD model data is required for components in the system such as: IC package, printed circuit board (PCB), connectors, capacitors, cables, etc. Requirements for high frequency (HF) spectral content have been investigated by many authors. It is generally accepted the FD model should contain data to a frequency of at least 0.35 divided by the signal rise time (T_r). Requirements for low frequency (LF) data have been less thoroughly investigated and are the focus of this paper.

The technical objectives were to understand the requirements for LF spectral content of FD models, how to best store/transmit this information and how to most successfully apply the information for SSO analyses with TD circuit simulators. The goal was a best known method (BKM) applicable to various FD model extraction tools and various TD circuit simulation tools.

Preliminary

The first task is to unambiguously define "low frequency". Generally, this is the frequency range below which interesting spectral variations no longer occur and the device whose FD model is being extracted exhibits DC behavior. The entire system being modeled may have interesting spectral variations below this frequency bound, but the individual devices being modeled should each exhibit DC behavior. For example, a power delivery network (PDN) may have bulk capacitors and active device voltage regulator module (VRM) models that result in interesting spectral variations in the double-digit to triple-digit kHz frequency range. However, the electrical behavior of the PCB PDN geometry (absent these mounted components) should be devoid of interesting spectral content. The LF open/short circuit impedance of a PDN is "interesting" and enables determination of static (DC) capacitance/inductance, but the two most common effects of unloaded resonances and frequency-dependent resistance should not exist in the LF range.

Of these two most common effects frequency-dependent resistance usually occurs at a lower frequency than the first unloaded PDN resonance. PDN resonances are easily determined for PCBs and packages with FD extraction tools but will not be discussed in this paper. For most modern chip-package-board systems frequency-dependent resistance is the controlling factor to define the LF region. Frequency dependent resistance is easily approximated analytically to a surprisingly high accuracy, enabling an intuitive understanding based on simple physics.

First, assume a wide metal in which current flows with no edge effect. This reduces the analysis to only one dimension. To good approximation, the current density within the metal will decay exponentially relative to the density at the top/bottom surface as the position is separated from the surfaces. Different current density amplitude may be assumed at the top and bottom of the metals to address non-symmetric stripline or microstrip. This does not appreciably change the character of the results for frequency-dependent resistance but dos slightly extend the bandwidth over which transition from HF to LF effects will dominate. The total current **I** is simply the integral from bottom to top of the assumed current density. Consider a value **J** defined as the integral from bottom to top of the square of the current density. Frequency-dependent resistance is simply the DC value scaled by the frequency-dependent value of ($\mathbf{J}^2/\mathbf{I}^2$). This frequency-dependent resistance value is variational with respect to the accuracy of the assumed current distribution. This implies a first-order error in the assumed current distribution results in only a second-order error in the value of resistance to yield surprisingly accurate results from such a simple analysis.

Based on this frequency-dependent scale factor it is quickly determined that the frequency-dependent resistance of a metal remains within 10% of its DC value up to frequencies where the metal thickness (T) is about two skin depths (δ). Comparison of the results of this variational one-dimensional analysis to the classical skin loss equation shows less than a 10% variation for frequencies above which T is greater than about 5 δ. For frequencies below which T= δ the frequency-dependent resistance varies negligibly from its DC resistance. For a design that applies copper for all planes and traces the largest value of metal thickness will define the lower bound of meaningful frequency-dependent resistance effects. The smallest value of meal thickness will define the upper bound of meaningful frequency-dependent resistance effects. If some metals are very thin, this simply implies they will exhibit a bit of frequency-dependent resistance effect into a range where other spectral effects have likely already come to dominate.

FD extraction tools vary significantly. Since DC (0 Hz) is a frequency point, DC analyses are a subset of the more broad class of AC analyses. The difference between DC extraction and AC extraction is the most distinct and considered first. DC extraction must solve separately for electrostatic (capacitance and shunt conductance) and magnetostatic (inductance and series resistance) effects. DC extraction is typically a less resource intensive task performed by DC-focused extraction tools. The numerical manipulations are often real valued rather than complex-valued and algorithms better numerically conditioned for a more stable solution. DC results, and only DC results, are available from DC solvers. AC circuit simulation may be performed where the frequency behavior of circuits is approximated through user driven distribution of the DC extracted parasitic. For example, for a thru signal net, the DC extracted series L value may be split and combined with the separately DC extracted C value to form a TEE circuit to approximate AC behavior.

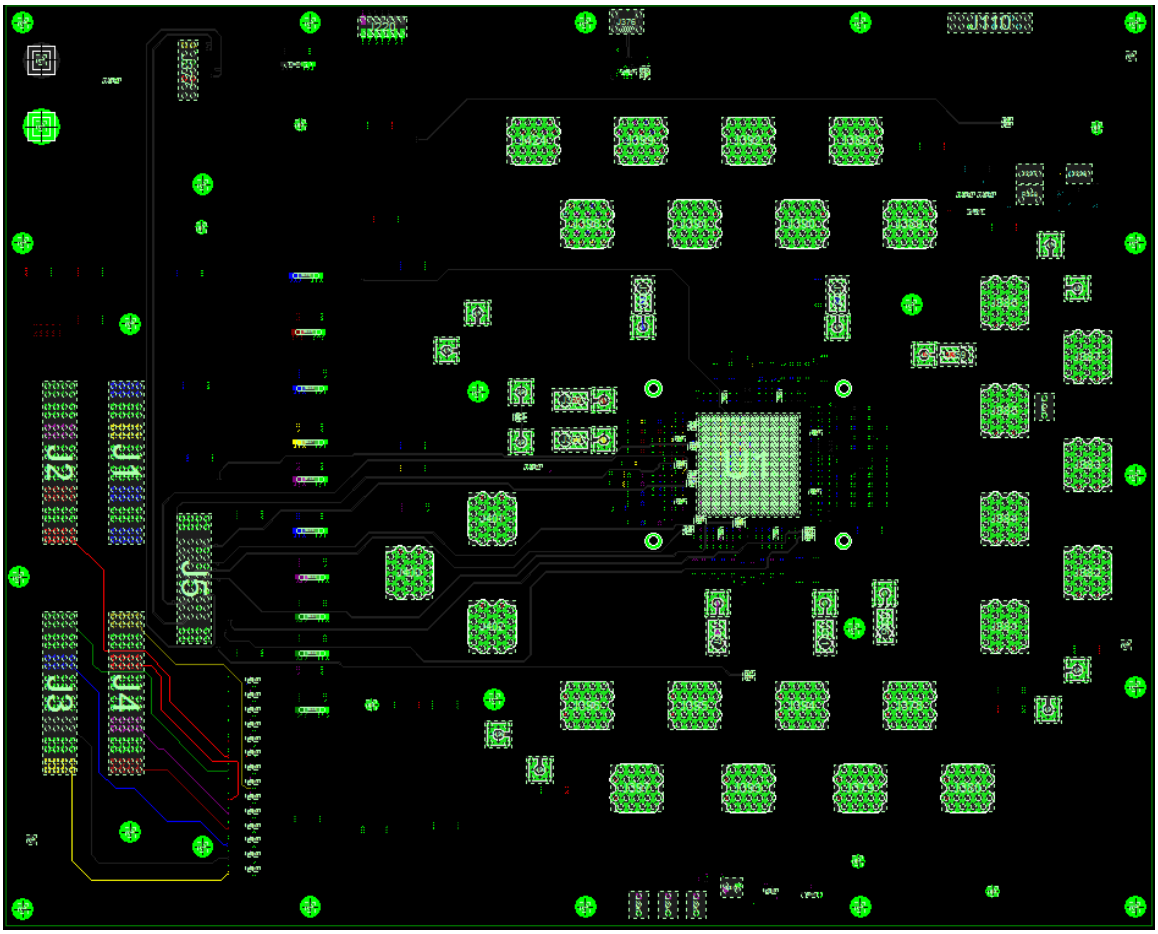
In contrast, AC FD electromagnetic (EM) analyses simultaneously solve for both capacitive and inductive effects. A matrix equation is typically setup to solve for each frequency point of interest. The elements of this matrix equation involve both capacitive

terms with impedance proportional to $1/\omega$ and inductive terms with impedance proportional to ω. Therefore, as ω approaches zero (DC) the matrix equation becomes ill conditioned as $1/\omega^2$ and the lowest frequency extraction results are unreliable. DC results are therefore rarely available from AC extraction tools, even if special pre-conditioning algorithms are applied to reduce the frequency of eventual numerical instability. This numerical stability behavior varies depending upon the analysis algorithm selected and any special approaches considered in the specific implementation. It also depends significantly on the complexity of the design being considered, with less well conditioned solutions for larger designs and geometries with extreme geometric aspect ratios. Some AC FD extraction tools cannot solve well into the frequency range below which frequency dependent resistance effects are negligible, typically on the order of 1MHz for PCB designs. Other extraction tools may be well conditioned (for some designs) below 1kHz. Whatever the lower frequency range for the extraction tool being applied, any presence of numerical noise will dramatically affect the success of so-called "DC extrapolation" of AC FD extraction results in the absence of explicitly available DC results.

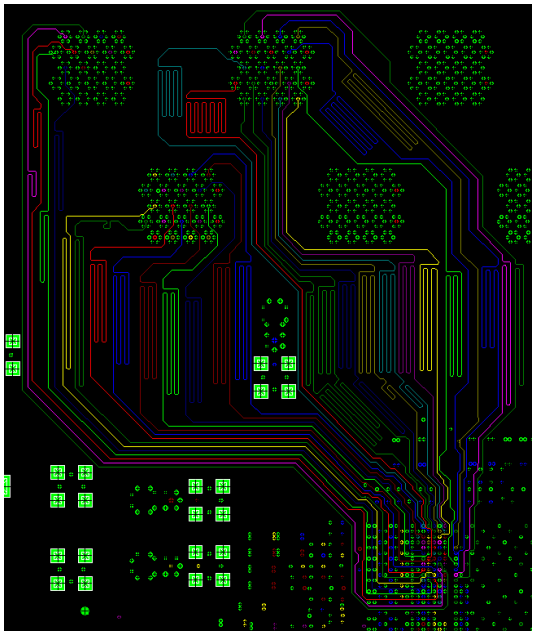
Test Case

The test case applied for this investigation was a verification board provided by Xilinx. The system characterized for SSO behavior contains models for chip, package, PCB, decaps, and cables. A set of 50 single-ended signals are considered along with the PDN. Power-aware IBSI models are applied for the on-chip drivers, including [Composite Current], [ISSO PU] and [ISSO PD] keywords. A simple on-die parasitic lumped RC model is applied. FD package and PCB models are extracted with a whole-board/package FD analysis tool based on a hybrid of electromagnetic and circuit analyses. A simple cable model is applied off-board for all 50 channels along with lumped 50 ohm terminations. The clock frequency was 254MHz with a rise time of 100pSec.

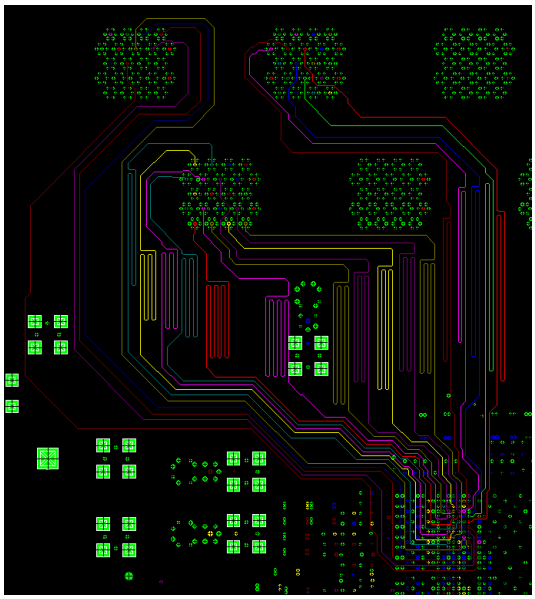
The PCB is significantly physically larger than other components in the system and should electrically dominate the need for broadband FD models with complex spectral content. The application of this PCB FD model is the gating factor for successful SSO simulation. The PCB is a 24-layer design with multiple power domains. The 50 single-ended signals were routed on layers 3 and 5 and are shown in the following figure.



Layer 2, Top



Layer 3, Upper Routing



Layer 5, Lower Routing

Investigation

For the upper frequency of FD model extraction a conservative value of 6GHz was applied. This exceeds the familiar suggested value of $0.35/T_r$=3.5GHz. Again, HF spectral effects are not considered as part of this.

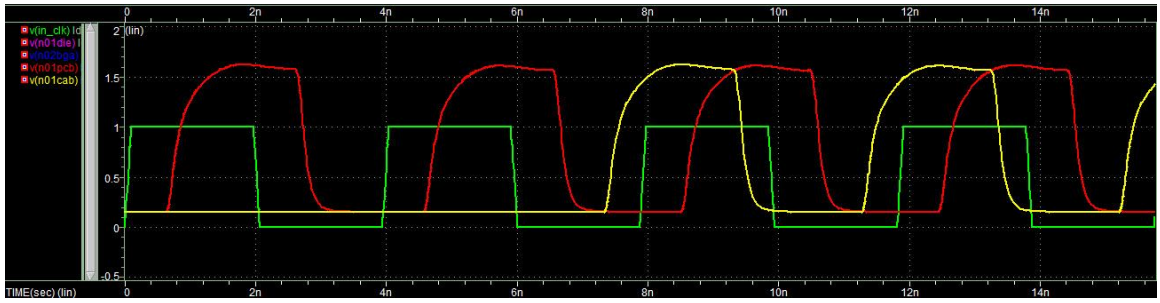
The above analysis of frequency-dependent resistance was applied to define the LF region. The maximum copper thickness for all layers was about 37um. This corresponds to a frequency of about 500kHz for a metal thickness of one skin depth; below which little frequency-dependent resistance should occur. A conservative choice was applied to define the LF range as: DC to 100kHz. This enables the FD results to have a region of at least a half decade for which only DC behavior will be exhibited. This decision was based on knowledge that some circuit simulation tools perform DC extrapolation based on a number of the lowest frequency results. These extrapolation frequency sample points may be selected only as explicitly available data or may be interpolated sample points. Combined with the intent to explore the effect of logarithmically sampled low frequency samples and lowest extraction frequency a half decade of bandwidth was deemed sufficient but not excessive.

Any variations within and above the dominant bulk loss to skin loss transition frequency range will be considered as general spectral content of the signal, will remain a constant effect as we investigate the LF domain and are therefore not a concern for this investigation.

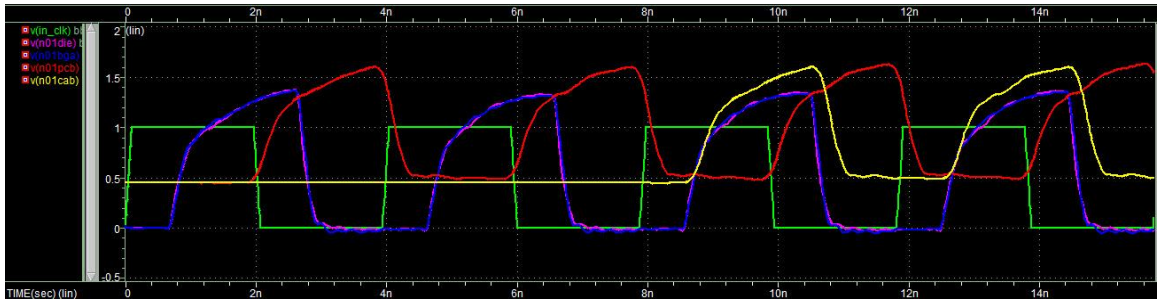
The general electrical behavior of the system design was explored prior to a detailed investigation of LF FD data effects on SSO. The following figures display a progressive level of detailed system model, progressing from an ideal design with only non-ideal driver models to the full consideration of all parasitics. The following results are displayed for each level of system modeling detail specified below.

1. Signal voltage sampled at:
    - on-die buffer input,
    - chip-package interface,
    - package-board interface,
    - board-cable interface,
    - load at the end of the cable.
2. PDN voltage sampled at:
    - on-board VRM,
    - chip-package interface,
    - package-board interface,
    - board-cable interface,
    - load at the end of the cable.

Non-ideal, power-aware IBIS drivers and on-die parasitics are augmented with ideal (i.e. thru) models for package, board and non-ideal cable models. As expected, the cable effect is minimal except for a delay.



Then a broadband package and a broadband PCB model are added. The board is observed to dominate the non-ideal behavior of the system for both signals and power.



IMPORTANT:

- All system design modeling variations examined for this investigation consider all available non-ideal device behaviors. Only the PCB 102-port FD model is varied from case-to-case with all other chip/package/decap/cable parasitics remaining the same for each different combination of extraction tool and circuit simulation tool options.
- The package requires a broadband FD model, and in some sense could affect the conclusions of this investigation if not simultaneously varied in exactly the same manner as the PCB model. To remove this possibility the package FD model is processed after extraction and before any circuit simulator to produce a known-good rational function model with assured passivity and assured causality. The circuit simulation tools considered during this investigation are known to apply this model directly without further preprocessing that may eliminate the assured passivity and causality.

Circuit simulator variations are summarized first. It was envisioned prior to this investigation that more simulator options would be explored in greater detail than what was decided to include as the investigation proceeded. This likely would have been the case had HF issues been [re]considered in this investigation. In the absence of discussing

options unique to each individual circuit simulator, the key option to consider is whether or not to apply a rational function for the transient simulation, which might be termed "*to fit or not to fit*". This is not as profound as Shakespeare's Hamlet pondering death, but this high level decision will dramatically affect circuit simulation. Fitting a rational function to FD data is not a trivial task and can require significant time, but the alternative is almost always much worse for large node count broadband FD models. This investigation found direct application of the 102-port PCB model to be impractical and therefore only rational function based circuit simulations were explored in detail. Excessive computation times were experienced along with convergence and accuracy relative to simulation of the nominal design setup. A benefit of applying a rational function model is that once the rational function is created for a set of FD data it may be re-used for any subsequent circuit. This is a dramatic time savings.

The investigation of FD extraction tool options was much more extensive, yet yielded less definitive conclusions. The following options for extraction data were explored:

1. discrete data points
    a. varying minimum extraction frequency
    b. linear vs. logarithmic frequency points
    c. explicit DC point
2. continuous data points
    a. with and without explicit DC point
3. external MM tool processing
    a. optional processing for passivity/causality

Discretely sampled FD extraction tool data is the most commonly available format. The lower the minimum extraction frequency the more difficult it is to sample uniformly at intervals of this minimum frequency. A minimum frequency of 1kHz would imply an obviously impractical 6 million data samples for the design considered in this investigation. Therefore, when data is uniformly sampled it is typically done at a varying interval for different bands of data. Each FD extraction tool will have a lower frequency of numerical stability, below which the FD data is susceptible to numerical noise. This is also design dependent. The FD extraction tool applied for this investigation produced visibly stable results to well below 1kHz but a minimum AC extraction of 1kHz was applied. Therefore, the low frequency range for this investigation was 1kHz to 100kHz. Corresponding to option **1.a** cite above, a number of uniform sampling intervals were examined between 1kHz and 20kHz. The HF data was sampled densely and remained fixed as the LF data was changed. Similarly, corresponding to option **1.b** above, the LF data was sampled with various logarithmic samples: (1, 3, 5, 10, 40) points per decade. Lastly, these sampling schemes were augmented with the addition of an explicitly generated DC result. This DC result was generated with a separate DC extraction tool. For this design value is typically within 10% of a value one would visually extrapolate when the results are viewed on a plot with logarithmic frequency axis.

A form of continuous FD results is available from some extraction tools. The extraction tool applied for this investigation generates refers to such format as "AFS", generated by an "adaptive frequency sweep" performed by the extractor to generate the data. A number

of commercially available FD extraction tools apply similar algorithms. These algorithms accept a specification of minimum and maximum frequency of extraction and then automatically select the extraction frequencies within this bandwidth to generate a continuous representation of the data. A set of discrete frequency samples are simulated that enable the underlying representation to predict results for any frequency point within the range to a reasonable accuracy. The continuous representations are typically considered proprietary and not user-accessible. The extractor applied for this study provides a binary file that may contain the continuous data representation. An API may be applied by circuit simulation tools to extract discrete data samples at any frequency point within the extracted data bandwidth.

There are two key benefits of this data representation. Firstly, this data representation is extremely compact. For the 102-port data and 6GHz bandwidth this binary, continuous format data file is about 20Mb while a discretely sampled data file required about 400Mb. The discrete sampling points were even selected with a goal of efficient storage while providing a reasonably good representation of the data. A variable (over frequency) blend of uniform and logarithmically spaced frequency samples. Typically, one to two orders of magnitude file size savings are observed for such continuous data representations. The next benefit is that this form of data representation may be viewed as a type of interpolation algorithm. It tends to yield smoother, more logical data than end-user (or circuit simulator based) interpolation of discretely sampled data. Peaks and nulls in the data are not missed by discrete samples and their precise location and value may be determined. A circuit simulator is free to provide unique benefit by sampling data at any frequency it desires without interpolating what may be already noise-infected, discretely sampled LF data.

As for discretely sampled data, addition of an externally generated DC data is explored. When this DC data is added an extractor-proprietary algorithm is applied to adjust the AC data to match exactly the externally generated DC data.

An external macromodel (MM) generation tool was applied to various sets of the above-described FD data. This enables investigation of preserving passivity and causality (corresponding to **3.a** above) as well as generating rational function and controlled source macromodels. A number of commercial and academic MM tools are available.

The importance of passivity and causality will be discussed below. Some circuit simulation tools require a rational function model to be pre-computed by an external MM. Other circuit simulation tools may apply these pre-computed models but are also able to automatically generate a rational function as part of the circuit simulation. These tools typically save the resulting rational function data to disk and have a “reuse” flag option available for the SPICE data element. It is certainly convenient to have the partial fraction model conversion performed automatically but little, if any, control over the process exists and no opportunity is provided to judge the quality of the resulting fit. Specifically, the passivity and causality of the rational function are of significant interest. The various MM tools have different levels of control over the process. Typical controls include: selection for the type of rational macromodel to generate, optional passivity

and/or causality enforcement and option to explicitly specify DC data. Some MM tools also provide utilities for validation of the macromodel and tuning the model generation process.

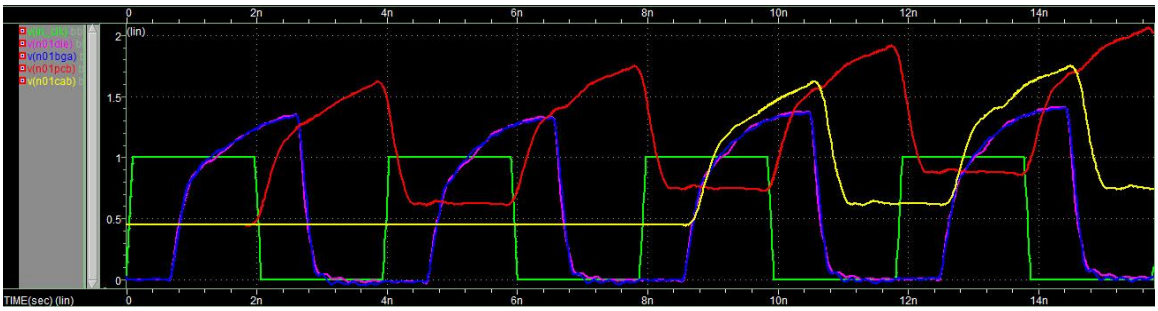
To assure successful TD circuit simulation it is important to assure the rational function model is both passive and causal. To assure passivity it is not adequate to assure the source FD data is passive. Though pre-processing the FD data prior to rational function generation can sometimes help, such algorithms are typically based on scaling of individual frequency point results and therefore inherently non-causal. They can also add "noise" to otherwise smooth LF FD data. If processing of the rational function to assure passivity will be applied, then pre-processing FD data for passivity may actually do more harm than provide benefit because of the extreme numerical sensitivity of generating DC data from LF FD data. LF passivity issues are often observed as ever-increasing DC offsets in the TD circuit simulation results, as shown in the results below. The external MM tool applied for this investigation simultaneously assures both passivity and causality so the two effects could not be investigated independently.

Some circuit simulation tools may not be able to apply a rational function model. The external MM tools often provide a controlled-source macromodel which may be applied for any SPICE-compatible TD circuit simulation tool. This model is not nearly as efficient as rational function models. This controlled source model has the same concerns with passivity and causality as described above for rational function models.

Observations and Discussion

The success of TD circuit simulation to support system-level SSO analysis with high node count, broadband FD models is highly dependent on the LF spectrum. Extreme numerical sensitivities to noisy data in the LF spectrum are observed.

Recall that all lower frequencies considered are 100kHz or below to assure avoidance of frequency dependent resistance effects. Seemingly random success and failure were observed for various discrete sampling options. As long as a reasonable number of samples, seemingly in the high single to low double digits, are available in the LF spectrum the sampling (both linear logarithmic) and lower frequency did not seem to matter much. This statement should be considered in the light of the additional observation that as long as a reasonable DC value may be numerically extrapolated the results were not highly dependent on this DC value. Variations of what seemed to be in the low double digits range for DC extrapolated values were not perceptible in the SSO TD responses. The key issue seems to be if the TD circuit simulation succeeds or it fails, not an issue of absolute accuracy when it succeeds. The following graphic shows a typical set of incorrect results observed when a macromodel is generated with improper DC values due to LF noise. Notice the ever-increasing DC offset of the waveform (red and yellow traces, PCB and load respectively) despite the reasonable AC behavior. This is an obvious failure early in the transient response. Less obvious failures in the later time responses were also observed, though it was more common to experience obvious early-time failures.



Typical incorrect time domain response caused by a low-frequency issue.

It is troubling that "seemingly random" failures are observed. For example, the same uniform sampling scheme starting at 1kHz succeeded but it failed for uniform sampling starting at 10kHz. Similarly, sampling of 5 points/decade was observed to succeed but failure observed for 10 points/decade and success again observed at 40 points/decade. Extreme numerical sensitivity is obvious. To explore this, slight changes were made in the FD extraction tools that resulted in slightly different but extremely similar results. Specifically, the consideration of voids in the ground plane was changed from actually being voids to being filled. Specific options were reexamined and some failures were now successes, but some previous successes were not failures. Upon further examination, the cases that failed tended to have numerical noise in the LF range in the third digit. As specific example, an impedance intuitively expected to have monotonic behavior as DC

is approached had non-monotonic behavior in the third digit of a data for a single frequency point near 10kHz . Though it was not explored in detail due to time constraints, this general behavior seems to indicate that more frequency samples in the LF range are not always better and may represent additional opportunities for numerical noise to creep into a DC extrapolation algorithm. There seems no definitive manner to assure success in the presence of noisy data and a variety of algorithms for DC extrapolation unique to each TD circuit simulator.

It was also observed that one should maintain as much correlation as possible between an explicitly provided DC value and what would be a visually user-interpreted DC extrapolation value. The lower in frequency the provided AC FD data and the larger the difference between explicitly-supplied and visually extrapolated DC results resulted is more frequent TD circuit simulation failures. Both the inline circuit simulation tool and external MM tool rational function generation process seem to be sensitive to this combined set of lowest frequency and DC value discrepancy. Therefore, considering the lack of sensitivity to exact DC value for SSO simulation, this observation implies it may be better in some cases to not provide an explicit DC value. Again, the key issue seems to be one of success and not a gradation of accuracy within that success. For designs where sensitivity to precise DC value exists, this conclusion would not be valid.

Continuous data representations were explored next. In general, success was far more frequent. As expected the failure mechanisms were much the same, just far fewer failures. Circuit simulation tools that apply this format perform an automated sampling of frequency points, implying no possible comparison to previously examined options for discretely sampled data. When an explicit DC point is added the AC results are slightly changed to extrapolate to the fixed DC point. The difference in the TD circuit simulation results could not be perceived, again due to the lack of sensitivity to the LF spectrum for successful simulation. One case was observed for which this adjust met of AC data yielded human perceptible a single non-monotonic impedance in the double digit kHz range. This case failed with the above displayed ever-increasing DC offset type behavior. The extraction of continuous data is not only easier for user consideration in the FD extraction tool but it is also more stable for subsequent TC circuit simulation.

The last option to explore is more of a postprocessing of FD extraction tool data using a MM tool. A number of the above options for discrete and continuously sampled data sets were externally converted to rational function models. This is essentially the same process that was performed inline by the circuit simulation tools applied. As expected, the success of subsequent TD circuit simulation was not significantly affected. There was not a perfect one-to-one correspondence between the success of externally generated versus internally generated rational functions, the correlation was very similar.

When the externally generated rational function models were further processed to preserve passivity and causality success of TD circuit simulation was assured for all cases. Passivity is exclusively discussed here because the applied algorithm implicitly assures causality. This assured success statement must be qualified by noting that for one of the cases examined the passivity algorithm initially in the MM tool flagged failure.

The rational function behavior was observed in the MM tool and data from one particularly noisy frequency point was manually excluded. The MM tool passivity/causality preservation process then completed and yielded successful TD circuit simulation results.

It should be noted that even with a passivity and causality ensured model a circuit simulator could potentially fail. For example, if passive and causal discrete data samples are passed to a circuit simulator where they are subsequently interpolated then passivity and causality may not be maintained. Direct application of the underlying rational function model avoids this potential issue.

Summary and Guidelines

In the absence of assured passive and causal LF data it is difficult to assure success of SSO analyses for high node count, broadband FD data. Sensitivity were observed to data noise level not humanly perceptible in plots of FD results. Avoiding numerical noise is the key issue for such FD results. An understanding of the LF performance of the FD extraction tool applied is key to success. Lower minimum frequencies and more data points do not assure success but are often helpful (in the absence of noise). Continuous data yields greater success relative to what may be more elaborate (yet more heuristic) end-user sampling schemes. Sensitivity of SSO TC circuit simulation results to precise DC value seems low, but this was not verified for a board class of SSO designs. The key issue required to assure successful TC circuit simulation is passivity and causality enforcement.

The following is a BKM guideline for addressing low frequency issues for successful system-level SOO characterization. The first item is preferred and the others are required. They key to assured success is item 5.

1. Apply an adaptively sampled frequency sweep in the FD extraction tool. (preference)
2. Minimum frequency should be specified well below the lowest frequency at which frequency dependent resistance is expected to occur.
3. Minimum frequency should be specified high enough to avoid numerical noise in the FD extraction tool being applied.
4. Do not apply explicit DC data that is inconsistent with the AC data.
5. Generate a rational function model with assured passivity and causality.
6. Apply this rational function directly in the TD circuit simulator.