DesignCon® 2014

Distributed Modeling and Characterization of On-Chip/System Level PDN and Jitter Impact

Dmitry Klokotov, Yong Wang, and Jin Shi
Xilinx Inc.

XILINX
ALL PROGRAMMABLE™

January 28-31, 2014 | Santa Clara Convention Center | Santa Clara, CA

UBM Tech

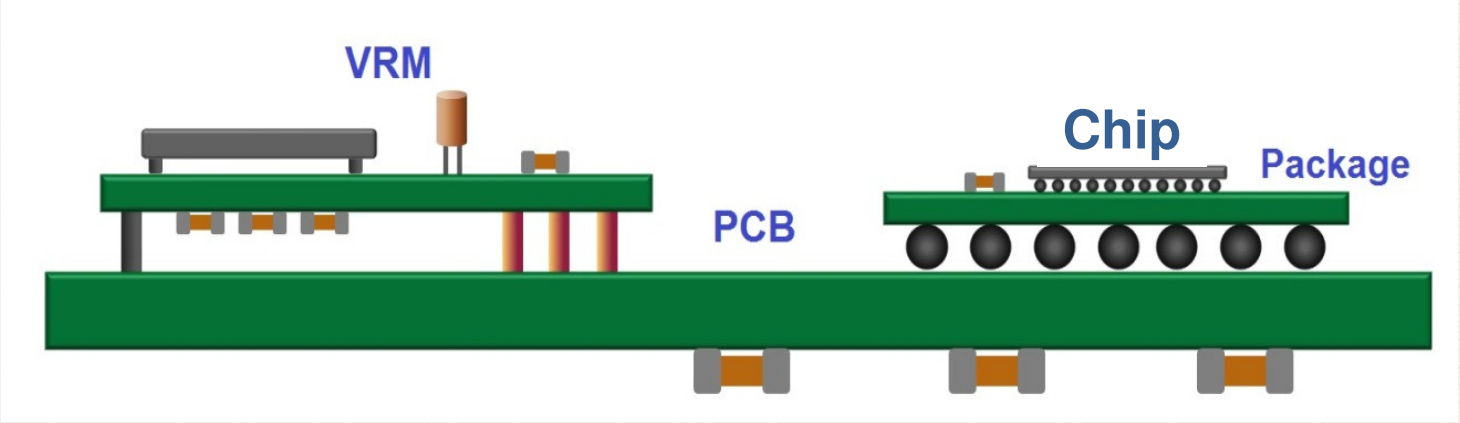
Intro

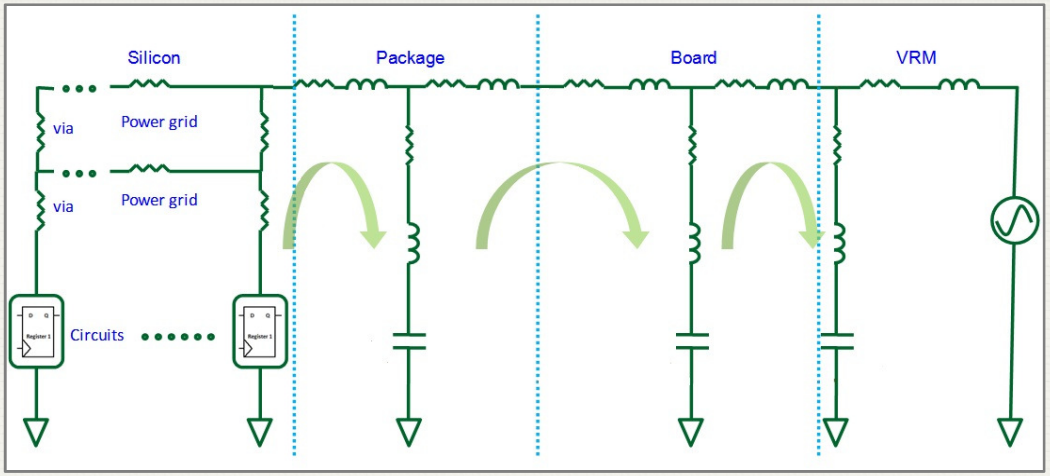
- **Power integrity challenges**
  - More logic with each new generation of ICs
  - Higher data rates
  - Lower supply voltages
  - Shrinking timing margins
  - Cost optimization
- **To create a successful design need to**
  - Develop system-level PDN modeling methodology
  - Work out design specs and performance metrics
  - Develop characterization methodology
  - Correlate measured results with simulation predictions
  - Learn from the correlation, make adjustments
  - Repeat…

In This Presentation

- PDN components, their physical nature and contribution to voltage noise
- Approach to modeling
- Time domain and frequency domain metrics
- Simulation results
- Characterization options offered by FPGAs
- Measurement and correlation
- Voltage noise impact on system timing. Jitter

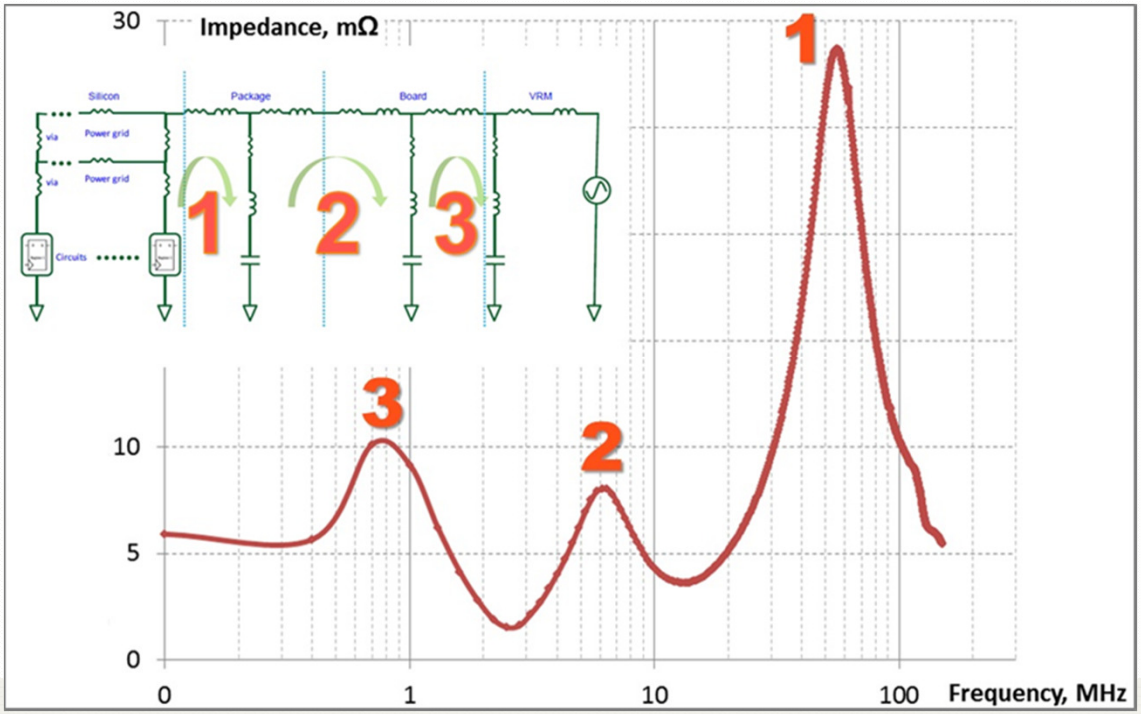
PDN Components



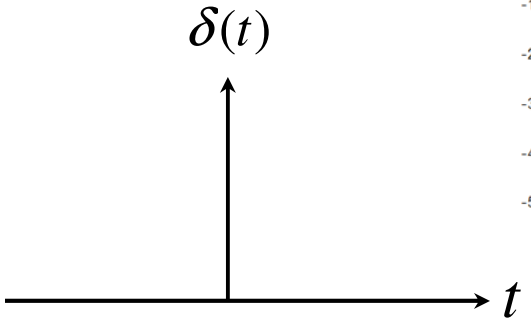


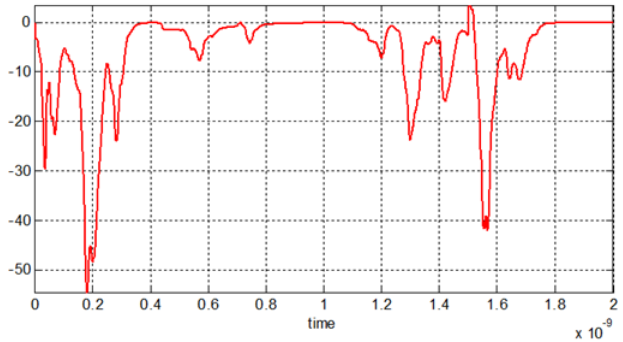
PDN Impedance

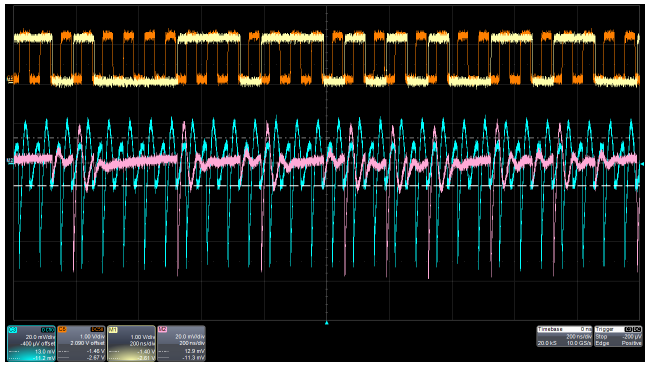
- **Resonances**
  - On-die capacitance & package inductance
  - Package decoupling capacitors & PCB inductance
  - Smaller PCB decoupling capacitors & board-level PDN inductance
  - Bulk PCB decoupling capacitors & VRM



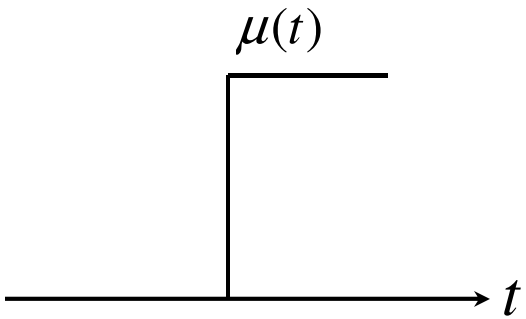
Voltage Noise

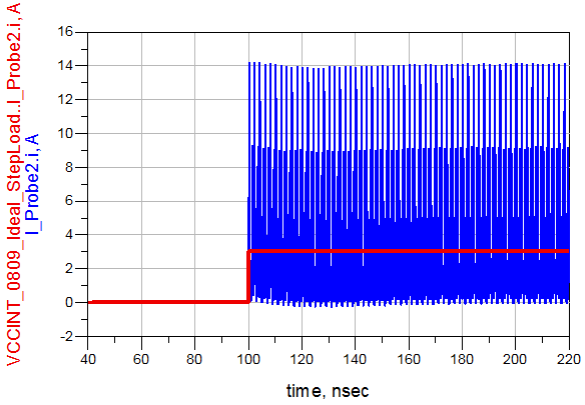


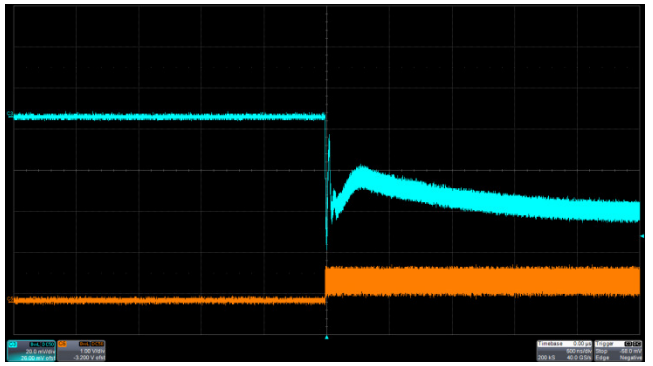




High Frequency Switching

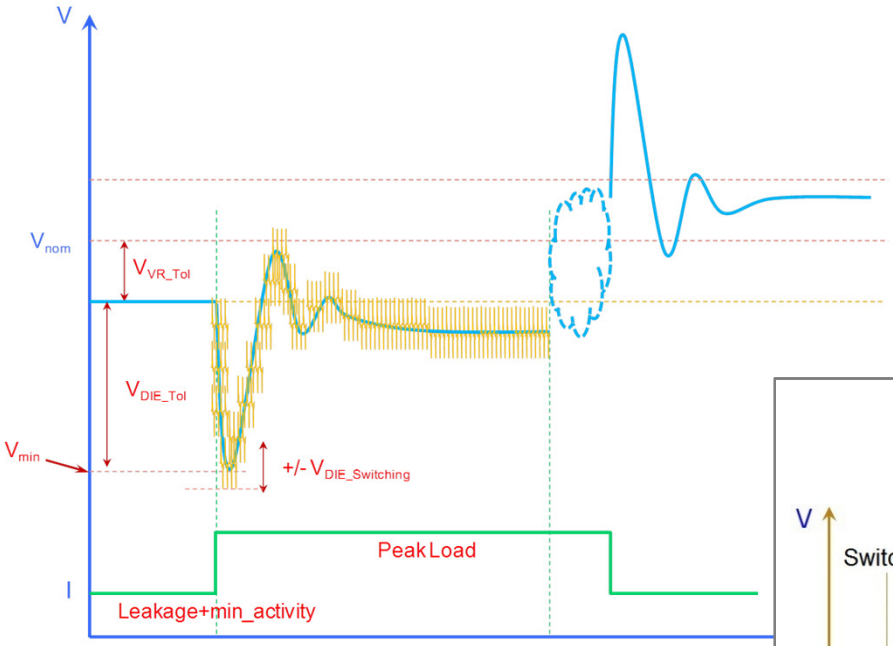


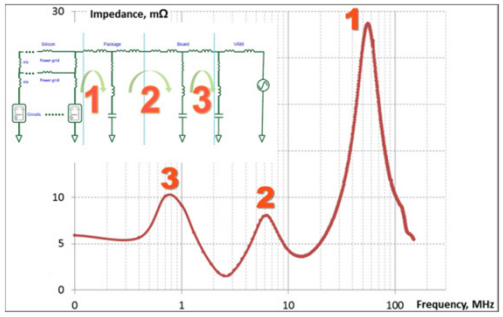


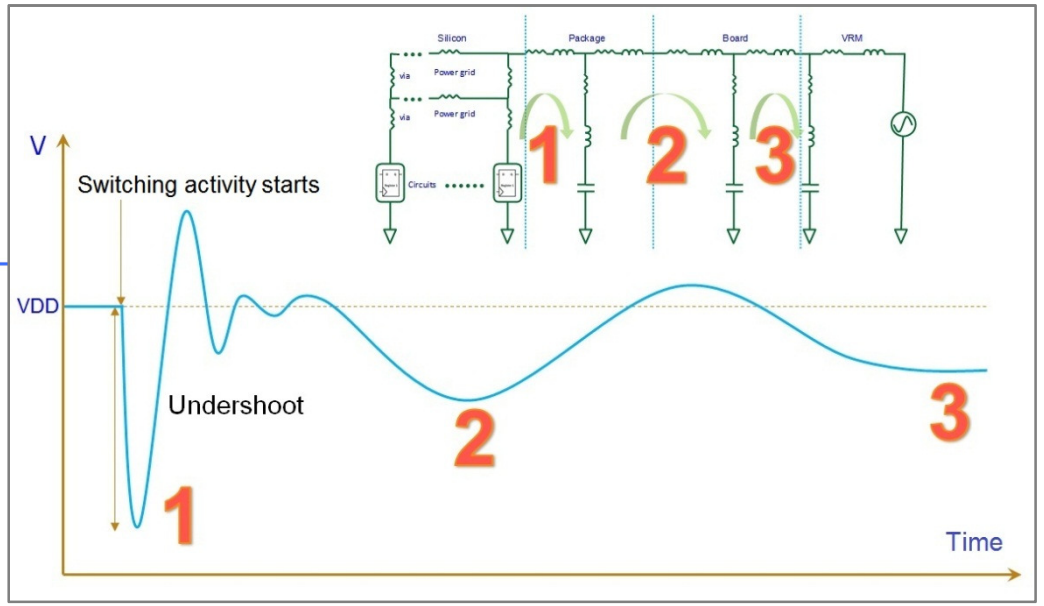


Event Driven

Voltage Noise

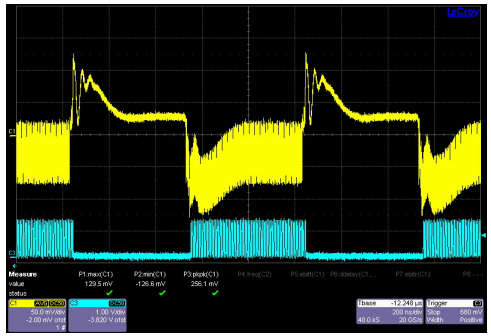




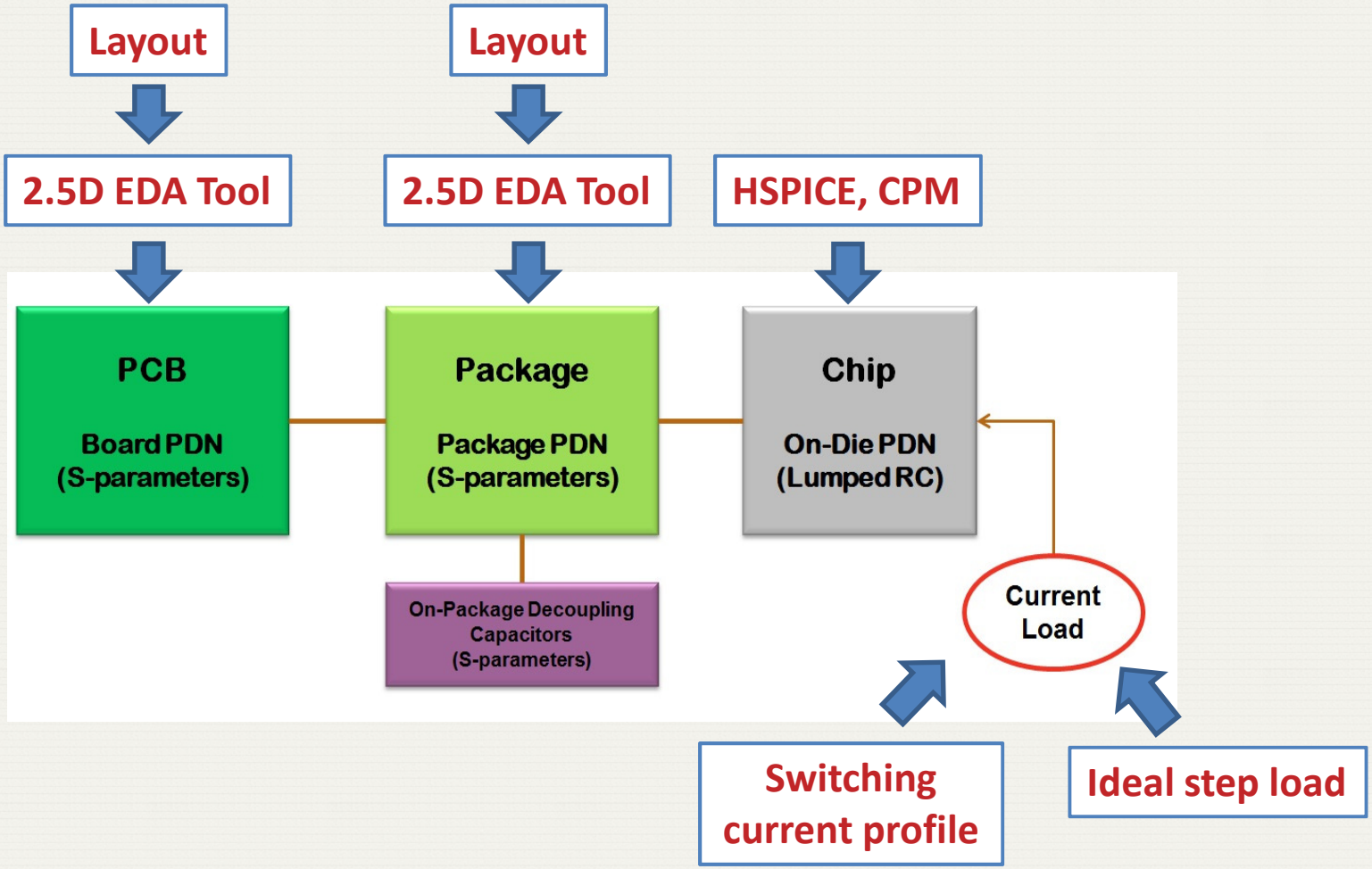


Noise

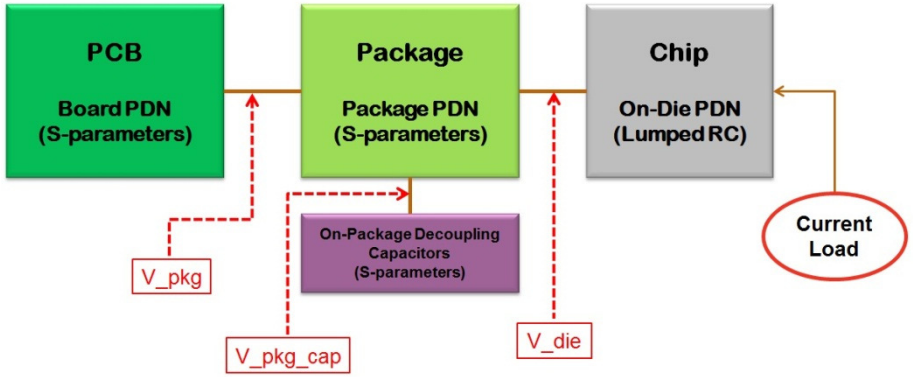
CLK

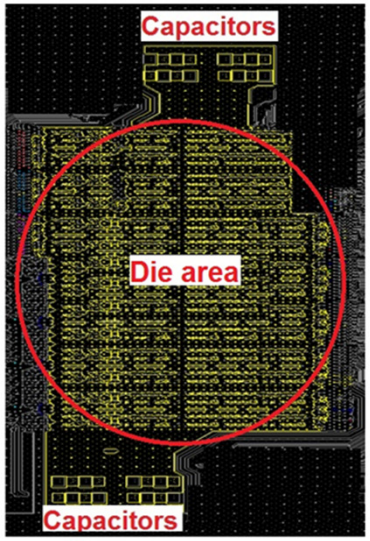


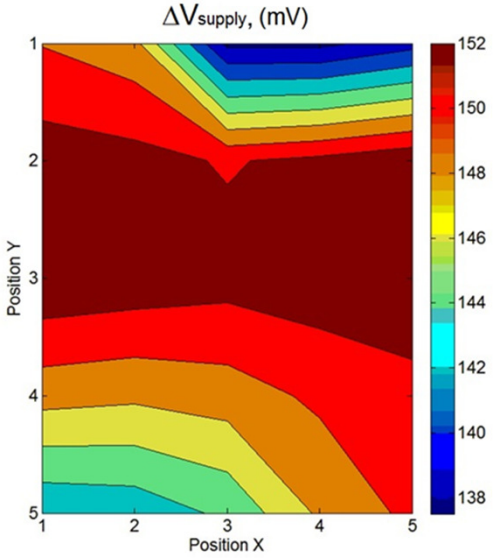
PDN Model

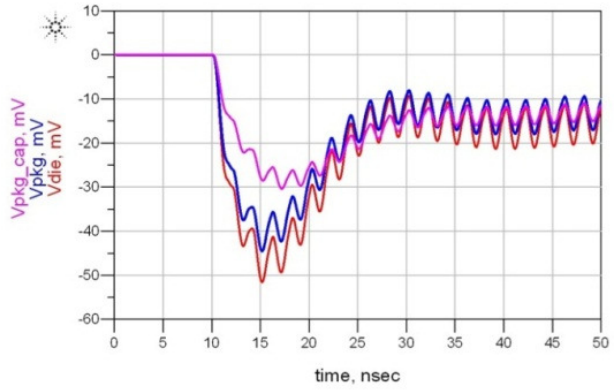

Layout
Layout
2.5D EDA Tool
2.5D EDA Tool
HSPICE, CPM
PCB
Board PDN
(S-parameters)
Package
Package PDN
(S-parameters)
Chip
On-Die PDN
(Lumped RC)
On-Package Decoupling
Capacitors
(S-parameters)
Current
Load
Switching
current profile
Ideal step load

Location, Location, Location

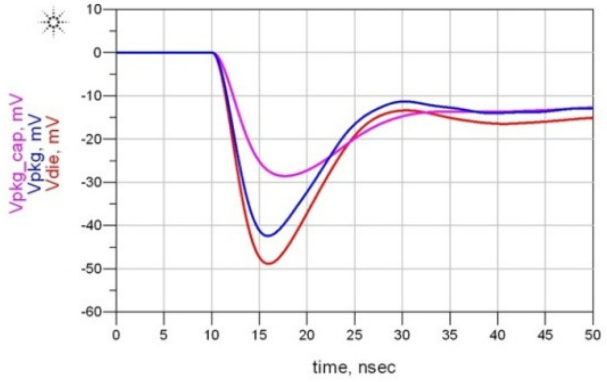






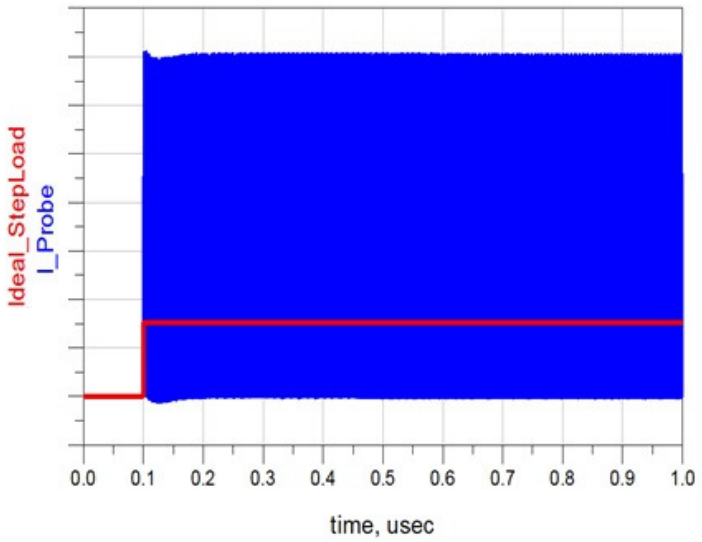


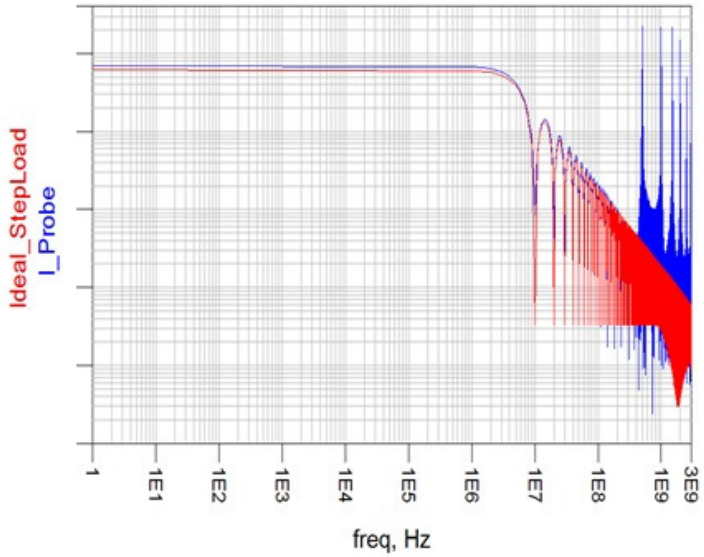
(a)

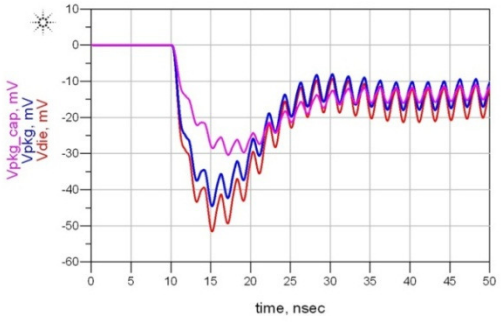


(b)

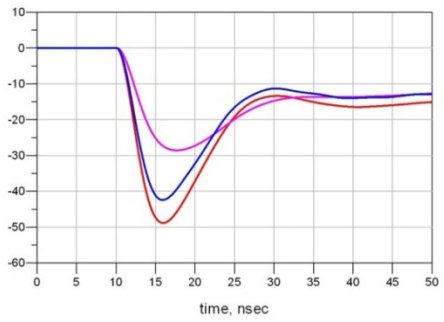
Ideal Step Load vs. Realistic One







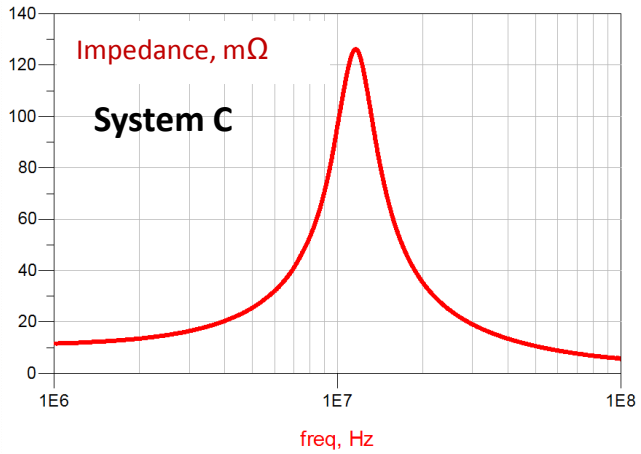
(a)

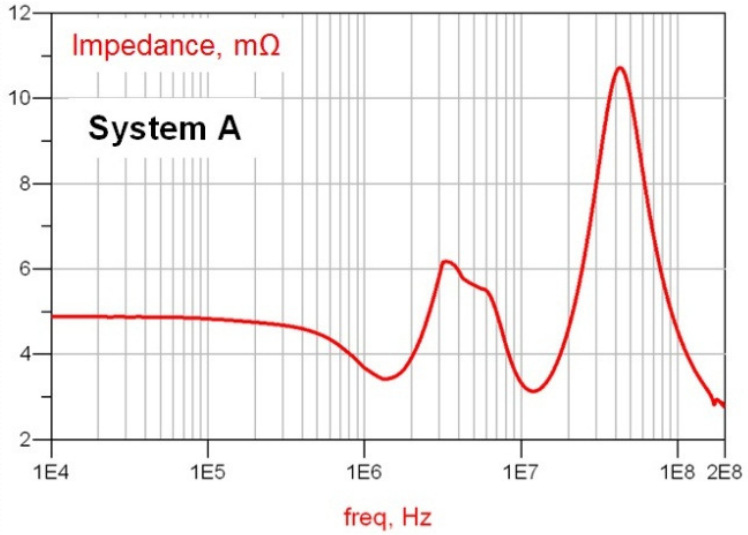


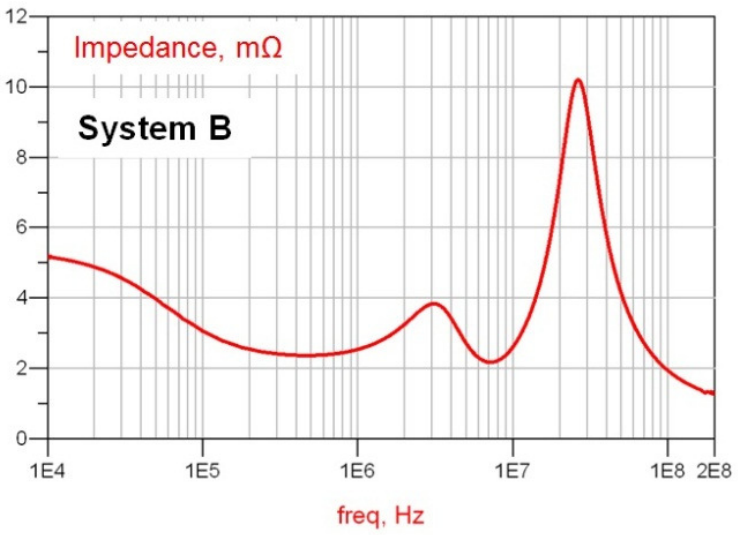
(b)

Simulated Impedance Profiles

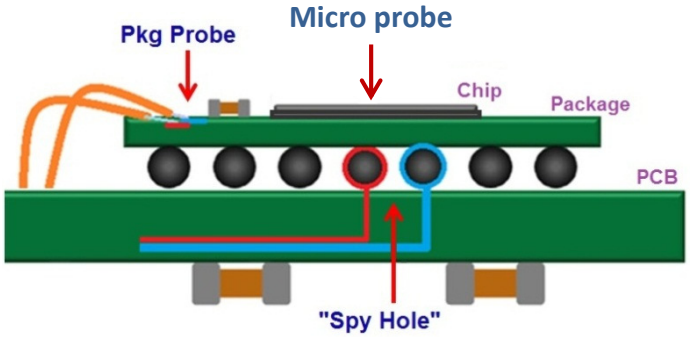
- **System A** – SoC, medium-sized, flip-chip
- **System B** – Large monolithic FPGA, flip-chip
- **System C** – Smaller FPGA, wire-bond

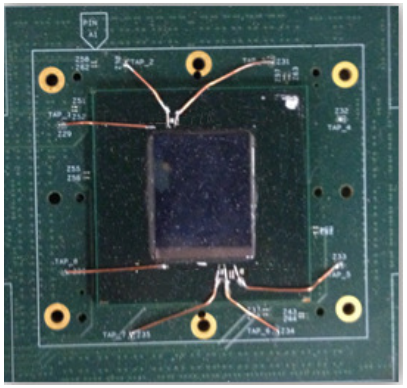


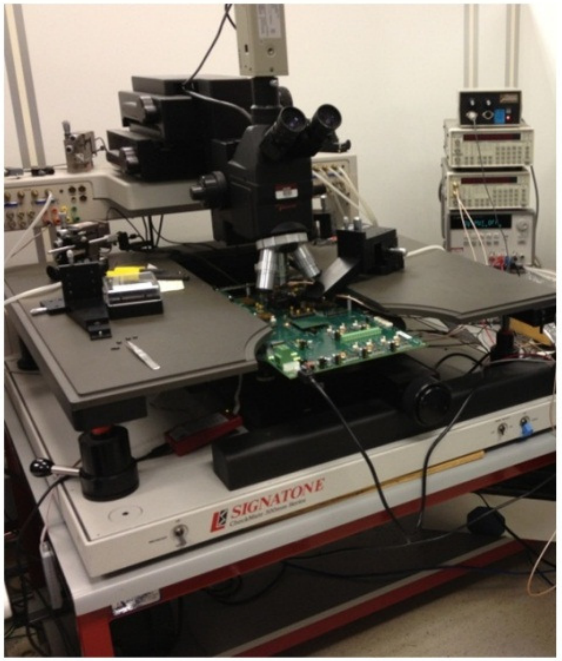


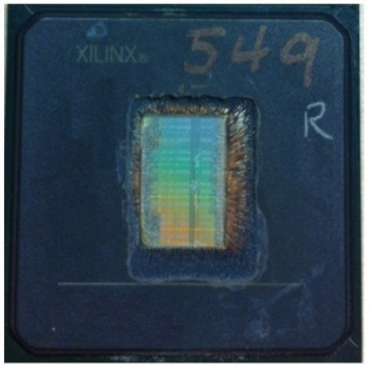


Measurements. Probing solutions

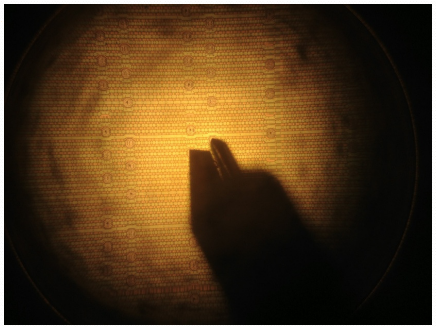


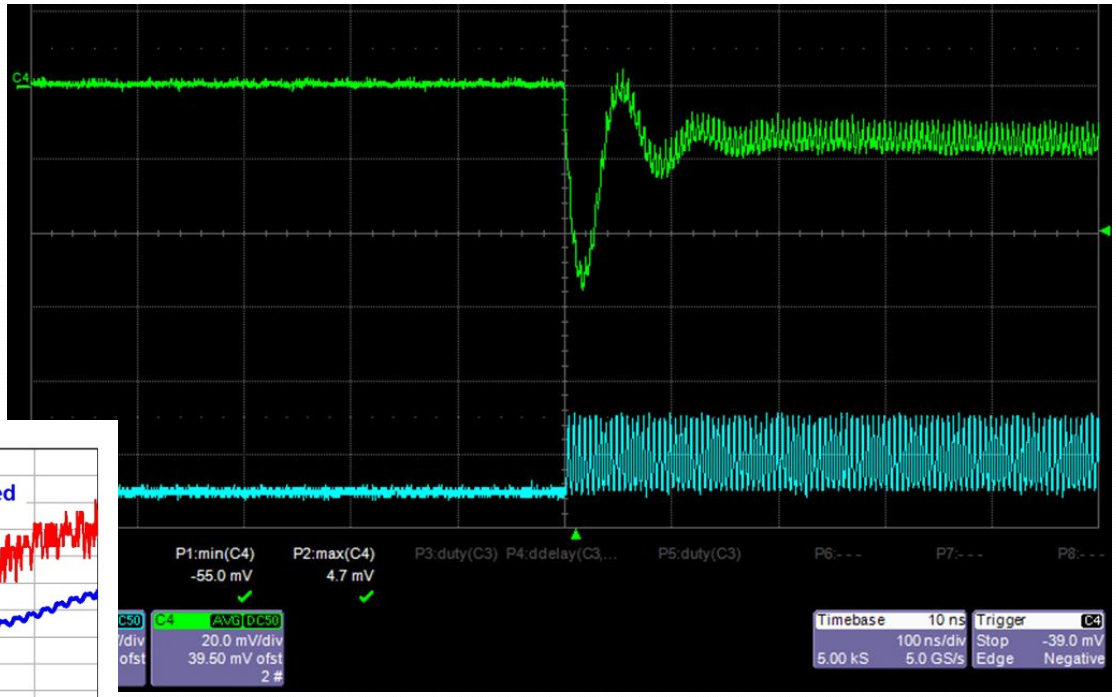


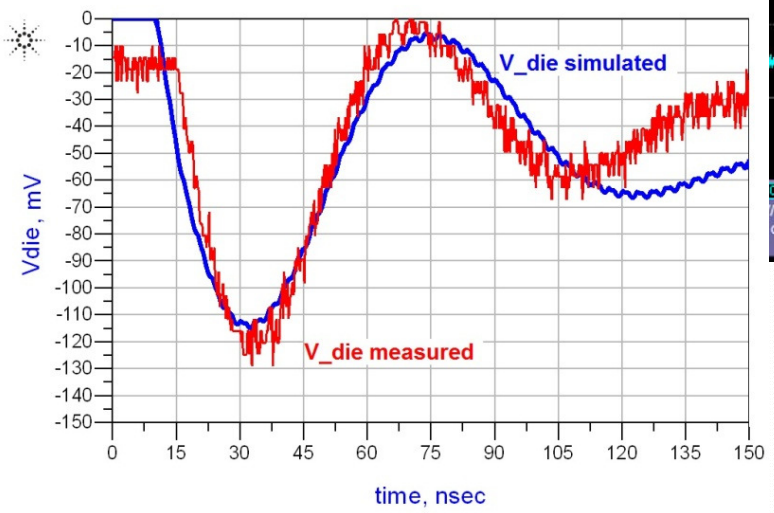




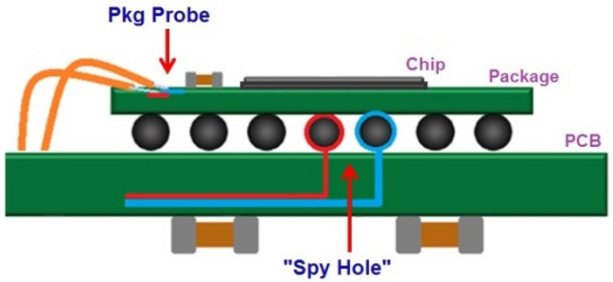
Transient Step Response. System C

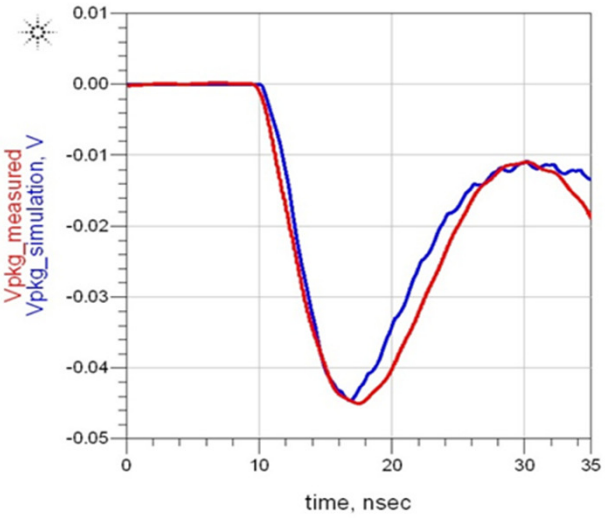


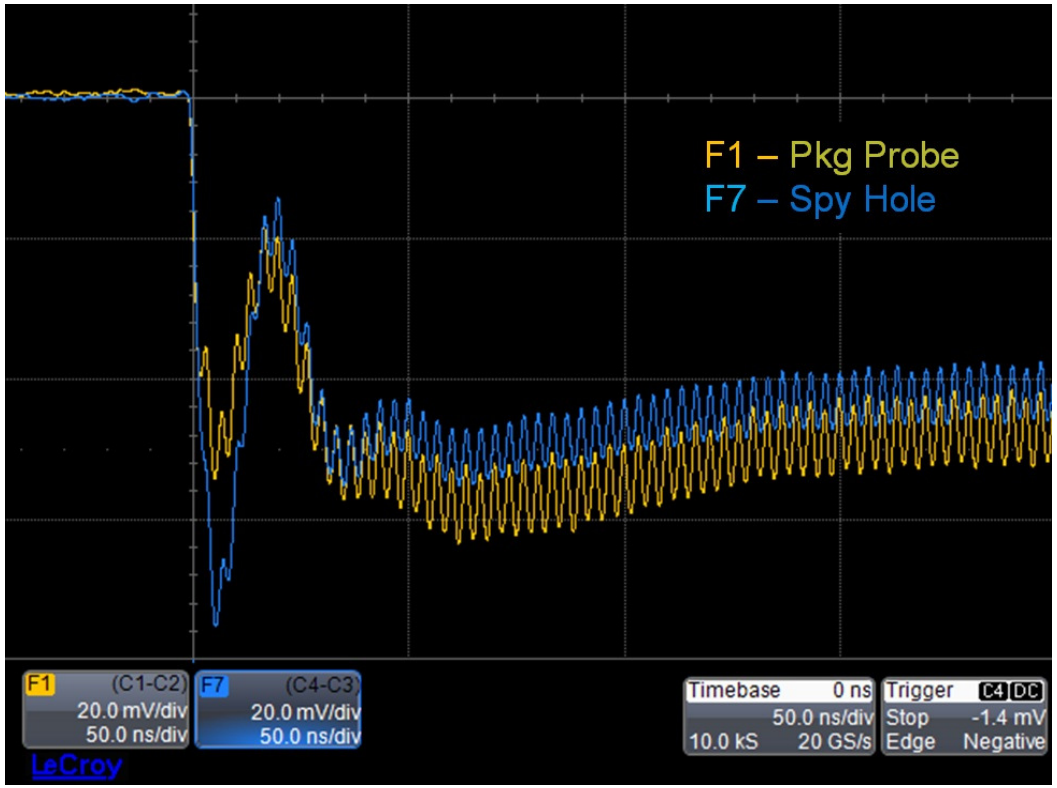




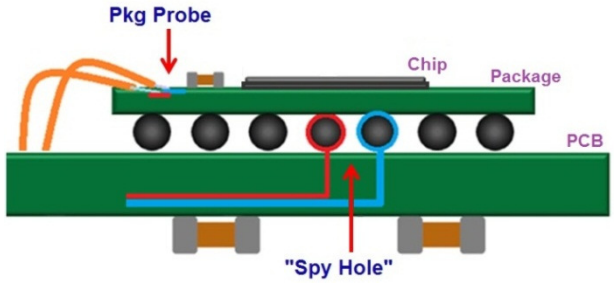
Step Response. System A

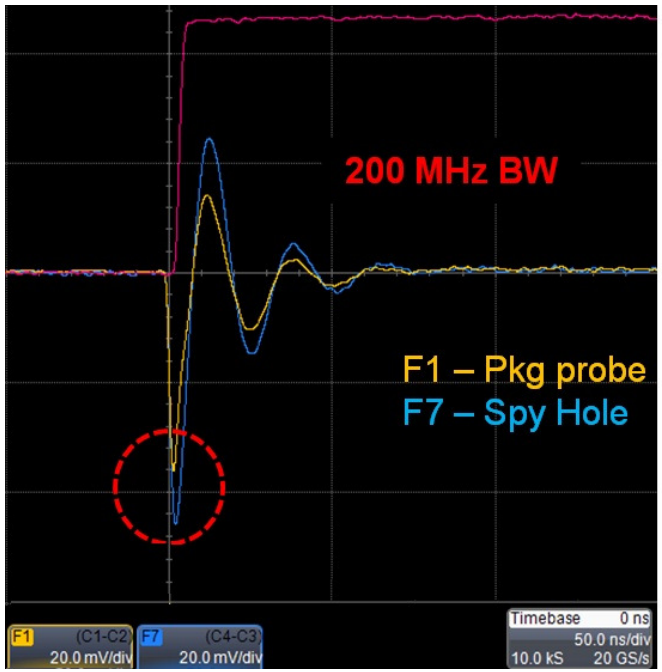


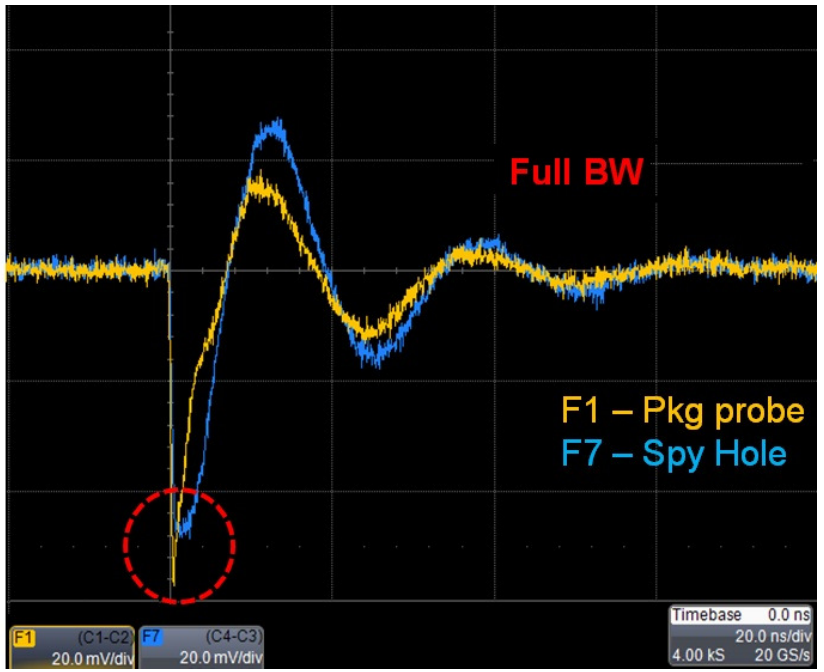




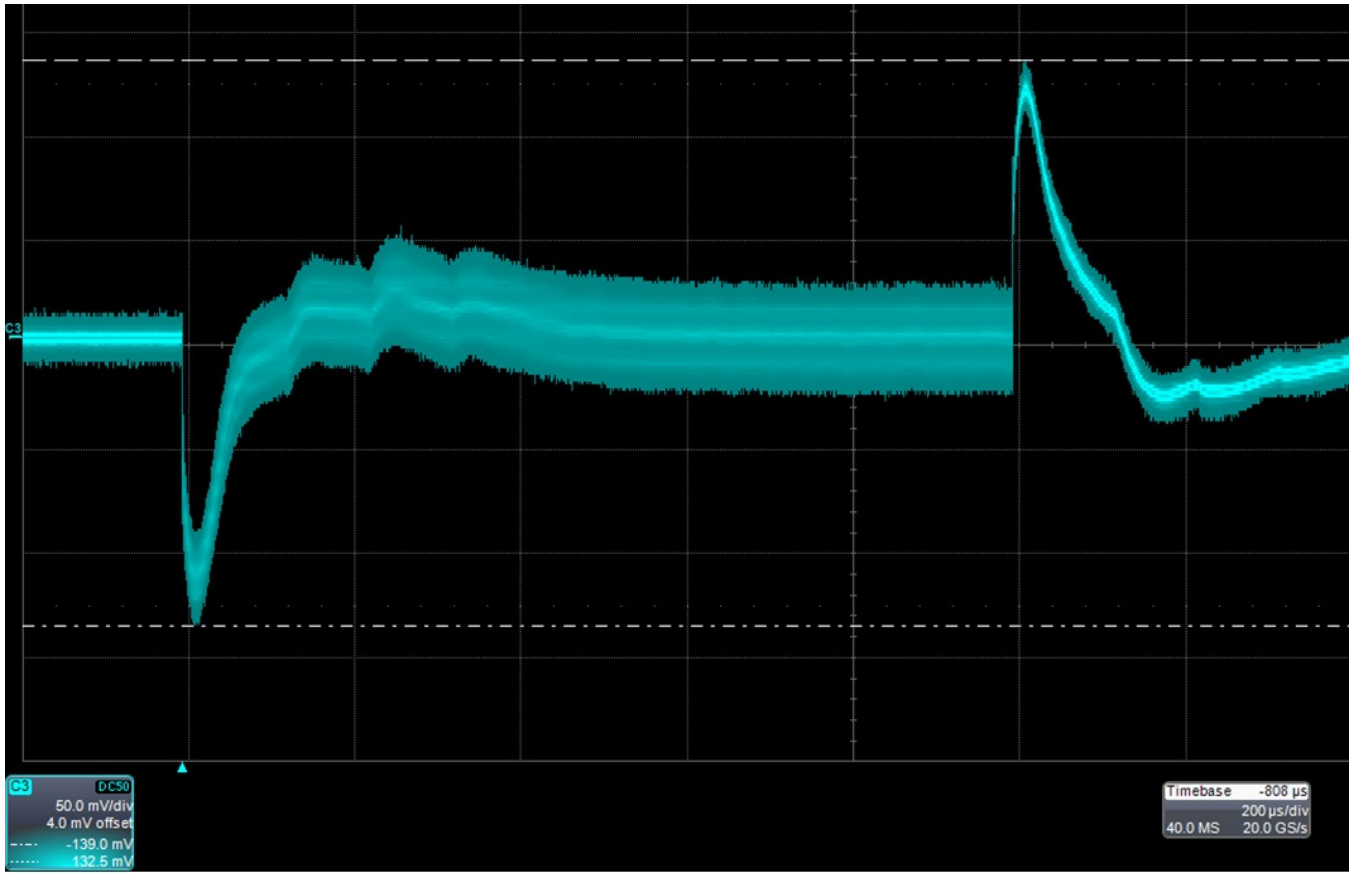
Impulse Response. System A







Full Cycle. System A



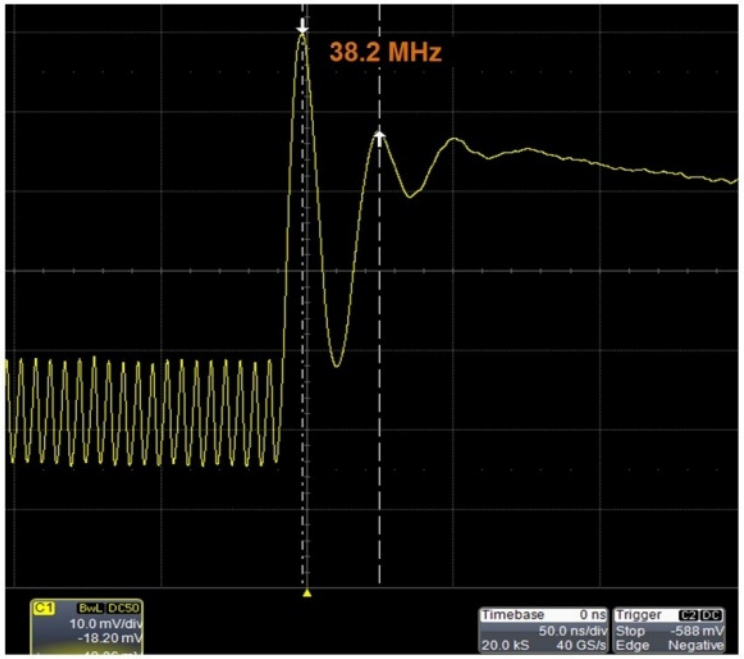
Impedance Measurement

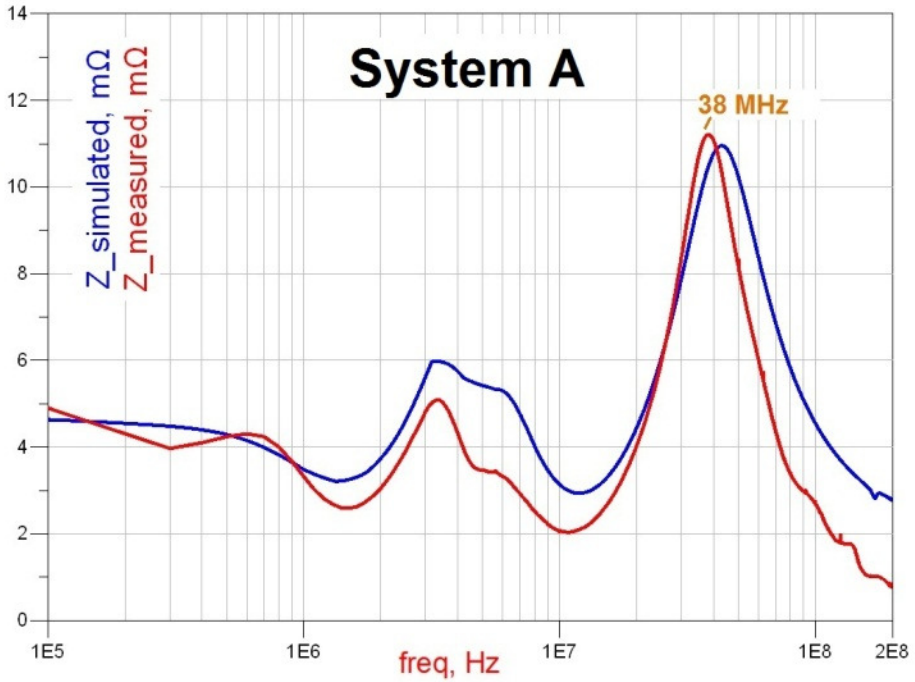
- If we create a known excitation *i(t,f)* and measure the response *v(t,f)* → can derive *Z(f)*

- **Time-domain measurements**
  - Only characteristic frequencies (resonances)
  - Impedance magnitude at resonance frequencies
- **Frequency-domain characterization**
  - Complete impedance profile of the system

Correlation. System A

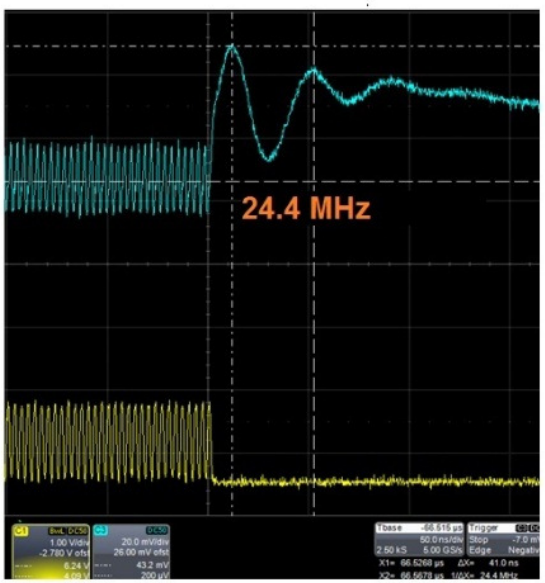
- **System A** has a suboptimal board-level decoupling solution

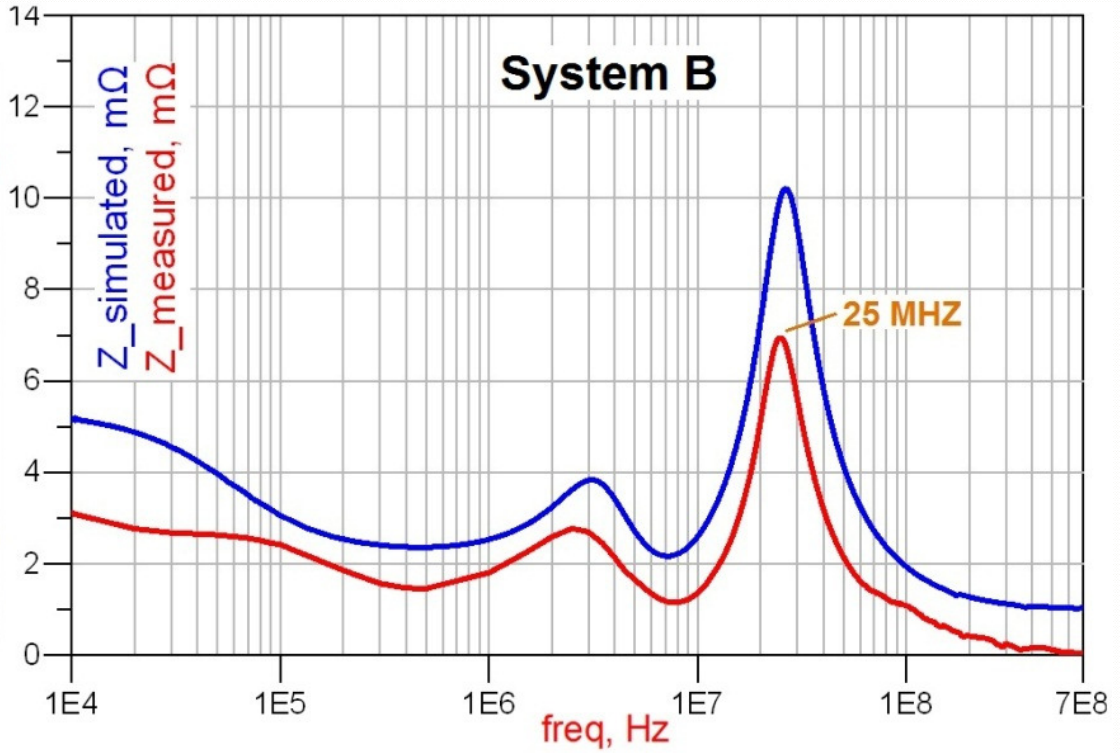




Correlation. System B

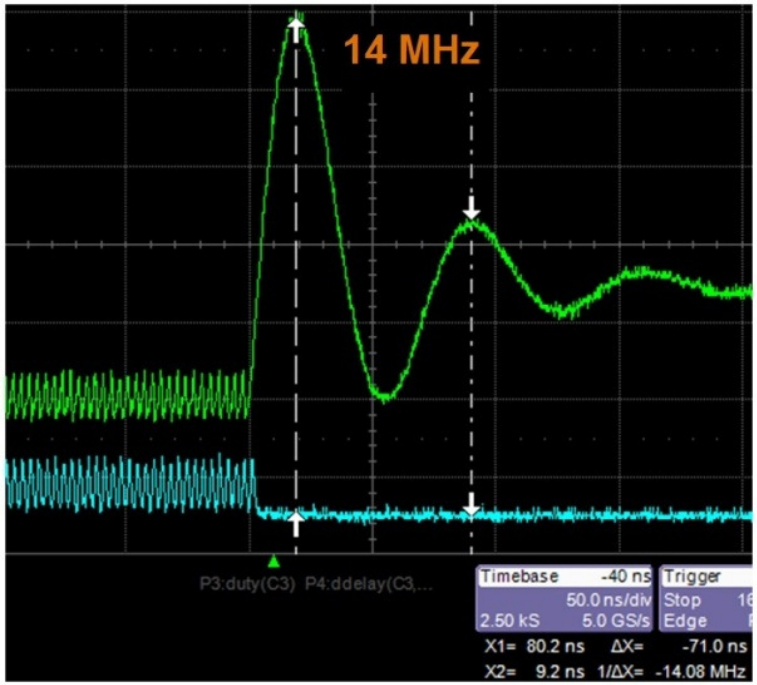
- **System B** has a larger die than System A → die/package resonance is at a lower frequency

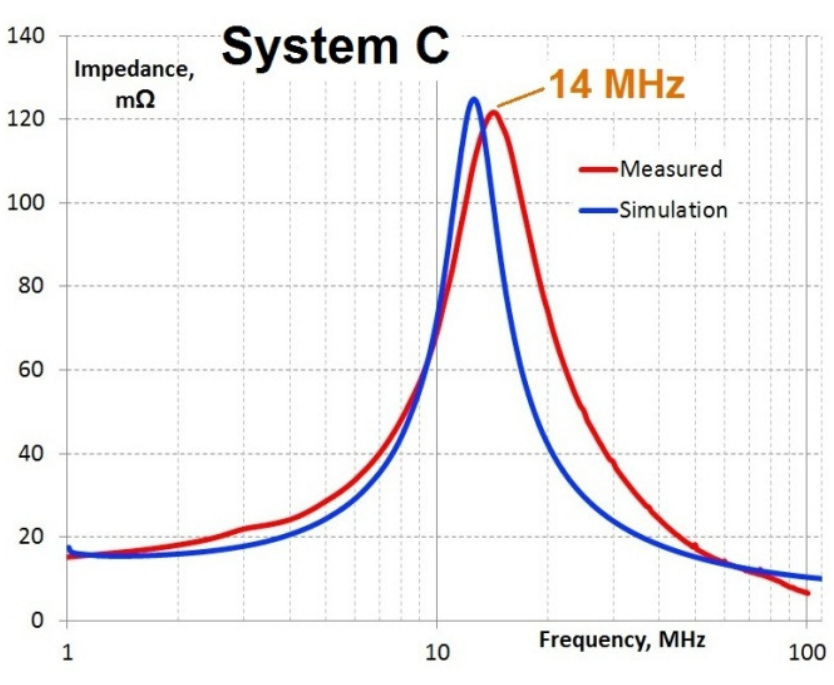




Correlation. System C

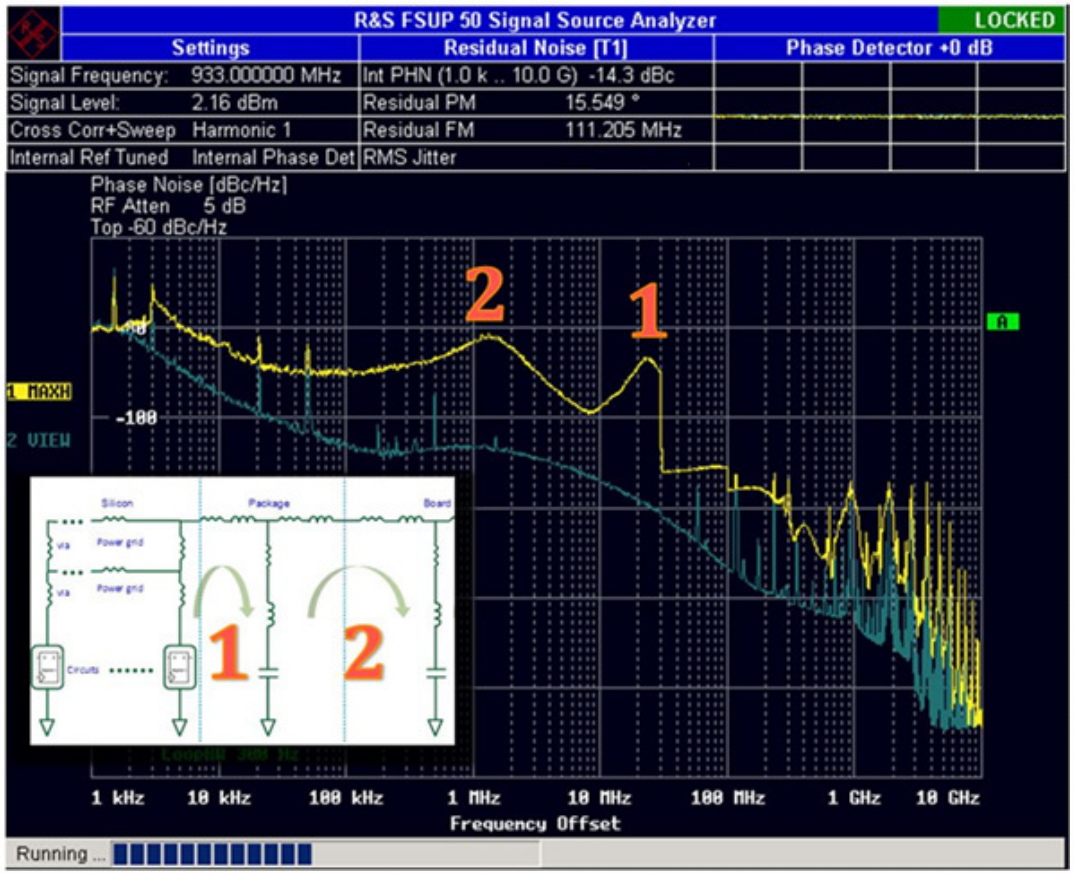
- **System C** has no on-package decoupling capacitors → single resonance peak
- **System C** has a wire-bond package → high value of PDN impedance





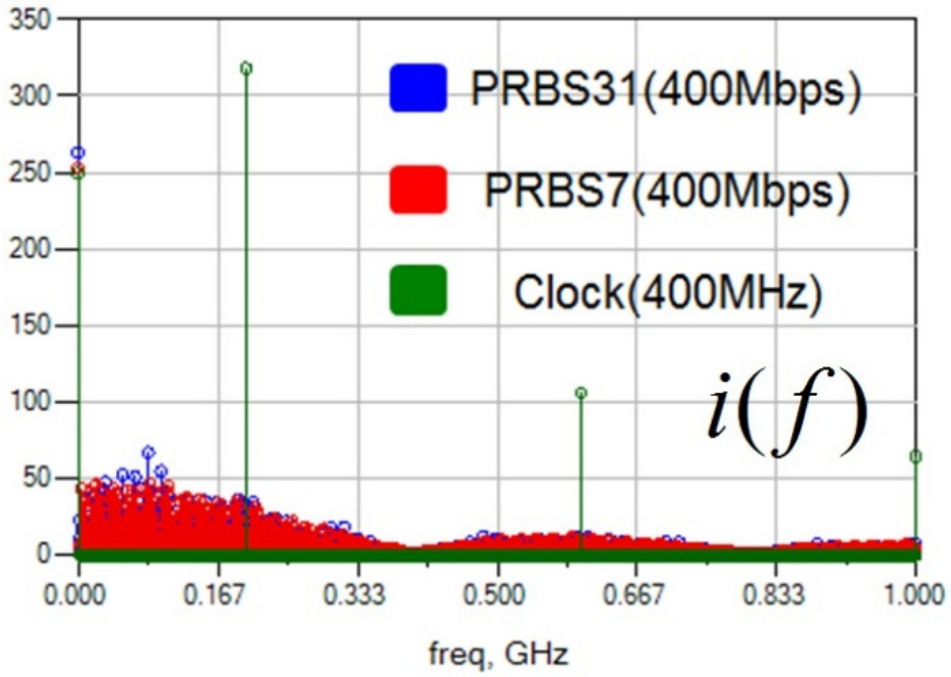
Supply Noise Impact on System Timing

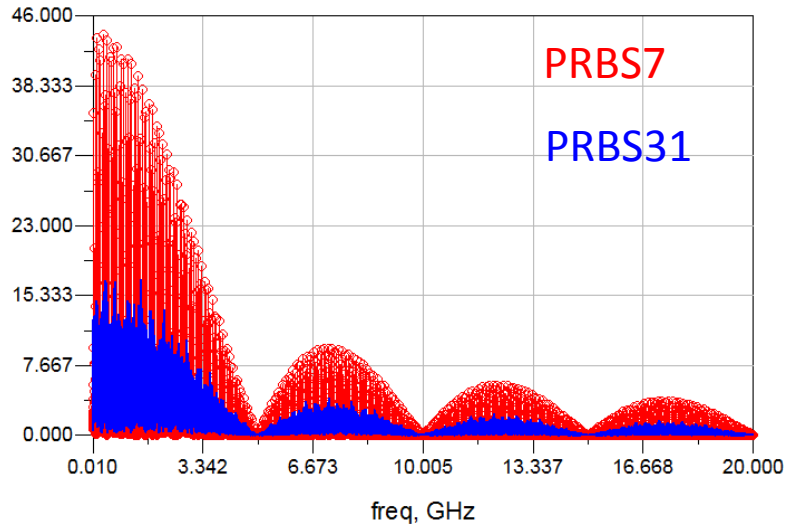
- Can be characterized as **phase noise** in frequency domain and translated into **jitter** in time domain



Excitation Options

- What is the “best” way to create noise?

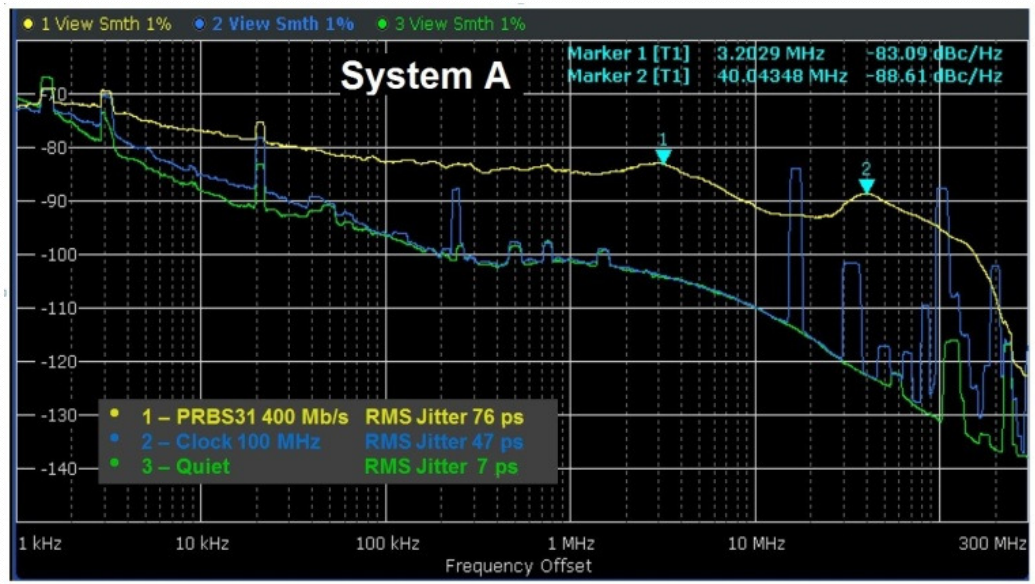


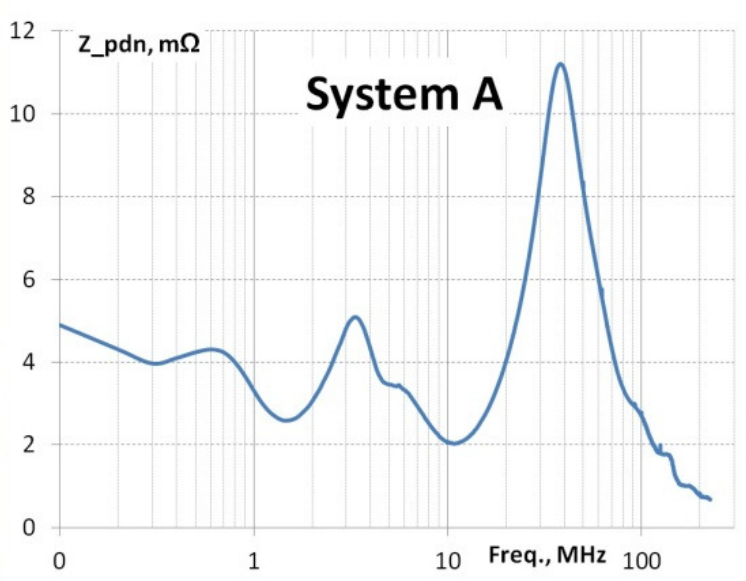


$$\left(\int i(f) \bullet z(f) df\right) \times JitterSensitivity \Rightarrow jitter$$

Correlation. System A

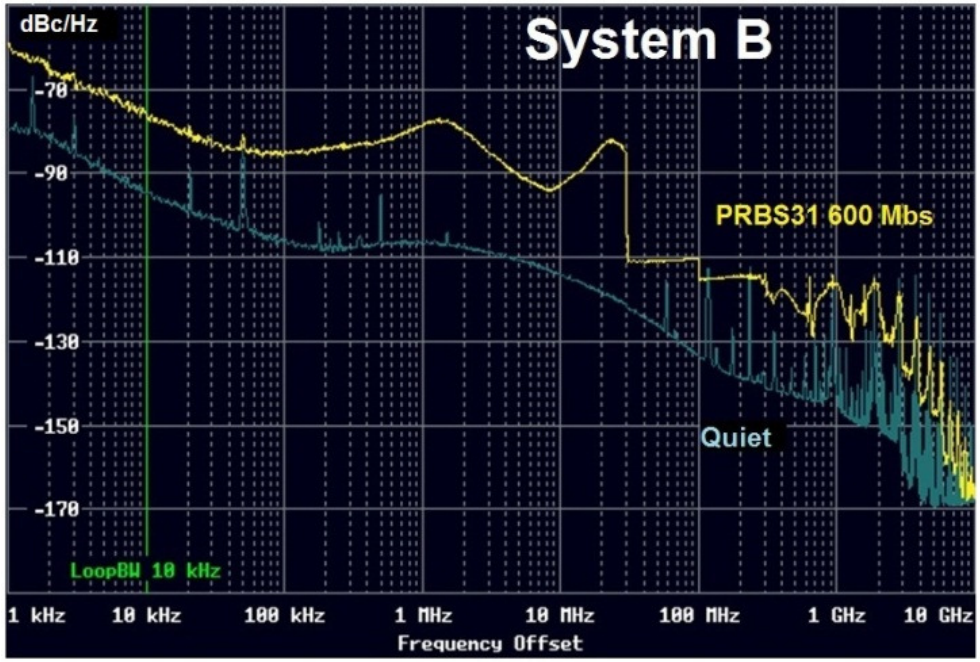
- Impedance profile shapes the phase noise curve

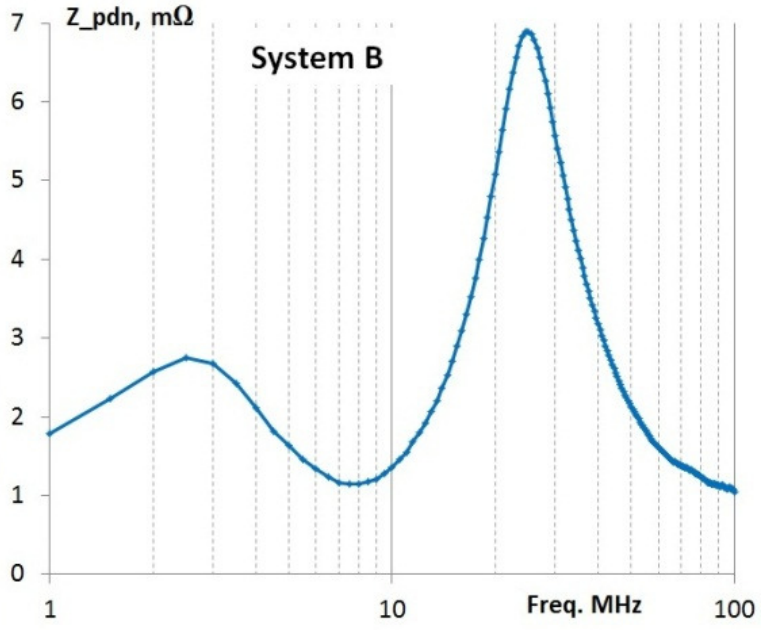




$$\left(\int i(f) \bullet z(f) df\right) \times JitterSensitivity \Rightarrow jitter$$

Correlation. System B





$$\left(\int i(f) \bullet z(f) df\right) \times JitterSensitivity \Rightarrow jitter$$

Summary and Conclusions

- System-level approach to power integrity
- Time domain and frequency domain characteristics, metrics and specs
- Time domain and frequency domain cross-correlation
- Leveraging FPGA flexibility to create test setups with well-controlled conditions
- Complete impedance profile of system-level PDN
- PDN impact on system timing. Phase noise and jitter