

DESIGNCON[®] 2014

De-Mystifying the 28 Gb/s PCB Channel: Design to Measurement

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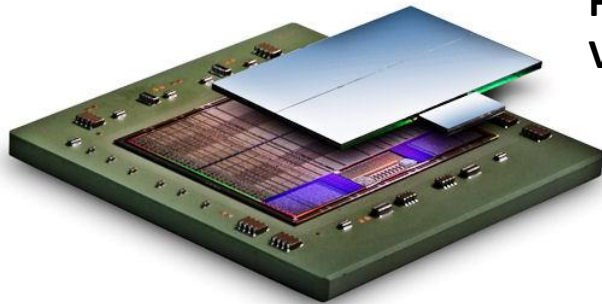
January 28-31, 2014 | Santa Clara Convention Center | Santa Clara, CA



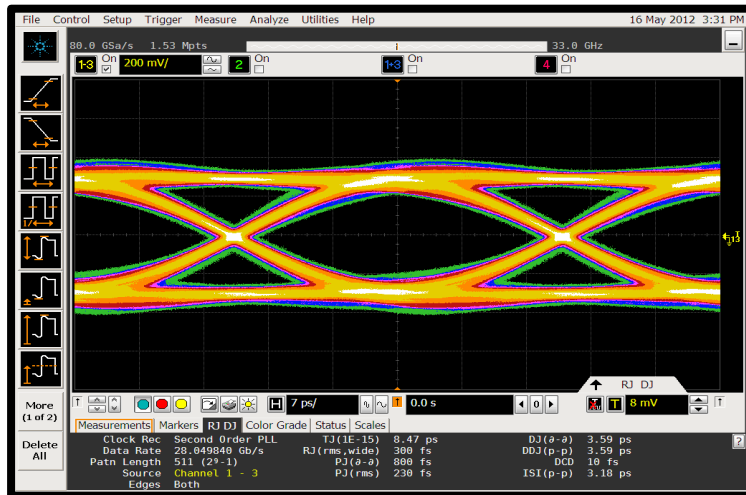
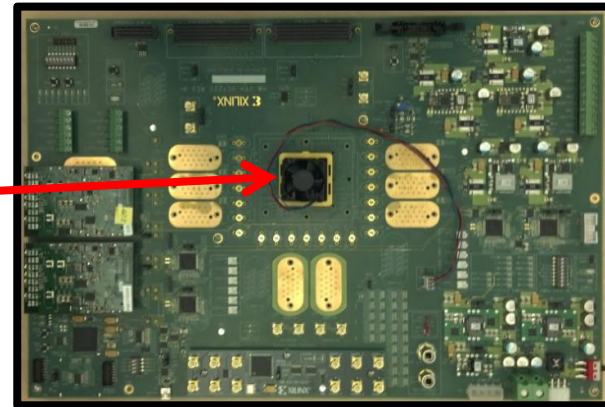
Outline

- **28 Gb/s SERDES Channel Overview**
- **Design Analysis for Band Limited Fixture Removal**
- **Fixture Removal Methods**
- **28 Gb/s SERDES Measurements at the DUT**

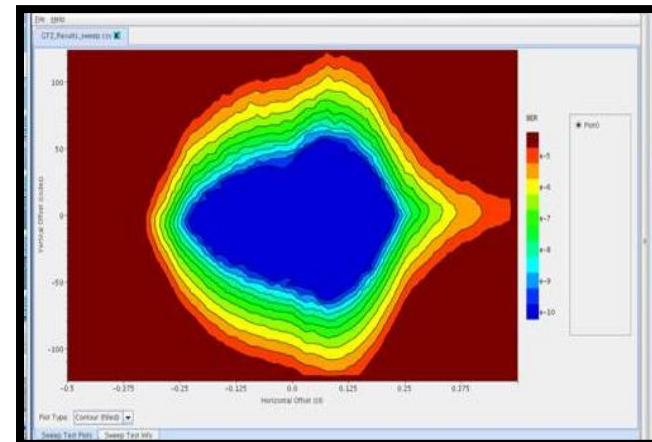
28nm FPGA with GTZ XCVR 7H580T



Heterogeneous
VH580T

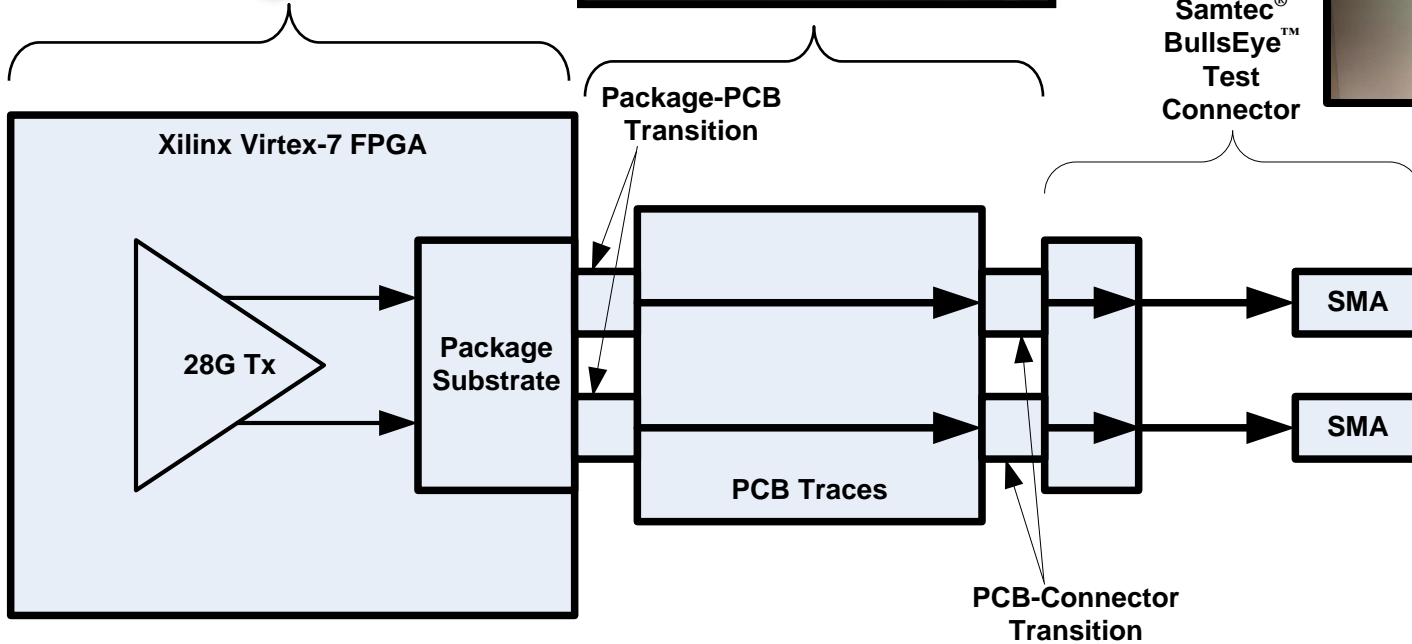
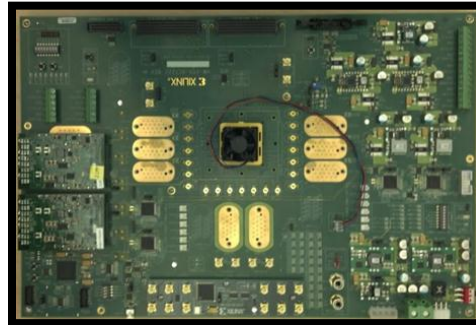
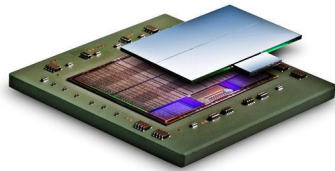


VH580T GTZ TX
Eye Diagram: 28.05Gb/s



VH580T GTZ
RX Eye Scan: 28.05Gb/s
Through a 12.5 dB Lossy Trace

28 Gb/s Channel



Physical Description PCB Stackup

PCB Stackup

- 22 Layers
- HS signal layers: Panasonic Megtron6
- Other layers: ISOLA 370HR - FR4
- For Megtron6 and 370HR interleaved in lower layers for mechanical stability

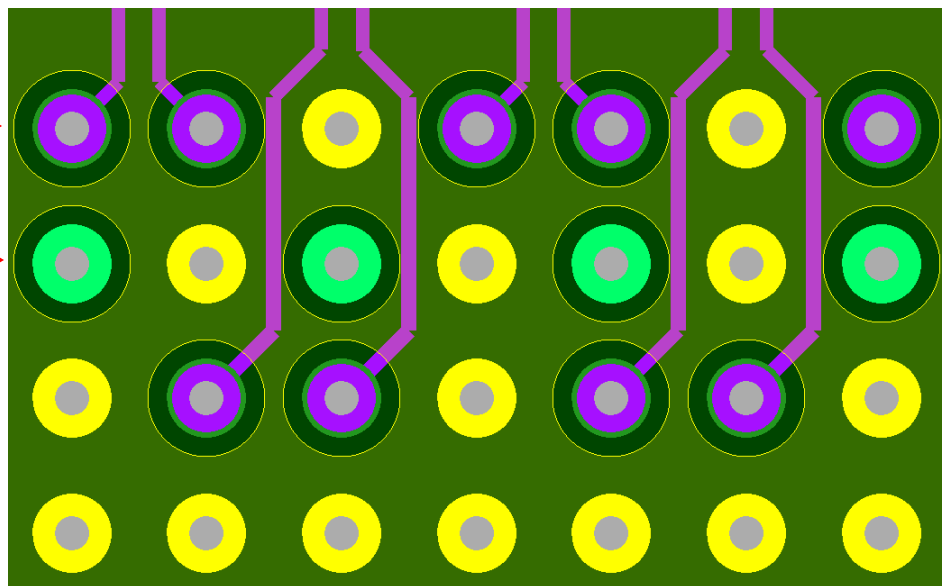
Note: For economic reasons other layers are standard FR4 (ISOLA 370HR)

Layer	Type	CU Weight	CU %	Material Description	Via Structure	Segment
Soldermask						
1	Signal	H	20	Press thk = 4.56 mil		Foil
2	Plane	H	94	3.9 mil H/H		Core
3	Signal	H	20	Press thk = 5.38 mil		Prepreg
4	Plane	H	94	3.9 mil H/H		Core
5	Signal	H	5	Press thk = 5.29 mil		Prepreg
6	Plane	H	94	3.9 mil H/H		Core
7	Signal	H	5	Press thk = 5.29 mil		Prepreg
8	Plane	H	94	3.9 mil H/H		Core
9	Mixed	H	9	Press thk = 5.32 mil		Prepreg
10	Plane	H	94	3.0 mil H/H		Core
11	Plane	H	91	Press thk = 5.31 mil		Prepreg
12	Plane	H	94	3.0 mil H/H		Core
13	Plane	H	89	Press thk = 5.78 mil		Prepreg
14	Plane	H	91	3.0 mil H/H		Core
15	Plane	H	94	Press thk = 5.50 mil		Prepreg
16	Mixed	H	39	4.0 mil H/H		Core
17	Plane	H	94	Press thk = 5.28 mil		Prepreg
18	Signal	H	3	4.0 mil H/H		Core
19	Plane	H	94	Press thk = 5.28 mil		Prepreg
20	Signal	H	3	4.0 mil H/H		Core
21	Plane	H	94	Press thk = 4.56 mil		Prepreg
22	Signal	H	21			Foil
Soldermask						

Physical Description Pin/Via Breakout

BGA Pin Via Field

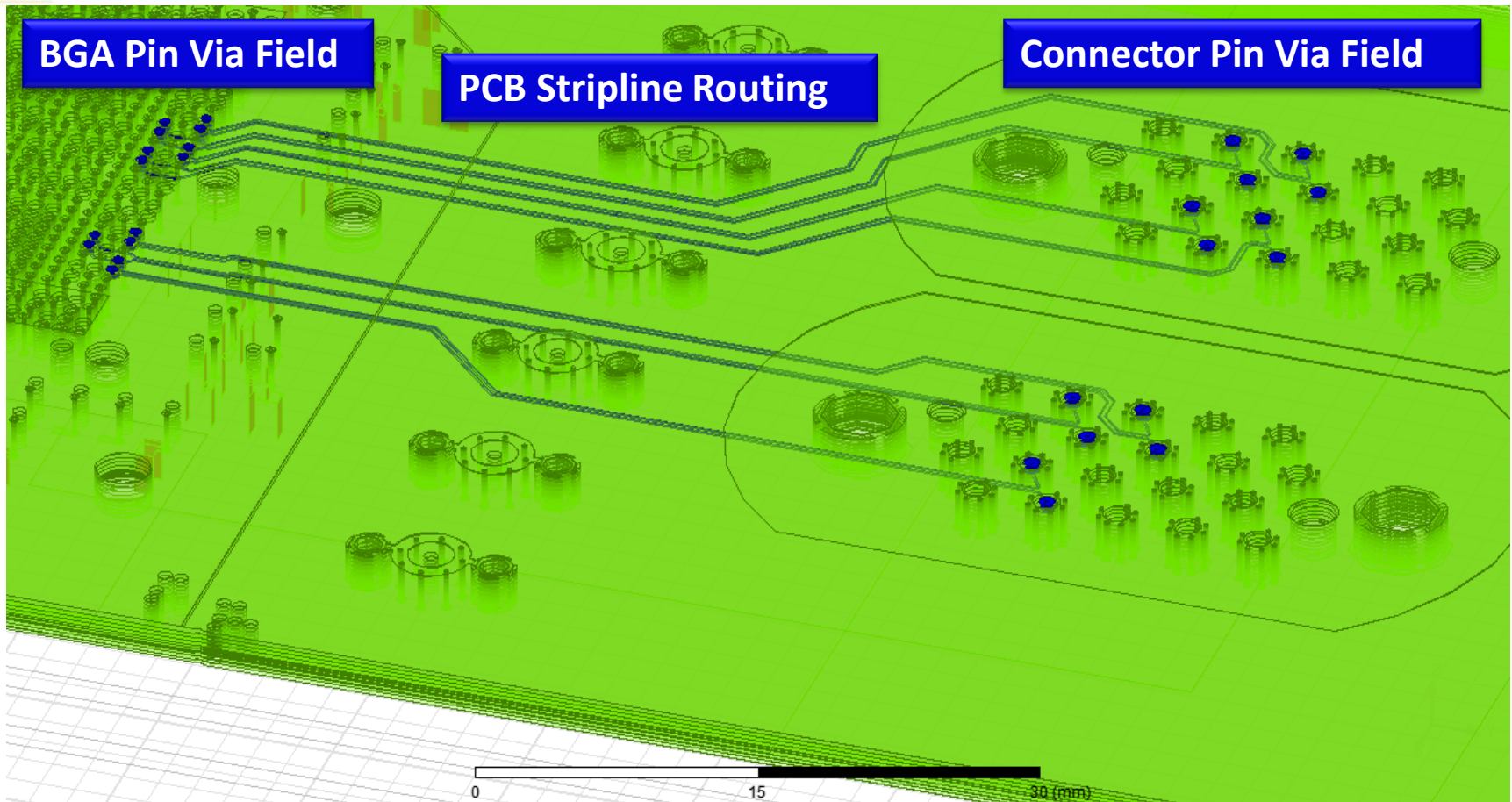
- High-speed Signal Via (Backdrilled) →
- Standard Signal Via (Not Backdrilled) →
- Ground Via (Not Backdrilled) →



Via Topology

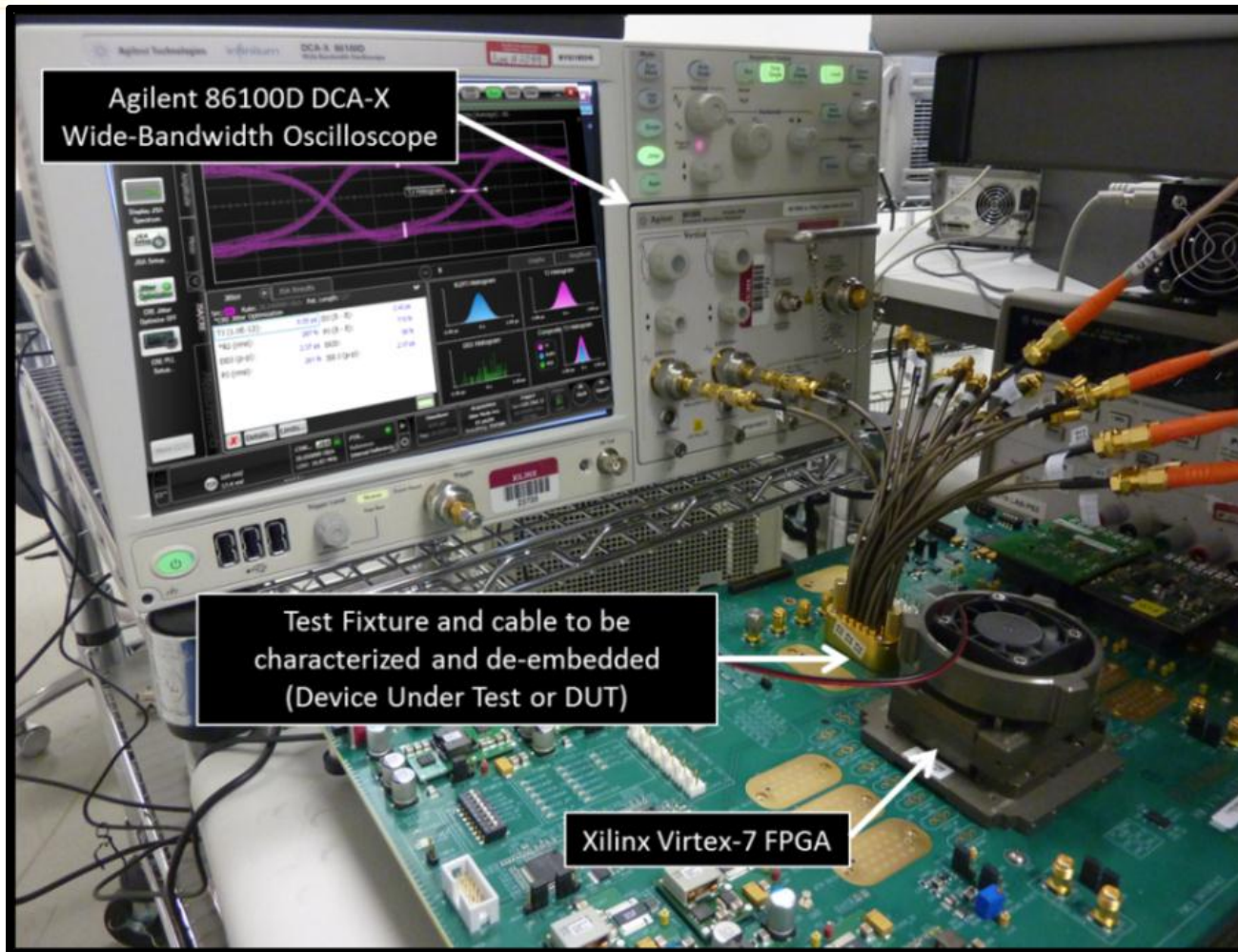
- 10 mil Drill
- 20 mil pad
- 28 mil anti-pad
- Backdrill – 8 mils from target layer +/- 3mils

Physical Description - PCB Layout



Differential Pair Routing: 3.5 mil Traces with 10 mil gap

28 Gb/s Tx Measurement Challenge

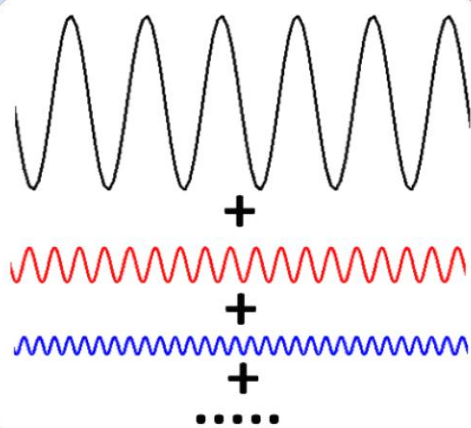


Measurement Fixture

Coaxial Adapters
Cable Assembly
PCB Routing
BGA Via Field

Band-Limited S-Parameters for De-Embedding

Frequency to Time Domain
Inverse Fourier Transform

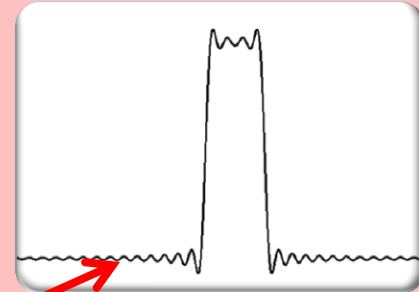


Summation of Sine Waves

Case 1
Infinite Sum of Sine Waves



Case 2
Finite Sum of Sine Waves



Non-Causal Ripple - Gibbs Phenomena

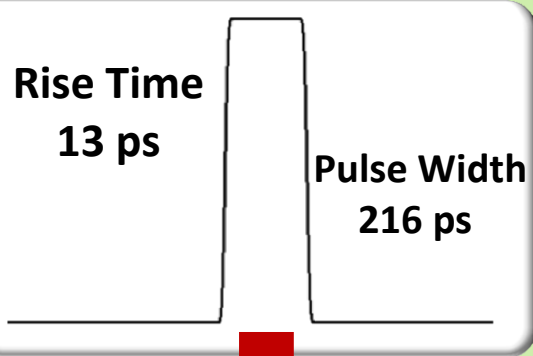
28 Gb/s Tx	Bandwidth Rule-of-Thumb
Rise Time 13 ps 3 dB B.W.	17 GHz
Rise Time 5 ps 3 dB B.W.	44 GHz
3 rd Harmonic	42 GHz
5 th Harmonic	70 GHz

Error Due to Gibbs Phenomena

Time Domain Simulated Pulse

Rise Time
13 ps

Pulse Width
216 ps



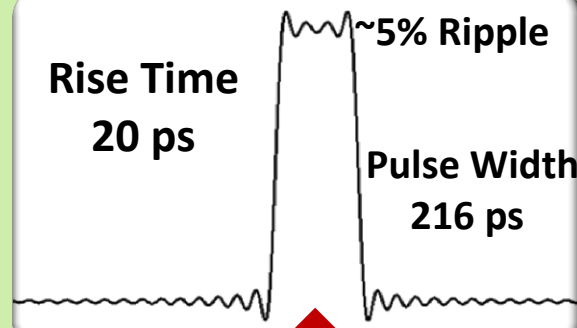
1

Time Domain i-FFT of Bandlimited Frequency Domain Data

Rise Time
20 ps

Pulse Width
216 ps

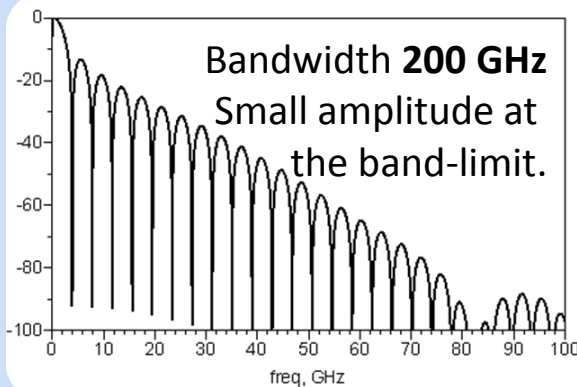
~5% Ripple



3

Frequency Domain (FFT of Pulse)

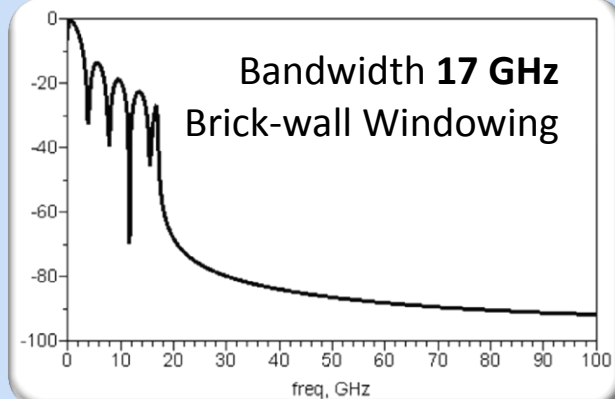
Bandwidth 200 GHz
Small amplitude at
the band-limit.



2

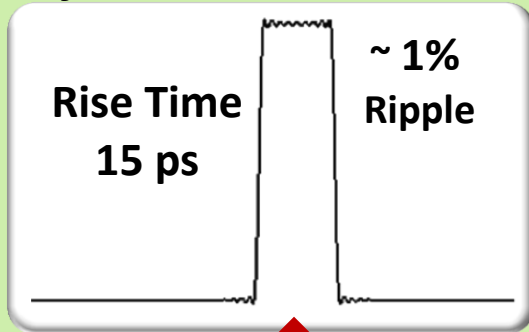
Frequency Domain (FFT of Pulse)

Bandwidth 17 GHz
Brick-wall Windowing



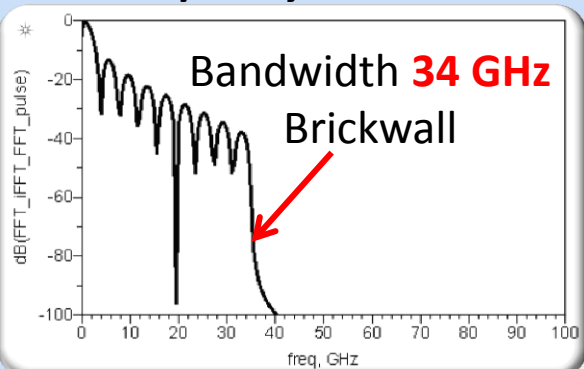
Required Channel Bandwidth

Time Domain
i-FFT of **34 GHz** Bandlimited Data

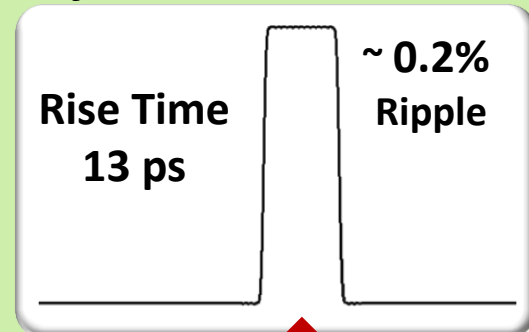


↑
Inverse-FFT

Frequency Domain

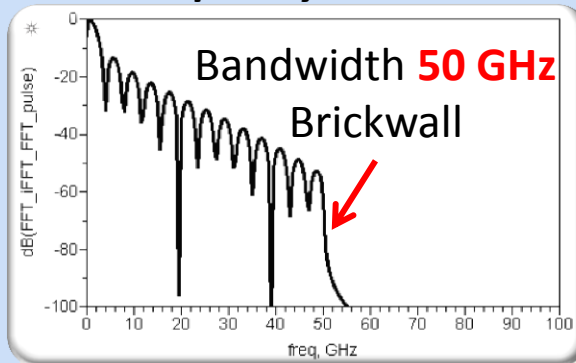


Time Domain
i-FFT of **50 GHz** Bandlimited Data



↑
Inverse-FFT

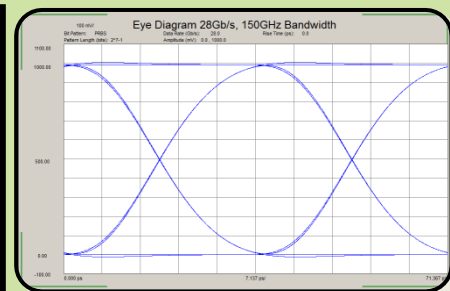
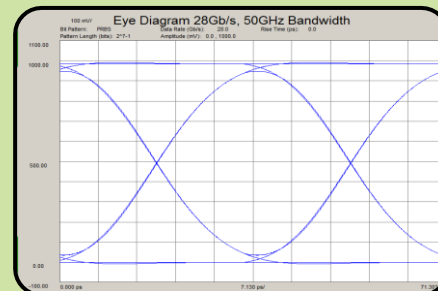
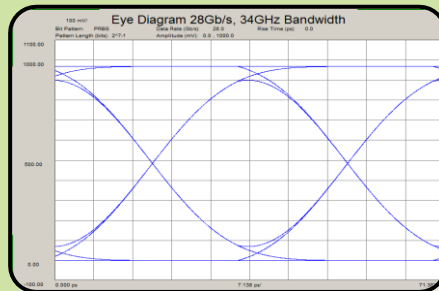
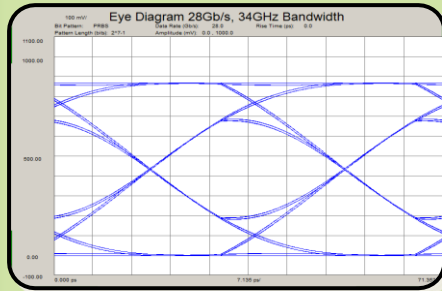
Frequency Domain



Eye Diagrams with Band-Limited S-Parameters

28 Gb/s , PRBS 7 Eye Diagrams

Inverse Fourier Transform with 4th Order Bessel Windowing

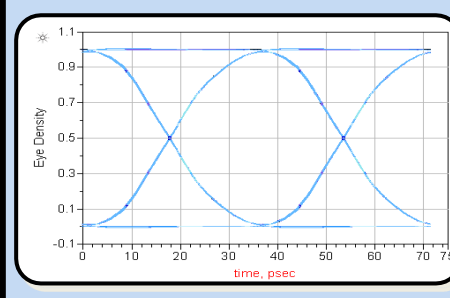
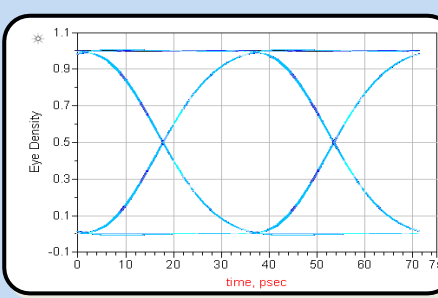
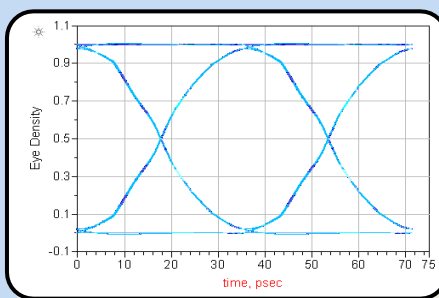
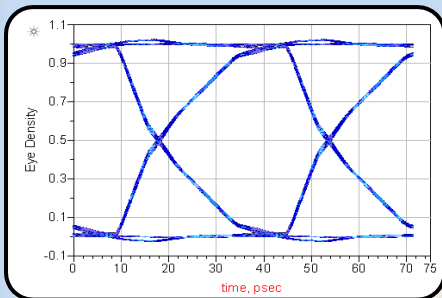


**Bandlimited
17 GHz
S-Parameters**

**Bandlimited
34 GHz
S-Parameters**

**Bandlimited
50 GHz
S-Parameters**

**Bandlimited
100 GHz
S-Parameters**

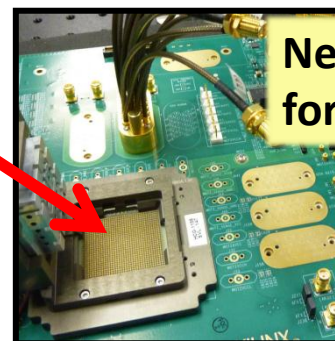
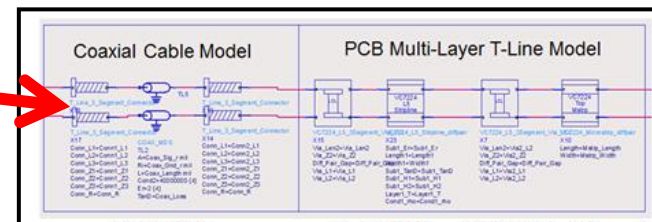
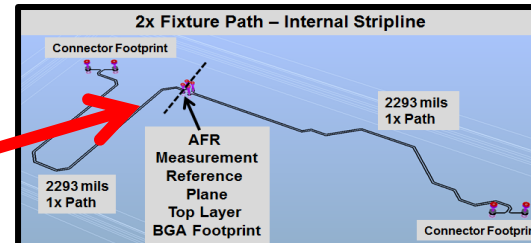
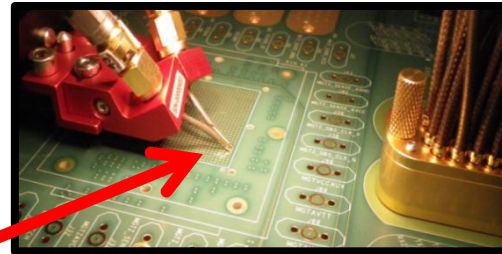


Hilbert Transform with Causality Enforcement

Fixture De-Embedding Methods

Channel Model De-Embedding Options

- 1) Direct Probe Measurement
- 2) Test Coupon Structure with AFR
- 3) Hybrid Multi-Path Simulation with Minimal Test Structures
- 4) Direct Reflect Measurement with AFR algorithm.

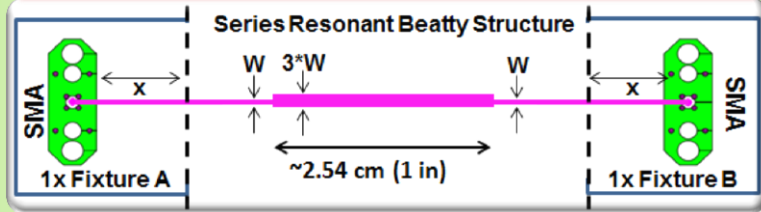


New Technique
for 2014

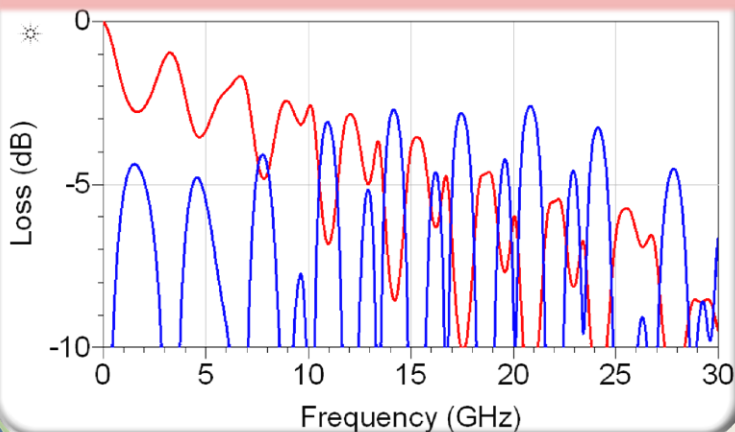
Fixture Removal Review

BEFORE

FIXTURE + Resonant Beatty Structure



S-Parameters before Fixture De-Embed

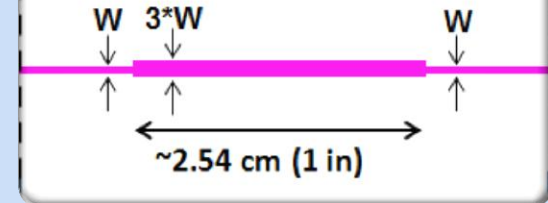


FIXTURE
DE-EMBED

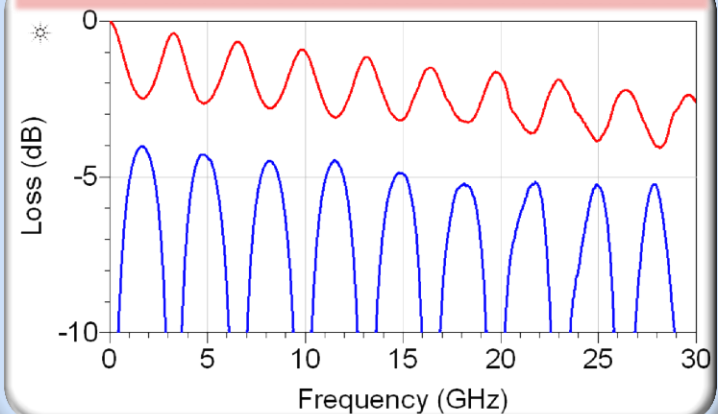
T-Matrix

AFTER

DUT with Fixture Removed Series Resonant Beatty Structure



S-Parameters after Fixture De-Embed



New 1-Port Automatic Fixture Removal

1-Port AFR

1-Port, Open at DUT
In-Situ Path Measurement

Note: Only 4 S-Parameters are used to calculate the differential .s4p fixture behavioral model.



Measure S11, S33, S13, S31
into a reflective open or short.

S ₁₁	S ₁₂	S ₁₃	S ₁₄
S ₂₁	S ₂₂	S ₂₃	S ₂₄
S ₃₁	S ₃₂	S ₃₃	S ₃₄
S ₄₁	S ₄₂	S ₄₃	S ₄₄

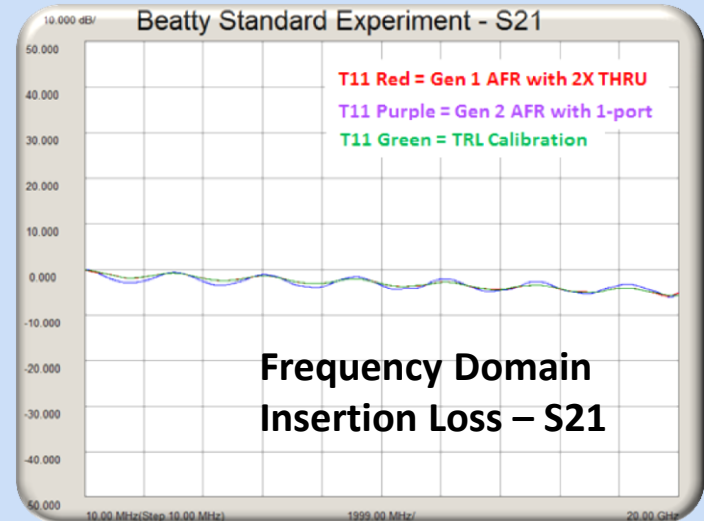
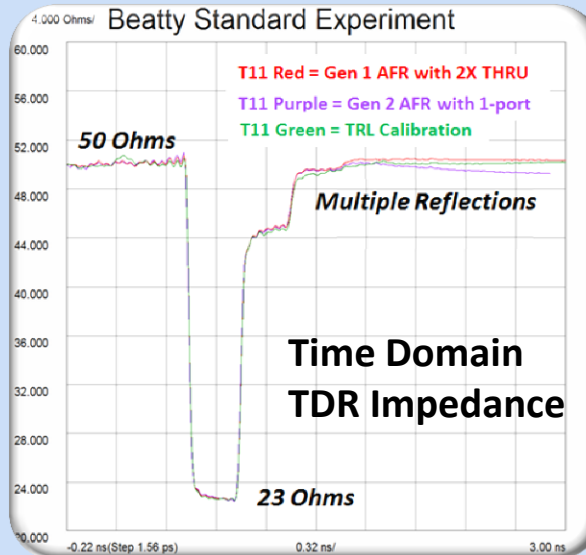
Calculate full .s4p

Compare

2x Thru AFR

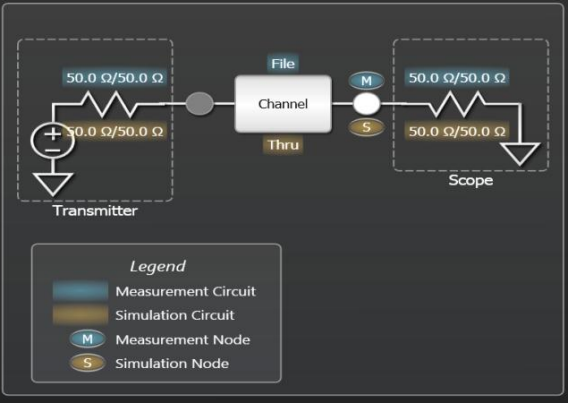
1-Port AFR

TRL Multiple Stds



Partial vs. Full De-Embedding

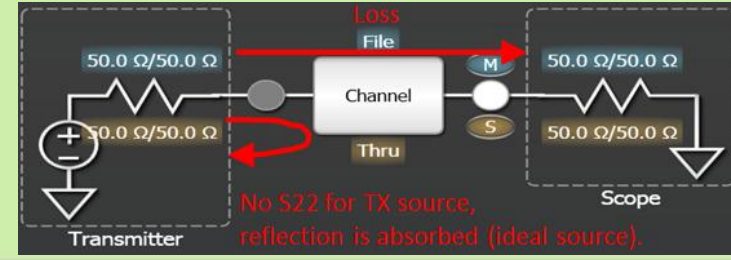
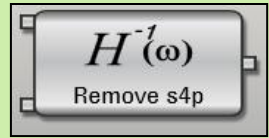
Preset Configuration: Remove insertion loss of a fixture or cable



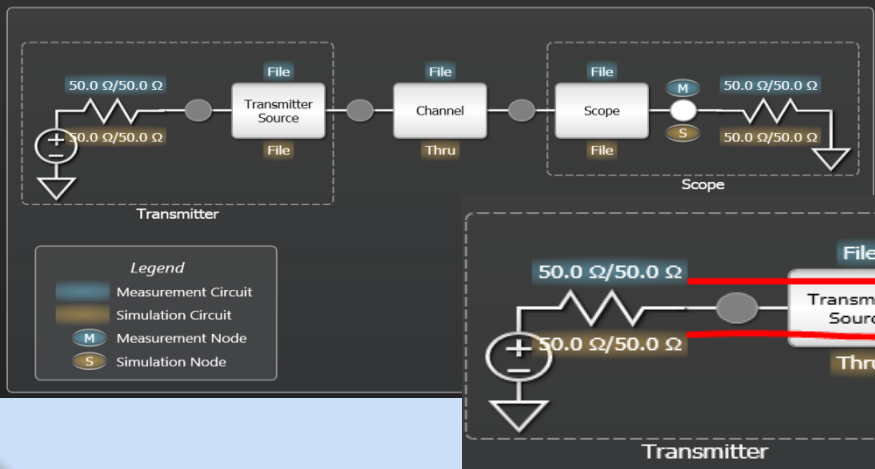
Partial De-embedding:

This paper's focus.

- Removes insertion loss
- Does NOT remove reflections (assumes an ideal source, receiver)
- Easier to implement

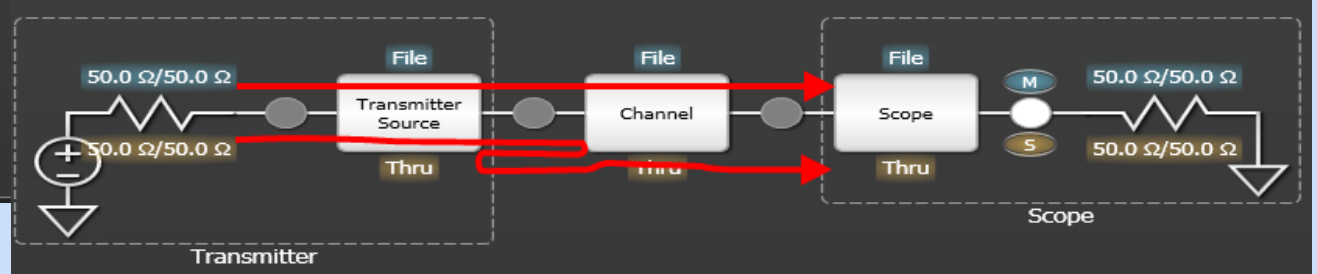
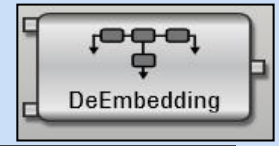


Preset Configuration: Remove all effects of a fixture or cable



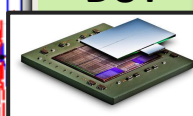
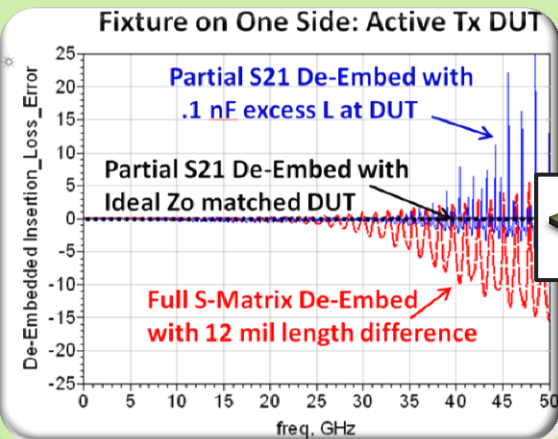
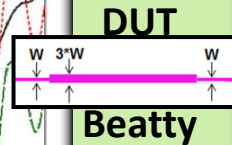
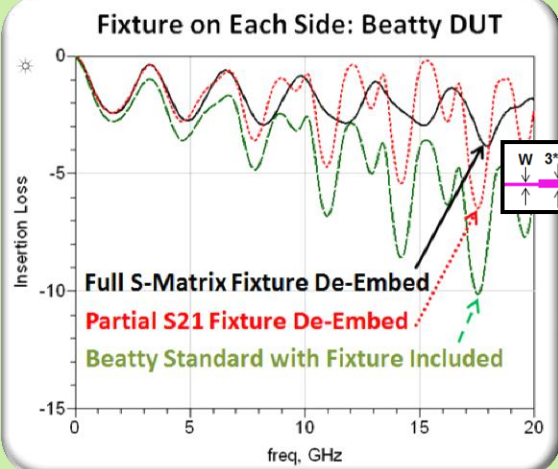
Full De-embedding:

- Removes insertion loss and reflections between circuit elements
- More accurate (but less forgiving if models/delays are not correct)

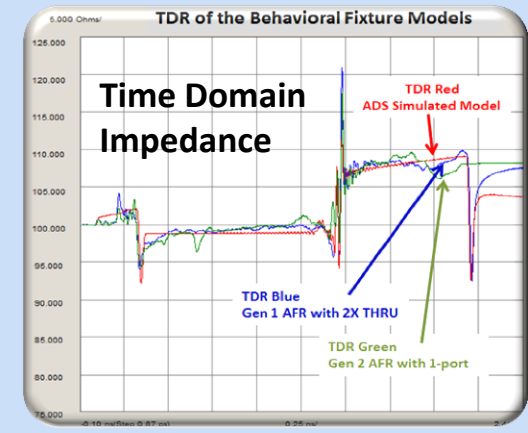
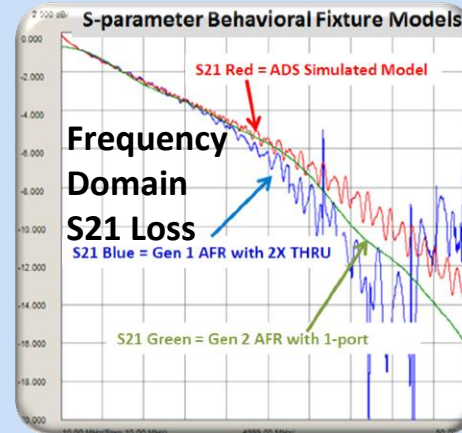


Partial S21 De-Embedding for 28 Gb/s Fixture

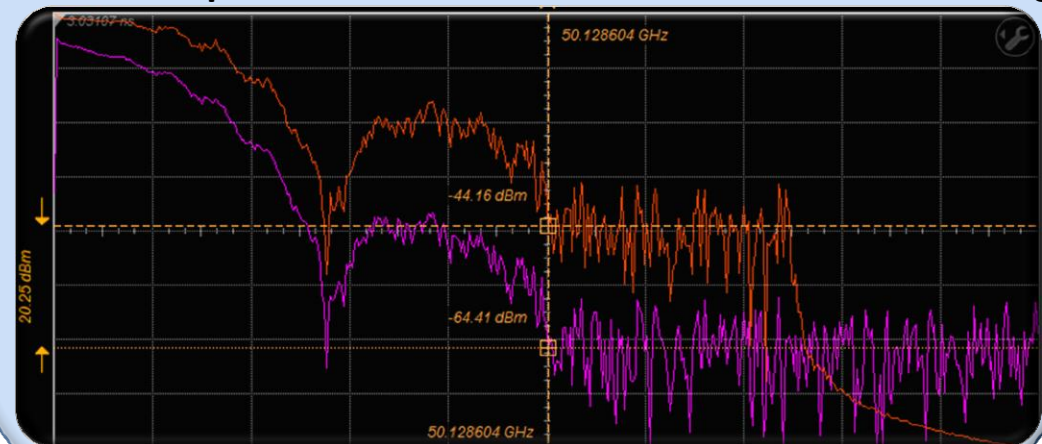
Partial vs. Full De-Embedding



Fixture Behavioral Models



Tx PRBS7 Spectrum Before and After Partial De-Embedding



Device Characterization

Measurements used to compare de-embed models

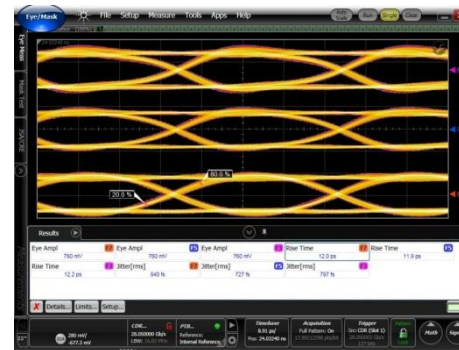
- **Waveform**

- Compare specific bit sequences (bits onscreen)
- Rise/Fall Time
- Amplitude



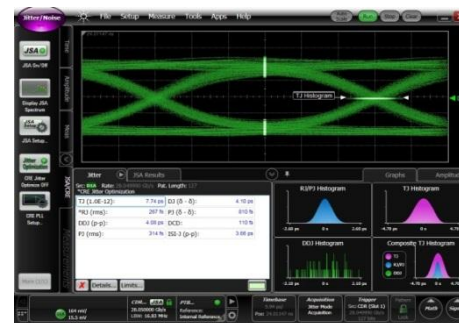
- **Eye Diagram**

- Fast and efficient, examine all bits in a pattern
- Rise/Fall Time
- Eye Amplitude
- Eye Height



- **Jitter and Amplitude Analysis**

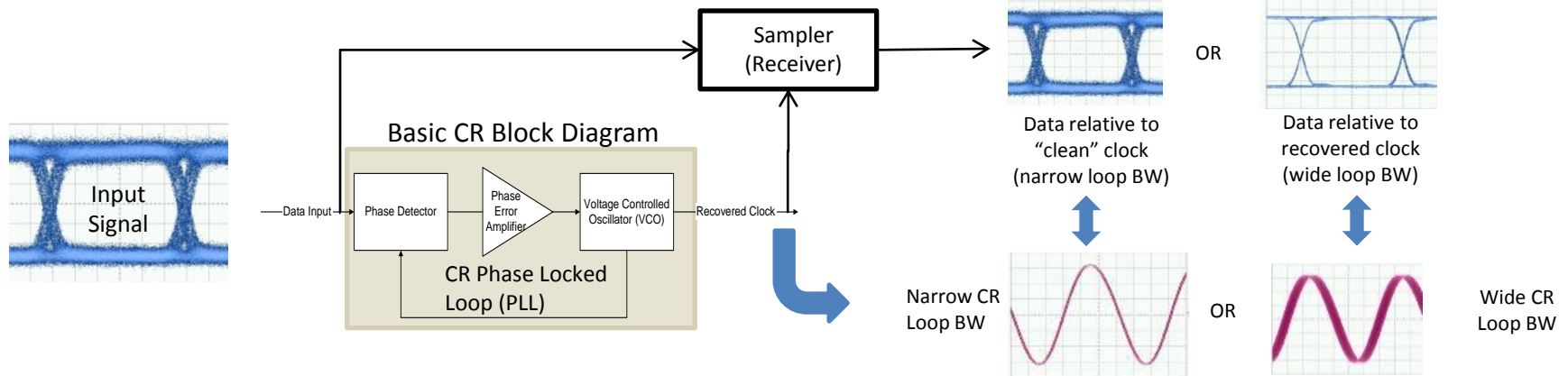
- Isolate random and deterministic components
- Focus on inter-symbol interference (ISI)



(check efficacy of S-parameter models used for de-embedding) **DESIGNCON 2014**

Clock Recovery (CR) Basics

Clock Recovery is required for compliant jitter measurements.



PLL "Jitter Transfer Function" (JTF)

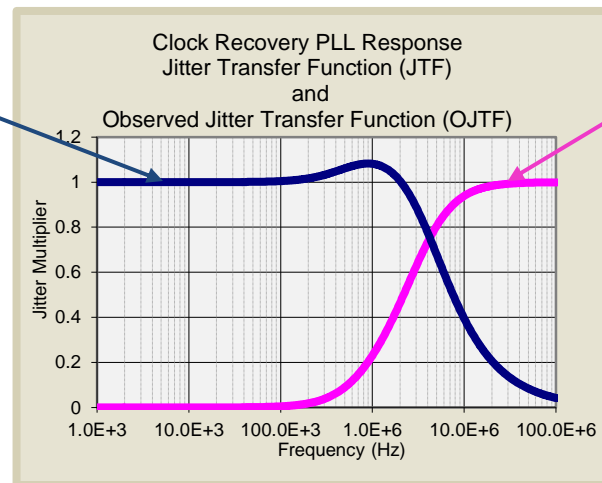
- indicates how much of the jitter on the input signal is "transferred" to the recovered clock (output)
- low-pass filter function (LPF)

JTF = Closed loop gain

$$= \frac{\phi_{out}}{\phi_{in}} = \frac{A(s)}{1 + A(s)} = G(s) = |G(s)|e^{j\phi(s)}$$

Standards Specify:

- PLL Order/Type
- PLL Bandwidth
- Peaking (Damping Factor)



"Observed Jitter Transfer Function" (OJTF)

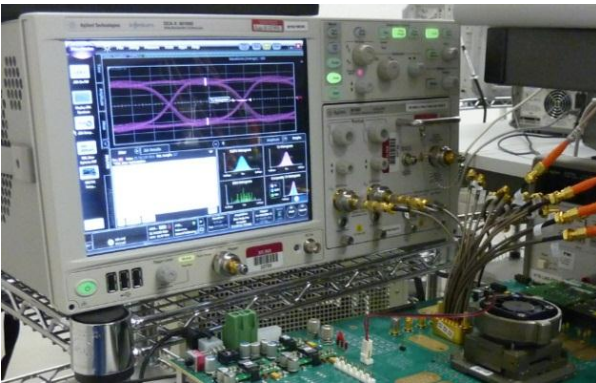
- indicates the jitter that is "observed" by the receiver (scope)
- high frequency jitter on the data stream is "transferred" to the receiver (HPF)

$$OJTF = 1 - JTF$$

$$= 1 - G(s) = 1 - |G(s)|e^{j\phi(s)}$$

28 Gb/s Performance of Fixture Removal Methods

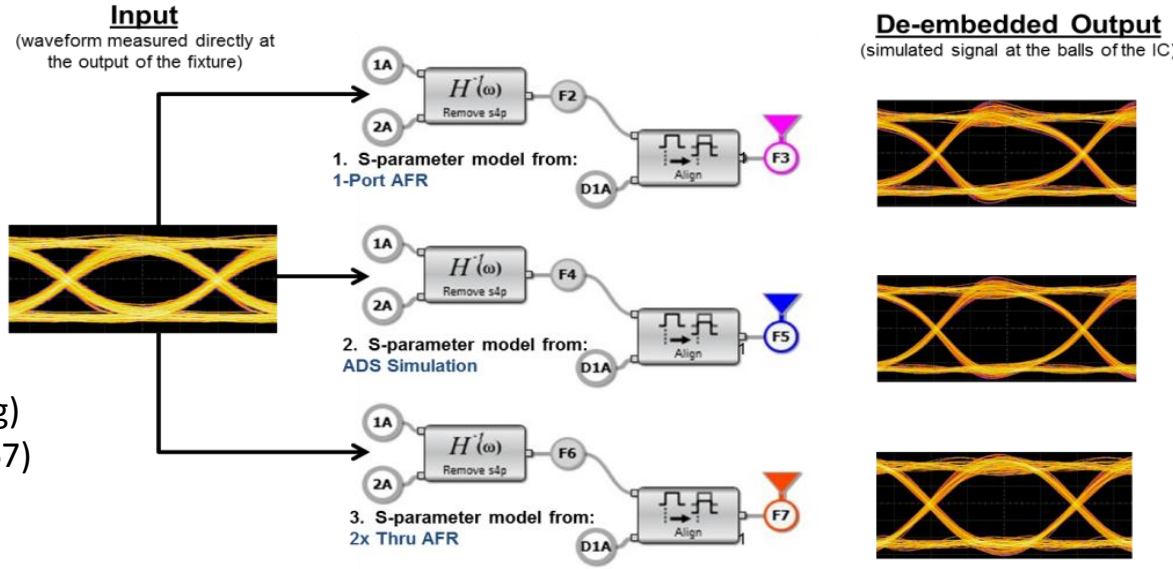
Test Equipment Setup



Xilinx 28G GTZ Transmitter	PCB Channel	BullsEye Connector	DCA (Scope)	De-Embedding: None
Xilinx 28G GTZ Transmitter	PCB Channel	BullsEye Connector	DCA (Scope)	De-Embedding: Gen 1 AFR 2XTHRU
Xilinx 28G GTZ Transmitter	PCB Channel	BullsEye Connector	DCA (Scope)	De-Embedding: ADS Model
Xilinx 28G GTZ Transmitter	PCB Channel	BullsEye Connector	DCA (Scope)	De-Embedding: Gen 2 AFR 1-Port

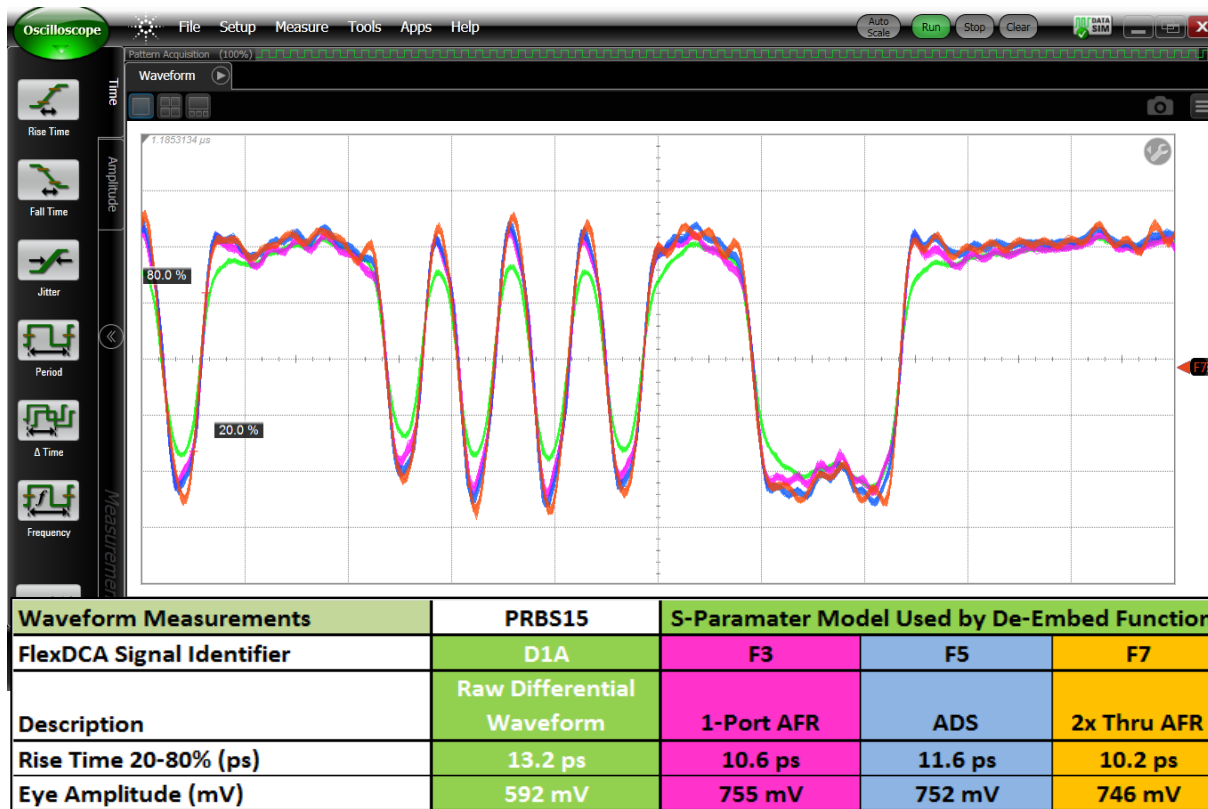
Agilent 86100D DCA-X with 86108B module

- Bandwidth: 50 GHz
- Intrinsic Random Jitter: < 50 fs rms
- Integrated Clock Recovery
 - Data Rate (DR): 28.05 Gb/s
 - Loop Order: 1st Order (0 dB Peaking)
 - PLL Bandwidth: 16.8 MHz (DR/1667)



Note 1 – the "Align" function simply removes filter delay and aligns waveforms making it easier to compare waveforms.

Waveform Measurements



1-Port AFR Model:

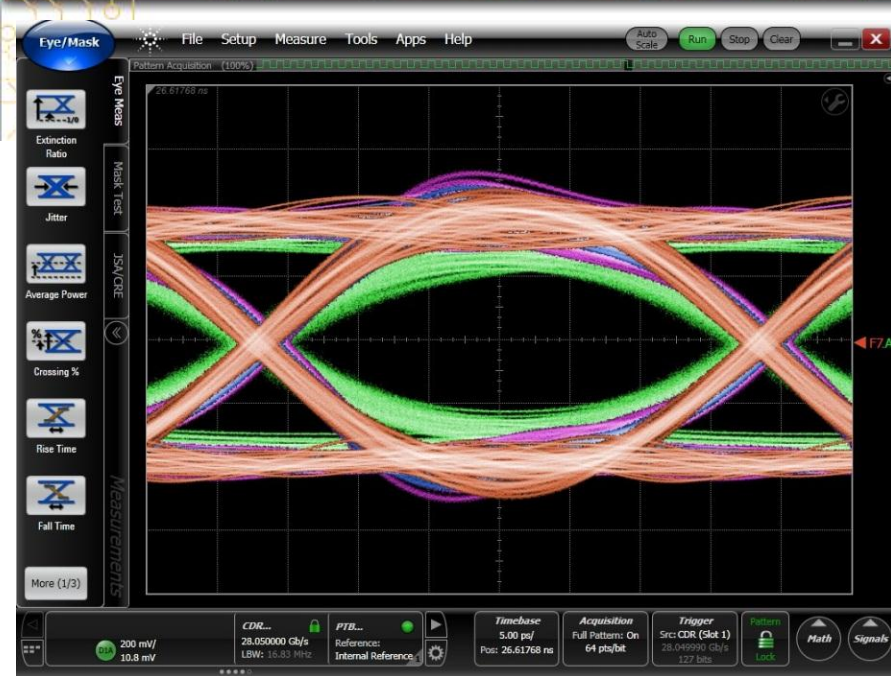
- Rise time (20%-80%): 2.6 ps faster (20% improvement)
- Amplitude: 163 mV higher (27% improvement)

Waveform Measurements

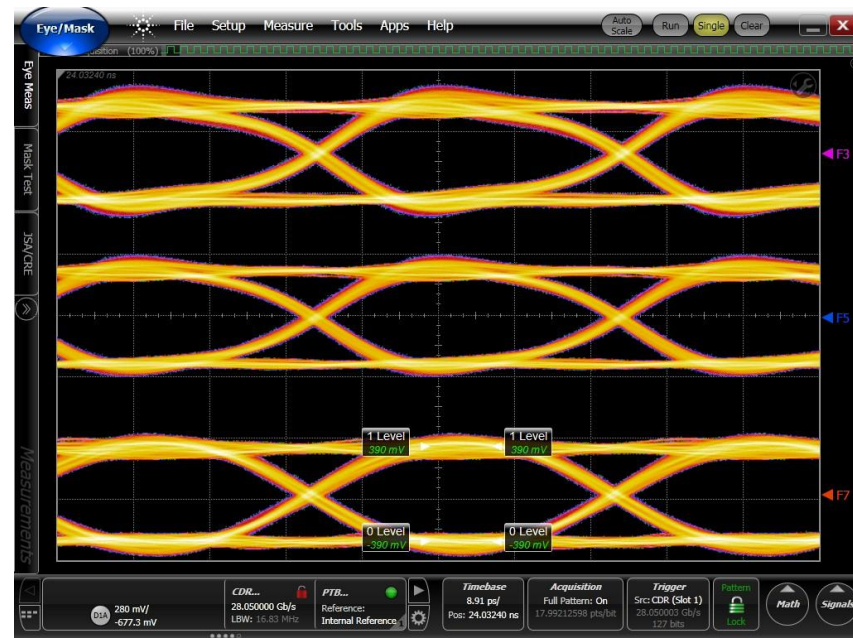


- Where does the ringing come from after de-embedding?

Eye Diagram Measurements



Eye Diagram	PRBS7	S-Paramater Model Used by De-Embed Function		
FlexDCA Signal Identifier	D1A	F3	F5	F7
Description	Raw Differential Waveform	1-Port AFR	ADS	2x Thru AFR
Rise Time 20-80% (ps)	15.3	11.9	11.5	11.9
Eye Amplitude (mV)	908	1134	1134	1169.0
Eye Height (mV)	560	679	814	803.0
Jitter (rms) (fs)	934	563	510	665.0

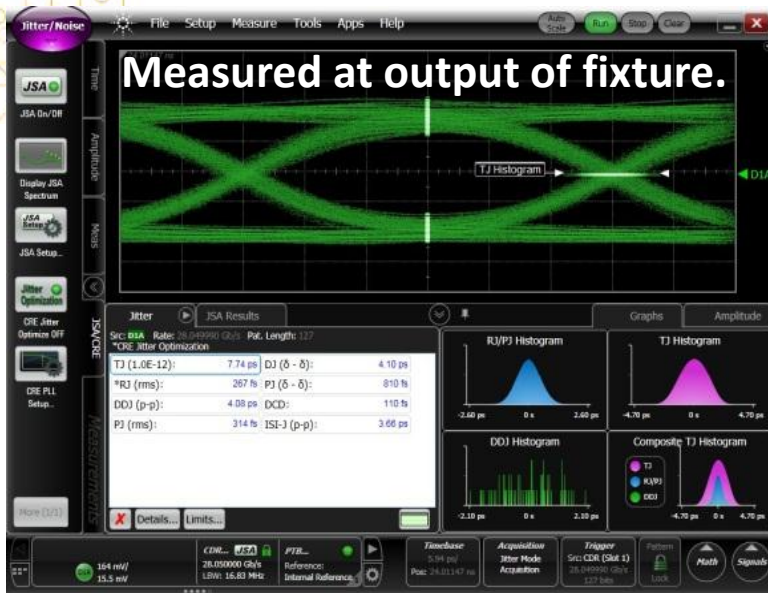


Eye Diagram	PRBS15	S-Paramater Model Used by De-Embed Function		
FlexDCA Signal Identifier	D1A	F3	F5	F7
Description	Raw Differential Waveform	1-Port AFR	ADS	2x Thru AFR
Rise Time 20-80% (ps)	15.2	12.1	11.5	11.6
Eye Amplitude (mV)	610	763	762	785.0
Eye Height (mV)	375	455	545	539.0
Jitter (rms) (fs)	993	615	537	702.0

1-Port AFR Model:

- Rise time (20%-80%): 3.1 ps faster (20% improvement)
- Eye Amplitude: 204 mV higher (25% improvement)

Jitter Measurements



Jitter Analysis	PRBS7	S-Paramater Model Used by De-Embed Function		
FlexDCA Signal Identifier	D1A	F3	F5	F7
Description	Raw Differential Waveform	1-Port AFR	ADS	2x Thru AFR
Total Jitter (@ 1E-12) (p-p)	7.74	6.05	5.72	6.10
Random Jitter, RJ rms (fs)	267	267	277	256
Deterministic Jitter ($\delta - \delta$) (ps)	4.1	2.40	1.92	2.60
Inter-Symbol Interference (ISI) (p-p)	3.66	2.37	1.76	2.36



Jitter Analysis	PRBS15	S-Paramater Model Used by De-Embed Function		
FlexDCA Signal Identifier	D1A	F3	F5	F7
Description	Raw Differential Waveform	1-Port AFR	ADS	2x Thru AFR
Total Jitter (1E-12) (p-p)	6.76	4.98	4.34	5.11
Random Jitter, RJ rms (fs)	267	267	277	256
Deterministic Jitter ($\delta - \delta$) (ps)	4.1	2.40	1.92	2.60
Inter-Symbol Interference (ISI) (p-p)	3.66	2.37	1.76	2.36

1-Port AFR Model (PRBS7):

- Total Jitter (1E-12): 6.05ps (1.7ps lower)
- Random Jitter (RJ): 267 fs (~ unchanged)
- Deterministic Jitter (DJ): 2.4ps (1.7ps lower)
- Inter-Symbol Interference (ISI): 2.37ps (1.4 ps lower)

1-Port AFR Model (PRBS15):

- ISI: 4.98ps (1.8 ps lower)

Summary

- **Fixture de-embedding Lessons Learned:**
 - **Test Fixture** is simple to build and measure
 - **Full de-embedding** is sensitive to reference plane errors.
 - **Partial de-embedding**
 - A practical solution when Tx is impedance matched.
 - Substantially less effort than full de-embed
 - Results are sufficient in most cases
 - **1-Port AFR** enables simple in-situ fixture channel measurement.

Conclusion

- This methodology is useful
 - Economical use of time and resources
 - Does not require elaborate measurement equipment and set up
 - Results are adequate without expensive effort and resources

“Accurate 28 Gb/s Tx real-time measurements at the DUT package require fixture de-embedding.”

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