2017 Xilinx Security Working Group (XSWG) Paris, France Agenda

Novotel Massy Palaiseau, 18-20 rue Emile Baudot, 91120 Palaiseau

Monday December 4, 2017		
Topic	**Presenter**	**Time**
Check In and Pre-Conference Luncheon		11:45am - 1:00
Welcome and Introductions	**Xilinx**	1:00 - 1:15
Next Generation Security Architecture	**Xilinx**	1:15 - 2:30
Break		2:30 - 2:45
Using Security in Zynq UltraScale+ MPSoC Devices	**Xilinx**	2:45 - 4:15
Isolation for Security in Zynq UltraScale+ MPSoC Devices	**Xilinx**	4:15 - 5:30
Day 1 Wrap Up	**Xilinx**	5:30 - 5:40
Evening Social and Partner Demonstrations		5:45 - 7:00

Tuesday December 5, 2017		
Topic	**Presenter**	**Time**
Continental Breakfast		7:30 - 8:00
Day 2 Re-Greet	**Xilinx**	8:00 - 8:15
Designing a Secure System with UltraScale/UltraScale+ MPSoC Devices	**Xilinx**	8:15 - 9:30
Break		9:30 - 9:45
SecMon Update	**Xilinx**	9:45 -11:00
Security Lifecycle Manager	**Xilinx**	11:00 - 12:00
Lunch		12:00 - 1:00

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Tuesday December 5, 2017 (cont.)			
Note after lunch that attendees may choose from an alternate track for demo / walkthrough sessions. Contents of demo session I and demo session II are identical.			
Lecture Track : Main Assembly Room		**Demo Track : Breakout Room**	
Accelerated TLS for Xilinx	**wolfSSL**	**Building a Zynq UltraScale+ MPSoC Devices, Secure Boot Design Cradle to Grave Session I Xilinx**	1:00 - 1:45
Trust in Xilinx Products: Assurance in Your Supply Chain	**Xilinx**		1:45 - 2:15
Cybersecurity Concept Design	**Mocana**		2:15 - 3:00
Break			3:00 - 3:15
Secure Device Provisioning	**Xilinx**	**Building a Zynq UltraScale+ MPSoC Devices, Secure Boot Design Cradle to Grave Session II Xilinx**	3:15 - 4:15
Design Guidance From an Expert: How To Be Successful with Your Next Xilinx Design	**Xilinx**		4:15 - 5:00
XSWG2017 General Session Adjournment (Main Assembly Room)			**5:00 - 5:10**