2017 Xilinx Security Working Group (XSWG) Herndon VA Agenda

Optional : Classified Session

Tuesday November 7, 2017

Participants MUST possess valid US Security Clearance (minimum of L/Secret), be US Citizen, and have Visit Request Processed and Confirmed

Host : Integrity Applications Incorporated

Check in Time : 12:30pm - 1pm

Session Time : 1:00pm - 6:00pm

2017 Xilinx Security Working Group (XSWG) Herndon VA Agenda

Hilton Washington Dulles Airport,13869 Park Center Road, Herndon, Virginia 20171

Wednesday November 8, 2017		
Topic	**Presenter**	**Time**
Check In and Continental Breakfast		7:15 - 8:00
Welcome and Introductions	**Xilinx**	8:00 - 8:15
Keynote Address	**DARPA**	8:15 - 9:00
Next Generation Security Architecture	**Xilinx**	9:00 - 10:15
Break		10:15 - 10:30
Using Security in ZU+	**Xilinx**	10:30 - 12:00
Lunch		12:00 - 1:00
Isolation for Security in ZU+	**Xilinx**	1:00 - 2:15
Designing a Secure System with UltraScale/UltraScale+ FPGAs	**Xilinx**	2:15 - 3:30
Break		3:30 - 3:45
SecMon Update	**Xilinx**	3:45 - 5:00
Day 1 Wrap Up	**Xilinx**	5:00 - 5:10
Evening Social and Partner Demonstrations		5:30 - 7:00

2017 Xilinx Security Working Group (XSWG) Herndon VA Agenda

Hilton Washington Dulles Airport,13869 Park Center Road, Herndon, Virginia 20171

Thursday November 9, 2017			
Topic		**Presenter**	**Time**
Continental Breakfast			7:30 - 8:00
Day 2 Re-Greet		**Xilinx**	8:00 - 8:15
Cryptographically Secure Immutable Memory		**Graf Research**	8:15 - 9:00
Accelerated TLS for Xilinx		**wolfSSL**	9:00 - 9:45
Cybersecurity Concept Design		**Mocana**	9:45 - 10:30
Break			10:30 - 10:45
Security Lifecycle Manager (Formerly Security Wizard)		**Xilinx**	10:45 - 11:45
Lunch			11:45 - 12:45
Note after lunch that attendees may choose from an alternate track for demo / walkthrough sessions. Contents of demo session I and demo session II are identical.			
Lecture Track : Main Assembly		**Demo Track : Breakout Room**	
Physical Device Modification "Protecting the Blindside"	**Draper**	**Building a ZU+ Secure Boot Design, Cradle to Grave Session I Xilinx**	12:45 - 1:30
Trust in Xilinx Products: Assurance in Your Supply Chain	**Xilinx**		1:30 - 2:15
JFAC Update	**USG**		2:15 - 3:00
Break			3:00 - 3:15
Secure Device Provisioning	**Xilinx**	**Building a ZU+ Secure Boot Design, Cradle to Grave Session II Xilinx**	3:15 - 4:15
Design Guidance From an Expert: How To Be Successful with Your Next Xilinx Design	**Xilinx**		4:15 - 5:00
XSWG2017 General Session Adjournment (Main Assembly)			**5:00 - 5:10**